THE DATASHEET OF

DS1013S-60

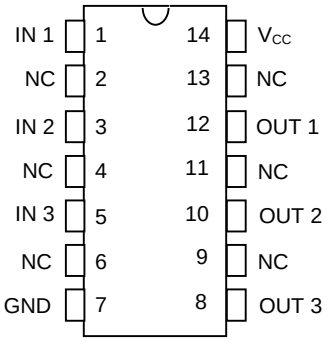
DS1013
3-in-1 Silicon Delay Line

www.dalsemi.com

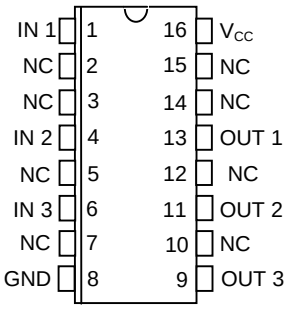
FEATURES

- All-silicon time delay
- 3 independent buffered delays
- Delay tolerance ±2ns for -10 through –60
- Stable and precise over temperature and voltage range
- Leading and trailing edge accuracy
- Economical
- Auto-insertable, low profile
- Standard 14-pin DIP, 8-pin DIP, or 16-pin SOIC
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom delays available
- Quick turn prototypes
- Extended temperature ranges available

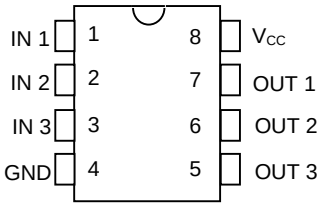
PIN ASSIGNMENT



DS1013 14-pin DIP (300-mil)
See Mech. Drawings Section



DS1013S 16-pin SOIC
(300-mil)
See Mech. Drawings Section



DS1013M 8-pin DIP (300-mil)
See Mech. Drawings Section

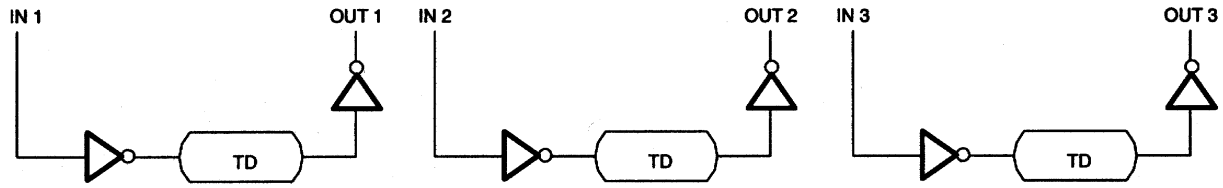
PIN DESCRIPTION

IN 1, IN 2, IN 3	- Inputs
OUT 1, OUT 2, OUT 3	- Outputs
GND	- Ground
V_{CC}	- +5 Volts
NC	- No Connection

DESCRIPTION

The DS1013 series of delay lines has three independent logic buffered delays in a single package. The devices are offered in a standard 14-pin DIP which is pin-compatible with hybrid delay lines. Alternative 8-pin DIP and surface mount packages are available which save PC board area. Since the DS1013 products are an all silicon solution, better economy is achieved when compared to older methods using hybrid techniques. The DS1013 series delay lines provide a nominal accuracy of ±2ns for delay times ranging from 10 ns to 60 ns, increasing to 5% for delays of 150 ns and longer. The DS1013 delay line reproduces the input logic state at the output after a fixed delay as specified by the dash number extension of the part number. The DS1013 is designed to reproduce both leading and trailing edges with equal precision. Each output is capable of driving up to 10 74LS loads. Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (972) 371–4348.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PHL}, t_{PLH}) Table 1

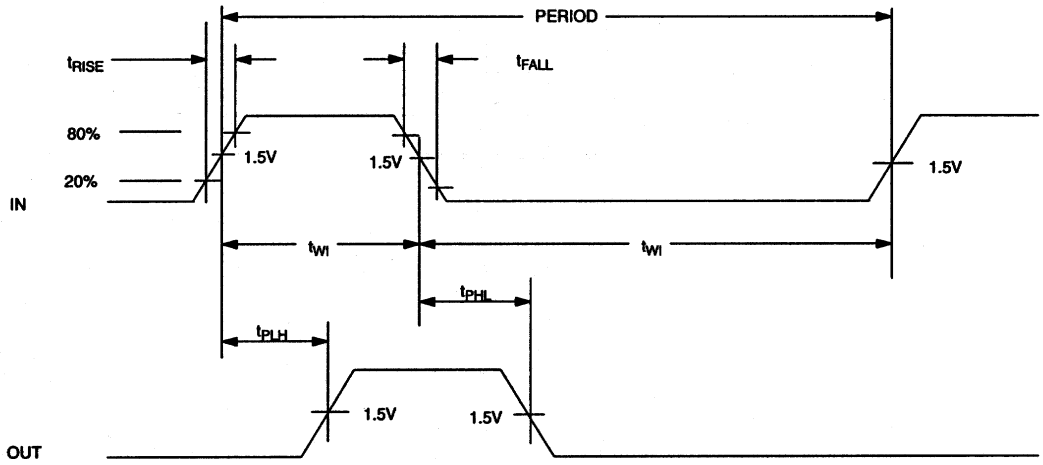
PART NO.	DELAY PER OUTPUT (ns)
DS1013-10	10/10/10
DS1013-12	12/12/12
DS1013-15	15/15/15
DS1013-20	20/20/20
DS1013-25	25/25/25
DS1013-30	30/30/30
DS1013-35	35/35/35
DS1013-40	40/40/40
DS1013-45	45/45/45
DS1013-50	50/50/50
DS1013-60	60/60/60
DS1013-70*	70/70/70
DS1013-75*	75/75/75
DS1013-80*	80/80/80
DS1013-100*	100/100/100
DS1013-150**	150/150/150
DS1013-200**	200/200/200

Custom delays available

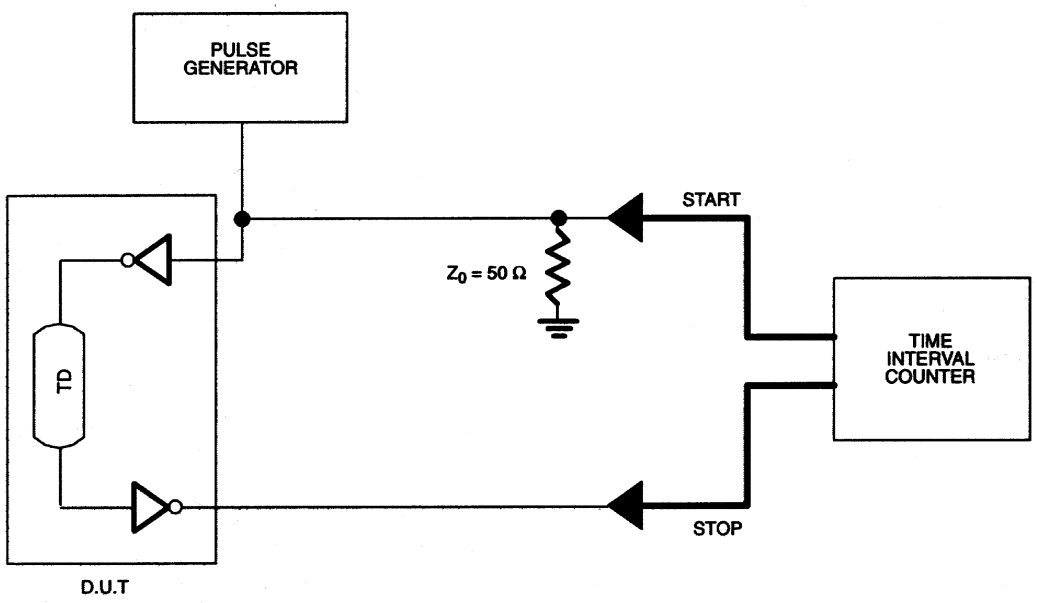
* ±3% tolerance

** ±5% tolerance

TIMING DIAGRAM: SILICON DELAY LINE Figure 2



TEST CIRCUIT Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC} + 0.5		
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	µA	
Active Current	I_{CC}	V_{CC}=Max; Period=Min.		40	70	mA	2
High Level Output Current	I_{OH}	V_{CC}=Min. V_{OH}=4.0V			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC}=Min. V_{OL}=0.5V	12.0			mA	

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	100% of t_{PLH}			ns	
Input to Output Delay (leading edge)	t_{PLH}		Table 1		ns	3, 4, 5, 6
Input to Output Delay (trailing edge)	t_{PHL}		Table 1		ns	3, 4, 5, 6
Power-up Time	t_{PU}			100	ms	
	Period	3 (t_{WI})			ns	7

CAPACITANCE (T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

NOTES:

1. All voltages are referenced to ground.

2. Measured with outputs open.

3. V_{CC} = 5V @ 25°C. Delays accurate on both rising and falling edges within ±2 ns for -10 to -60, ±3% for -70 to 100 and ±5% for -150 and longer delays.

4. See "Test Conditions" section.

5. The combination of temperature variations from 25°C to 0°C or 25°C to 70°C and voltage variations from 5.0V to 4.75V or 5.0V to 5.25V may produce an additional delay shift of ±1.5 ns or ±3%, whichever is greater.

6. All output delays tend to vary unidirectionally over temperature or voltage ranges (i.e., if OUT 1 slows down, all other outputs also slow down).

7. Period specifications may be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).

TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any tap output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1013. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between each input and corresponding output. Each output is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 ohms Max.
Rise and Fall Time:	3.0 ns Max.
Pulse Width:	500 ns
Period:	1 µs

OUTPUT:

Each output is loaded with the equivalent of one 74F04 input gate. Delay is measured at the 1.5V level on the rising and falling edge.

NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

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