THE DATASHEET OF

MAX311CPE+

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MAXIM

CMOS RF/Video Multiplexers

General Description

Maxim's MAX310 and MAX311 are CMOS monolithic analog multiplexer/demultiplexers designed for use with signal frequencies ranging from DC through video. The MAX310 is a 1-of-8 multiplexer while the MAX311 is for 2-of-8 (4 channel differential) applications.

A key feature of the MAX310/311 is extremely high off isolation at high frequencies. The isolation of each off channel to the output is guaranteed to be -66dB at 5MHz. The input signal range is +12V to -15V with ±15V power supplies while power consumption is typically 1.1mW.

All control inputs are fully compatible with TTL and CMOS logic. Decoding is in standard BCD format and an Enable input is also provided to simplify cascading of devices. The MAX310 and MAX311 will operate with nearly any power supply combination which totals less than 36V ($V^+ - V^-$) including single supply operation at +12V, +15V, and +28V with V^- connected to GND.

Applications

Video Switching and Crosspoint Systems

Automatic Test Equipment

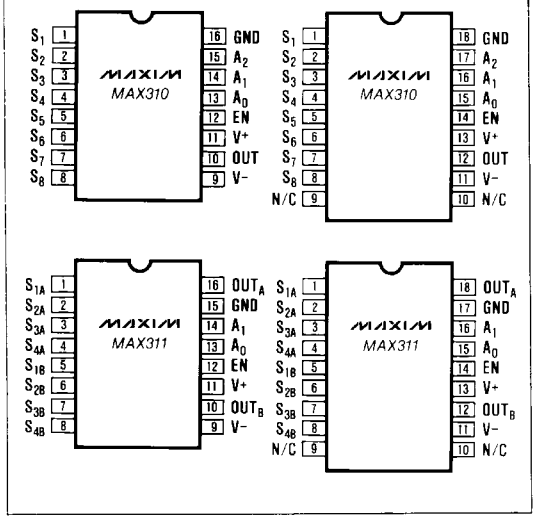
Medical Ultrasound Phased Array Systems

Data Logging of High Frequency Signals

Digital Signal Processing

Pin Configuration

Top View



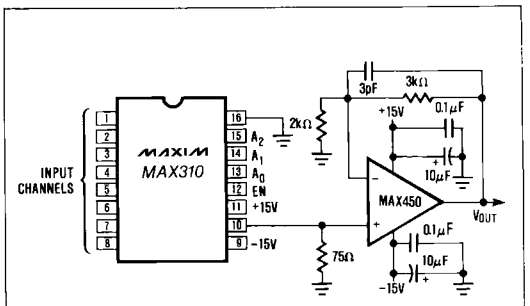
Features

- **-76dB Typical Off Isolation at 5MHz**
- **-63dB Typical "All Channel Off" Isolation at 5MHz**
- **Phase Shift Match Between Channels, <1° at 5MHz**
- **Break-Before-Make Switching**
- **Wide Supply Range, ±4.5V to ±16.5V and Single Supply**
- **Symmetrical, Bi-directional Operation**
- **Latch-Up Proof Construction**

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX310C/D	0°C to +70°C	Dice
MAX310CPE	0°C to +70°C	16 Lead Plastic DIP
MAX310CWN	0°C to -70°C	18 Lead Wide SO
MAX310EPE	40°C to +85°C	16 Lead Plastic DIP
MAX310EWN	-40°C to +85°C	18 Lead Wide SO
MAX310EJE	-40°C to +85°C	16 Lead CERDIP
MAX310MJE	-55°C to +125°C	16 Lead CERDIP
MAX311C/D	0°C to +70°C	Dice
MAX311CPE	0°C to +70°C	16 Lead Plastic DIP
MAX311CWN	0°C to -70°C	18 Lead Wide SO
MAX311EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX311EWN	-40°C to +85°C	18 Lead Wide SO
MAX311EJE	-40°C to +85°C	16 Lead CERDIP
MAX311MJE	-55°C to +125°C	16 Lead CERDIP

Typical Operating Circuit



No Insertion Loss, 8 Channel Mux

MAXIM is a registered trademark of Maxim Integrated Products.

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ABSOLUTE MAXIMUM RATINGS

Voltage referenced to V⁻
- V⁺ ..... +36V
- GND ..... +24V
- Digital Inputs ..... V⁻ to V⁺

Input Current
- S and COMMON OUT ..... ±50mA
- All pins except S and COM. OUT ..... ±30mA

Lead Temperature ..... +300°C

Storage Temperature ..... -65°C to +150°C

Operating Temperature Range
- MAX310C, MAX311C ..... 0°C to +70°C
- MAX310E, MAX311E ..... -40°C to +85°C
- MAX310M, MAX311M ..... -55°C to +125°C

Power Dissipation (16-Pin packages)
- CERDIP (derate 10mW/°C above +75°C) 750mW
- Plastic DIP (derate 7.35mW/°C above +75°C) 550mW
- Small Outline (derate 9mW/°C above +75°C) 550mW

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Over Temperature. V^+ = +15V, V^- = -15V, GND = 0V unless otherwise indicated)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Analog Signal Range		V^+, V^- = ±15V V^+, V^- = ±5V	-15 -5		+12 +2	V
Channel ON Resistance	R_{ON}	V_{IN} = ±5V, I_{OUT} = 10mA T_A = +25°C Over Temp.		150	250 300	Ω
ON Resistance Match	ΔR_{ON}	V_{IN} = ±5V, I_{OUT} = 10mA		6		%
OFF Input Leakage Current	$I_{S(OFF)}$	Figure 10, T_A = +25°C Over Temp		0.4 3	10 100	nA
OFF Output Leakage Current	$I_{D(OFF)}$	Figure 11, T_A = +25°C MAX310 Over Temp. MAX311 Over Temp.		0.8 20 10	10 100 50	nA
ON Channel Leakage Current	$I_{D(ON)}$	Figure 12, T_A = +25°C MAX310 Over Temp. MAX311 Over Temp.		1 30 15	10 200 100	nA
Input Low Threshold	V_{AL}	V^+/V^- = ±15V, ±5V			0.8	V
Input High Threshold	V_{AH}	V^+/V^- = ±15V, ±5V	2.4			V
Input Current (Logic)	I_A	V_A = 0V or 5V			±10	µA
Access Time	t_{ACC}	Figure 7; T_A = +25°C Over Temp.		0.6	1.5 2.0	µs
Enable Delay ON or OFF	$t_{EN(ON/OFF)}$	Figure 8; T_A = +25°C Over Temp.		0.3	1.0 2.0	µs
Break-Before-Make Delay	t_{ON}-t_{OFF}	Figure 9	30	100		ns
OFF Isolation, Single Channel to OUT	ISO_{SC}	Figure 3; T_A = +25°C	-66	-76		dB
OFF Isolation, All Channels to OUT	ISO_{AC}	Figure 4, 5, T_A = +25°C MUX Disabled, EN = +0.8V MUX Enabled, EN = +2.4V		-63 -58		dB
Adjacent Channel Crosstalk	ISO_X	Figure 6, T_A = +25°C		-72		dB
Channel Input Capacitance OFF State ON State	 $C_{S(OFF)}$ $C_{S(ON)}$	T_A = +25°C, V_{IN} = 10mV_{RMS} 10 MHz		 5 45		pF
Channel Output Capacitance OFF State ON State	 $C_{D(OFF)}$ $C_{D(OFF)}$	T_A = +25°C; EN = +0.8V, MAX310 MAX311 EN = +2.4V, MAX310 MAX311		 38 20 57 40		pF
Charge Injection	Q	Figure 13, T_A = +25°C		110		pC
Supply Current; V^+ V^-	I^+ I^-	EN, A0, A1, A2 = 0V or +5V		75 0.1	200 100	µA
Supply Voltage Range		T_A = +25°C	±4.5		±16.5	V

Detailed Description

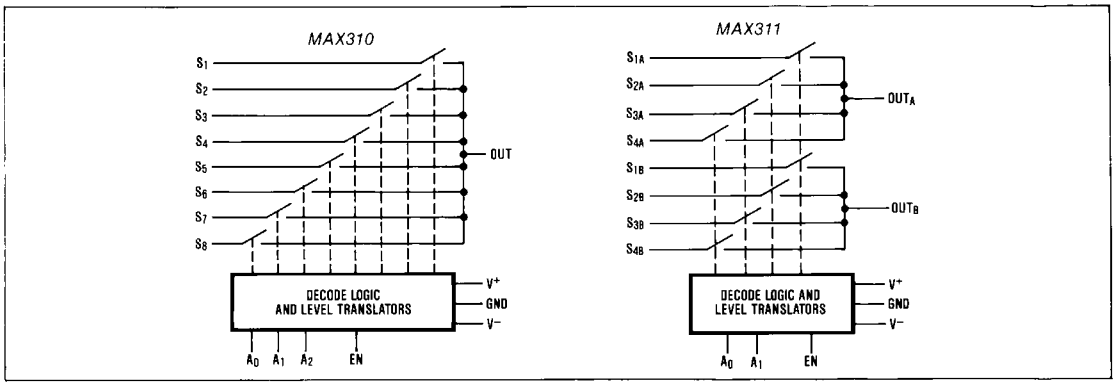


Figure 1. Functional Block Diagrams

The Maxim MAX310 and MAX311 contain 8 video switches combined with an address decoder and level translators (Figure 1). Each of the 8 video switches consists of 3 N-channel FETs configured as shown in Figure 2. This "T" configuration provides the high frequency OFF isolation required when switching wide-band video, audio, or digital signals.

N-channel FETs are used in the MAX310/311's "T" switches because of their low capacitance and consequently superior isolation characteristics. A side effect is that the N-channel ON resistance varies somewhat with the voltage difference between the analog input signal and V^+. This effect is shown in the Typical Operating Characteristics section.

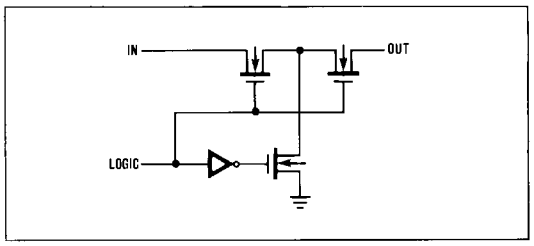


Figure 2. N-channel T Switch

Channel selection is performed by applying a binary input to the address inputs A_0, A_1 and A_2 (A_0 and A_1 only for MAX311). The address decoder selects channels as shown in the truth tables (Table 1). All digital inputs are compatible with TTL and CMOS logic levels.

Break-before-make switch timing is guaranteed for both multiplexers. This prevents momentary shorting of inputs when changing multiplexer channels.

The MAX310 and MAX311 are also fully bilateral and so can be used "backwards", as demultiplexers, with no loss in performance. Specifically, one input signal can be routed to one of several outputs.

TABLE 1. CHANNEL SELECTION INPUT CODES

MAX310					MAX311			
A_2	A_1	A_0	EN	ON Channel	A_1	A_0	EN	ON Channel
0	0	0	1	1	0	0	1	1A + 1B
0	0	1	1	2	0	1	1	2A + 2B
0	1	0	1	3	1	0	1	3A + 3B
0	1	1	1	4	1	1	1	4A + 4B
1	0	0	1	5	X	X	0	ALL OFF
1	0	1	1	6				
1	1	0	1	7				
1	1	1	1	8				
X	X	X	0	ALL OFF				

Application Hints

Maximizing Isolation

With all high frequency circuits, careful printed circuit board layout is essential for optimum performance. To maintain the high frequency isolation of the MAX310/311, signal paths should be of minimum length and ground plane should be used where possible, including between adjacent input pins. A ground or power supply trace between adjacent inputs will markedly improve isolation between channels.

Both V^+ and V^- should be bypassed to ground with 0.1μF ceramic capacitors. The leads of the capacitors should be kept as short as possible to minimize

series inductance. The bypass capacitors should also be located as physically close to the multiplexer as possible.

Input Capacitance

The capacitance of an input channel changes from about 5pF in the OFF state to around 45pF when ON. To minimize bandwidth reduction due to input capacitance, the inputs should be driven from a low impedance source. A 75Ω source impedance results in a 3dB frequency response of 47MHz when loaded with 45pF.

Charge Injection

With ±15V supplies, injected charge from the internal switch drive circuitry to the analog signal path is typically 110 picocoulombs. As shown in the Typical Characteristics graph, charge injection is relatively independent of the analog signal voltage.

Insertion Loss

With ±15V supplies and ±2V video signals, the 120Ω typical ON resistance of the MAX310/311 results in -8.3dB insertion loss when used with a 75Ω output load. This insertion loss is virtually constant from DC to over 20MHz.

TABLE 2. PHASE SHIFT AT 10MHz

INPUT CHANNEL MAX311	OUTPUT - INPUT PHASE SHIFT	
	R_L = 10kΩ	R_L = 75Ω
S_1	-22°	-12°
S_2	-21°	-11.5°
S_3	-20°	-11.5°
S_4	-20°	-11.2°
S_5	-20°	-11.2°
S_6	-20.5°	-11.4°
S_7	-20.7°	-11.5°
S_8	-20.4°	-11.5°

Test Conditions: V^+ = +15V, V^- = -15V, V_{IN} = 1.25V_{RMS} at 10MHz, OFF inputs terminated with 75Ω.

Operation with Power Supplies Other Than ±15V

Table 3 shows how different power supply voltages affect the MAX310/311's analog signal range and channel ON resistance (R_{ON}). This data is also shown graphically in the Typical Operating Characteristics section. Since N-channel FETs are used in the switches, R_{ON} is determined by the voltage difference between V^+ and the input voltage. For lowest R_{ON}, use a negative power supply (V^-) equal to the most negative input voltage, and a positive power supply (V^+) 30V above the negative supply. For example, if only positive signals need to be switched, use 0V for V^- and +30V for V^+ to achieve minimum R_{ON}. This also reduces ON resistance variation with analog signal level and input voltage dependent changes in insertion loss, which minimizes differential gain errors.

The digital input thresholds are nearly independent of V^+, remaining near +1.4V over the entire operating supply voltage range of ±4.5V to ±18V (9V to 36V single supply).

The MAX310/311 switching delay times vary somewhat with power supply voltage. Access time (see Figure 2) increases from typically 600ns with ±15V supplies to 3μs with ±5V supplies. Other switching times are also proportionately longer with ±5V power supplies.

Propagation Delay and Phase Shift

In Table 2, the typical phase shift for each channel is shown. Note that both the phase shift and the phase shift difference between channels are reduced with a 75Ω output load. At 10MHz, the channel-to-channel match is better than 1° with a 75Ω load and improves as the frequency is reduced.

Phase shift measurements for the MAX311 are similar to those in Table 2. The data for the MAX310 channels 1 to 4 corresponds to MAX311 channels 1A to 4A, Channels 5 to 8 correspond to MAX311 channels 1B to 4B.

TABLE 3. SIGNAL RANGE AND R_{ON} vs SUPPLY VOLTAGE

SUPPLY VOLTAGE		SIGNAL RANGE	TYPICAL R_{ON} AT V_{IN}	
V^-	V^+		NEGATIVE	POSITIVE
-15	+15V	-15V to +12V	104Ω at -10V	265Ω at +10V
		-5V to +5V	115Ω at -5V	150Ω at +5V
GND	+15V	0V to +12V	120Ω at 0V	150Ω at +5V
GND	+30V	0V to +27V	90Ω at 0V	100Ω at +5V
-5V	+5V	-5V to +2V	240Ω at -2V	480Ω at +2V
-10V	+10V	-10V to +7V	140Ω at -5V	220Ω at +5V
-5V	+15V	-5V to +12V	115Ω at -5V	150Ω at +5V

OFF Isolation Measurements

Figure 3 is used to test and specify the MAX310/311's single channel OFF isolation. In the case illustrated, channel S_1 has signal applied while all other inputs are grounded through 75Ω except for the ON channel (S_2 in Figure 3). This is shorted directly to ground to prevent pickup from external wiring. Each channel meets this test to an isolation limit of -66dB at 5MHz.

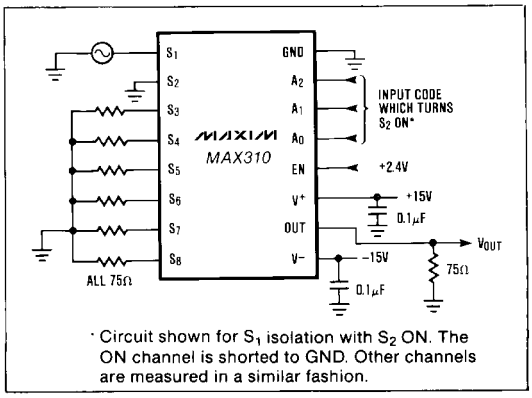


Figure 3. Single Channel OFF Isolation (ISO_{SC}) Test Circuit

Figure 4 shows the test circuit for OFF isolation with all channels driven. The impedance of the source connected to the selected channel (in this case, S_4) significantly affects feedthrough. With a 75Ω source impedance the typical measured OFF isolation is -58dB at 5MHz. This increases to -63dB if the source impedance is reduced to 10Ω or less. OFF isolation also increases with decreasing frequency. For example, when the frequency is reduced from 10MHz to 1MHz the isolation improvement is typically -20dB. Figure 5 shows a similar circuit for testing all-channel isolation with the multiplexer disabled (EN low).

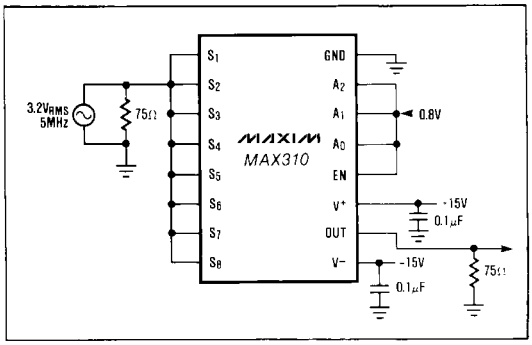


Figure 4. All Channel OFF Isolation (ISO_{AC}) Test Circuit (MUX Disabled)

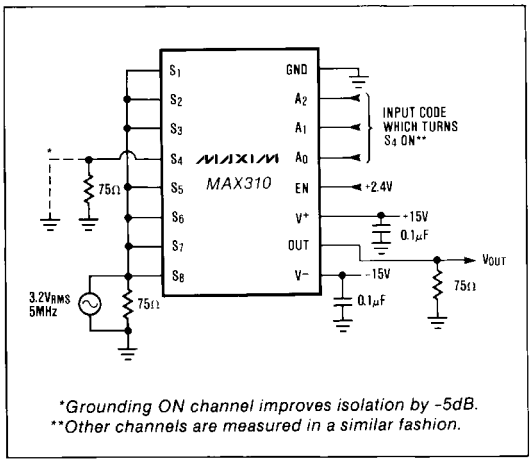
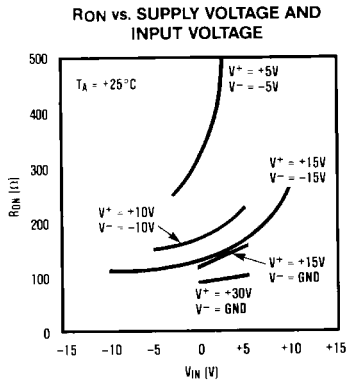
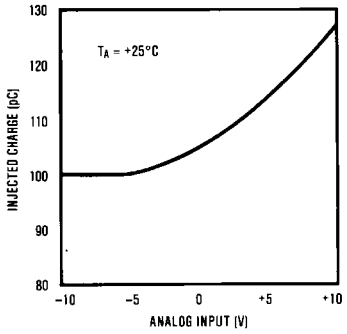
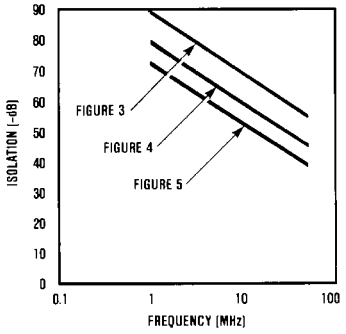


Figure 5. All Channel OFF Isolation (ISO_{AC}) Test Circuit (MUX Enabled)

Typical Operating Characteristics







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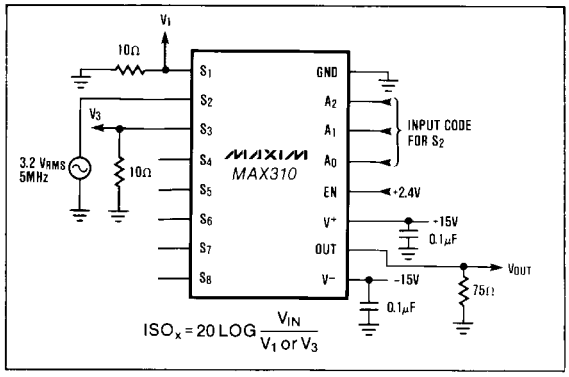


Figure 6. Adjacent Channel Crosstalk (ISO_X) Test Circuit

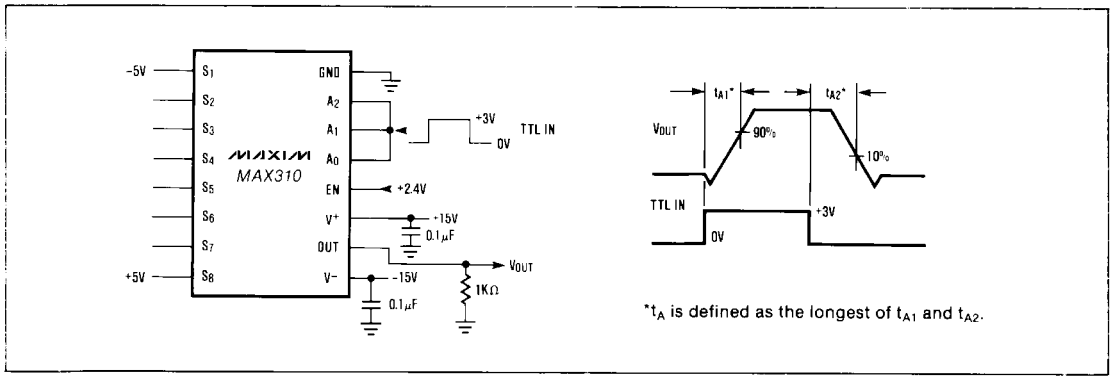


Figure 7. Access Time (t_A) Test Circuit.

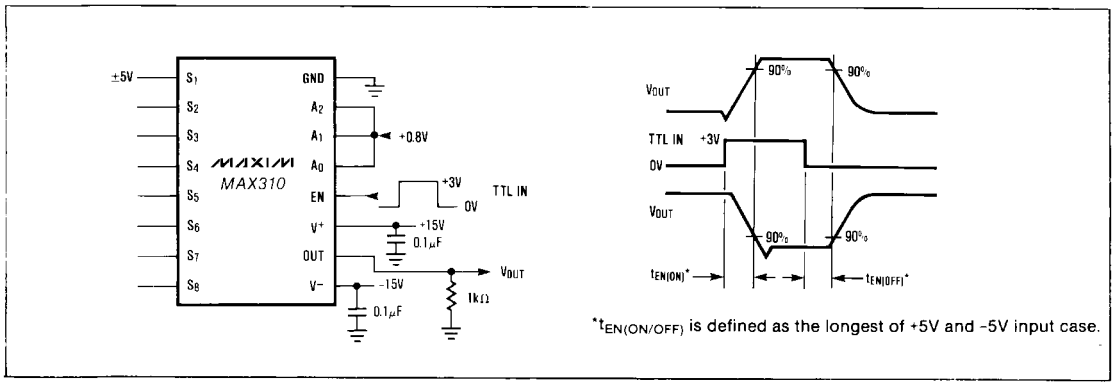


Figure 8. Enable Delay ($t_{EN(ON/OFF)}$) Test Circuit.

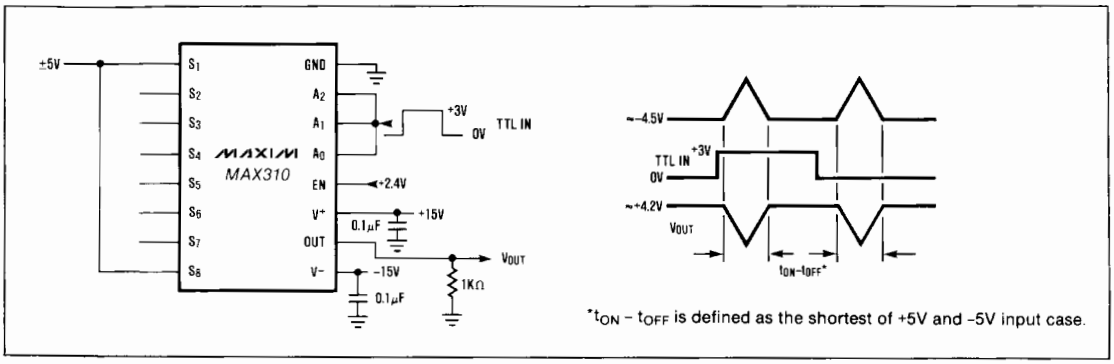


Figure 9. Break-Before-Make Delay (t_{ON}-t_{OFF}) Test Circuit.

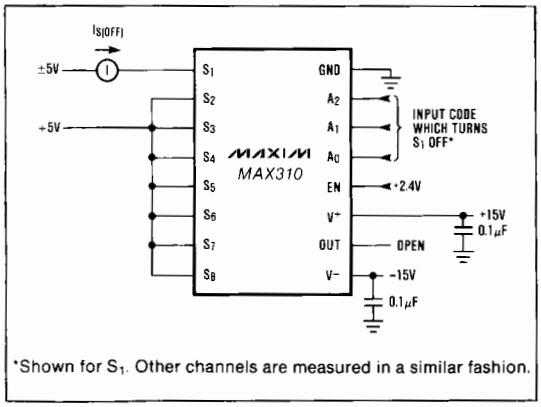


Figure 10. OFF Input Leakage Current Test Circuit.

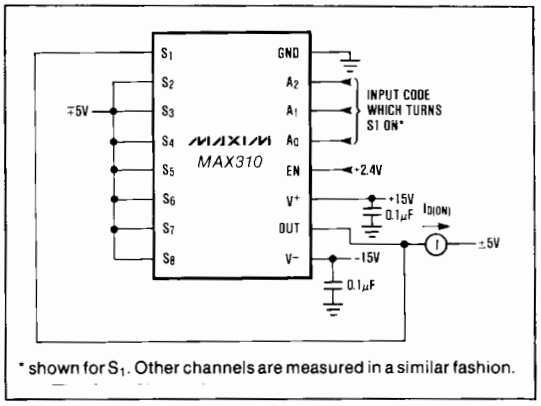


Figure 12. ON Output Leakage Current Test Circuit.

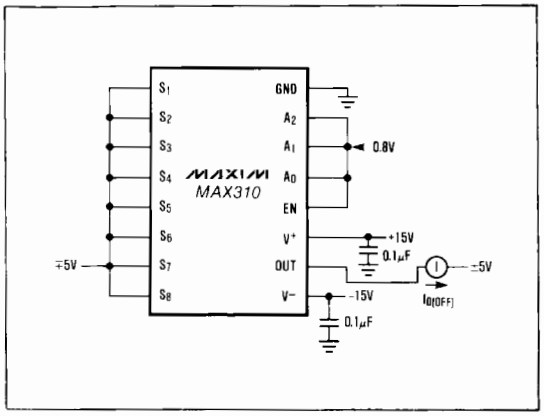


Figure 11. OFF Output Leakage Current Test Circuit.

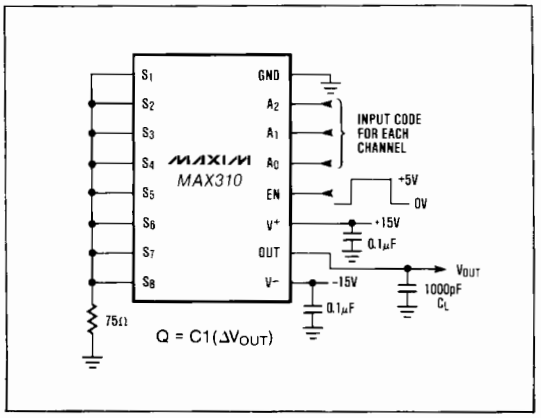


Figure 13. Charge Injection (Q) Test Circuit

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