THE DATASHEET OF

MAX4996LETG+

www.win-source.net 0086-755-83957316

19-4036; Rev 0; 2/08

Triple DPDT, Low-Capacitance Data Switches

General Description

The MAX4996/MAX4996L triple DPDT analog switches operate from a single +2.5V to +5.5V supply, and feature 2.0Ω (typ) on-resistance, low 6pF (typ) on-capacitance, and low power-supply current consumption. The MAX4996/MAX4996L combine the low capacitance and low resistance necessary for high-frequency switching applications in portable electronics.

The MAX4996/MAX4996L have three logic inputs to control the switches in pairs. The MAX4996 has an active-high enable input (EN) to disable the switches, while the MAX4996L has an active-low enable input ($\overline{EN}$) to disable the switches. The enable input decreases the supply current and also places the COM_ outputs in a high-impedance state.

The MAX4996/MAX4996L feature a 5µA (max) supply-current consumption when the logic inputs are not rail-to-rail. This feature is especially valuable in applications where direct interface to low-voltage processors is necessary.

The MAX4996/MAX4996L are available in a space-saving 24-pin (3.5mm x 3.5mm) TQFN package and operate over the -40°C to +85°C temperature range.

Applications

SD Card Switching

USB Signal Switching

UART Signal Switching

Cell Phones

PDAs

GPS

Portable Media Players (PMP)

Ordering Information

PART	PIN-PACKAGE	PACKAGE CODE
MAX4996ETG+	24 TQFN-EP*	T243A3-1
MAX4996LETG+	24 TQFN-EP*	T243A3-1

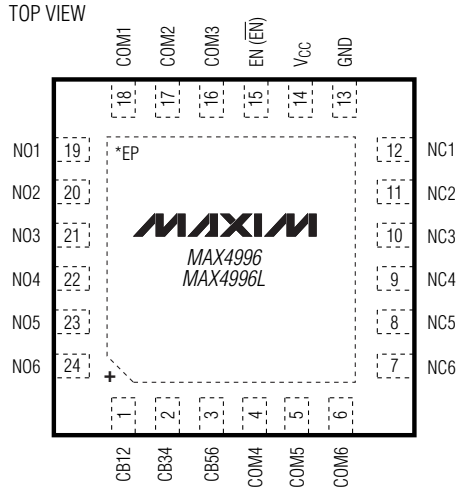
Note: *All devices operate over the -40°C to +85°C extended temperature range.*
+Denotes a lead-free package.
**EP = Exposed paddle.*

Typical Operating Circuit appears at end of data sheet.

Features

- **Multiplex SD2.0/SDIO Interfaces**
- **Low Power Consumption (2µA max)**
- **+2.5V to +5.5V Supply Voltage Range**
- **Rail-to-Rail Signal Handling**
- **Low-Capacitance Switches, 6pF (typ)**
- **Low On-Resistance, 2Ω (typ)**
- **Excellent On-Resistance Flatness Over the Range of 0V to V_{CC}**
- **Wide -3dB Bandwidth, 670MHz**
- **Small 24-Pin TQFN (3.5mm x 3.5mm)**

Pin Configuration/Truth Tables



TQFN
3.5mm x 3.5mm

($\overline{EN}$) FOR MAX4996L ONLY.
*CONNECT EXPOSED PADDLE TO GROUND.

TRUTH TABLES

MAX4996/MAX4996L

CB12	NO1/NO2	NC1/NC2
LOW	OFF	ON
HIGH	ON	OFF
CB34	**NO3/NO4**	**NC3/NC4**
LOW	OFF	ON
HIGH	ON	OFF
CB56	**NO5/NO6**	**NC5/NC6**
LOW	OFF	ON
HIGH	ON	OFF

MAX4996

EN	CB_	NO_	NC_
HIGH	LOW	OFF	ON
HIGH	HIGH	ON	OFF
LOW	X	OFF	OFF

MAX4996L

$\overline{EN}$	CB_	NO_	NC_
LOW	LOW	OFF	ON
LOW	HIGH	ON	OFF
HIGH	X	OFF	OFF

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Triple DPDT, Low-Capacitance Data Switches

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +6.0V
EN, $\overline{EN}$, CB_ .....-0.3V to +6.0V
All Other Pins to GND .....-0.3V to V_{CC} + 0.3V
Continuous Current
NO_, NC_, COM_ .....±150mA
Peak Current NO_, NC_, COM_
(pulsed at 1ms, 50% Duty Cycle).....±300mA
(pulsed at 1ms, 10% Duty Cycle).....±450mA
ESD per Human Body Model.....±2kV

Continuous Power Dissipation (T_A = +70°C)
24-Pin TQFN (derate 20.8mW/°C
above +70°C).....1228mW
Thermal Resistance (Note 1)
θ_{JA}.....65.1°C/W
θ_{JC}.....5.4°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering).....+300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations see **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.5V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 2.8V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG SWITCH						
Analog Signal Range	V_{COM}, V_{NO}, $V_{NC_}$		0		V_{CC}	V
On-Resistance	R_{ON}	$V_{COM_}$ = 0 to V_{CC} , $I_{COM_}$ = 25mA		2	4	Ω
On-Resistance Match Between Channels	ΔR_{ON}	V_{CC} = 2.8V, $I_{COM_}$ = 25mA; $V_{NO_}$ = 1.5V or $V_{NC_}$ = 1.5V (Note 4)		0.1	0.2	Ω
On-Resistance Flatness	R_{FLAT}	V_{CC} = 2.5V, $I_{COM_}$ = 25mA; $V_{COM_}$ = 0 to V_{CC} (Note 5)		0.2	0.5	Ω
Off-Leakage Current	$I_{COM_}$ (OFF)	V_{CC} = 4V, $V_{COM_}$ = 0, 4V; $V_{NO_}$, $V_{NC_}$ = 4V, 0	-250		+250	nA
		V_{CC} = 5.5V, $V_{COM_}$ = 5.5V; V_{NO}, V_{NC} with 50µA sink current to GND			180	µA
On-Leakage Current	$I_{COM_}$ (ON)	V_{CC} = 5.5V, $V_{COM_}$ = 0, 5.5V; $V_{NO_}$, $V_{NC_}$unconnected	-250		+250	nA
-3dB Bandwidth	BW	R_L = R_S = 50Ω, C_L = 5pF, Figure 4		670		MHz
Off-Isolation	V_{ISO}	f = 1MHz, $V_{NO_}$, $V_{NC_}$ = 0; C_L = 5pF, R_L = R_S = 50Ω, Figure 4 (Note 6)		-60		dB
Crosstalk	V_{CT}	f = 1MHz, $V_{NO_}$, $V_{NC_}$ = 0; R_L = R_S = 50Ω, Figure 4 (Note 7)		-120		dB
LOGIC INPUTS						
Input Logic High	V_{IH}		1.4			V
Input Logic Low	V_{IL}				0.5	V
Input Leakage Current	I_{LEAK}	0 ≤ V ≤ V_{IL} and V_{IH} ≤ V ≤ V_{CC}; V_{CC} = 5.5V	-250		+250	nA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.5V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 2.8V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SWITCH DYNAMICS							
Turn-On Time	t_{ON}	V_{CC} = 2.7V, $V_{NO_}$ or $V_{NC_}$ = 1.5V; R_L = 50Ω, C_L = 35pF, Figure 1				100	µs
Turn-Off Time	t_{OFF}	V_{CC} = 2.7V, $V_{NO_}$ or $V_{NC_}$ = 1.5V; R_L = 50Ω, C_L = 35pF, Figure 1				6	µs
Break-Before-Make Interval	t_{BBM}	V_{CC} = 2.7V ; $V_{NO_}$, or $V_{NC_}$ = 1.5V; R_L = 50Ω, C_L = 35pF, Figure 2			10		µs
Output Skew Between Switches	t_{SKEW}	R_L = R_S = 50Ω, Figure 3			40		Ps
NO or NC Off-Capacitance	$C_{NO_ (OFF)}$ $C_{NC_ (OFF)}$	f = 10MHz, V_{BIAS} = 0V, signal = 500mV_{P-P}, Figure 5			2.5		pF
COM Off-Capacitance	$C_{COM_ (OFF)}$	f = 10MHz, V_{BIAS} = 0V, signal = 500mV_{P-P}, Figure 5			4		pF
COM On-Capacitance	$C_{COM_ (ON)}$	f = 10MHz, V_{BIAS} = 0V, signal = 500mV_{P-P}, Figure 5			6		pF
Operating Power-Supply Range	V_{CC}			2.5		5.5	V
Shutdown Supply Current		V_{EN} = 0 (MAX4996), $V_{\overline{EN}}$ = V_{CC} (MAX4996L)			0.1	0.5	µA
V_{CC} Supply Current	I_{CC}	$V_{CB_}$ = 0 or V_{CC}; V_{EN} = V_{CC} (MAX4996); $V_{\overline{EN}}$ = 0 (MAX4996L)	V_{CC} = 2.8V		1	2	µA
			V_{CC} = 5.5V		5	10	
Increase in Supply Current with V_{CB} / V_{EN} Voltage		0 ≤ $V_{CB_}$ ≤ V_{IL} or V_{IH} ≤ $V_{CB_}$ ≤ V_{CC} or 0 ≤ V_{EN} ≤ V_{IL} or V_{IH} ≤ V_{EN} ≤ V_{CC}				5	µA
ESD Protection		Human Body Model			±2		kV

Note 2: The algebraic convention is used. The most negative value is shown in the minimum column.

Note 3: Parts are 100% tested at T_A = +25°C. Limits across the full temperature range are guaranteed by correlation and design.

Note 4: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Note 6: Off-isolation = $20\log_{10} [V_{COM_} / (V_{NO_}$ or $V_{NC_})]$, $V_{COM_}$ = output, $V_{NO_}$ or $V_{NC_}$ = input to off switch.

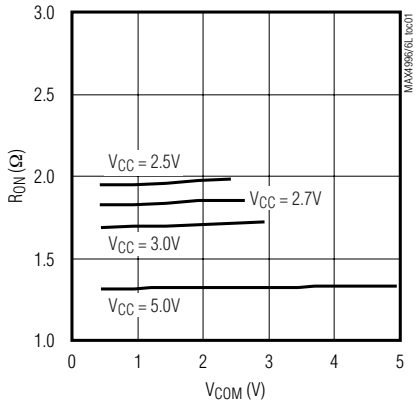
Note 7: Between any two switches.

Triple DPDT, Low-Capacitance Data Switches

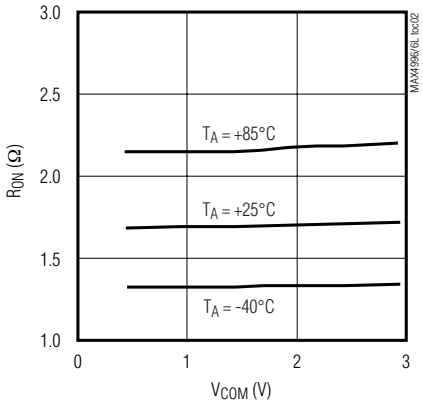
Typical Operating Characteristics

(V_{CC} = 3V, T_A = +25°C, unless otherwise noted.)

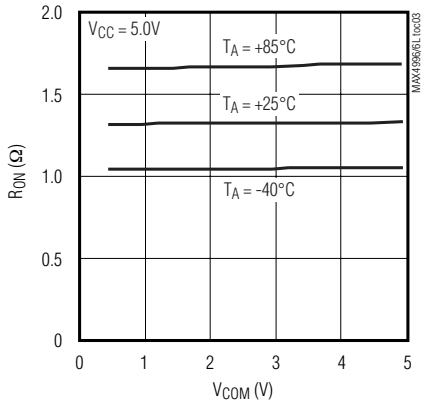
ON-RESISTANCE vs. V_{COM}



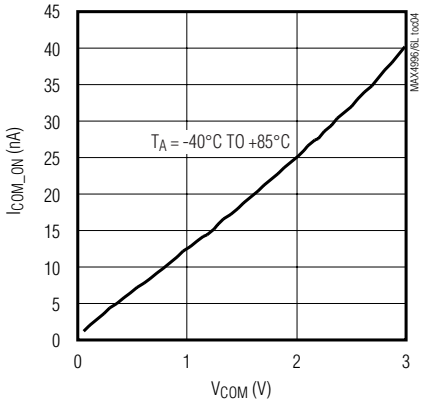
ON-RESISTANCE vs. V_{COM}



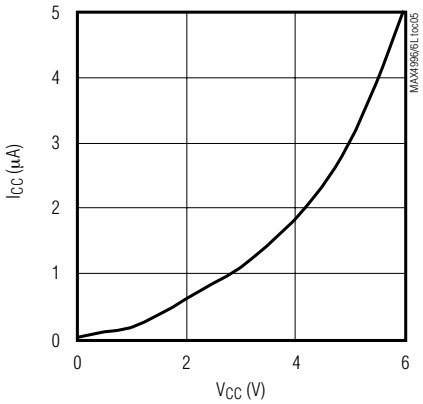
ON-RESISTANCE vs. V_{COM}



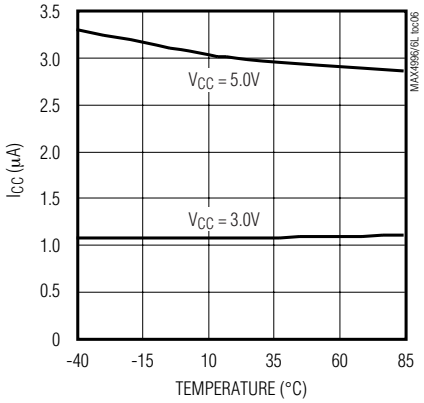
COM_ON LEAKAGE CURRENT vs. OVERTEMPERATURE



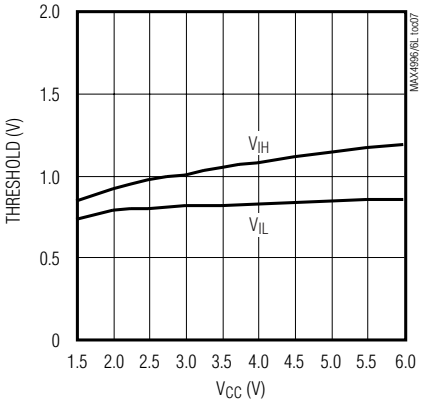
SUPPLY CURRENT vs. SUPPLY VOLTAGE



QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



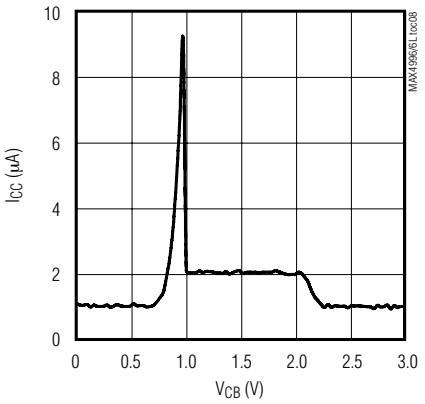
LOGIC THRESHOLD vs. SUPPLY VOLTAGE



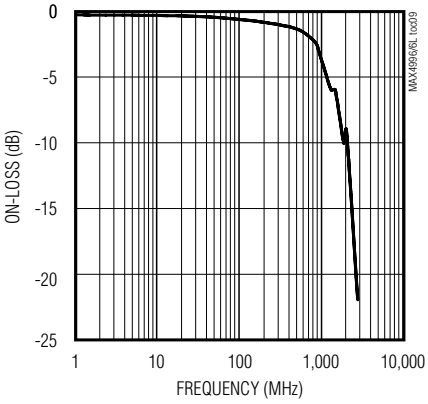
Typical Operating Characteristics (continued)

(V_{CC} = 3V, T_A = +25°C, unless otherwise noted.)

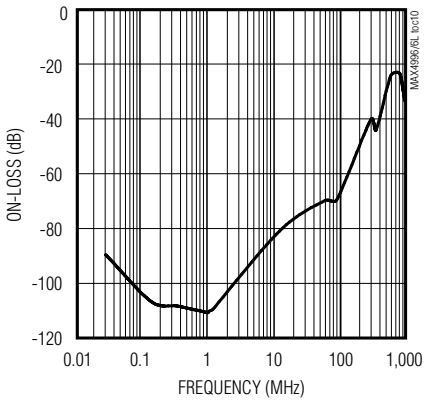
QUIESCENT SUPPLY CURRENT vs. LOGIC LEVEL



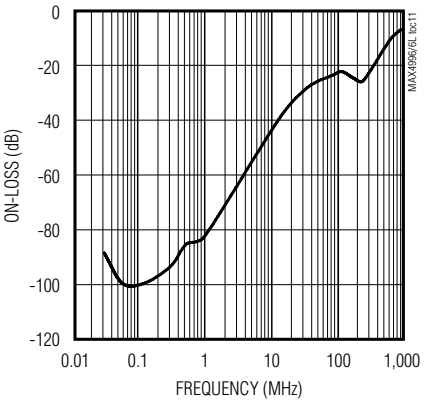
INPUT ON-LOSS FREQUENCY RESPONSE



INPUT CROSSTALK FREQUENCY RESPONSE



INPUT OFF-ISOLATION FREQUENCY RESPONSE



Pin Description

PIN	NAME	FUNCTION
1	CB12	Digital Control Input for Analog Switches 1 and 2. Drive CB12 low to connect COM1 to NC1 and COM2 to NC2. Drive CB12 high to connect COM1 to NO1 and COM2 to NO2.
2	CB34	Digital Control Input for Analog Switches 3 and 4. Drive CB34 low to connect COM3 to NC3 and COM4 to NC4. Drive CB34 high to connect COM3 to NO3 and COM4 to NO4.
3	CB56	Digital Control Input for Analog Switches 5 and 6. Drive CB56 low to connect COM5 to NC5 and COM6 to NC6. Drive CB56 high to connect COM5 to NO5 and COM6 to NO6.
4	COM4	Analog Switch 4—Common Terminal
5	COM5	Analog Switch 5—Common Terminal
6	COM6	Analog Switch 6—Common Terminal
7	NC6	Analog Switch 6—Normally Closed Terminal
8	NC5	Analog Switch 5—Normally Closed Terminal
9	NC4	Analog Switch 4—Normally Closed Terminal
10	NC3	Analog Switch 3—Normally Closed Terminal
11	NC2	Analog Switch 2—Normally Closed Terminal
12	NC1	Analog Switch 1—Normally Closed Terminal
13	GND	Ground
14	V_{CC}	Positive Supply Voltage. Bypass V_{CC} to GND with a 0.1µF ceramic capacitor as close as possible to the device.
15	EN, $\overline{EN}$	Enable Logic Input. For the MAX4996, drive EN high to enable all the switches. Drive EN low to disable all switches. For the MAX4996L, drive $\overline{EN}$ low to enable all the switches. Drive $\overline{EN}$ high to disable all switches. COM_ is high impedance when the switch is disabled. (See *Pin Configuration/Truth Tables*.)
16	COM3	Analog Switch 3—Common Terminal
17	COM2	Analog Switch 2—Common Terminal
18	COM1	Analog Switch 1—Common Terminal
19	NO1	Analog Switch 1—Normally Open Terminal
20	NO2	Analog Switch 2—Normally Open Terminal
21	NO3	Analog Switch 3—Normally Open Terminal
22	NO4	Analog Switch 4—Normally Open Terminal
23	NO5	Analog Switch 5—Normally Open Terminal
24	NO6	Analog Switch 6—Normally Open Terminal
—	EP	Exposed Paddle. Internally connected to GND. Connect to a large ground plane to maximize thermal performance; not intended as an electrical connection point.

Timing Circuits/Timing Diagrams

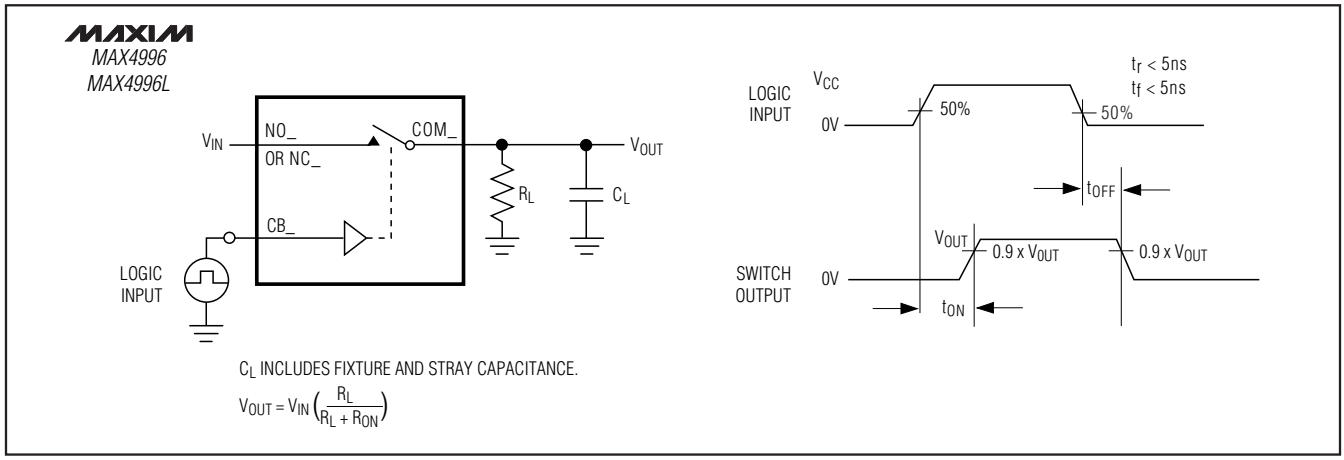


Figure 1. Switching Time

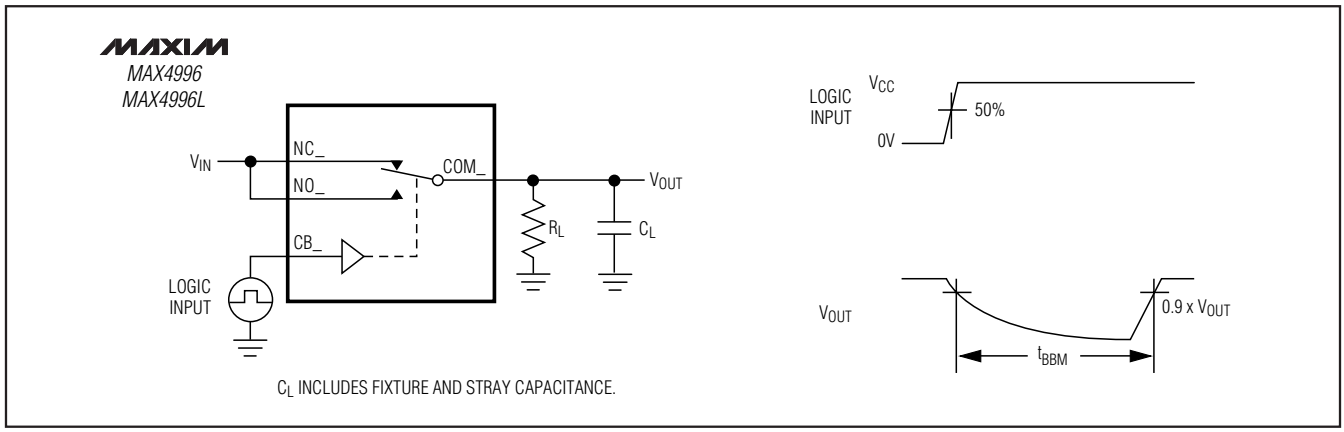


Figure 2. Break-Before-Make Interval

Timing Circuits/Timing Diagrams (continued)

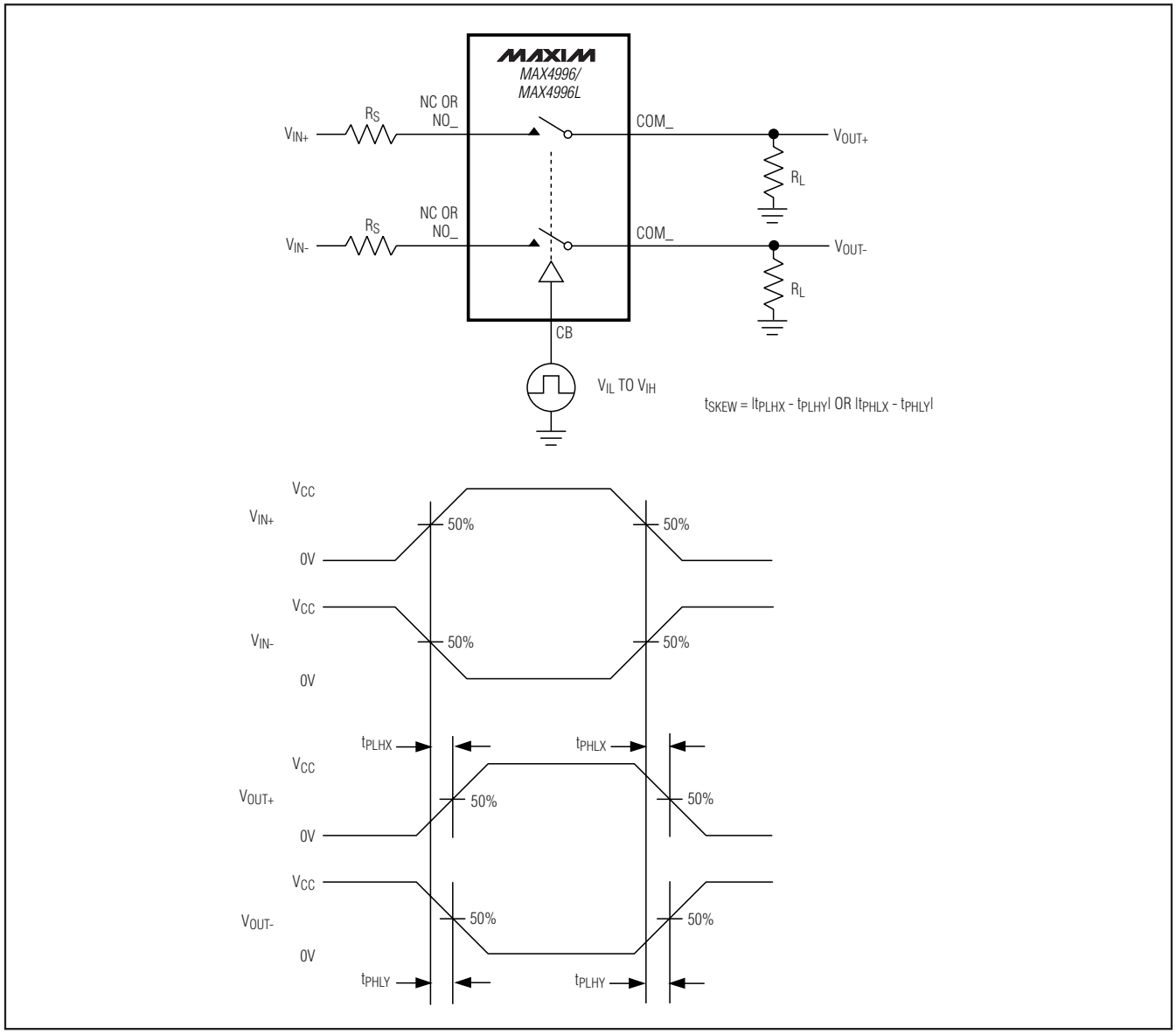


Figure 3. Input/Output Skew Timing Diagram

Timing Circuits/Timing Diagrams (continued)

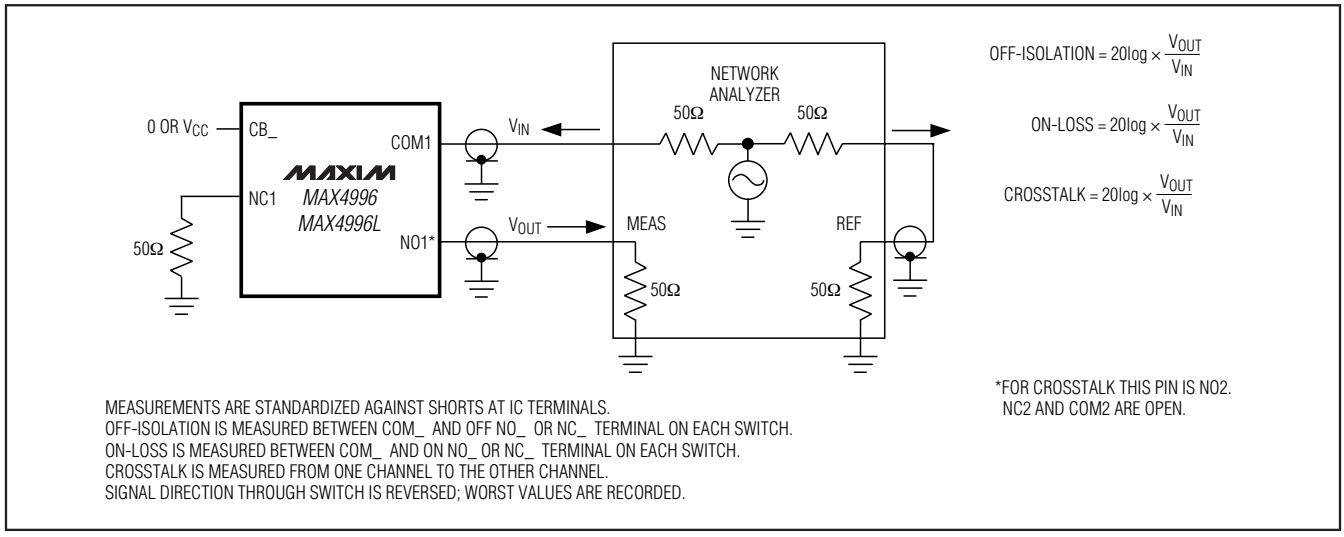


Figure 4. On-Loss, Off-Isolation, and Crosstalk

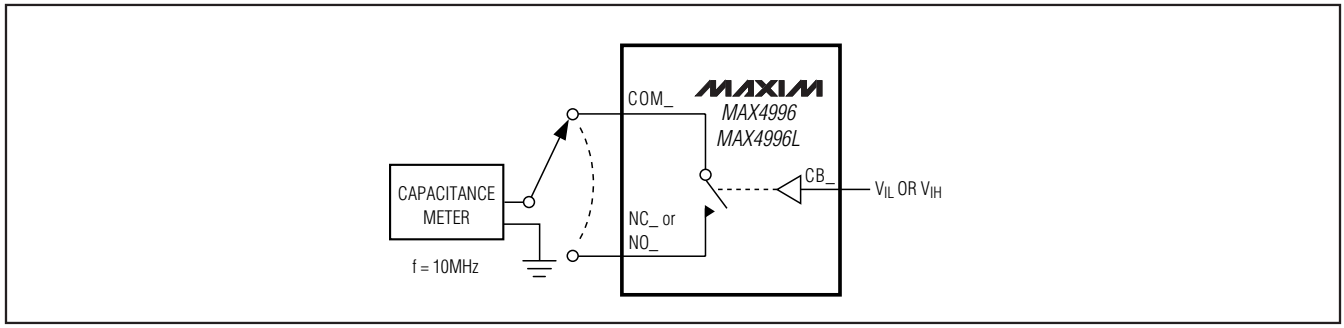


Figure 5. Channel On-/Off-Capacitance

Triple DPDT, Low-Capacitance Data Switches

Detailed Description

The MAX4996/MAX4996L triple DPDT analog switches operate from a single +2.5V to +5.5V supply and feature 2.0Ω (typ) on-resistance, low 6pF (typ) on-capacitance, and low power-supply current consumption. The combination of low resistance and low capacitance make this switch ideal for high-frequency applications.

The MAX4996 has an active-high enable input (EN) to disable the switches, while the MAX4996L has an active-low enable input ($\overline{EN}$) to disable the switches. The enable input decreases the supply current and also places the COM_ outputs in a high-impedance state.

Digital Control Inputs

Each pair of switches feature a digital-control logic input: CB_. CB_ controls the position of the switches as shown in the *Pin Configuration/Truth Tables*. The MAX4996/MAX4996L also feature an enable input to turn all switches on or off. Drive EN low on the MAX4996, or $\overline{EN}$ high on the MAX4996L, to disable the switches. While disabled, the switches are high-impedance and the supply current drops to 0.1µA (typ). To enable all switches, drive EN high on the MAX4996 or $\overline{EN}$ low on the MAX4996L.

Driving all digital inputs (CB_, EN, $\overline{EN}$) rail-to-rail minimizes supply current.

Analog Signal Levels

The on-resistance of the MAX4996/MAX4996L are very low and stable as the analog input signals are swept from ground to V_{CC} (see the *Typical Operating Characteristics*). These switches are bidirectional, allowing NO_, NC_, and COM_ to be configured as either inputs or outputs.

Applications Information

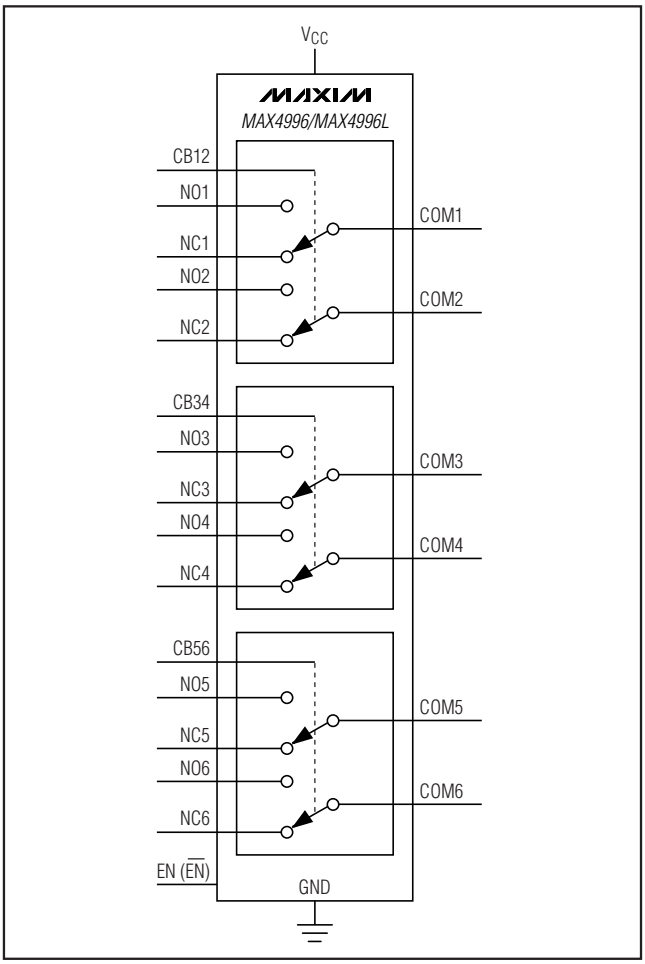
Power-Supply Bypassing

Power-supply bypassing improves noise margin and prevents switching noise from propagating from the V_{CC} supply to other components. A 0.1µF ceramic capacitor connected from V_{CC} to GND is adequate for most applications.

Power-Supply Sequencing

Always apply V_{CC} before the analog signals.

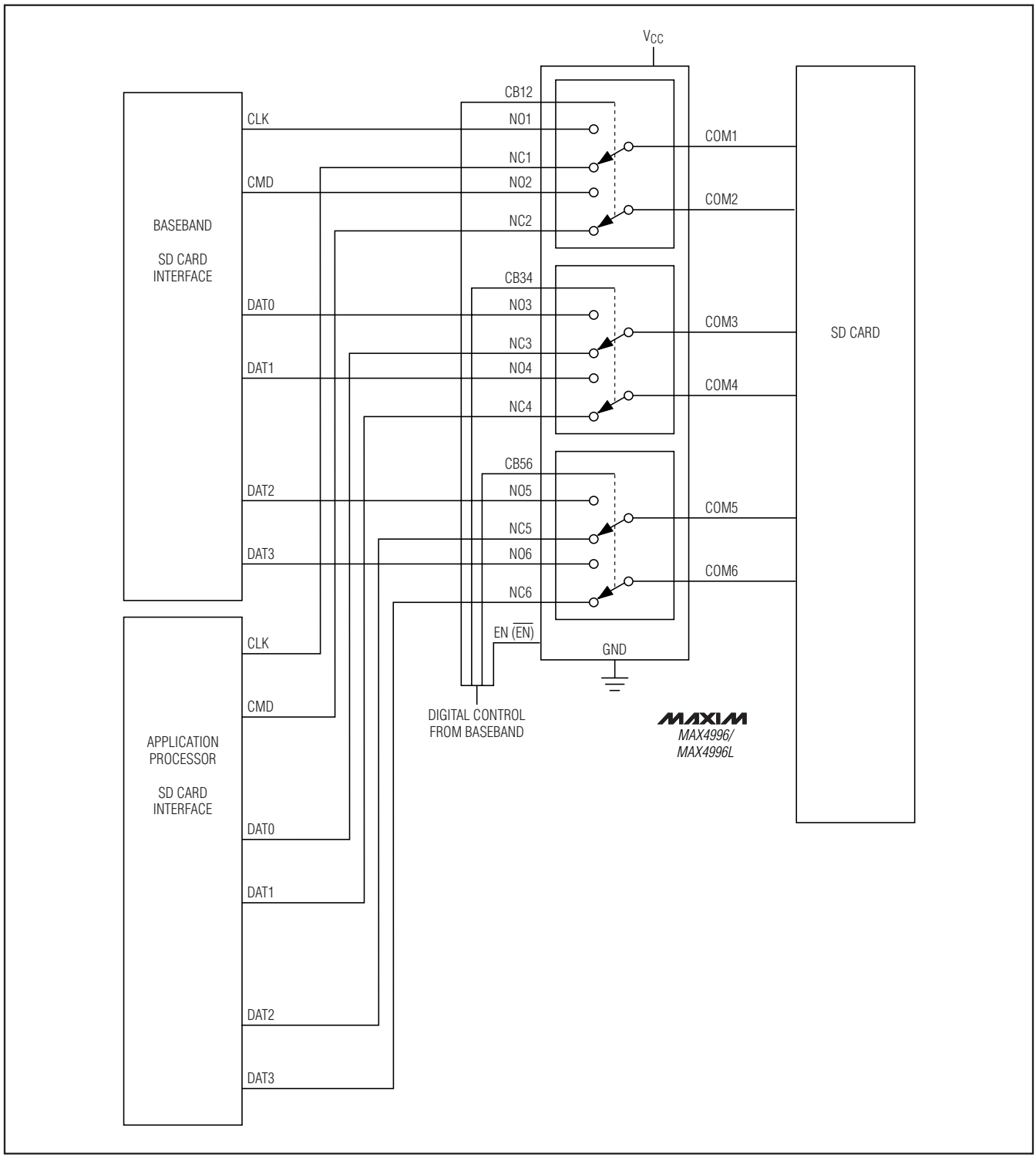
Functional Diagram



Chip Information

PROCESS: BiCMOS

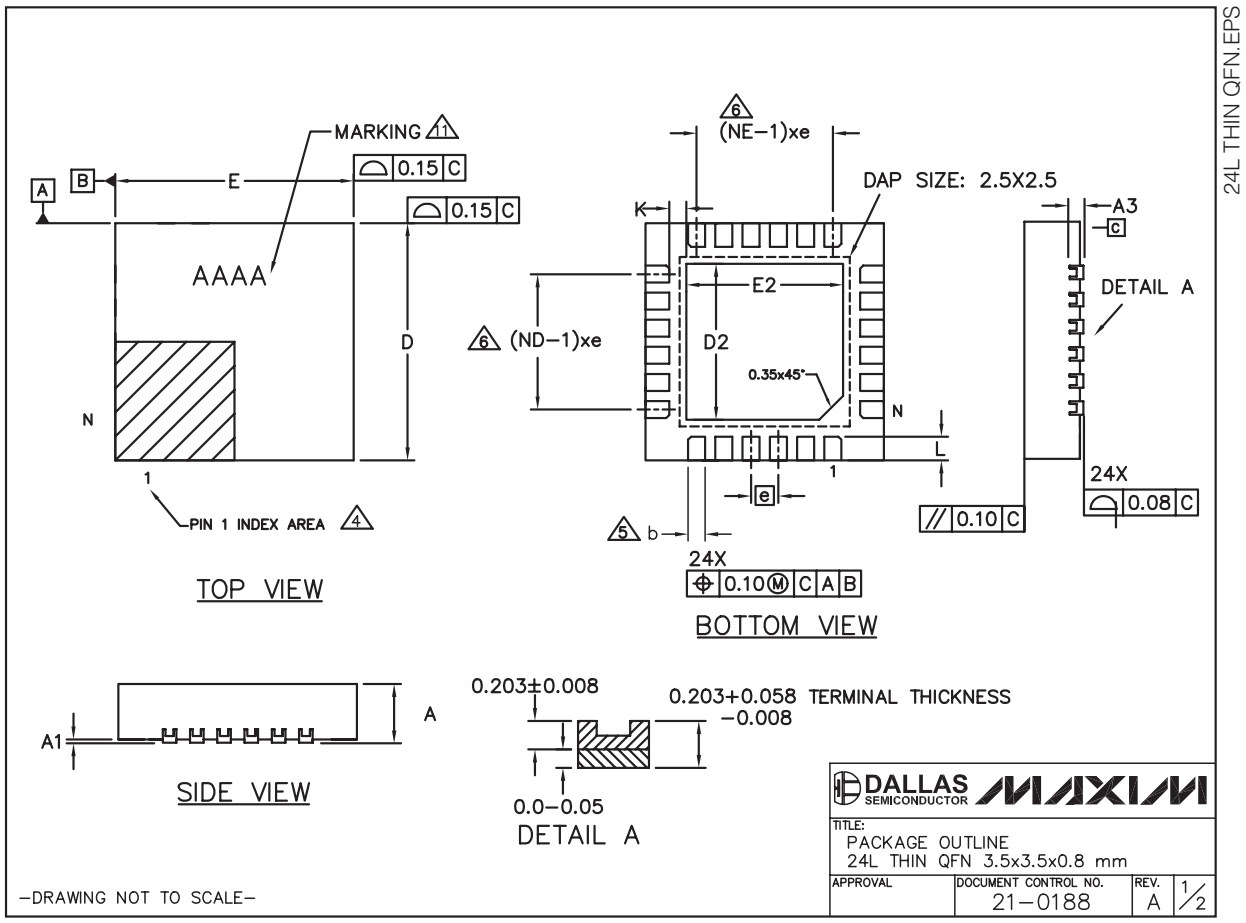
Typical Operating Circuit



Triple DPDT, Low-Capacitance Data Switches

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95–1 SPP–012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. REFER TO JEDEC MO–220 EXCEPT D2, E2, & L DIMENSIONS.
10. WARPAGE SHALL NOT EXCEED 0.10mm.
11. MARKING IS FOR PACKAGE ORIENTATION PURPOSE ONLY.

COMMON DIMENSION				NOTE
REF.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	
A1	0	–	0.05	
A3		0.20 REF		
b	0.15	0.20	0.25	
D	3.40	3.50	3.60	
E	3.40	3.50	3.60	
e		0.40 BSC.		
K	0.25	–	–	
L	0.30	0.35	0.40	
N		24		
ND		6		
NE		6		

EXPOSED PAD VARIATIONS						
	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T243A3–1	2.20	2.30	2.40	2.20	2.30	2.40

–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM

TITLE:
PACKAGE OUTLINE
24L THIN QFN 3.5x3.5x0.8 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21–0188	A	2/2

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