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THE DATASHEET OF

MCP42100-I/P

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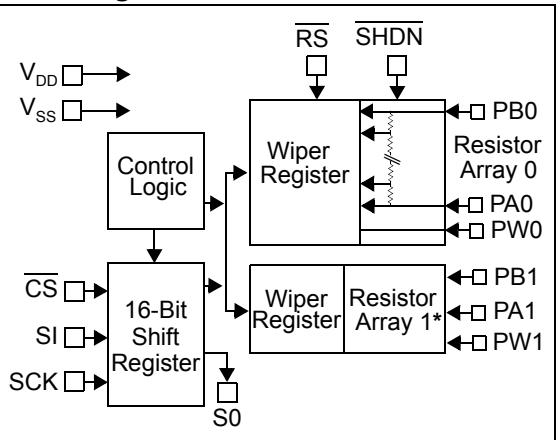
MCP41XXX/42XXX

Single/Dual Digital Potentiometer with SPI™ Interface

Features

- 256 taps for each potentiometer
- Potentiometer values for 10 kΩ, 50 kΩ and 100 kΩ
- Single and dual versions
- SPI™ serial interface (mode 0,0 and 1,1)
- ±1 LSB max INL & DNL
- Low power CMOS technology
- 1 µA maximum supply current in static operation
- Multiple devices can be daisy-chained together (MCP42XXX only)
- Shutdown feature open circuits of all resistors for maximum power savings
- Hardware shutdown pin available on MCP42XXX only
- Single supply operation (2.7V - 5.5V)
- Industrial temperature range: -40°C to +85°C
- Extended temperature range: -40°C to +125°C

Block Diagram



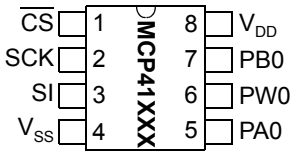
*Potentiometer P1 is only available on the dual MCP42XXX version.

Description

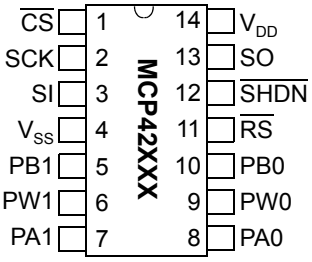
The MCP41XXX and MCP42XXX devices are 256-position, digital potentiometers available in 10 kΩ, 50 kΩ and 100 kΩ resistance versions. The MCP41XXX is a single-channel device and is offered in an 8-pin PDIP or SOIC package. The MCP42XXX contains two independent channels in a 14-pin PDIP, SOIC or TSSOP package. The wiper position of the MCP41XXX/42XXX varies linearly and is controlled via an industry-standard SPI interface. The devices consume <1 µA during static operation. A software shutdown feature is provided that disconnects the "A" terminal from the resistor stack and simultaneously connects the wiper to the "B" terminal. In addition, the dual MCP42XXX has a $\overline{SHDN}$ pin that performs the same function in hardware. During shutdown mode, the contents of the wiper register can be changed and the potentiometer returns from shutdown to the new value. The wiper is reset to the mid-scale position (80h) upon power-up. The $\overline{RS}$ (reset) pin implements a hardware reset and also returns the wiper to mid-scale. The MCP42XXX SPI interface includes both the SI and SO pins, allowing daisy-chaining of multiple devices. Channel-to-channel resistance matching on the MCP42XXX varies by less than 1%. These devices operate from a single 2.7 - 5.5V supply and are specified over the extended and industrial temperature ranges.

Package Types

PDIP/SOIC



PDIP/SOIC/TSSOP



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1.0 ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS: 10 kΩ VERSION

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +2.7V to 5.5V, T_A = -40°C to +85°C (TSSOP devices are only specified at +25°C and +85°C). Typical specifications represent values for V_{DD} = 5V, V_{SS} = 0V, V_B = 0V, T_A = +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Rheostat Mode						
Nominal Resistance	R	8	10	12	kΩ	T_A = +25°C **(Note 1)**
Rheostat Differential Non Linearity	R-DNL	-1	±1/4	+1	LSB	**Note 2**
Rheostat Integral Non Linearity	R-INL	-1	±1/4	+1	LSB	**Note 2**
Rheostat Tempco	$\Delta R_{AB}/\Delta T$	—	800	—	ppm/°C	
Wiper Resistance	R_W	—	52	100	Ω	V_{DD} = 5.5V, I_W = 1 mA, code 00h
	R_W	—	73	125	Ω	V_{DD} = 2.7V, I_W = 1 mA, code 00h
Wiper Current	I_W	-1	—	+1	mA	
Nominal Resistance Match	ΔR/R	—	0.2	1	%	**MCP42010 only**, P0 to P1; T_A = +25°C
Potentiometer Divider						
Resolution	N	8	—	—	Bits	
Monotonicity	N	8	—	—	Bits	
Differential Non-Linearity	DNL	-1	±1/4	+1	LSB	**Note 3**
Integral Non-Linearity	INL	-1	±1/4	+1	LSB	**Note 3**
Voltage Divider Tempco	$\Delta V_W/\Delta T$	—	1	—	ppm/°C	Code 80h
Full Scale Error	V_{WFSE}	-2	-0.7	0	LSB	Code FFh, V_{DD} = 5V, see Figure 2-25
	V_{WFSE}	-2	-0.7	0	LSB	Code FFh, V_{DD} = 3V, see Figure 2-25
Zero Scale Error	V_{WZSE}	0	+0.7	+2	LSB	Code 00h, V_{DD} = 5V, see Figure 2-25
	V_{WZSE}	0	+0.7	+2	LSB	Code 00h, V_{DD} = 3V, see Figure 2-25
Resistor Terminals						
Voltage Range	$V_{A,B,W}$	0	—	V_{DD}		**Note 4**
Capacitance (C_A or C_B)		—	15	—	pF	f = 1 MHz, Code = 80h, see Figure 2-30
Capacitance	C_W	—	5.6	—	pF	f = 1 MHz, Code = 80h, see Figure 2-30
Dynamic Characteristics (All dynamic characteristics use V_{DD} = 5V)						
Bandwidth -3dB	BW	—	1	—	MHz	V_B = 0V, Measured at Code 80h, Output Load = 30 pF
Settling Time	t_S	—	2	—	µS	$V_A = V_{DD}$,V_B = 0V, ±1% Error Band, Transition from Code 00h to Code 80h, Output Load = 30 pF
Resistor Noise Voltage	e_{NWB}	—	9	—	nV/√Hz	V_A = Open, Code 80h, f =1 kHz
Crosstalk	C_T	—	-95	—	dB	$V_A = V_{DD}$, V_B = 0V **(Note 5)**
Digital Inputs/Outputs ($\overline{CS}$, SCK, SI, SO) See Figure 2-12 for $\overline{RS}$ and $\overline{SHDN}$ pin operation						
Schmitt Trigger High-Level Input Voltage	V_{IH}	$0.7V_{DD}$	—	—	V	
Schmitt Trigger Low-Level Input Voltage	V_{IL}	—	—	$0.3V_{DD}$	V	
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	—	$0.05V_{DD}$	—		
Low-Level Output Voltage	V_{OL}	—	—	0.40	V	I_{OL} = 2.1 mA, V_{DD} = 5V
High-Level Output Voltage	V_{OH}	V_{DD} - 0.5	—	—	V	I_{OH} = -400 µA, V_{DD} = 5V
Input Leakage Current	I_{LI}	-1	—	+1	µA	$\overline{CS}$ = V_{DD}, V_{IN} = V_{SS} or V_{DD}, includes V_A $\overline{SHDN}$=0
Pin Capacitance (All inputs/outputs)	C_{IN}, C_{OUT}	—	10	—	pF	V_{DD} = 5.0V, T_A = +25°C, f_c = 1 MHz
Power Requirements						
Operating Voltage Range	V_{DD}	2.7	—	5.5	V	
Supply Current, Active	I_{DDA}	—	340	500	µA	V_{DD} = 5.5V, $\overline{CS}$ = V_{SS}, f_{SCK} = 10 MHz, SO = Open, Code FFh **(Note 6)**
Supply Current, Static	I_{DDS}	—	0.01	1	µA	$\overline{CS}$, $\overline{SHDN}$, $\overline{RS}$ = V_{DD} = 5.5V, SO = Open **(Note 6)**
Power Supply Sensitivity	PSS	—	0.0015	0.0035	%/%	V_{DD} = 4.5V - 5.5V, V_A = 4.5V, Code 80h
	PSS	—	0.0015	0.0035	%/%	V_{DD} = 2.7V - 3.3V, V_A = 2.7V, Code 80h

Note 1: $V_{AB} = V_{DD}$, no connection on wiper.

2: Rheostat position non-linearity R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. I_W = 50 µA for V_{DD} = 3V and I_W = 400 µA for V_{DD} = 5V for 10 kΩ version. See Figure 2-26 for test circuit.

3: INL and DNL are measured at V_W with the device configured in the voltage divider or potentiometer mode. $V_A = V_{DD}$ and V_B = 0V. DNL specification limits of ±1 LSB max are specified monotonic operating conditions. See Figure 2-25 for test circuit.

4: Resistor terminals A,B and W have no restrictions on polarity with respect to each other. Full-scale and zero-scale error were measured using Figure 2-25.

5: Measured at V_W pin where the voltage on the adjacent V_W pin is swinging full-scale.

6: Supply current is independent of current through the potentiometers.

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DC CHARACTERISTICS: 50 kΩ VERSION

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +2.7V to 5.5V, T_A = -40°C to +85°C (TSSOP devices are only specified at +25°C and +85°C). Typical specifications represent values for V_{DD} = 5V, V_{SS} = 0V, V_B = 0V, T_A = +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Rheostat Mode						
Nominal Resistance	R	35	50	65	kΩ	T_A = +25°C **(Note 1)**
Rheostat Differential Non-Linearity	R-DNL	-1	±1/4	+1	LSB	**Note 2**
Rheostat Integral Non-Linearity	R-INL	-1	±1/4	+1	LSB	**Note 2**
Rheostat Tempco	$\Delta R_{AB}/\Delta T$	—	800	—	ppm/°C	
Wiper Resistance	R_W	—	125	175	Ω	V_{DD} = 5.5V, I_W = 1 mA, code 00h
	R_W	—	175	250	Ω	V_{DD} = 2.7V, I_W = 1 mA, code 00h
Wiper Current	I_W	-1	—	+1	mA	
Nominal Resistance Match	ΔR/R	—	0.2	1	%	**MCP42050 only**, P0 to P1;T_A = +25°C
Potentiometer Divider						
Resolution	N	8	—	—	Bits	
Monotonicity	N	8	—	—	Bits	
Differential Non-Linearity	DNL	-1	±1/4	+1	LSB	**Note 3**
Integral Non-Linearity	INL	-1	±1/4	+1	LSB	**Note 3**
Voltage Divider Tempco	$\Delta V_W/\Delta T$	—	1	—	ppm/°C	Code 80h
Full-Scale Error	V_{WFSE}	-1	-0.25	0	LSB	Code FFh, V_{DD} = 5V, see Figure 2-25
	V_{WFSE}	-1	-0.35	0	LSB	Code FFh, V_{DD} = 3V, see Figure 2-25
Zero-Scale Error	V_{WZSE}	0	+0.25	+1	LSB	Code 00h, V_{DD} = 5V, see Figure 2-25
	V_{WZSE}	0	+0.35	+1	LSB	Code 00h, V_{DD} = 3V, see Figure 2-25
Resistor Terminals						
Voltage Range	$V_{A,B,W}$	0	—	V_{DD}		**Note 4**
Capacitance (C_A or C_B)		—	11	—	pF	f =1 MHz, Code = 80h, see Figure 2-30
Capacitance	C_W	—	5.6	—	pF	f =1 MHz, Code = 80h, see Figure 2-30
Dynamic Characteristics (All dynamic characteristics use V_{DD} = 5V)						
Bandwidth -3dB	BW	—	280	—	MHz	V_B = 0V, Measured at Code 80h, Output Load = 30 pF
Settling Time	t_S	—	8	—	µS	$V_A = V_{DD}$,V_B = 0V, ±1% Error Band, Transition from Code 00h to Code 80h, Output Load = 30 pF
Resistor Noise Voltage	e_{NWB}	—	20	—	nV/√Hz	V_A = Open, Code 80h, f =1 kHz
Crosstalk	C_T	—	-95	—	dB	$V_A = V_{DD}$, V_B = 0V **(Note 5)**
Digital Inputs/Outputs ($\overline{CS}$, SCK, SI, SO) See Figure 2-12 for $\overline{RS}$ and $\overline{SHDN}$ pin operation.						
Schmitt Trigger High-Level Input Voltage	V_{IH}	$0.7V_{DD}$	—	—	V	
Schmitt Trigger Low-Level Input Voltage	V_{IL}	—	—	$0.3V_{DD}$	V	
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	—	$0.05V_{DD}$	—		
Low-Level Output Voltage	V_{OL}	—	—	0.40	V	I_{OL} = 2.1 mA, V_{DD} = 5V
High-Level Output Voltage	V_{OH}	V_{DD} - 0.5	—	—	V	I_{OH} = -400 µA, V_{DD} = 5V
Input Leakage Current	I_{LI}	-1	—	+1	µA	$\overline{CS} = V_{DD}$, $V_{IN} = V_{SS}$ or V_{DD}, includes V_A $\overline{SHDN}$=0
Pin Capacitance (All inputs/outputs)	C_{IN}, C_{OUT}	—	10	—	pF	V_{DD} = 5.0V, T_A = +25°C, f_c = 1 MHz
Power Requirements						
Operating Voltage Range	V_{DD}	2.7	—	5.5	V	
Supply Current, Active	I_{DDA}	—	340	500	µA	V_{DD} = 5.5V, $\overline{CS} = V_{SS}$, f_{SCK} = 10 MHz, SO = Open, Code FFh **(Note 6)**
Supply Current, Static	I_{DDS}	—	0.01	1	µA	$\overline{CS}$, $\overline{SHDN}$, $\overline{RS} = V_{DD}$ = 5.5V, SO = Open **(Note 6)**
Power Supply Sensitivity	PSS	—	0.0015	0.0035	%/%	V_{DD} = 4.5V - 5.5V, V_A = 4.5V, Code 80h
	PSS	—	0.0015	0.0035	%/%	V_{DD} = 2.7V - 3.3V, V_A = 2.7V, Code 80h

Note 1: $V_{AB} = V_{DD}$, no connection on wiper.

2: Rheostat position non-linearity R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. $I_W = V_{DD}/R$ for +3V or +5V for 50 kΩ version. See Figure 2-26 for test circuit.

3: INL and DNL are measured at V_W with the device configured in the voltage divider or potentiometer mode. $V_A = V_{DD}$ and V_B = 0V. DNL specification limits of ±1 LSB max are specified monotonic operating conditions. See Figure 2-25 for test circuit.

4: Resistor terminals A,B and W have no restrictions on polarity with respect to each other. Full-scale and zero-scale error were measured using Figure 2-25.

5: Measured at V_W pin where the voltage on the adjacent V_W pin is swinging full scale.

6: Supply current is independent of current through the potentiometers.

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DC CHARACTERISTICS: 100 kΩ VERSION

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +2.7V to 5.5V, T_A = -40°C to +85°C (TSSOP devices are only specified at +25°C and +85°C). Typical specifications represent values for V_{DD} = 5V, V_{SS} = 0V, V_B = 0V, T_A = +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Rheostat Mode						
Nominal Resistance	R	70	100	130	kΩ	T_A = +25°C **(Note 1)**
Rheostat Differential Non-Linearity	R-DNL	-1	±1/4	+1	LSB	**Note 2**
Rheostat Integral Non-Linearity	R-INL	-1	±1/4	+1	LSB	**Note 2**
Rheostat Tempco	$\Delta R_{AB}/\Delta T$	—	800	—	ppm/°C	
Wiper Resistance	R_W	—	125	175	Ω	V_{DD} = 5.5V, I_W = 1 mA, code 00h
	R_W	—	175	250	Ω	V_{DD} = 2.7V, I_W = 1 mA, code 00h
Wiper Current	I_W	-1	—	+1	mA	
Nominal Resistance Match	ΔR/R	—	0.2	1	%	MCP42010 only, P0 to P1;T_A = +25°C
Potentiometer Divider						
Resolution	N	8	—	—	Bits	
Monotonicity	N	8	—	—	Bits	
Differential Non-Linearity	DNL	-1	±1/4	+1	LSB	**Note 3**
Integral Non-Linearity	INL	-1	±1/4	+1	LSB	**Note 3**
Voltage Divider Tempco	$\Delta V_W/\Delta T$	—	1	—	ppm/°C	Code 80h
Full-Scale Error	V_{WFSE}	-1	-0.25	0	LSB	Code FFh, V_{DD} = 5V, see Figure 2-25
	V_{WFSE}	-1	-0.35	0	LSB	Code FFh, V_{DD} = 3V, see Figure 2-25
Zero-Scale Error	V_{WZSE}	0	+0.25	+1	LSB	Code 00h, V_{DD} = 5V, see Figure 2-25
	V_{WZSE}	0	+0.35	+1	LSB	Code 00h, V_{DD} = 3V, see Figure 2-25
Resistor Terminals						
Voltage Range	$V_{A,B,W}$	0	—	V_{DD}		**Note 4**
Capacitance (C_A or C_B)		—	11	—	pF	f =1 MHz, Code = 80h, see Figure 2-30
Capacitance	C_W	—	5.6	—	pF	f =1 MHz, Code = 80h, see Figure 2-30
Dynamic Characteristics (All dynamic characteristics use V_{DD} = 5V.)						
Bandwidth -3dB	BW	—	145	—	MHz	V_B = 0V, Measured at Code 80h, Output Load = 30 pF
Settling Time	t_S	—	18	—	µS	V_A = V_{DD},V_B = 0V, ±1% Error Band, Transition from Code 00h to Code 80h, Output Load = 30 pF
Resistor Noise Voltage	e_{NWB}	—	29	—	nV/√Hz	V_A = Open, Code 80h, f =1 kHz
Crosstalk	C_T	—	-95	—	dB	V_A = V_{DD}, V_B = 0V **(Note 5)**
Digital Inputs/Outputs ($\overline{CS}$, SCK, SI, SO) See Figure 2-12 for $\overline{RS}$ and $\overline{SHDN}$ pin operation.						
Schmitt Trigger High-Level Input Voltage	V_{IH}	0.7V_{DD}	—	—	V	
Schmitt Trigger Low-Level Input Voltage	V_{IL}	—	—	0.3V_{DD}	V	
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	—	0.05V_{DD}	—		
Low-Level Output Voltage	V_{OL}	—	—	0.40	V	I_{OL} = 2.1 mA, V_{DD} = 5V
High-Level Output Voltage	V_{OH}	V_{DD} - 0.5	—	—	V	I_{OH} = -400 µA, V_{DD} = 5V
Input Leakage Current	I_{LI}	-1	—	+1	µA	$\overline{CS}$ = V_{DD}, V_{IN} = V_{SS} or V_{DD}, includes V_A $\overline{SHDN}$=0
Pin Capacitance (All inputs/outputs)	C_{IN}, C_{OUT}	—	10	—	pF	V_{DD} = 5.0V, T_A = +25°C, f_c = 1 MHz
Power Requirements						
Operating Voltage Range	V_{DD}	2.7	—	5.5	V	
Supply Current, Active	I_{DDA}	—	340	500	µA	V_{DD} = 5.5V, $\overline{CS}$ = V_{SS}, f_{SCK} = 10 MHz, SO = Open, Code FFh **(Note 6)**
Supply Current, Static	I_{DDS}	—	0.01	1	µA	$\overline{CS}$, $\overline{SHDN}$, $\overline{RS}$ = V_{DD} = 5.5V, SO = Open **(Note 6)**
Power Supply Sensitivity	PSS	—	0.0015	0.0035	%/%	V_{DD} = 4.5V - 5.5V, V_A = 4.5V, Code 80h
	PSS	—	0.0015	0.0035	%/%	V_{DD} = 2.7V - 3.3V, V_A = 2.7V, Code 80h

Note 1: V_{AB} = V_{DD}, no connection on wiper.

2: Rheostat position non-linearity R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. I_W = 50 µA for V_{DD} = 3V and I_W = 400 µA for V_{DD} = 5V for 10 kΩ version. See Figure 2-26 for test circuit.

3: INL and DNL are measured at V_W with the device configured in the voltage divider or potentiometer mode. V_A = V_{DD} and V_B = 0V. DNL specification limits of ±1 LSB max are specified monotonic operating conditions. See Figure 2-25 for test circuit.

4: Resistor terminals A,B and W have no restrictions on polarity with respect to each other. Full-scale and zero-scale error were measured using Figure 2-25.

5: Measured at V_W pin where the voltage on the adjacent V_W pin is swinging full-scale.

6: Supply current is independent of current through the potentiometers.

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Absolute Maximum Ratings †

V_{DD}.....7.0V

All inputs and outputs w.r.t. V_{SS} ..... -0.6V to V_{DD} +1.0V

Storage temperature .....-60°C to +150°C

Ambient temp. with power applied .....-60°C to +125°C

ESD protection on all pins .....≥ 2 kV

† Notice: Stresses above those listed under “maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

AC TIMING CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +2.7V to 5.5V, T_A = -40°C to +85°C.

Parameter	Sym	Min.	Typ.	Max.	Units	Conditions
Clock Frequency	F_{CLK}	—	—	10	MHz	V_{DD} = 5V **(Note 1)**
Clock High Time	t_{HI}	40	—	—	ns	
Clock Low Time	t_{LO}	40	—	—	ns	
$\overline{CS}$ Fall to First Rising CLK Edge	t_{CSSR}	40	—	—	ns	
Data Input Setup Time	t_{SU}	40	—	—	ns	
Data Input Hold Time	t_{HD}	10	—	—	ns	
SCK Fall to SO Valid Propagation Delay	t_{DO}		—	80	ns	C_L = 30 pF **(Note 2)**
SCK Rise to $\overline{CS}$ Rise Hold Time	t_{CHS}	30	—	—	ns	
SCK Rise to $\overline{CS}$ Fall Delay	t_{CS0}	10	—	—	ns	
$\overline{CS}$ Rise to CLK Rise Hold	t_{CS1}	100	—	—	ns	
$\overline{CS}$ High Time	t_{CSH}	40	—	—	ns	
Reset Pulse Width	t_{RS}	150	—	—	ns	**Note 2**
$\overline{RS}$ Rising to $\overline{CS}$ Falling Delay Time	t_{RSCS}	150	—	—	ns	**Note 2**
$\overline{CS}$ rising to $\overline{RS}$ or $\overline{SHDN}$ falling delay time	t_{SE}	40	—	—	ns	**Note 3**
$\overline{CS}$ low time	t_{CSL}	100	—	—	ns	**Note 3**
Shutdown Pulse Width	t_{SH}	150	—	—	ns	**Note 3**

Note 1: When using the device in the daisy-chain configuration, maximum clock frequency is determined by a combination of propagation delay time (t_{DO}) and data input setup time (t_{SU}). Max. clock frequency is therefore ~ 5.8 MHz based on SCK rise and fall times of 5 ns, t_{HI} = 40 ns, t_{DO} = 80 ns and t_{SU} = 40 ns.

2: Applies only to the MCP42XXX devices.

3: Applies only when using hardware pins to exit software shutdown mode, MCP42XXX only.

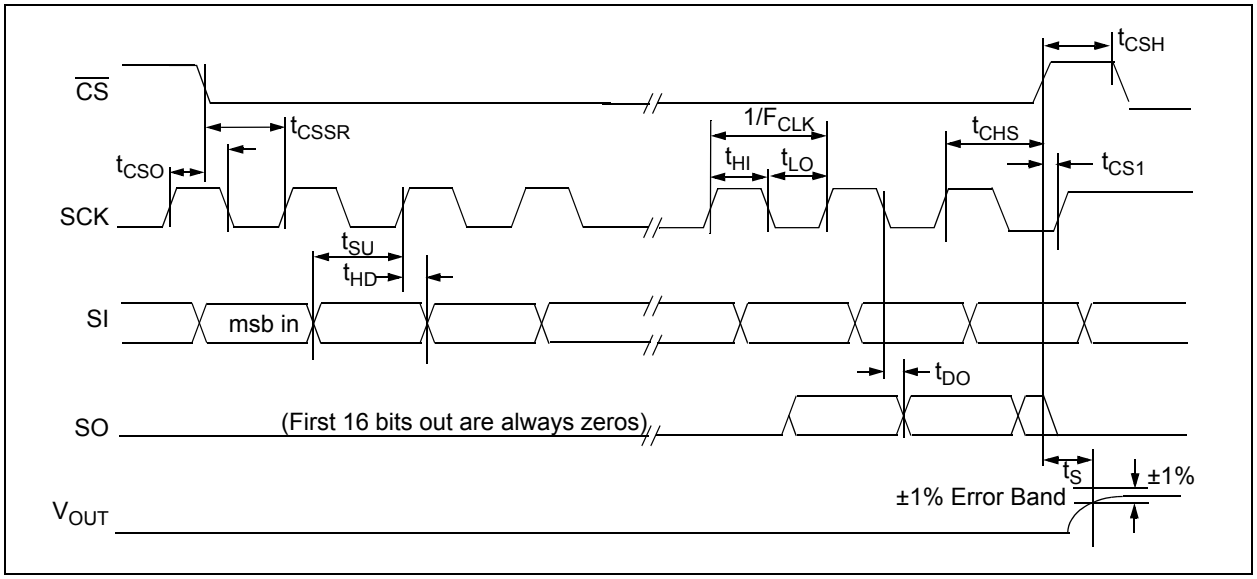

FIGURE 1-1: *Detailed Serial interface Timing.*

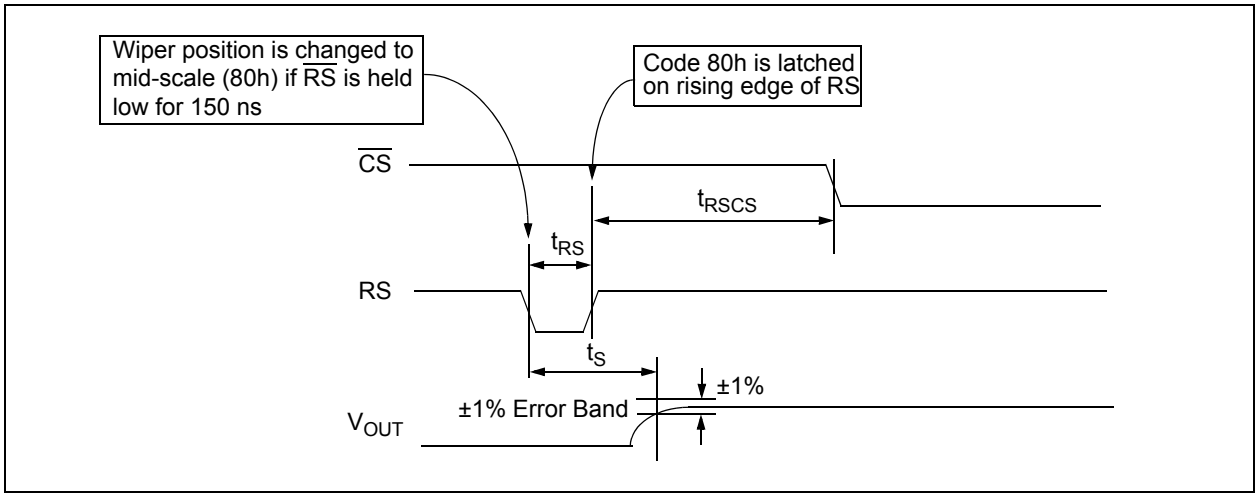

FIGURE 1-2: *Reset Timing.*

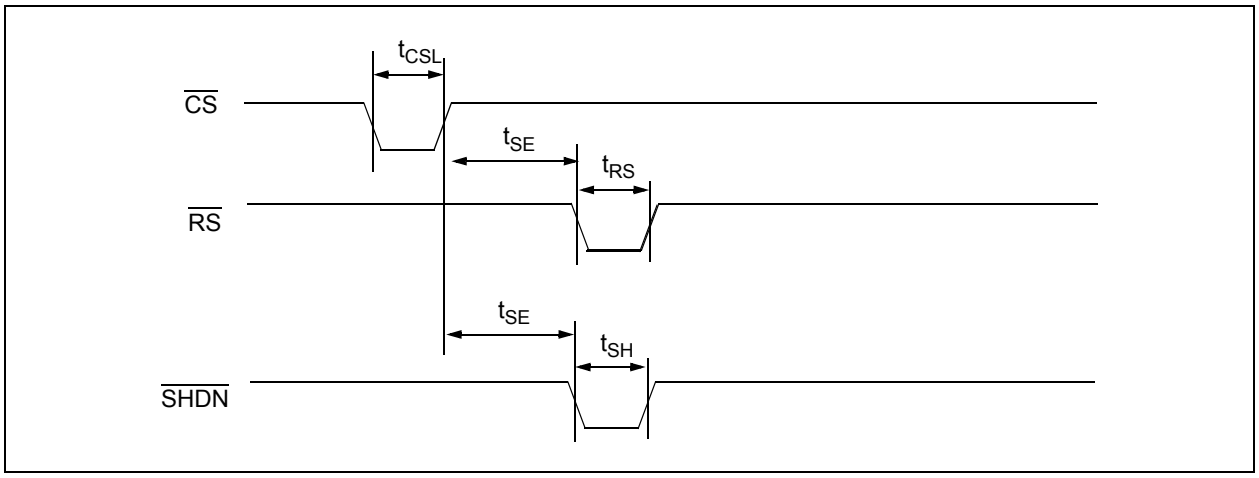

FIGURE 1-3: *Software Shutdown Exit Timing.*

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, curve represents 10 kΩ, 50 kΩ and 100 kΩ devices, V_{DD} = 5V, V_{SS} = 0V, T_A = +25°C, V_B = 0V.

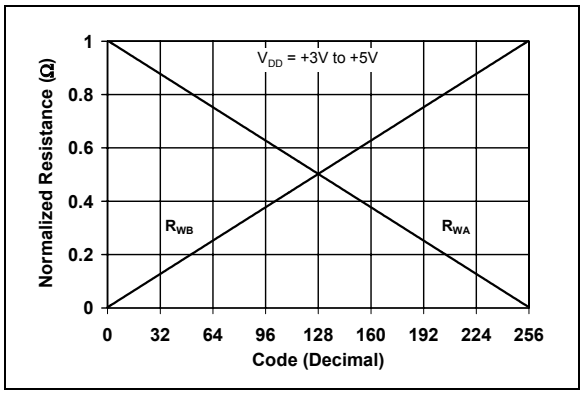

FIGURE 2-1: *Normalized Wiper to End Terminal Resistance vs. Code.*

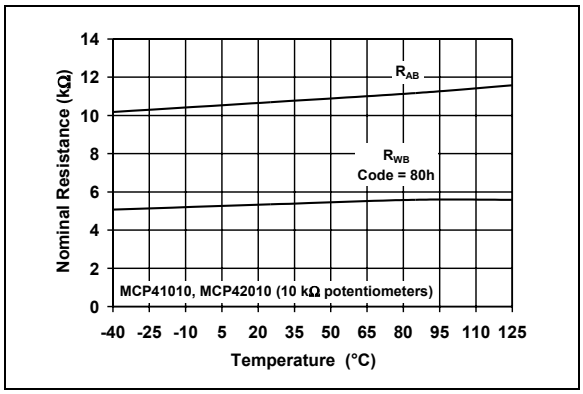

FIGURE 2-4: *Nominal Resistance 10 kΩ vs. Temperature.*

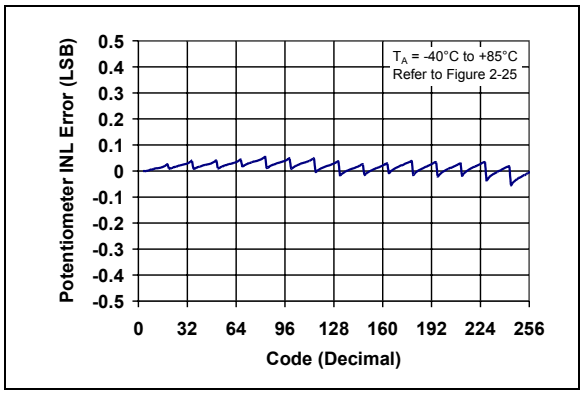

FIGURE 2-2: *Potentiometer INL Error vs. Code.*

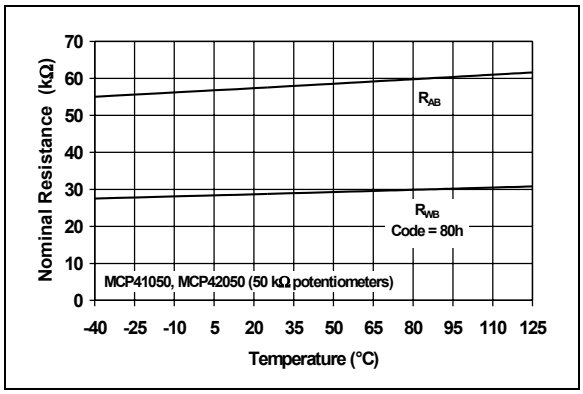

FIGURE 2-5: *Nominal Resistance 50 kΩ vs. Temperature.*

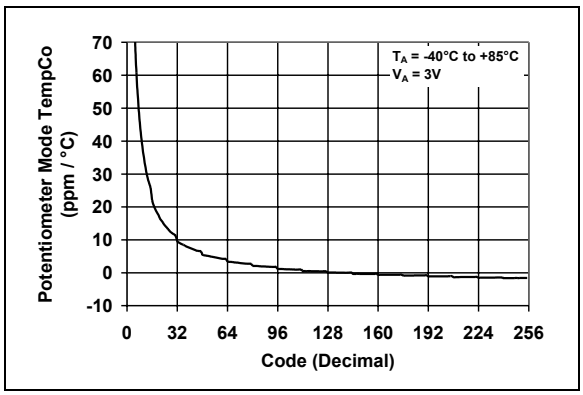

FIGURE 2-3: *Potentiometer Mode Tempco vs. Code.*

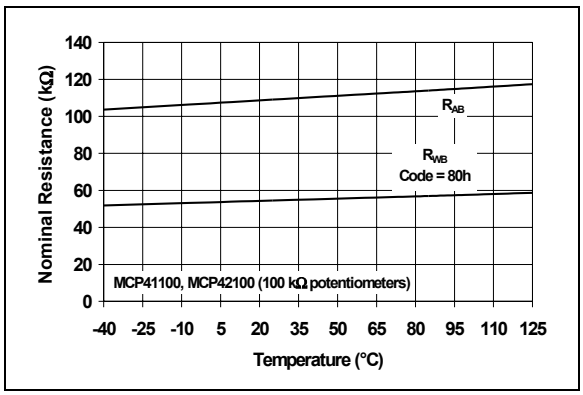

FIGURE 2-6: *Nominal Resistance 100 kΩ vs. Temperature.*

Note: Unless otherwise indicated, curve represents 10 kΩ, 50 kΩ and 100 kΩ devices, V_{DD} = 5V, V_{SS} = 0V, T_A = +25°C, V_B = 0V.

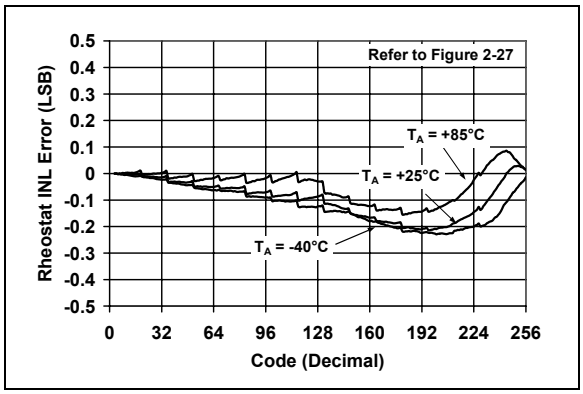

FIGURE 2-7: *Rheostat INL Error vs. Code.*

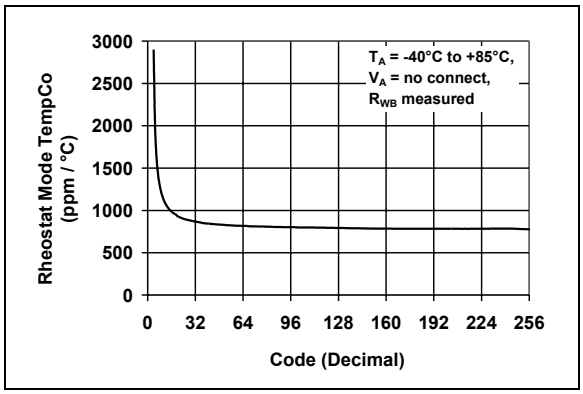

FIGURE 2-8: *Rheostat Mode Tempco vs. Code.*

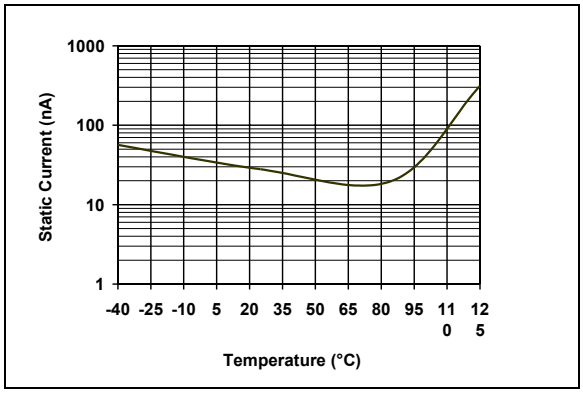

FIGURE 2-9: *Static Current vs. Temperature.*

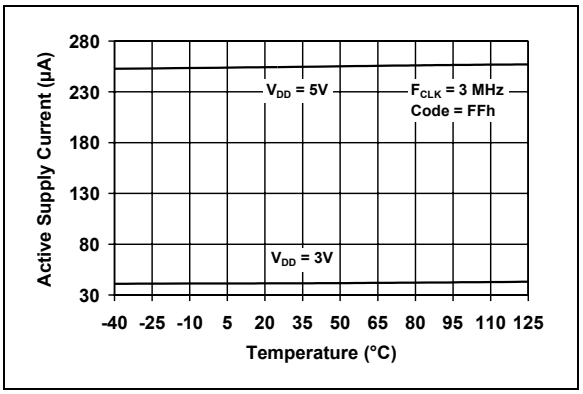

FIGURE 2-10: *Active Supply Current vs. Temperature.*

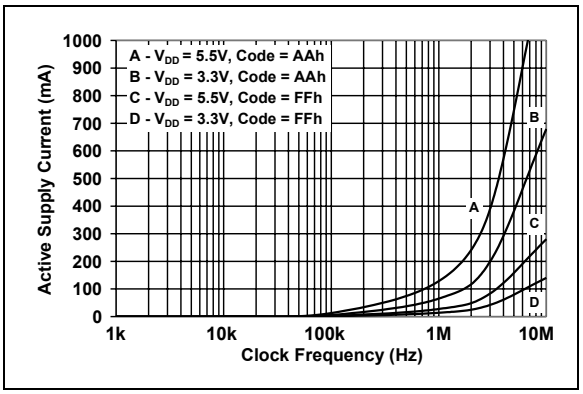

FIGURE 2-11: *Active Supply Current vs. Clock Frequency.*

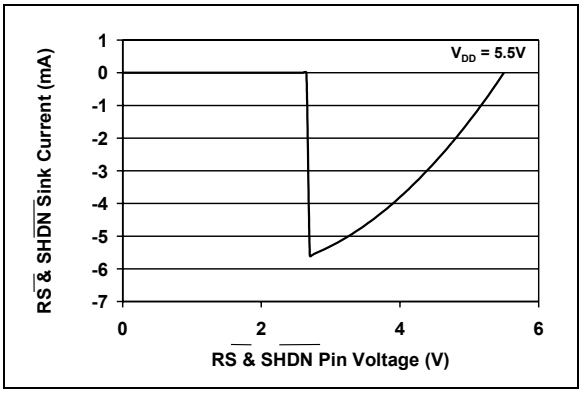

FIGURE 2-12: *Reset & Shutdown Pins Current vs. Voltage.*

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Note: Unless otherwise indicated, curve represents 10 kΩ, 50 kΩ and 100 kΩ devices, V_{DD} = 5V, V_{SS} = 0V, T_A = +25°C, V_B = 0V.

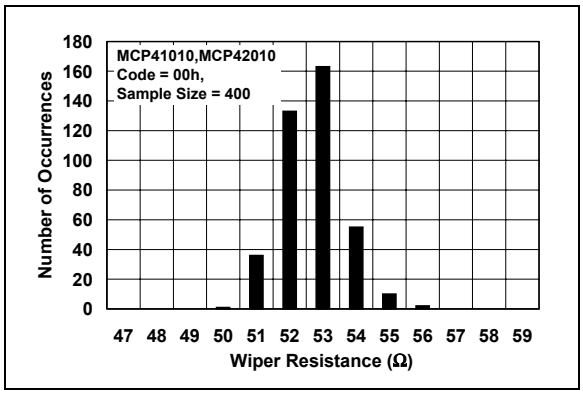

FIGURE 2-13: *10 kΩ Device Wiper Resistance Histogram.*

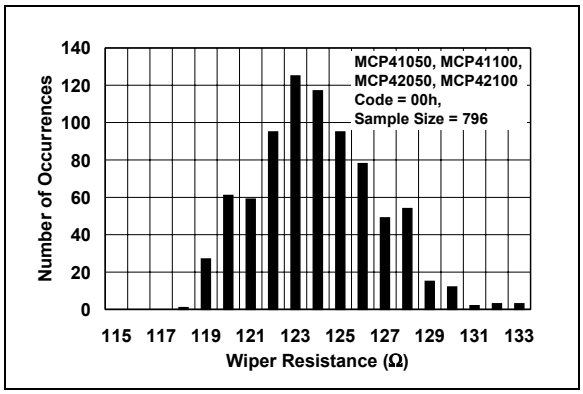

FIGURE 2-14: *50 kΩ, 100 kΩ Device Wiper Resistance Histogram.*

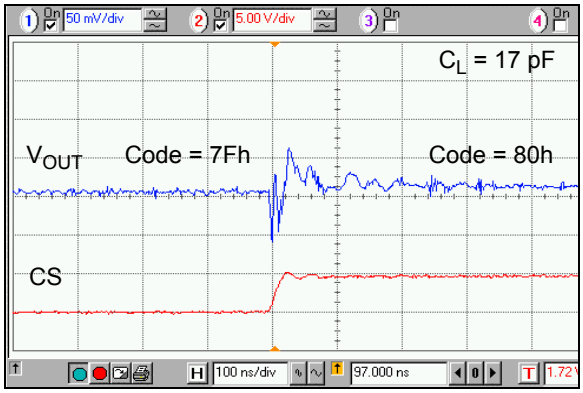

FIGURE 2-15: *One Position Settling Time.*

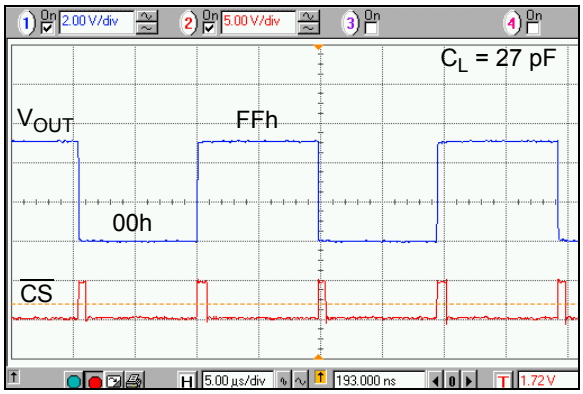

FIGURE 2-16: *Full-Scale Settling Time.*

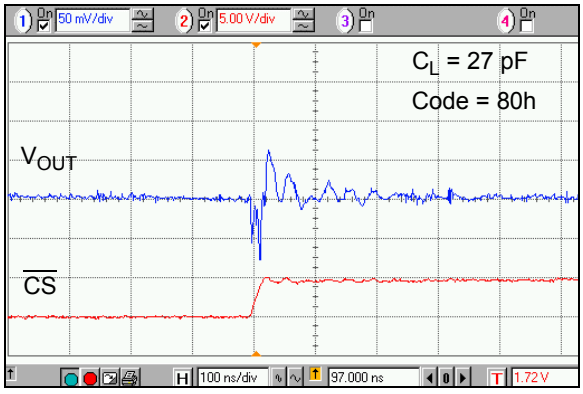

FIGURE 2-17: *Digital Feed through vs. Time.*

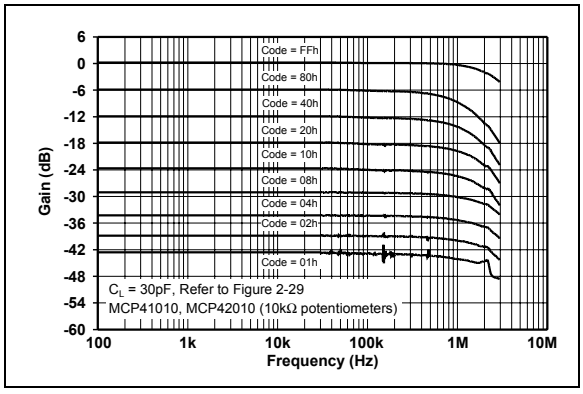

FIGURE 2-18: *Gain vs. Frequency for 10 kΩ Potentiometer.*

Note: Unless otherwise indicated, curve represents 10 kΩ, 50 kΩ and 100 kΩ devices, V_{DD} = 5V, V_{SS} = 0V, T_A = +25°C, V_B = 0V.

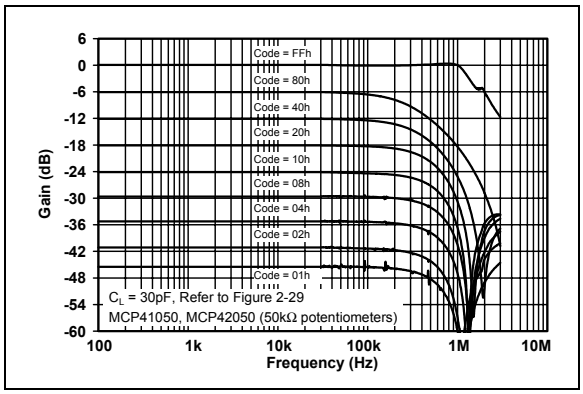

FIGURE 2-19: *Gain vs. Frequency for 50kΩ Potentiometer.*

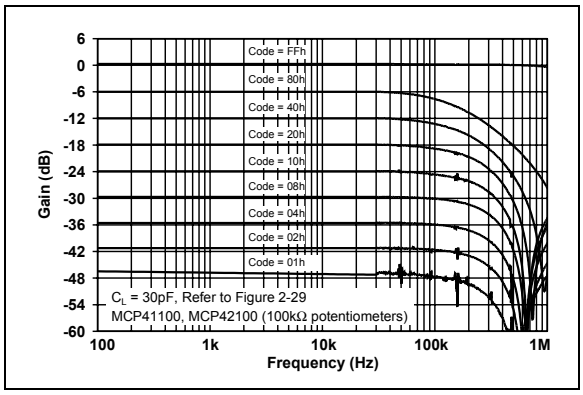

FIGURE 2-20: *Gain vs. Frequency for 100kΩ Potentiometer.*

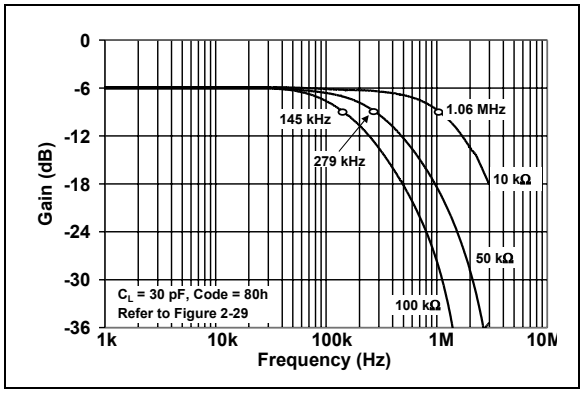

FIGURE 2-21: *-3 dB Bandwidths.*

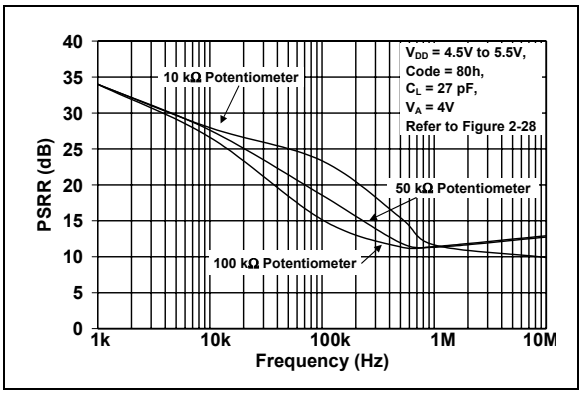

FIGURE 2-22: *Power Supply Rejection Ratio vs. Frequency.*

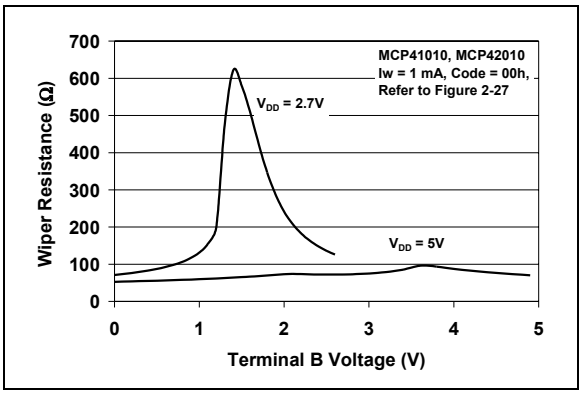

FIGURE 2-23: *10 kΩ Wiper Resistance vs. Voltage.*

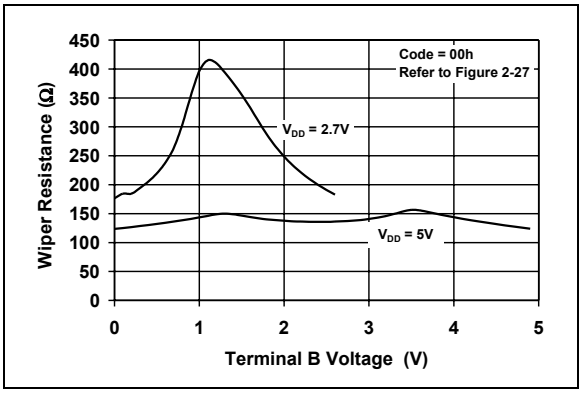

FIGURE 2-24: *50 kΩ & 100 kΩ Wiper Resistance vs. Voltage.*

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2.1 Parametric Test Circuits

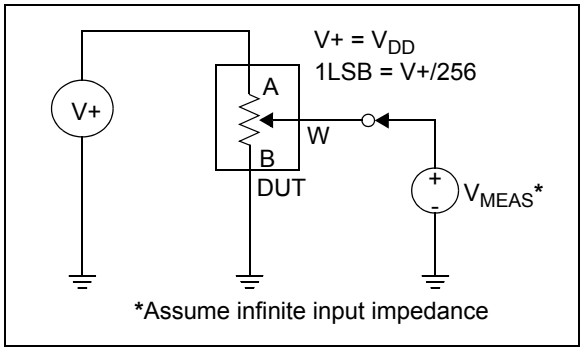

FIGURE 2-25: *Potentiometer Divider Non-Linearity Error Test Circuit (DNL, INL).*

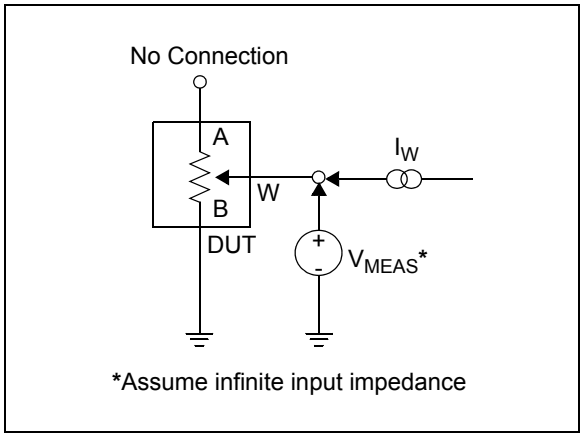

FIGURE 2-26: *Resistor Position Non-Linearity Error Test Circuit (Rheostat operation DNL, INL).*

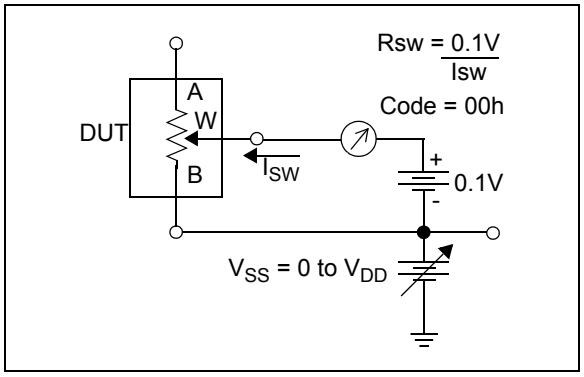

FIGURE 2-27: *Wiper Resistance Test Circuit.*

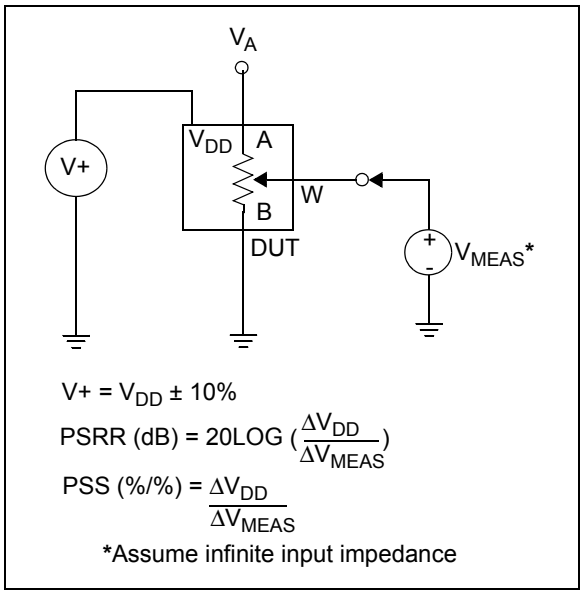

FIGURE 2-28: *Power Supply Sensitivity Test Circuit (PSS, PSRR).*

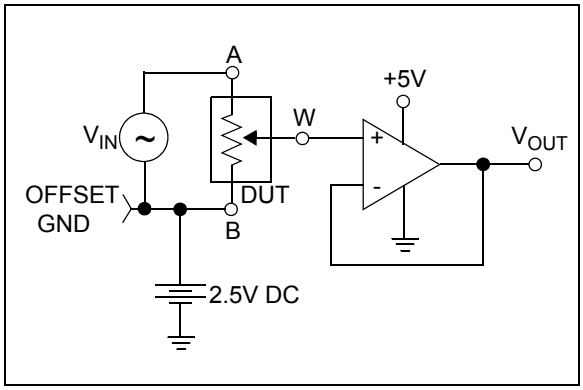

FIGURE 2-29: *Gain vs. Frequency Test Circuit.*

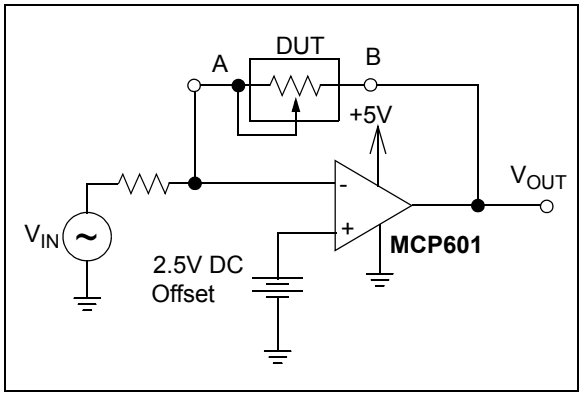

FIGURE 2-30: *Capacitance Test Circuit.*

3.0 PIN DESCRIPTIONS

3.1 PA0, PA1

Potentiometer Terminal A Connection.

3.2 PB0, PB1

Potentiometer Terminal B Connection.

3.3 PW0, PW1

Potentiometer Wiper Connection.

3.4 Chip Select ($\overline{CS}$)

This is the SPI port chip select pin and is used to execute a new command after it has been loaded into the shift register. This pin has a Schmitt Trigger input.

3.5 Serial Clock (SCK)

This is the SPI port clock pin and is used to clock-in new register data. Data is clocked into the SI pin on the rising edge of the clock and out the SO pin on the falling edge of the clock. This pin is gated to the $\overline{CS}$ pin (i.e., the device will not draw any more current if the SCK pin is toggling when the $\overline{CS}$ pin is high). This pin has a Schmitt Trigger input.

3.6 Serial Data Input (SI)

This is the SPI port serial data input pin. The command and data bytes are clocked into the shift register using this pin. This pin is gated to the $\overline{CS}$ pin (i.e., the device will not draw any more current if the SI pin is toggling when the $\overline{CS}$ pin is high). This pin has a Schmitt Trigger input.

3.7 Serial Data Output (SO) (MCP42XXX devices only)

This is the SPI port serial data output pin used for daisy-chaining more than one device. Data is clocked out of the SO pin on the falling edge of clock. This is a push-pull output and **does not** go to a high-impedance state when $\overline{CS}$ is high. It will drive a logic-low when $\overline{CS}$ is high.

3.8 Reset ($\overline{RS}$) (MCP42XXX devices only)

The Reset pin will set all potentiometers to mid-scale (Code 80h) if this pin is brought low for at least 150 ns. This pin should not be toggled low when the $\overline{CS}$ pin is low. It is possible to toggle this pin when the $\overline{SHDN}$ pin is low. In order to minimize power consumption, this pin has an active pull-up circuit. The performance of this circuit is shown in Figure 2-12. This pin will draw negligible current at logic level '0' and logic level '1'. Do not leave this pin floating.

3.9 Shutdown ($\overline{SHDN}$) (MCP42XXX devices only)

The Shutdown pin has a Schmitt Trigger input. Pulling this pin low will put the device in a power-saving mode where A terminal is opened and the B and W terminals are connected for all potentiometers. This pin should not be toggled low when the $\overline{CS}$ pin is low. In order to minimize power consumption, this pin has an active pull-up circuit. The performance of this circuit is shown in Figure 2-12. This pin will draw negligible current at logic level '0' and logic level '1'. Do not leave this pin floating.

TABLE 3-1: MCP41XXX Pins

Pin #	Name	Function
1	$\overline{CS}$	Chip Select
2	SCK	Serial Clock
3	SI	Serial Data Input
4	V_{SS}	Ground
5	PA0	Terminal A Connection For Pot 0
6	PW0	Wiper Connection For Pot 0
7	PB0	Terminal B Connection For Pot 0
8	V_{DD}	Power

TABLE 3-2: MCP42XXX Pins

Pin #	Name	Function
1	$\overline{CS}$	Chip Select
2	SCK	Serial Clock
3	SI	Serial Data Input
4	V_{SS}	Ground
5	PB1	Terminal B Connection For Pot 1
6	PW1	Wiper Connection For Pot 1
7	PA1	Terminal A Connection For Pot 1
8	PA0	Terminal A Connection For Pot 0
9	PW0	Wiper Connection For Pot 0
10	PB0	Terminal B Connection For Pot 0
11	$\overline{RS}$	Reset Input
12	$\overline{SHDN}$	Shutdown Input
13	SO	Data Out for Daisy-Chaining
14	V_{DD}	Power

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4.0 APPLICATIONS INFORMATION

The MCP41XXX/42XXX devices are 256 position single and dual digital potentiometers that can be used in place of standard mechanical pots. Resistance values of 10 kΩ, 50 kΩ and 100 kΩ are available. As shown in Figure 4-1, each potentiometer is made up of a variable resistor and an 8-bit (256 position) data register that determines the wiper position. There is a nominal wiper resistance of 52Ω for the 10 kΩ version, 125Ω for the 50 kΩ and 100 kΩ versions. For the dual devices, the channel-to-channel matching variation is less than 1%. The resistance between the wiper and either of the resistor endpoints varies linearly according to the value stored in the data register. Code 00h effectively connects the wiper to the B terminal. At power-up, all data registers will automatically be loaded with the mid-scale value (80h). The serial interface provides the means for loading data into the shift register, which is then transferred to the data registers. The serial interface also provides the means to place individual potentiometers in the shutdown mode for maximum power savings. The $\overline{SHDN}$ pin can also be used to put all potentiometers in shutdown mode and the $\overline{RS}$ pin is provided to set all potentiometers to mid-scale (80h).

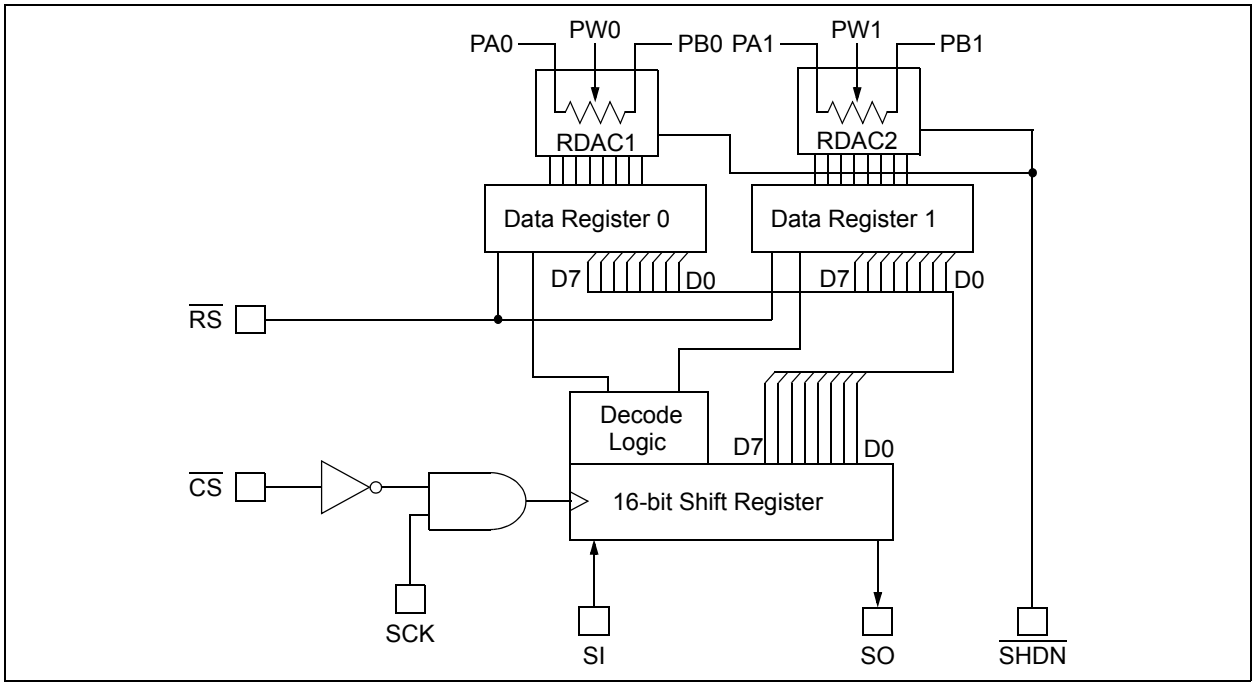
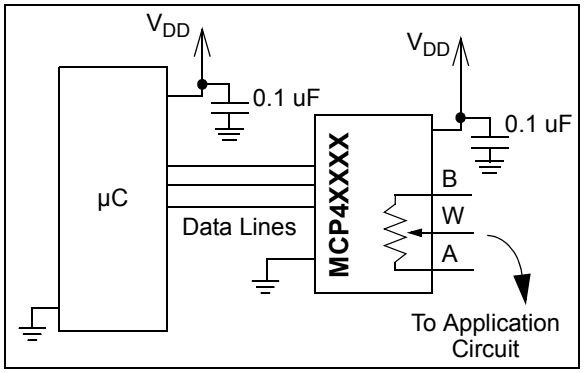


FIGURE 4-1: *Block diagram showing the MCP42XXX dual digital potentiometer. Data register 0 and data register 1 are 8-bit registers allowing 256 positions for each wiper. Standard SPI pins are used with the addition of the Shutdown (SHDN) and Reset (RS) pins. As shown, reset affects the data register and wipers, bringing them to mid-scale. Shutdown disconnects the A terminal and connects the wiper to B, without changing the state of the data registers.*



When laying out the circuit for your digital potentiometer, bypass capacitors should be used. These capacitors should be placed as close as possible to the device pin. A bypass capacitor value of 0.1 µF is recommended. Digital and analog traces should be separated as much as possible on the board, with no traces running underneath the device or the bypass capacitor. Extra precautions should be taken to keep traces with high-frequency signals (such as clock lines) as far as possible from analog traces. Use of an analog ground plane is recommended in order to keep the ground potential the same for all devices on the board.

4.1 Modes of Operation

Digital potentiometer applications can be divided into two categories: rheostat mode and potentiometer, or voltage divider, mode.

4.1.1 RHEOSTAT MODE

In the rheostat mode, the potentiometer is used as a two-terminal resistive element. The unused terminal should be tied to the wiper, as shown in Figure 4-2. Note that reversing the polarity of the A and B terminals will not affect operation.

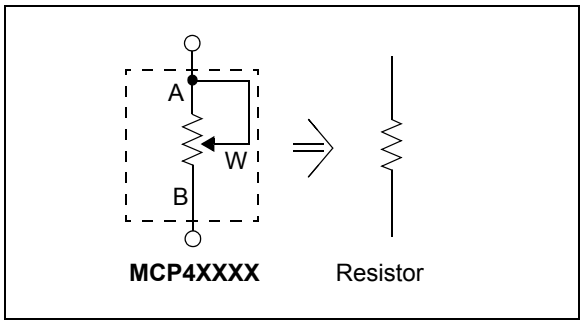


FIGURE 4-2: *Two-terminal or rheostat configuration for the digital potentiometer. Acting as a resistive element in the circuit, resistance is controlled by changing the wiper setting.*

Using the device in this mode allows control of the total resistance between the two nodes. The total measured resistance would be the least at code 00h, where the wiper is tied to the B terminal. The resistance at this code is equal to the wiper resistance, typically 52Ω for the 10 kΩ MCP4X010 devices, 125Ω for the 50 kΩ (MCP4X050), and 100 kΩ (MCP4X100) devices. For the 10 kΩ device, the LSB size would be 39.0625Ω (assuming 10 kΩ total resistance). The resistance would then increase with this LSB size until the total measured resistance at code FFh would be 9985.94Ω. The wiper will never directly connect to the A terminal of the resistor stack.

In the 00h state, the total resistance is the wiper resistance. To avoid damage to the internal wiper circuitry in this configuration, care should be taken to ensure the current flow never exceeds 1 mA.

For dual devices, the variation of channel-to-channel matching of the total resistance from A to B is less than 1%. The device-to-device matching, however, can vary up to 30%. In the rheostat mode, the resistance has a positive temperature coefficient. The change in wiper-to-end terminal resistance over temperature is shown in Figure 2-8. The most variation over temperature will occur in the first 6% of codes (code 00h to 0Fh) due to the wiper resistance coefficient affecting the total resistance. The remaining codes are dominated by the total resistance tempco R_{AB}, typically 800 ppm/°C.

4.1.2 POTENTIOMETER MODE

In the potentiometer mode, all three terminals of the device are tied to different nodes in the circuit. This allows the potentiometer to output a voltage proportional to the input voltage. This mode is sometimes called voltage divider mode. The potentiometer is used to provide a variable voltage by adjusting the wiper position between the two endpoints as shown in Figure 4-3. Note that reversing the polarity of the A and B terminals will not affect operation.

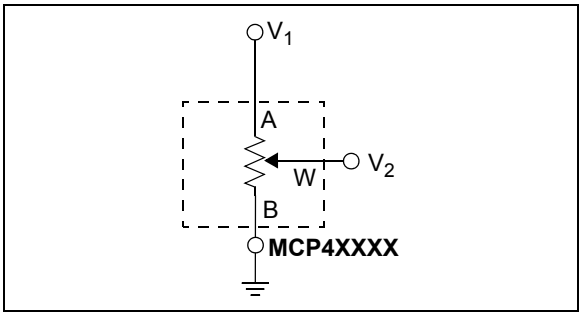


FIGURE 4-3: *Three terminal or voltage divider mode.*

In this configuration, the ratio of the internal resistance defines the temperature coefficient of the device. The resistor matching of the R_{WB} resistor to the R_{AB} resistor performs with a typical temperature coefficient of 1 ppm/°C (measured at code 80h). At lower codes, the wiper resistance temperature coefficient will dominate. Figure 2-3 shows the effect of the wiper. Above the lower codes, this figure shows that 70% of the states will typically have a temperature coefficient of less than 5 ppm/°C. 30% of the states will typically have a ppm/°C of less than 1.

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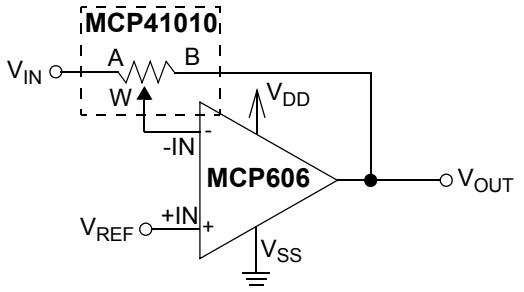
4.2 Typical Applications

4.2.1 PROGRAMMABLE SINGLE-ENDED AMPLIFIERS

Potentiometers are often used to adjust system reference levels or gain. Programmable gain circuits using digital potentiometers can be realized in a number of different ways. An example of a single-supply, inverting gain amplifier is shown in Figure 4-4. Due to the high input impedance of the amplifier, the wiper resistance is not included in the transfer function. For a single-supply, non-inverting gain configuration, the circuit in Figure 4-5 can be used.



$$V_{OUT} = -V_{IN}\left(\frac{R_B}{R_A}\right) + V_{REF}\left(1 + \frac{R_B}{R_A}\right)$$

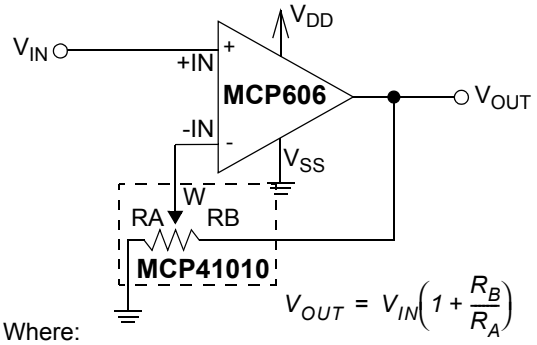
Where:

$$R_A = \frac{R_{AB}(256 - D_n)}{256} \quad R_B = \frac{R_{AB}D_n}{256}$$

R_{AB} = *Total Resistance of pot*

D_n = *Wiper setting for* D_n = 0 to 255

FIGURE 4-4: *Single-supply, programmable, inverting gain amplifier using a digital potentiometer.*



$$V_{OUT} = V_{IN}\left(1 + \frac{R_B}{R_A}\right)$$

Where:

$$R_A = \frac{R_{AB}(256 - D_n)}{256} \quad R_B = \frac{R_{AB}D_n}{256}$$

R_{AB} = *Total Resistance of pot*

D_n = *Wiper setting for* D_n = 0 to 255

FIGURE 4-5: *Single-supply, programmable, non-inverting gain amplifier.*

In order for these circuits to work properly, care must be taken in a few areas. For linear operation, the analog input and output signals must be in the range of V_{SS} to V_{DD} for the potentiometer and input and output rails of the op-amp. The circuit in Figure 4-4 requires a virtual ground or reference input to the non-inverting input of the amplifier. Refer to Application Note 682, *"Using Single-Supply Operational Amplifiers in Embedded Systems" (DS00682),* for more details. At power-up or reset ($\overline{RS}$), the resistance is set to mid-scale, with R_A and R_B matching. Based on the transfer function for the circuit, the gain is -1 V/V. As the code is increased and the wiper moves towards the A terminal, the gain increases. Conversely, when the wiper is moved towards the B terminal, the gain decreases. Figure 4-6 shows this relationship. Notice the pseudo-logarithmic gain around decimal code 128. As the wiper approaches either terminal, the step size in the gain calculation increases dramatically. Due to the mismatched ratio of R_A and R_B at the extreme high and low codes, small increments in wiper position can dramatically affect the gain. As shown in Figure 4-3, recommended gains lie between 0.1 and 10 V/V.

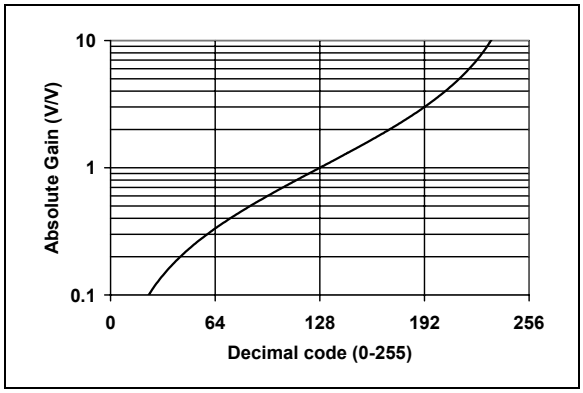
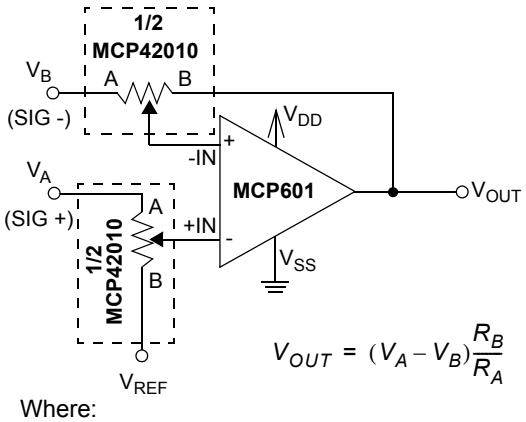


FIGURE 4-6: *Gain vs. Code for inverting and differential amplifier circuits.*

4.2.2 PROGRAMMABLE DIFFERENTIAL AMPLIFIER

An example of a differential input amplifier using digital potentiometers is shown in Figure 4-7. For the transfer function to hold, both pots must be programmed to the same code. The resistor-matching from channel-to-channel within a dual device can be used as an advantage in this circuit. This circuit will also show stable operation over temperature due to the low potentiometer temperature coefficient. Figure 4-6 also shows the relationship between gain and code for this circuit. As the wiper approaches either terminal, the step size in the gain calculation increases dramatically. This circuit is recommended for gains between 0.1 and 10 V/V.



Where:

$$R_A = \frac{R_{AB}(256 - D_n)}{256} \quad R_B = \frac{R_{AB}D_n}{256}$$

R_{AB} = *Total Resistance of pot*

D_n = *Wiper setting for* D_n = *0 to 255*

NOTE: Potentiometer values must be equal

FIGURE 4-7: *Single Supply programmable differential amplifier using digital potentiometers.*

4.2.3 PROGRAMMABLE OFFSET TRIM

For applications requiring only a programmable voltage reference, the circuit in Figure 4-8 can be used. This circuit shows the device used in the potentiometer mode along with two resistors and a buffered output. This creates a circuit with a linear relationship between voltage-out and programmed code. Resistors R_1 and R_2 can be used to increase or decrease the output voltage step size. The potentiometer in this mode is stable over temperature. The operation of this circuit over temperature is shown in Figure 2-3. The worst performance over temperature will occur at the lower codes due to the dominating wiper resistance. R_1 and R_2 can also be used to affect the boundary voltages, thereby eliminating the use of these lower codes.

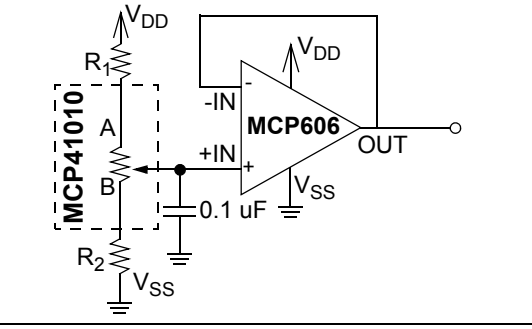
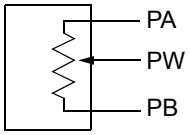


FIGURE 4-8: *By changing the values of R_1 and R_2, the voltage output resolution of this programmable voltage reference circuit is affected.*

4.3 Calculating Resistances

When programming the digital potentiometer settings, the following equations can be used to calculate the resistances. Programming code 00h effectively brings the wiper to the B terminal, leaving only the wiper resistance. Programming higher codes will bring the wiper closer to the A terminal of the potentiometer. The equations in Figure 4-9 can be used to calculate the terminal resistances. Figure 4-10 shows an example calculation using a 10 kΩ potentiometer.

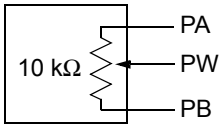


$$R_{WA}(D_n) = \frac{(R_{AB})(256 - D_n)}{256} + R_W$$

$$R_{WB}(D_n) = \frac{(R_{AB})(D_n)}{256} + R_W$$

Where:
PA is the A terminal
PB is the B terminal
PW is the wiper terminal
R_{WA} is resistance between Terminal A and wiper
R_{WB} is resistance between Terminal B and Wiper
R_{AB} is overall resistance for pot (10 kΩ, 50 kΩ or 100 kΩ)
R_W is wiper resistance
D_n is 8-bit value in data register for pot number n

FIGURE 4-9: *Potentiometer resistances are a function of code. It should be noted that, when using these equations for most feedback amplifier circuits (see Figure 4-4 and Figure 4-5), the wiper resistance can be omitted due to the high impedance input of the amplifier.*



Example:
R = 10 kΩ
Code = C0h = 192d

$$R_{WA}(D_n) = \frac{(R_{AB})(256 - D_n)}{256} + R_W$$

$$R_{WA}(C0h) = \frac{(10k\Omega)(256 - 192)}{256} + 52\Omega$$

$$R_{WA}(C0h) = 2552\Omega$$

$$R_{WB}(D_n) = \frac{(R_{AB})(D_n)}{256} + R_W$$

$$R_{WB}(C0h) = \frac{(10k\Omega)(192)}{256} + 52\Omega$$

$$R_{WB}(C0h) = 7552\Omega$$

Note: All values shown are typical and actual results will vary.

FIGURE 4-10: *Example Resistance calculations.*

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5.0 SERIAL INTERFACE

Communications from the controller to the MCP41XXX/42XXX digital potentiometers is accomplished using the SPI serial interface. This interface allows three commands:

1. Write a new value to the potentiometer data register(s).
2. Cause a channel to enter low power shutdown mode.
3. NOP (No Operation) command.

Executing any command is accomplished by setting $\overline{CS}$ low and then clocking-in a command byte followed by a data byte into the 16-bit shift register. The command is executed when $\overline{CS}$ is raised. Data is clocked-in on the rising edge of clock and out the SO pin on the falling edge of the clock (see Figure 5-1). The device will track the number of clocks (rising edges) while $\overline{CS}$ is low and will abort all commands if the number of clocks is not a multiple of 16.

5.1 Command Byte

The first byte sent is always the command byte, followed by the data byte. The command byte contains two command select bits and two potentiometer select bits. Unused bits are 'don't care' bits. The command select bits are summarized in Figure 5-2. The command select bits C1 and C0 (bits 4:5) of the command byte determine which command will be executed. If the command bits are both 0's or 1's, then a NOP command will be executed once all 16 bits have been loaded. This command is useful when using the daisy-chain configuration. When the command bits are 0,1, a write command will be executed with the 8 bits sent in the data byte. The data will be written to the potentiometer(s) determined by the potentiometer select bits. If the command bits are 1,0, then a shutdown command will be executed on the potentiometers determined by the potentiometer select bits.

For the MCP42XXX devices, the potentiometer select bits P1 and P0 (bits 0:1) determine which potentiometers are to be acted upon by the command. A corresponding '1' in the position signifies that the command for that potentiometer will get executed, while a '0' signifies that the command will not effect that potentiometer (see Figure 5-2).

5.2 Writing Data Into Data Registers

When new data is written into one or more of the potentiometer data registers, the write command is followed by the data byte for the new value. The command select bits C1, C0 are set to 0,1. The potentiometer selection bits P1 and P0 allow new values to be written to potentiometer 0, potentiometer 1 (or both) with a single command. A '1' for either P1 or P0 will cause the data to be written to the respective data register and a '0' for P1 or P0 will cause no change. See Figure 5-2 for the command format summary.

5.3 Using The Shutdown Command

The shutdown command allows the user to put the application circuit into a power-saving mode. In this mode, the A terminal is open-circuited and the B and W terminals are shorted together. The command select bits C1, C0 are set to 1,0. The potentiometer selection bits P1 and P0 allow each potentiometer to be shutdown independently. If either P1 or P0 are high, the respective potentiometer will enter shutdown mode. A '0' for P1 or P0 will have no effect. The eight data bits following the command byte still need to be transmitted for the shutdown command, but they are 'don't care' bits. See Figure 5-2 for command format summary. Once a particular potentiometer has entered the shutdown mode, it will remain in this mode until:

- A new value is written to the potentiometer data register, provided that the $\overline{SHDN}$ pin is high. The device will remain in the shutdown mode until the rising edge of the $\overline{CS}$ is detected, at which time the device will come out of shutdown mode and the new value will be written to the data register(s). If the $\overline{SHDN}$ pin is low when the new value is received, the registers will still be set to the new value, but the device will remain in shutdown mode. This scenario assumes that a valid command was received. If an invalid command was received, the command will be ignored and the device will remain in the shutdown mode.

It is also possible to use the hardware shutdown pin and reset pin to remove a device from software shutdown. To do this, a low pulse on the chip select line must first be sent. For multiple devices, sharing a single $\overline{SHDN}$ or $\overline{RESET}$ line allows you to pick an individual device on that chain to remove from software shutdown mode. See Figure 1-3 for timing. With a preceding chip select pulse, either of these situations will also remove a device from software shutdown:

- A falling edge is seen on the $\overline{RS}$ pin and held low for at least 150 ns, provided that the $\overline{SHDN}$ pin is high. If the $\overline{SHDN}$ pin is low, the registers will still be set to mid-scale, but the device will remain in shutdown mode. This condition assumes that $\overline{CS}$ is high, as bringing the $\overline{RS}$ pin low while $\overline{CS}$ is low is an invalid state and results are indeterminate.
- A rising edge on the $\overline{SHDN}$ pin is seen after being low for at least 100 ns, provided that the $\overline{CS}$ pin is high. Toggling the $\overline{SHDN}$ pin low while $\overline{CS}$ is low is an invalid state and results are indeterminate.
- The device is powered-down and back up.

Note:	The hardware $\overline{SHDN}$ pin will always put the device in shutdown regardless of whether a potentiometer has already been put in the shutdown mode using the software command.

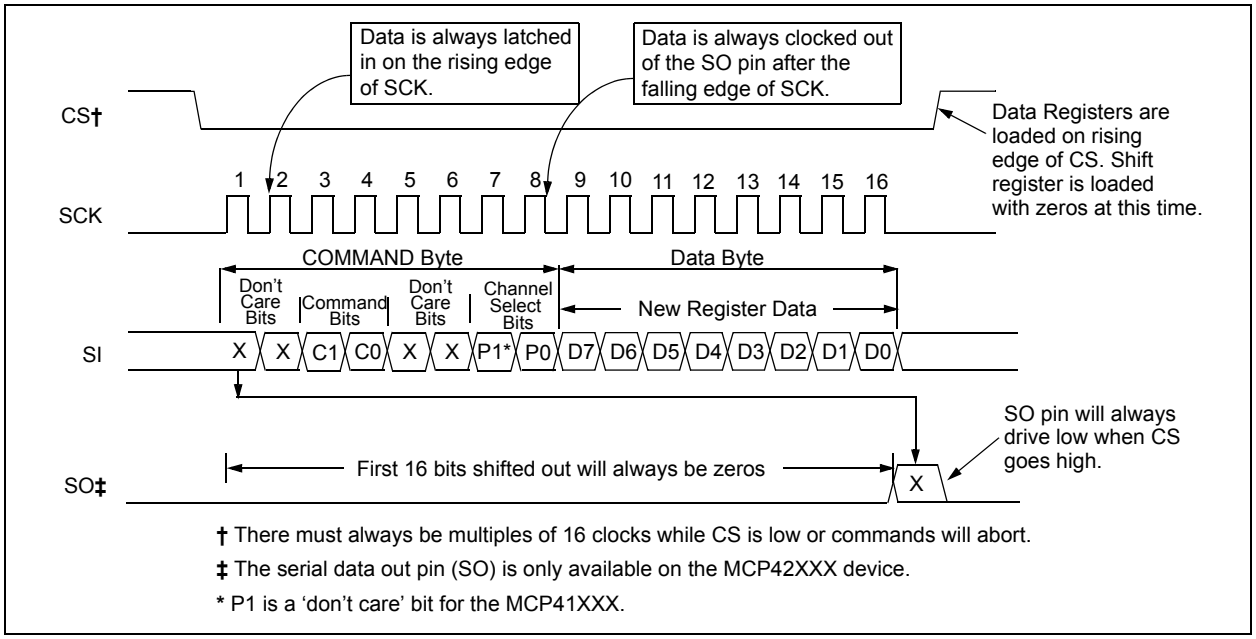

FIGURE 5-1: *Timing Diagram for Writing Instructions or Data to a Digital Potentiometer.*

COMMAND BYTE

X	X	C1	C0	X	X	P1*	P0

Command Selection Bits

Potentiometer Selection Bits

C1	C0	Command	Command Summary
0	0	None	No Command will be executed.
0	1	Write Data	Write the data contained in Data Byte to the potentiometer(s) determined by the potentiometer selection bits.
1	0	Shutdown	Potentiometer(s) determined by potentiometer selection bits will enter Shutdown Mode. Data bits for this command are 'don't cares'.
1	1	None	No Command will be executed.

P1*	P0	Potentiometer Selections
0	0	Dummy Code: Neither Potentiometer affected.
0	1	Command executed on Potentiometer 0.
1	0	Command executed on Potentiometer 1.
1	1	Command executed on both Potentiometers.

FIGURE 5-2: *Command Byte Format.*

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5.4 Daisy-Chain Configuration

Multiple MCP42XXX devices can be connected in a daisy-chain configuration, as shown in Figure 5-4, by connecting the SO pin from one device to the SI pin on the next device. The data on the SO pin is the output of the 16-bit shift register. The daisy-chain configuration allows the system designer to communicate with several devices without using a separate $\overline{CS}$ line for each device. The example shows a daisy-chain configuration with three devices, although any number of devices (with or without the same resistor values) can be configured this way. While it is not possible to use a MCP41XXX at the beginning or middle of a daisy-chain (because it does not provide the serial data out (SO) pin), it is possible to use the device at the end of a chain. As shown in the timing diagram in Figure 5-3, data will be clocked-out of the SO pin on the falling edge of the clock. The SO pin has a CMOS push-pull output and will drive low when $\overline{CS}$ goes high. SO **will not** go to a high-impedance state when $\overline{CS}$ is held high.

When using the daisy-chain configuration, the maximum clock speed possible is reduced to ~5.8 MHz, because of the propagation delay of the data coming out of the SO pin.

When using the daisy-chain configuration, keep in mind that the shift register of each device is automatically loaded with zeros whenever a command is executed ($\overline{CS}$ = high). Because of this, the first 16 bits that come out of the SO pin once the $\overline{CS}$ line goes low will always be zeros. This means that when the first command is being loaded into a device, it will always shift a `NOP` command into the next device on the chain because the command bits (and all the other bits) will be zeros. This feature makes it necessary only to send command and data bytes to the device farthest down the chain that needs a new command. For example, if there were three devices on the chain and it was desired to send a command to the device in the middle, only 32 bytes of data need to be transmitted. The last device on the chain will have a `NOP` loaded from the previous device so no registers will be affected when the $\overline{CS}$ pin is raised to execute the command. **The user must always ensure that multiples of 16 clocks are always provided (while $\overline{CS}$ is low), as all commands will abort if the number of clocks provided is not a multiple of 16.**

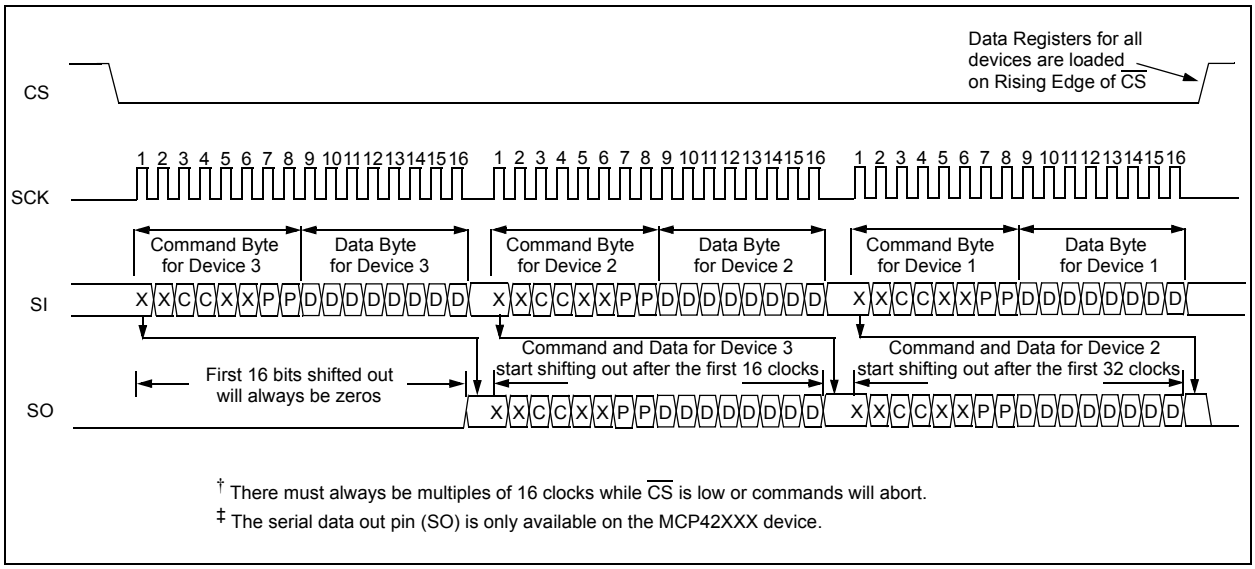

FIGURE 5-3: *Timing Diagram for Daisy-Chain Configuration.*

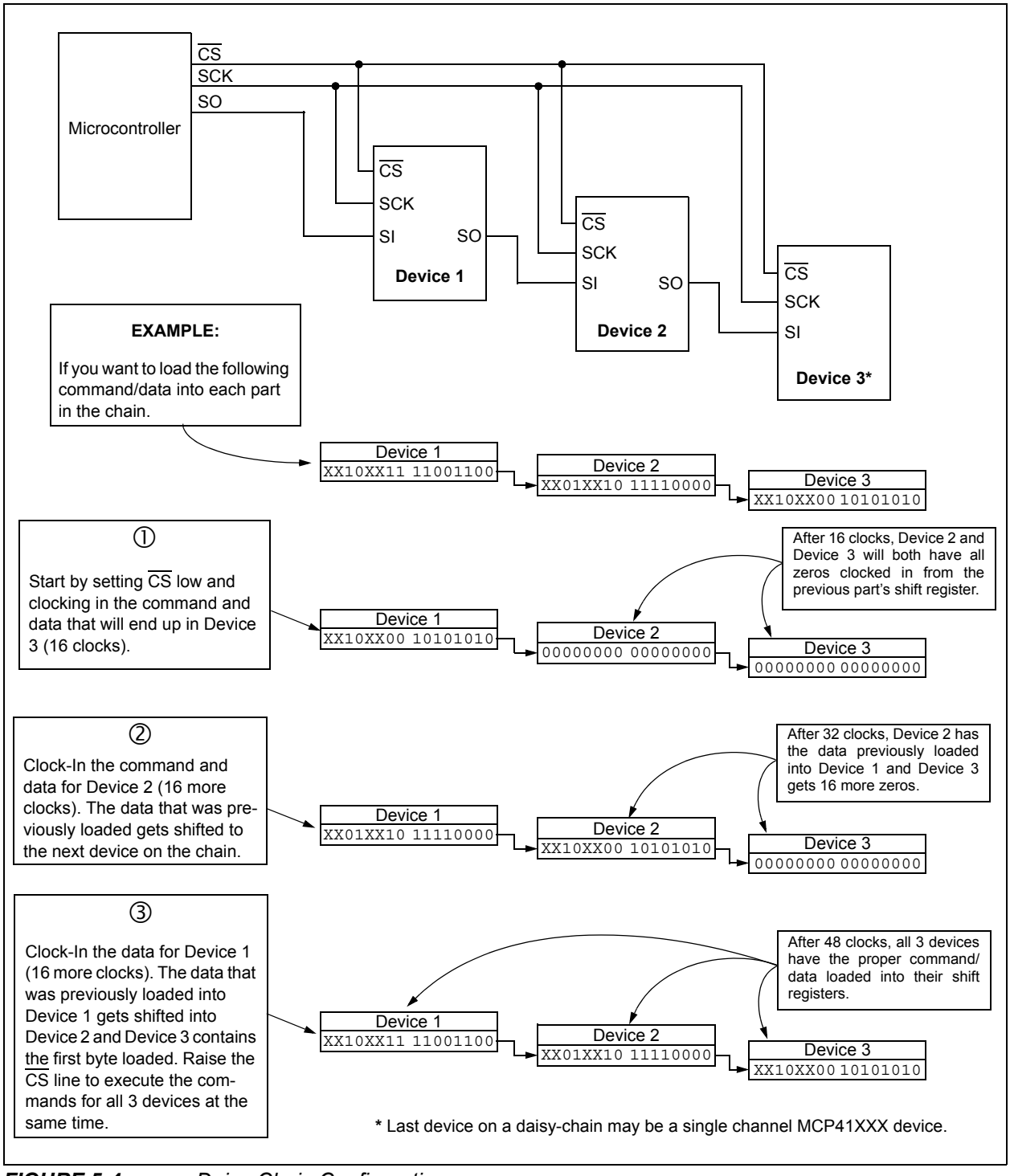

FIGURE 5-4: *Daisy-Chain Configuration.*

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5.5 Reset ($\overline{RS}$) Pin Operation

The Reset pin ($\overline{RS}$) will automatically set all potentiometer data latches to mid-scale (Code 80h) when pulled low (provided that the pin is held low at least 150 ns and $\overline{CS}$ is high). The reset will execute regardless of the position of the SCK, $\overline{SHDN}$ and SI pins. It is possible to toggle $\overline{RS}$ low and back high while $\overline{SHDN}$ is low. In this case, the potentiometer registers will reset to mid-scale, but the potentiometer will remain in shutdown mode until the $\overline{SHDN}$ pin is raised.

Note:	Bringing the $\overline{RS}$ pin low while the $\overline{CS}$ pin is low constitutes an invalid operating state and will result in indeterminate results when $\overline{RS}$ and/or $\overline{CS}$ are brought high.

5.6 Shutdown ($\overline{SHDN}$) Pin Operation

When held low, the shutdown pin causes the application circuit to go into a power-saving mode by open-circuiting the A terminal and shorting the B and W terminals for all potentiometers. Data register contents are not affected by entering shutdown mode (i.e., when the $\overline{SHDN}$ pin is raised, the data register contents are the same as before the shutdown mode was entered).

While in shutdown mode, it is still possible to clock in new values for the data registers, as well as toggling the $\overline{RS}$ pin to cause all data registers to go to mid-scale. The new values will take affect when the $\overline{SHDN}$ pin is raised.

If the device is powered-up with the $\overline{SHDN}$ pin held low, it will power-up in the shutdown mode with the data registers set to mid-scale.

Note:	Bringing the $\overline{SHDN}$ pin low while the $\overline{CS}$ pin is low constitutes an invalid operating state and will result in indeterminate results when $\overline{SHDN}$ and/or $\overline{CS}$ are brought high.

5.7 Power-up Considerations

When the device is powered on, the data registers will be set to mid-scale (80h). A power-on reset circuit is utilized to ensure that the device powers up in this known state.

TABLE 5-1: TRUTH TABLE FOR LOGIC INPUTS

SCK	$\overline{CS}$	$\overline{RS}$	$\overline{SHDN}$	Action
X	Ø	H	H	Communication is initiated with device. Device comes out of standby mode.
L	L	H	H	No action. Device is waiting for data to be clocked into shift register or $\overline{CS}$ to go high to execute command.
¦	L	H	X	Shift one bit into shift register. The shift register can be loaded while the $\overline{SHDN}$ pin is low.
Ø	L	H	X	Shift one bit out of shift register on the SO pin. The SO pin is active while the $\overline{SHDN}$ pin is low.
X	¦	H	H	Based on command bits, either load data from shift register into data latches or execute shutdown command. Neither command executed unless multiples of 16 clocks have been entered while $\overline{CS}$ is low. SO pin goes to a logic low.
X	H	H	H	Static Operation.
X	H	Ø	H	All data registers set and latched to code 80h.
X	H	Ø	L	All data registers set and latched to code 80h. Device is in hardware shutdown mode and will remain in this mode.
X	H	H	Ø	All potentiometers put into hardware shutdown mode; terminal A is open and W is shorted to B.
X	H	H	¦	All potentiometers exit hardware shutdown mode. Potentiometers will also exit software shutdown mode if this rising edge occurs after a low pulse on $\overline{CS}$. Contents of data latches are restored.

5.8 Using the MCP41XXX/42XXX in SPI Mode 1,1

It is possible to operate the devices in SPI modes 0,0 and 1,1. The only difference between these two modes is that, when using mode 1,1, the clock idles in the high state, while in mode 0,0, the clock idles in the low state. In both modes, data is clocked into the devices on the rising edge of SCK and data is clocked out the SO pin once the falling edge of SCK. Operations using mode 0,0 are shown in Figure 5-1. The example in Figure 5-5 shows mode 1,1.

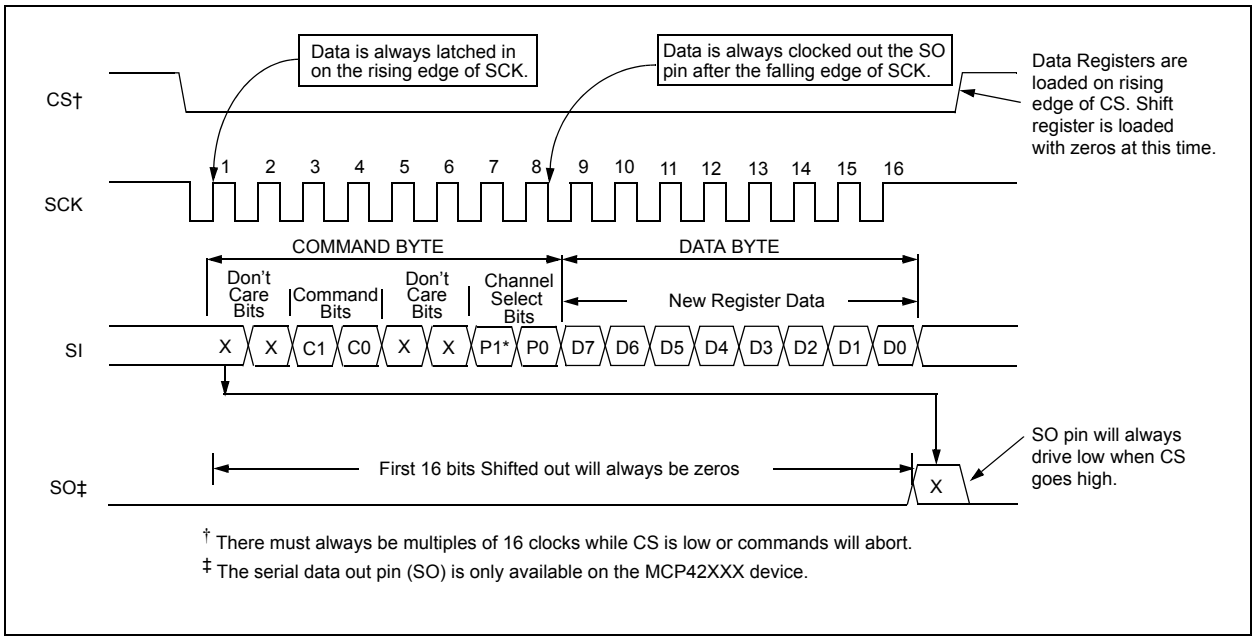

FIGURE 5-5: *Timing Diagram for SPI Mode 1,1 Operation.*

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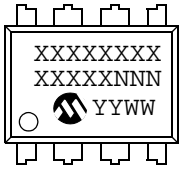
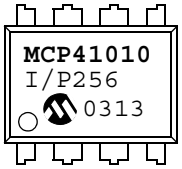
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

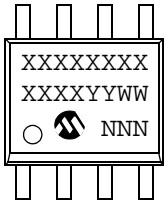
8-Lead PDIP (300 mil)



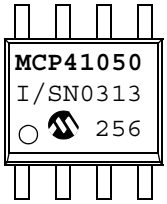
Example:



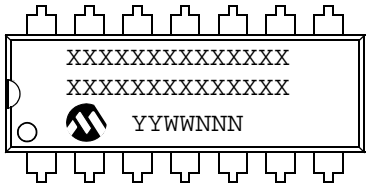
8-Lead SOIC (150 mil)



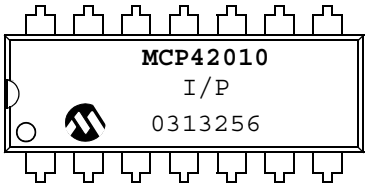
Example:



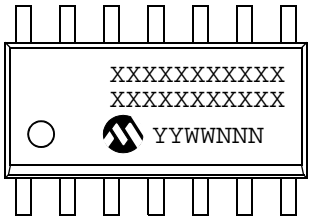
14-Lead PDIP (300 mil)



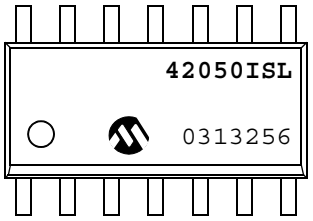
Example:



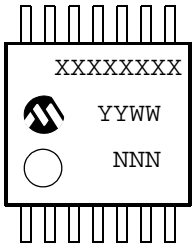
14-Lead SOIC (150 mil)



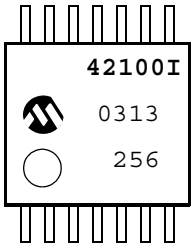
Example:



14-Lead TSSOP (4.4mm) *



Example:

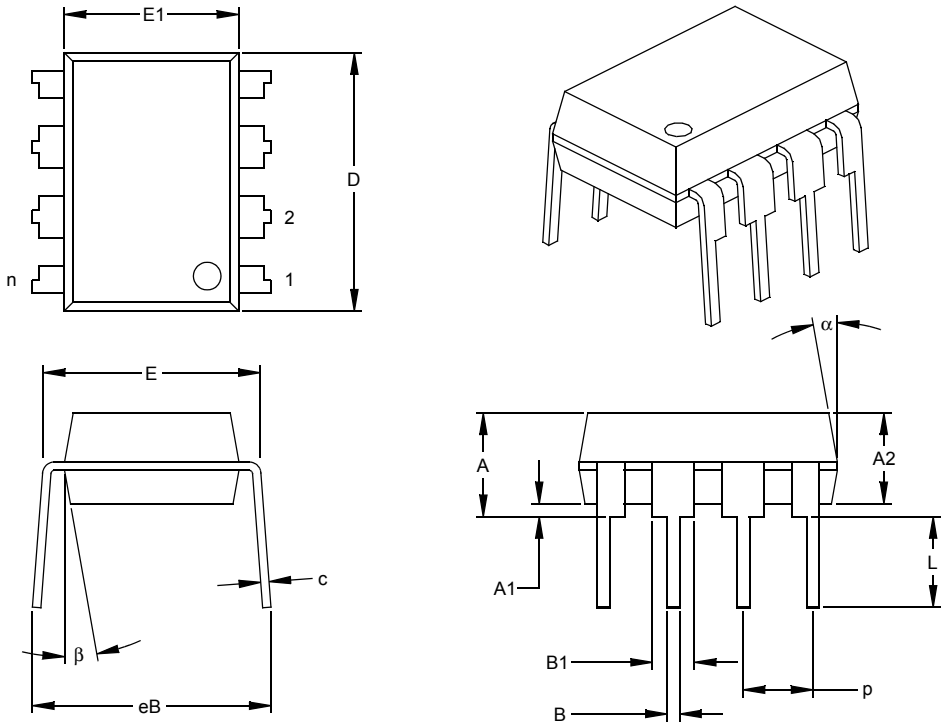


Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

***** Standard marking consists of Microchip part number, year code, week code, facility code, mask rev#, and assembly code.

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

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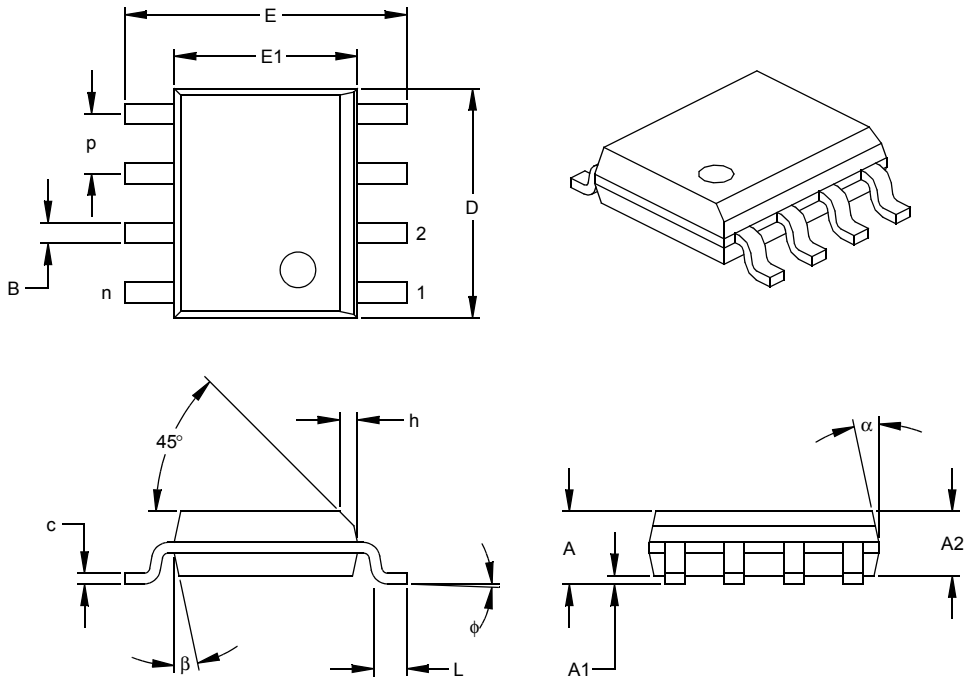
8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)

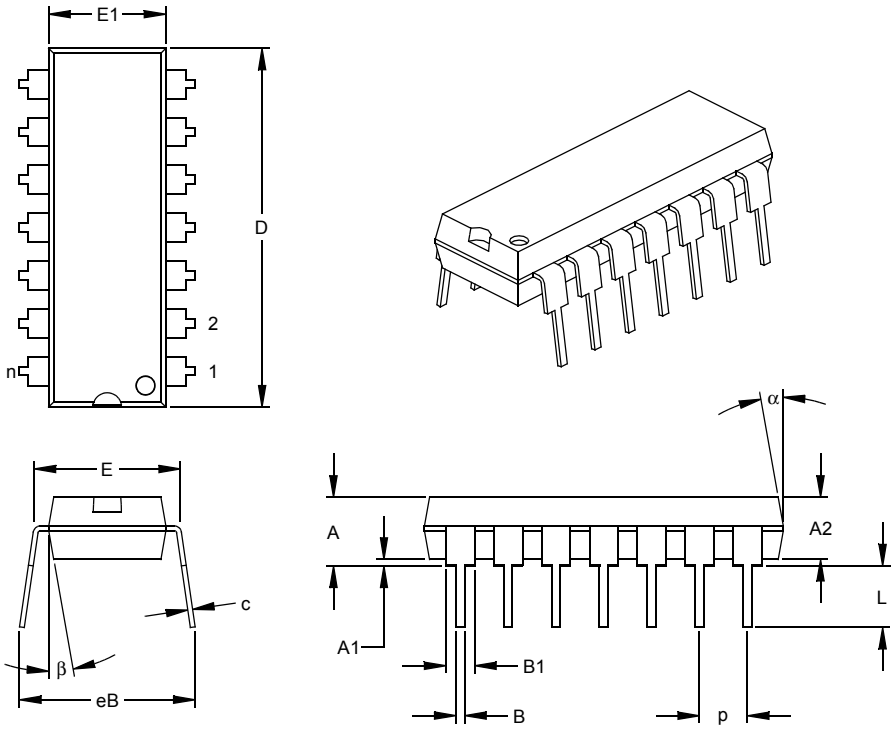


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-005

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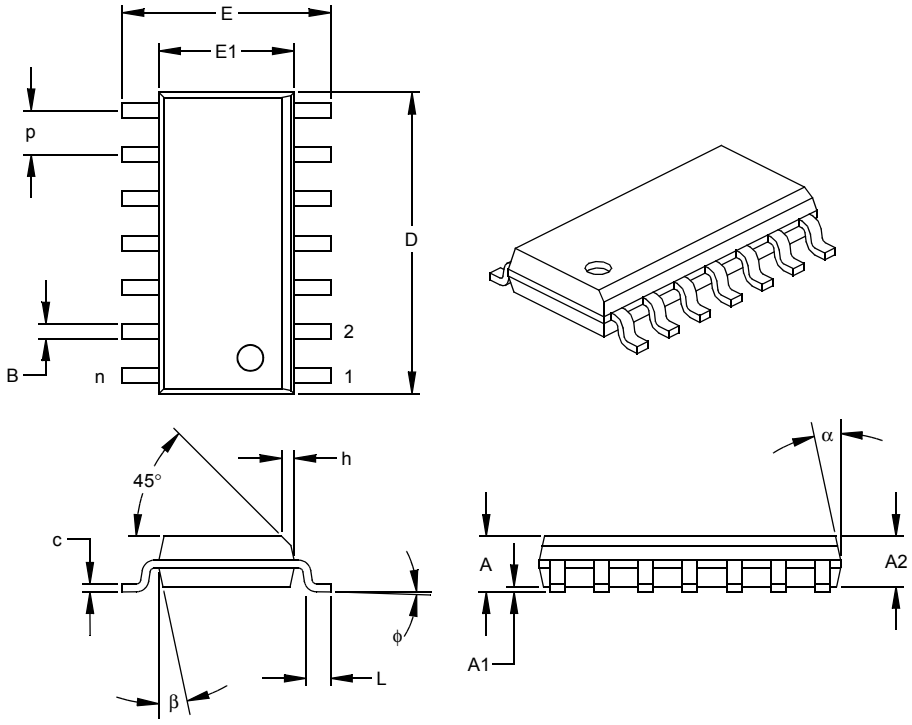
14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)

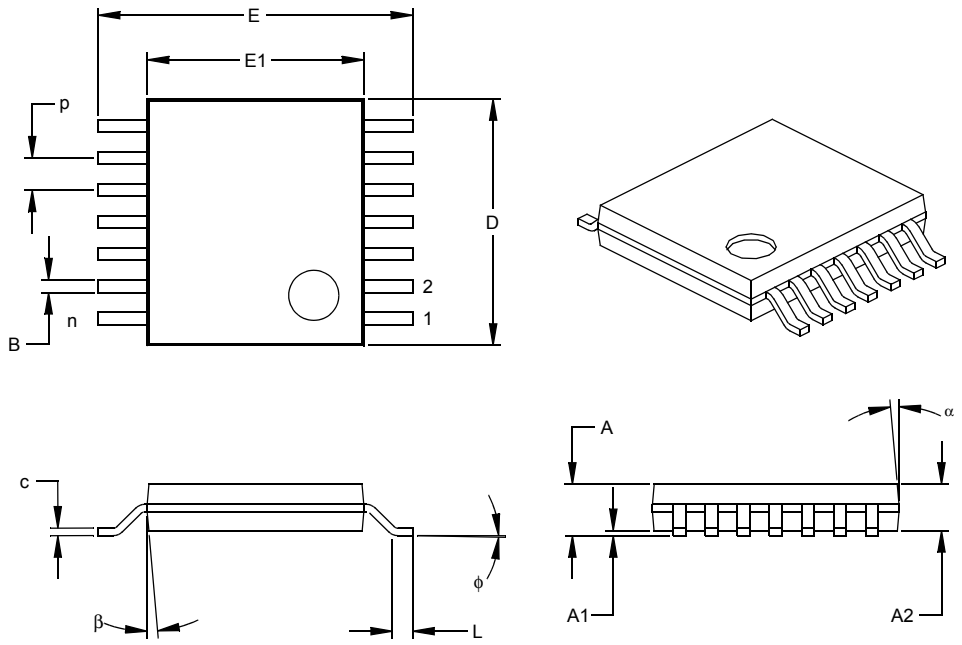


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-065

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-087

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	MCP41010:	Single Digital Potentiometer (10 kΩ)
	MCP41010T:	Single Digital Potentiometer (10 kΩ) (Tape and Reel)
	MCP41050:	Single Digital Potentiometer (50 kΩ) (Tape and Reel)
	MCP41050T:	Single Digital Potentiometer (50 kΩ)
	MCP41100:	Single Digital Potentiometer (100 kΩ) (Tape and Reel)
	MCP41100T:	Single Digital Potentiometer (100 kΩ)
	MCP42010:	Dual Digital Potentiometer (10 kΩ)
	MCP42010T:	Dual Digital Potentiometer (10 kΩ) (Tape and Reel)
	MCP42050:	Dual Digital Potentiometer (50 kΩ)
	MCP42050T:	Dual Digital Potentiometer (50 kΩ) (Tape and Reel)
	MCP42100:	Dual Digital Potentiometer (100 kΩ)
	MCP42100T:	Dual Digital Potentiometer (100 kΩ) (Tape and Reel)
Temperature Range:	I =	-40°C to +85°C
	E =	-40°C to +125°C
Package:	P =	Plastic DIP (300 mil Body), 8-lead, 14-lead
	SN =	Plastic SOIC (150 mil Body), 8-lead
	SL =	Plastic SOIC (150 mil Body), 14-lead
	ST =	TSSOP (4.4mm Body), 14-lead

Examples:

a)	MCP41010-I/SN:	I-Temp., 8LD SOIC pkg.
b)	MCP41010-E/P:	E-Temp., 8LD PDIP pkg.
c)	MCP41010T-I/SN:	Tape and Reel, I-Temp., 8LD SOIC pkg.
d)	MCP41050-E/SN:	E-Temp., 8LD SOIC pkg.
e)	MCP41050-I/P:	I-Temp., 8LD PDIP pkg.
f)	MCP41050-E/SN:	E-Temp., 8LD SOIC pkg.
g)	MCP41100-I/SN:	I-Temp., 8LD SOIC package.
h)	MCP41100-E/P:	E-Temp., 8LD PDIP pkg.
i)	MCP41100T-I/SN:	I-Temp., 8LD SOIC pkg.
a)	MCP42010-E/P:	E-Temp., 14LD PDIP pkg.
b)	MCP42010-I/SL:	I-Temp., 14LD SOIC pkg.
c)	MCP42010-E/ST:	E-Temp., 14LD TSSOP pkg.
d)	MCP42010T-I/ST:	Tape and Reel, I-Temp., 14LD TSSOP pkg.
e)	MCP42050-E/P:	E-Temp., 14LD PDIP pkg.
f)	MCP42050T-I/SL:	Tape and Reel, I-Temp., 14LD SOIC pkg.
g)	MCP42050-E/SL:	E-Temp., 14LD SOIC pkg.
h)	MCP42050-I/ST:	I-Temp., 14LD TSSOP pkg.
i)	MCP42050T-I/SL:	Tape and Reel, I-Temp., 14LD SOIC pkg.
j)	MCP42050T-I/ST:	Tape and Reel, I-Temp., 14LD TSSOP pkg.
k)	MCP42100-E/P:	E-Temp., 14LD PDIP pkg.
l)	MCP42100-I/SL:	I-Temp., 14LD SOIC pkg.
m)	MCP42100-E/ST:	E-Temp., 14LD TSSOP pkg.
n)	MCP42100T-I/SL:	Tape and Reel, I-Temp., 14LD SOIC pkg.
o)	MCP42100T-I/ST:	Tape and Reel, I-Temp., 14LD TSSOP pkg.

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