THE DATASHEET OF

MT8920BPR1

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MT8920B

ST-BUS Parallel Access Circuit

Data Sheet

August 2005

Features

- High speed parallel access to the serial ST-BUS
- Parallel bus optimized for 68000 μP (mode 1)
- Fast dual-port RAM access (mode 2)
  Access time: 120 nsec
- Parallel bus controller (mode 3) - no external controller required
- Flexible interrupt capabilities - two independent/programmable interrupt sources with auto-vectoring
- Selectable 24 and 32 channel operation
- Programmable loop-around modes
- Low power CMOS technology

Applications

- Parallel control/data access to T1/CEPT digital trunk interfaces
- Digital signal processor interface to ST-BUS
- Computer to Digital PABX link
- Voice store and forward systems
- Interprocessor communications

Ordering Information

MT8920BE	28 Pin PDIP	Tubes
MT8920BP	28 Pin PLCC	Tubes
MT8920BS	28 Pin SOIC	Tubes
MT8920BE1	28 Pin PDIP*	Tubes
MT8920BP1	28 Pin PLCC*	Tubes
MT8920BS1	28 Pin SOIC*	Tubes
MT8920BPR1	28 Pin PLCC*	Tape & Reel

*PB Free Matte Tin

-40°C to 85°C

Description

The ST-BUS Parallel Access Circuit (STPA) provides a simple interface between Zarlink's ST-BUS and parallel system environments.

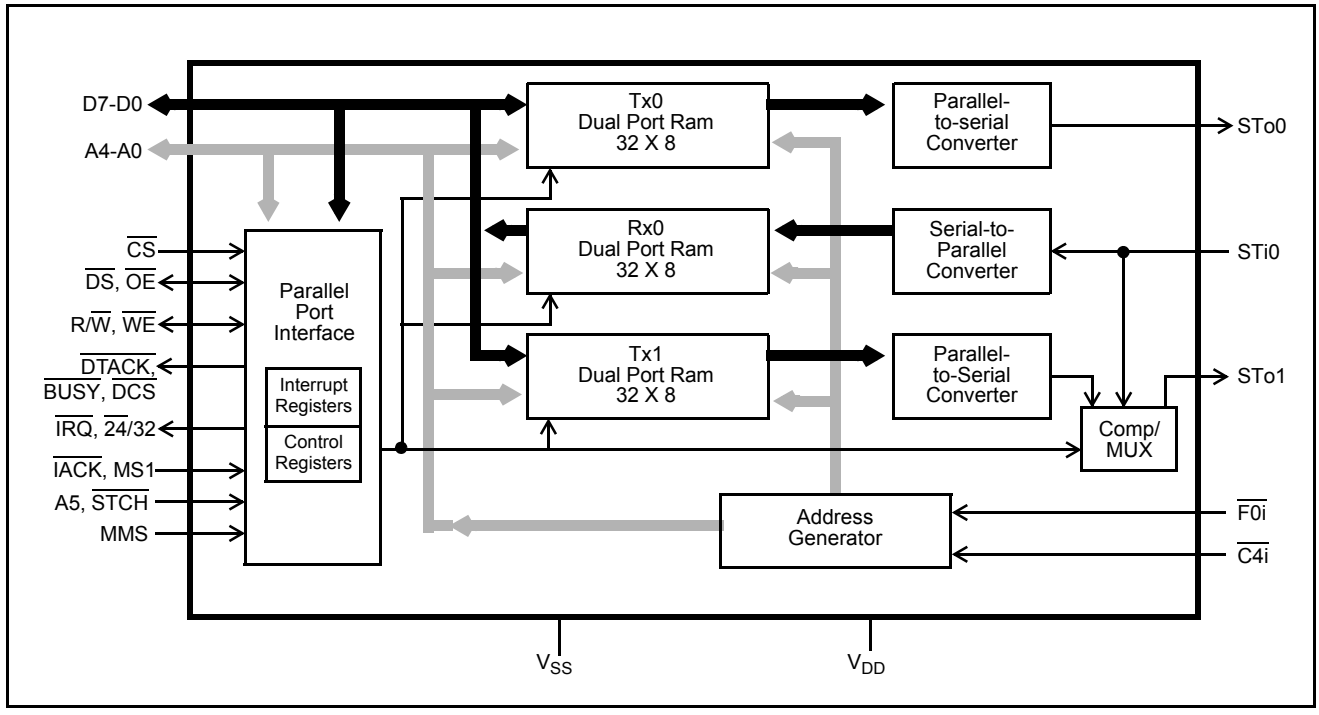


Figure 1 - Functional Block Diagram

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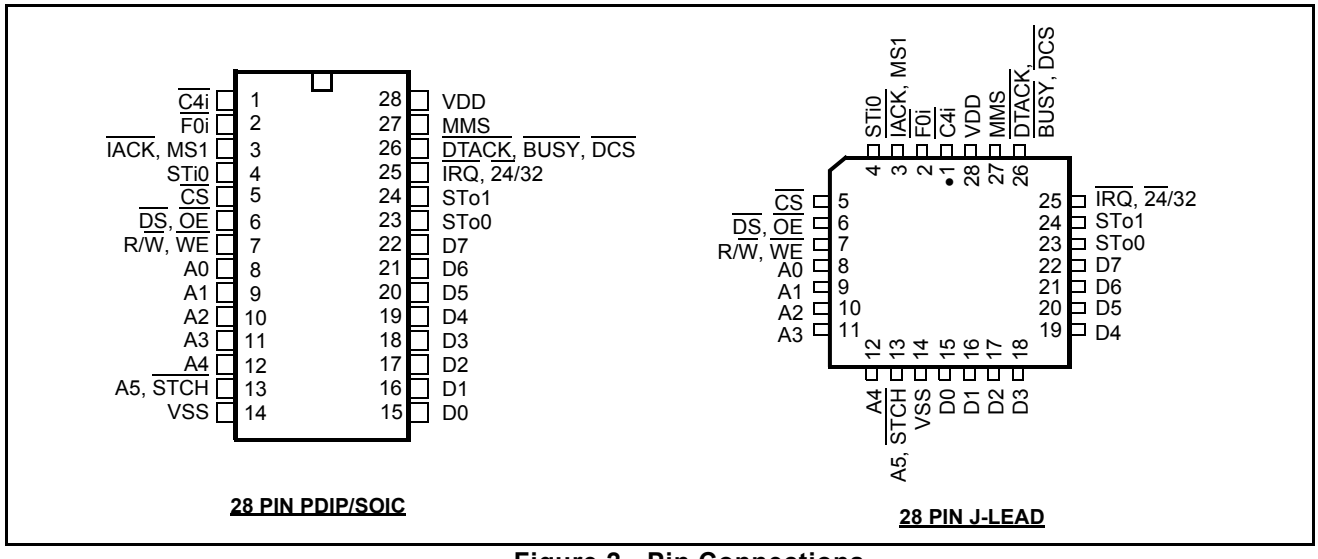


Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description‡
1	$\overline{C4i}$	**4.096 MHz Clock.** The ST-BUS timing clock used to establish bit cell boundaries for the serial bus.
2	$\overline{F0i}$	**Framing Pulse.** A low going pulse used to synchronize the STPA to the 2048 kbit/s ST-BUS stream. The first falling edge of $\overline{C4i}$ subsequent to the falling edge of $\overline{F0i}$ identifies the start of a frame.
3	$\overline{IACK}$	**Interrupt Acknowledge (Mode 1).** This active low input signals that the current bus cycle is an interrupt vector fetch cycle. Upon receiving this acknowledgement, the STPA will output a user-programmed vector number on D_0 - D_7 indicating the source of the interrupt.
	MS1	**Mode Select 1 (Mode 2,3).** This input is used to select the device operating modes. A low applied to this pin will select mode 3 while a high will select mode 2. (Refer to Table 1.)
4	STi0	**ST-BUS Input 0.** This is the input for the 2048 kbit/s ST-BUS serial data stream.
5	$\overline{CS}$	**Chip Select.** This active low input is used to select the STPA for a parallel access .
6	$\overline{DS}$	**Data Strobe (Mode 1).** This active low input indicates to the STPA that valid data is on the data bus during a write operation or that the STPA must output valid data on the data bus during a read operation.
	$\overline{OE}$	**Output Enable (Mode 2).** This active low input enables the data bus driver outputs.
	$\overline{OE}$	**Output Enable (Mode 3).** This active low output indicates that the selected device is to be read and that the data bus is available for data transfer.
7	R/$\overline{W}$	**Read/Write (Mode 1,2).** This input defines the data bus transfer as a read (R/$\overline{W}$ = 1) or a write (R/$\overline{W}$= 0) cycle.
	$\overline{WE}$	**Write Enable (Mode 3).** This active low output indicates the data on the data bus is to be written into the selected location of an external device.
8-12	A0-A4	**Address Bus (Mode 1,2).** These inputs are used to select the internal registers and two-port memories of the STPA.
	A0-A4	**Address Bus (Mode 3).** These address outputs are generated by the STPA and reflect the position in internal RAM where the information will be fetched from or stored in. Addresses generated in this mode are used to access external devices for direct memory transfer.

Pin Description (continued)

Pin #	Name	Description‡
13	A5	**Address Bit A5 (Mode 1).** This input is used to extend the address range of the STPA. A5 selects internal registers when high and Tx/Rx RAM's when low.
	A5	**Address Bit A5 (Mode 2).** This input is used to extend the address range of the STPA. A5 selects Tx0/Rx0 RAM's when low and Tx1/Rx0 RAM's when high.
	$\overline{\text{STCH}}$	**Start of Channel (Mode 3).** This signal is a low going pulse which indicates the start of an ST-BUS channel. The pulse is four bits wide and begins at the start of each valid channel.
14	V_{SS}	**Ground.**
15-22	D0-D7	**Bidirectional Data Bus.** This bus is used to transfer data to or from the STPA during a write or read operation.
23	STo0	**ST-BUS Output 0.** This output supplies the output ST-BUS 2048 kbit/s serial data stream from Tx0 two-port RAM.
24	STo1	**ST-BUS Output 1.** In modes 1 and 2 this output supplies the output ST-BUS 2048 kbit/s serial data stream from Tx1 two-port RAM. In mode 3, information arriving at STi0 is output here with one frame delay.
25	$\overline{\text{IRQ}}$	**Interrupt Request (Mode 1).** This open drain output, when low, indicates when an interrupt condition has been raised within the STPA.
	$\overline{24}$/32	**24 Channel/32 Channel Select (Mode 2,3).** This input is used to select the channel configuration in modes 2 and 3. A low applied to this pin will select a 24 (T1) channel mode while a high will select a 32 (CEPT) channel mode.
26	$\overline{\text{DTACK}}$	**Data Transfer Acknowledge (Mode 1).** This open drain output is supplied by the STPA to acknowledge the completion of data transfers back to the μP. On a read of the STPA, $\overline{\text{DTACK}}$ low indicates that the STPA has put valid data on the data bus. On a write, $\overline{\text{DTACK}}$ low indicates that the STPA has completed latching the μP's data from the data bus.
	$\overline{\text{BUSY}}$	**BUSY (Mode 2).** This open drain output signals that the controller and the ST-BUS are accessing the same location in the dual-port RAM's. It is intended to delay the controller access until after the ST-BUS completes its access.
	$\overline{\text{DCS}}$	**Delayed Chip Select (Mode 3).** This low going pulse, which is four bit cells long, is active during the last half of a valid channel. This signal is used to daisy-chain together two STPA's in mode 3 that are accessing devices on the same parallel data bus.
27	MMS	**Master Mode Select (Reset).** This Schmitt trigger input selects between either mode 1 (MMS = 1), or modes 2and 3 (MMS = 0). If MMS is pulsed low in Mode 1 operation the control and interrupt registers will be reset. (Refer to Table 1.) During power-up, the time constant of the reset circuit (see Fig. 8) must be a minimum of five times the rise time of the power supply.
28	V_{DD}	**Power Supply Input.** (+5V).

‡ Pin Descriptions pertain to all modes unless otherwise stated.

Mode	MMS	MS1	Mode of Operation	Function
1	1	N/A	μP Peripheral Mode	The STPA provides parallel-to-serial and serial-to-parallel conversions through a 68000-type interface. Two Tx RAMs and one Rx RAM are available along with full interrupt capability. 32 channel or 24 channel support is available. Control Register 1, bit D_5 (RAMCON) = 0 for 32 channel operation and D_5 (RAMCON)= 1 for 24 channel operation.
2	0	1	Fast RAM Mode	The STPA provides a fast access interface to Tx0, Tx1 and Rx0 RAMs. This mode is intended for full parallel support of 24 channel T1/ESF trunks and 32 channel CEPT trunks. Input 24/32 (pin 25) = 0 for 24 channel operation, input 24/32 (pin 25) = 1 for 32 channel operation.
3	0	0	Bus Controller Mode	The STPA will synchronously drive the parallel bus using the address generator and provide all data transfer signals. This mode is intended to support 24 or 32 channel devices in the absence of a parallel bus controller. Input 24/32 (pin 25) = 0 for 24 channel operation, input 24/32 (pin 25) = 1 for 32 channel operation.

Table 1. STPA Modes of Operation

Functional Description

The STPA (ST-BUS Parallel Access) device provides a simple interface between Zarlink's ST-BUS and parallel system environments. The ST-BUS is a synchronous, time division, multiplexed serial bussing scheme with data streams operating at 2048 kbit/s. The ST-BUS is the primary means of access for voice, data and control information to Zarlink's family of digital telecommunications components, including North American and European digital trunk interfaces, ISDN U and S digital line interfaces, filter codecs, rate adapters, etc. The STPA provides several modes of operation optimized according to the type of information being handled.

For interfacing parallel data and control information to the ST-BUS, such as signalling and link control for digital trunks, the STPA provides a μP access mode (Mode 1), and looks like a 68000 type peripheral. In this mode, the device provides powerful interrupt features, useful in monitoring digital trunk or line status (i.e., synchronization, alarms, etc.) or for setting up message communication links between microprocessors.

To interface high speed data or multi-channel voice/ data to the ST-BUS for switching or transmission, the STPA has a high speed synchronous access mode (Mode 2) and acts like a fast RAM. For voice storage and forward, bulk data transfer, data buffering and other similar applications, the STPA has a controllerless mode (Mode 3) in which it provides address and control signals to the parallel bus This is useful for performing direct transfers to the ST-BUS from external devices such as a RAM buffer.

The STPA is a two port device as shown in the functional block diagram in Figure 1. The parallel port provides direct access to three dual port RAM's, two transmit and one receive. The address, data and control busses are used to communicate between the RAM's and a parallel environment.

Two parallel-to-serial converters, and one serial-to-parallel converter interface the dual port RAM's to the ST-BUS port of the STPA. This port consists of two serial output streams and one serial input stream operating at 2048 kbit/s. This configuration of two outputs and one input was designed to allow a single STPA to form a complete control interface to Zarlink's digital trunk interfaces (MT8976, MT8978 and MT8979) which have two serial input and one serial output control streams.

ST-BUS clocking circuitry, address generator and various control and interrupt registers complete the STPA's functionality.

Modes of Operation

The three basic modes of operation, μP Peripheral Mode (Mode 1), Fast RAM Mode (Mode 2) and Bus Controller Mode (Mode 3) are selected using two external input pins. These inputs are MMS and MS1 and are decoded as shown in Table 1. Whenever MMS=1 the device resides in Mode 1. In this mode, MS1 pin is unavailable and is used for a different function.

When MMS=0, Modes 2 or 3 are selected as determined by input MS1. If MS1=1, Mode 2 is selected and if MS1 =0, Mode 3 is selected.

Each of the modes of the STPA provides a different pinout to ease interfacing requirements of different parallel environments. These are shown in Figure 3 below. In μP Peripheral Mode the device uses interface signals consistent with a 68000-type μP bus. Mode 2, Fast RAM Mode, uses signals typical of standard RAM type interfaces. Mode 3 interface signals are very similiar to Mode 2 signals except that the address and control signals are supplied as outputs by the STPA.

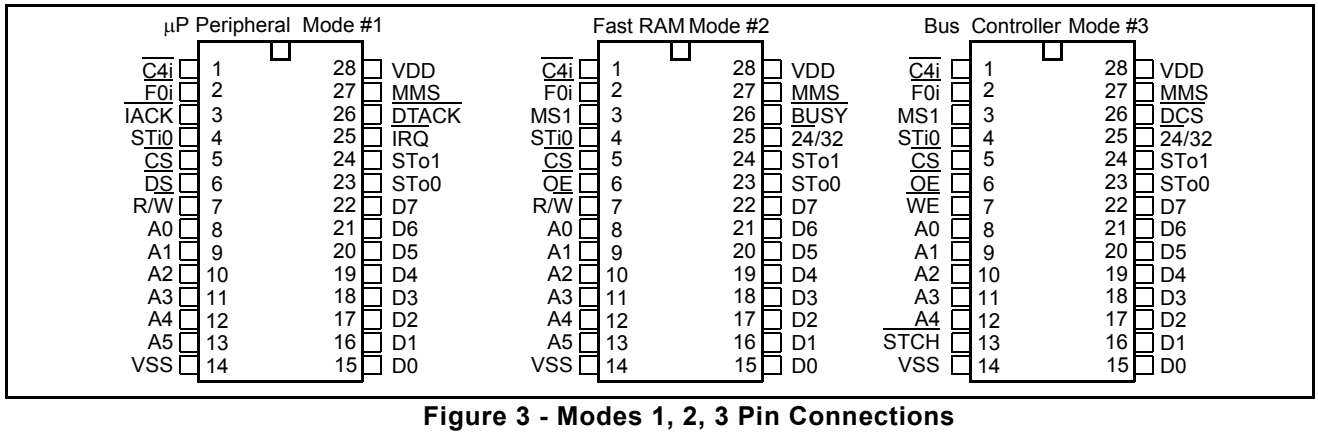


Figure 3 - Modes 1, 2, 3 Pin Connections

24/32 Channel Operation

The STPA may be configured to operate as a 32 channel or 24 channel device. This feature, which is available in all three modes of operation, is particularly useful in applications involving data access to CEPT and T1 digital trunk interfaces.

When used as a data interface to Zarlink's CEPT digital trunks, the STPA maps the 32 consecutive bytes of each dual port memory directly to ST-BUS channels 0-31. This is performed by the address generator shown in the functional block diagram (see Figure 1). Figures 4 c & d show the relationship between relative dual port RAM locations and corresponding ST-BUS channels, for both input and output serial streams, when the STPA is configured as a 32 channel device.

When used as a data interface to Zarlink's T1 trunk devices, however, only the first 24 consecutive RAM locations are mapped to 24 of the 32 ST-BUS channels. This mapping follows a specific pattern which corresponds with the data streams used by Zarlink's T1 products. Instead of a direct correlation (as in 32 channel operation), the 24 consecutive RAM locations are mapped to the ST-BUS with every fourth channel, beginning at channel 0, set to FF_{16} (ie. channel 0, 4, 8, 12, 16, 20, 24 and 28). Figures 4 a & b show the relationship between RAM locations and ST-BUS channel configuration. This feature allows the STPA to be interfaced directly to Zarlink's T1 trunk family.

When the STPA is operated in Mode 1, 24 and 32 channel configurations are selected using bit D_5 (RAMCON) in Control Register 1. D_5 = 0 selects 32 channel operation and D_5 = 1 selects 24 channel operation. When the STPA is operated in Modes 2 or 3, however, the channel configuration is done using input $\overline{24}/32$ (pin 25). When $\overline{24}/32$ = 1 the device uses all 32 channels and when $\overline{24}/32$ = 0 it uses 24.

Dual Port RAMS

Each of the three serial ST-BUS streams is interfaced to the parallel bus through a 32 byte dual port RAM. This allows parallel bus accesses to be performed asynchronously while accesses at the ST-BUS port are synchronous with ST-BUS clock. As with any dual port RAM interface between two asynchronous systems, the possibility of access contention exists. The STPA minimizes this occurrence by recognizing contention only when accesses are performed at the same time for the same 8-bit cell within the dual port RAM's. Furthermore, the probability of contention is lessened since ST-BUS accesses require only the last half cycle of $\overline{C4i}$ of every channel. When contention does occur, priority is always given to the ST-BUS access.

The STPA indicates this contention situation in a different manner for Modes 1 and 2. In Mode 1, the contention is masked by virtue of the "handshaking" method used to transfer data on this 68000-type interface. Data Strobe ($\overline{DS}$) and Data Transfer Acknowledge ($\overline{DTACK}$) control the exchange. If contention should occur the device will delay returning $\overline{DTACK}$ and thus stretch the bus cycle until the µP access can be completed.

In Mode 2, if access is attempted during a "contention window" the STPA will supply the $\overline{BUSY}$ signal to delay the start of the bus cycle. This "contention window" is defined as shown in Figure 16. The window exists during the last cycle of C4i clock in each channel timeslot. Although ST-BUS access is only required during the last half of this clock period, the "contention window" exists for the entire clock period since a parallel access occurring just prior to an ST-BUS access will not complete before the ST-BUS access begins. Figure 16 further shows four possible situations that may occur when parallel accesses are attempted in and around the "contention window". Condition 1 indicates that an access occurring prior to the contention window but lasting into the first half of it will complete normally with no contention arbitration. If the access should extend past the first half of the contention window and into the ST-BUS access period, the $\overline{BUSY}$ signal will be generated. Conditions 3 and 4 show accesses occurring inside the contention window. These accesses will result in $\overline{BUSY}$ becoming active immediately after the access is initiated and remaining active as shown in Figure 16.

Access contention is non-existent in Mode 3 since the parallel bus signals, driven by the STPA, are synchronized to the ST-BUS clocks.

Mode 1 - µP Peripheral Mode

In Mode 1, the STPA operates as an asynchronous 68000-type microprocessor peripheral. All three dual-port RAMS (Tx0, Tx1, Rx0) are made available and may be configured as 32 or 24 byte RAM's. Also available are the full complement of control and interrupt registers. The address map for Mode 1 is shown in Table 2.

The STPA, in Mode 1, uses signals $\overline{CS}$, R/$\overline{W}$, $\overline{DS}$ (Data Strobe), $\overline{DTACK}$ (Data Acknowledge) $\overline{IRQ}$, and $\overline{IACK}$ (Interrupt Acknowledge) at the parallel interface. The pinout of the device is shown in Figure 3.

STi0	0 X	1	2	3	4 X	5	6	7	8 X	9	10	11	12 X	13	14	15	16 X	17	18	19	20 X	21	22	23	24 X	25	26	27	28 X	29	30	31
RELATIVE RAM LOCATION		0	1	2		3	4	5		6	7	8		9	10	11		12	13	14		15	16	17		18	19	20		21	22	23

Figure 4 a) RELATIVE Rx RAM ADDRESS vs. ST-BUS CHANNEL - 24 CHANNEL MODE

STo0 STo1	0 X	1	2	3	4 X	5	6	7	8 X	9	10	11	12 X	13	14	15	16 X	17	18	19	20 X	21	22	23	24 X	25	26	27	28 X	29	30	31
RELATIVE RAM LOCATION		0	1	2		3	4	5		6	7	8		9	10	11		12	13	14		15	16	17		18	19	20		21	22	23

Figure 4 b) RELATIVE Tx RAM ADDRESS vs. ST-BUS CHANNEL - 24 CHANNEL MODE

STi0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
RELATIVE RAM LOCATION	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

Figure 4 c) RELATIVE Rx RAM ADDRESS vs. ST-BUS CHANNEL - 32 CHANNEL MODE

STo0 STo1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
RELATIVE RAM LOCATION	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

Figure 4 d) RELATIVE Tx RAM ADDRESS vs. ST-BUS CHANNEL - 32 CHANNEL MODE

X- unused channels marked X transmit FF_{16}

ADDRESS BITS							REGISTERS	
A_6	A_5	A_4	A_3	A_2	A_1	A_0	READ	WRITE
0	0	0	0	0	0	0	Rx0 - Channel 0	Tx0 - Channel 0
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
0	0	1	1	1	1	1	Rx0 - Channel 31	Tx0 - Channel 31
X	1	0	0	0	0	0	Control Register 1	Control Register 1
X	1	0	0	0	0	1	Control Register 2	Control Register 2
X	1	0	0	0	1	0	Interrupt Vector Register	Interrupt Vector Register
X	1	0	0	1	0	0	Interrupt Flag Register 1	-
X	1	0	0	1	0	1	Interrupt Flag Register 2	-
X	1	0	0	1	1	0	Image Register 1	-
X	1	0	0	1	1	1	Image Register 2	-
X	1	0	1	0	0	0	Interrupt Mask Register 1	Interrupt Mask Register 1
X	1	0	1	0	0	1	Interrupt Mask Register 2	Interrupt Mask Register 2
X	1	0	1	0	1	0	Match Byte Register 1	Match Byte Register 1
X	1	0	1	0	1	1	Match Byte Register 2	Match Byte Register 2
X	1	0	1	1	0	0	Interrupt Channel Address 1	Interrupt Channel Address 1
X	1	0	1	1	0	1	Interrupt Channel Address 2	Interrupt Channel Address 2
1	0	0	0	0	0	0	Rx0 - Channel 0	Tx1 - Channel 0
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	0	1	1	1	1	1	Rx0 - Channel 31	Tx1 - Channel 31

Table 2. Mode 1 Address Map

NOTES: X is don't care
A_6 is bit D_4 of Control Register 1

Bit	Name	Description
7	(Unused)	
6	IRQRST	**Interrupt Reset.** This bit, when set high, automatically clears the Interrupt Flag Register and the Interrupt Image Register without these registers being serviced. This bit automatically resets to zero after the register clear is completed.
5	RAMCON	**RAM Configuration.** This bit configures Tx0, Tx1 and Rx0 RAMS for 32 or 24 byte operation. D_5 = 0 for 32 channel; D_5 = 1 for 24 channel.
4	A_6	**Address Bit A6.** This bit extends the addressing range for access to Tx1 memory.
3	IRQ2MODE	**Interrupt Source 2 Mode Select.** This bit configures the source 2 interrupt generator. D_3 = 0 selects "static" interrupt mode; D_3 = 1 selects "dynamic" interrupt mode.
2	IRQ1MODE	**Interrupt Source 1 Mode Select.** This bit configures the source 1 interrupt generator. D_2 = 0 selects "static" interrupt mode; D_2 = 1 selects "dynamic" interrupt mode.
1	IRQ2EN	**Interrupt Source 2 Enable.** IRQ2EN = 1 enables interrupts to occur from source 2.
0	IRQ1EN	**Interrupt Source 1 Enable.** IRQ1EN = 1 enables interrupts to occur from source 1.

Table 3. Control Register 1 Bit Definitions

Timing information for data transfers on this interface is shown in Figure 14. The Mode 1 interface is designed to operate directly with a 68000-type asynchronous bus but can easily accommodate most other popular microprocessors as well.

Control Registers

Two control registers allow control of Mode 1 features. Control Register 1 provides bits to select the type of interrupt, to enable interrupts from two different and independent sources and to reset the interrupt registers. Also contained in Control Register 1 are bits to configure the device for 24 or 32 channel operation and to expand the address range for convenient access to the second transmit RAM Tx1. A description of the bit functions in Control Register 1 is shown in Table 3.

Mode 1 provides various loopback paths and output configuration options which are controlled by bits in Control Register 2. Bits D_0, D_1 of Control Register 2 configure loopbacks using input and output streams STi0, STo0 as described in Table 4. The input stream STi0 can be looped back to source the output stream STo0 as well as receive RAM Rx0. The transmit RAM Tx0 can be looped to source the receive RAM Rx0, as well as STo0 and, the transmit RAM Tx0 can be looped to the receive RAM Rx0 while STi0 sources STo0. The function of these loopback configurations is shown in Figure 5.

In a similar way, the output STo1 can be reconfigured for different functionality. Bits D_2 and D_3 of Control Register 2 allow STo1 to be sourced, with a one frame delay via Tx1 from receive stream STi0. STo1 can also output the result of a comparison of the contents of Tx1 ram with input stream STi0. These output configurations of STo1 are shown in Figure 6 a and b. Figure 6 c shows the effect of combining these two features.

Interrupt Registers

Interrupts can be generated in Mode 1 only. Two channels of the ST-BUS input stream, STi0, can be selected to provide an interrupt to the system. Interrupts can be of two types: Static or Dynamic. Static interrupts are caused when data within a selected channel matches a given pattern. Dynamic interrupts occur when bits in a selected channel change state (1 to 0, 0 to 1 or toggle). Interrupts are controlled through two identical paths (1 and 2) consisting of the following registers:

Interrupt Channel Address (1/2): The address (0-31) of the channel which will generate the interrupt is stored in this register.

Image Register (1/2): The contents of the channel causing the interrupt is stored in this register. Reading this register will clear its contents.

Match Byte Register (1/2): In static mode this register is used to store the byte which will be compared with the contents of the selected channel causing the interrupt.

In dynamic mode, the bits in this register and the corresponding bit in the Interrupt Mask Register define the type of dynamic interrupt (i.e., 0 to 1, 1 to 0, toggle). (Refer to Table 5.)

Bit	Name	Description
7-4	(Unused)	
3-2	CONFIG	**STo1 Output Configuration Bits:** D_3D_2 = 00- Normal operation. ST-BUS stream from Tx1 is output on STo1 pin. 01- STi0 stream is output on STo1 pin delayed one frame (Figure 6 a). 10- STi0 is compared through XOR (exclusive OR) with ST-BUS stream from Tx1 and output at STo1 (Figure 6 b). 11- STi0 stream, delayed one frame (via Tx1), is compared (XOR) with the next frame arriving at STi0 and the result output at STo1 (Figure 6 c).
1-0	LOOPBACK	**Internal Loopback Configuration Bits:** D_1D_0 = 00- Normal operation. No internal loops. 01- Loop STi0 to STo0 while still receiving STi0 in Rx0 (Figure 5 a). 10- Loop Tx0 output ST-BUS stream to Rx0 input ST-BUS stream while outputting Tx0 output to STo0. STi0 is not received (Figure 5 b). 11- Loop Tx0 output ST-BUS stream to Rx0 input ST-BUS stream. Loop STi0 to STo0 (Figure 5 c).

Table 4. Control Register 2 Bit Definitions

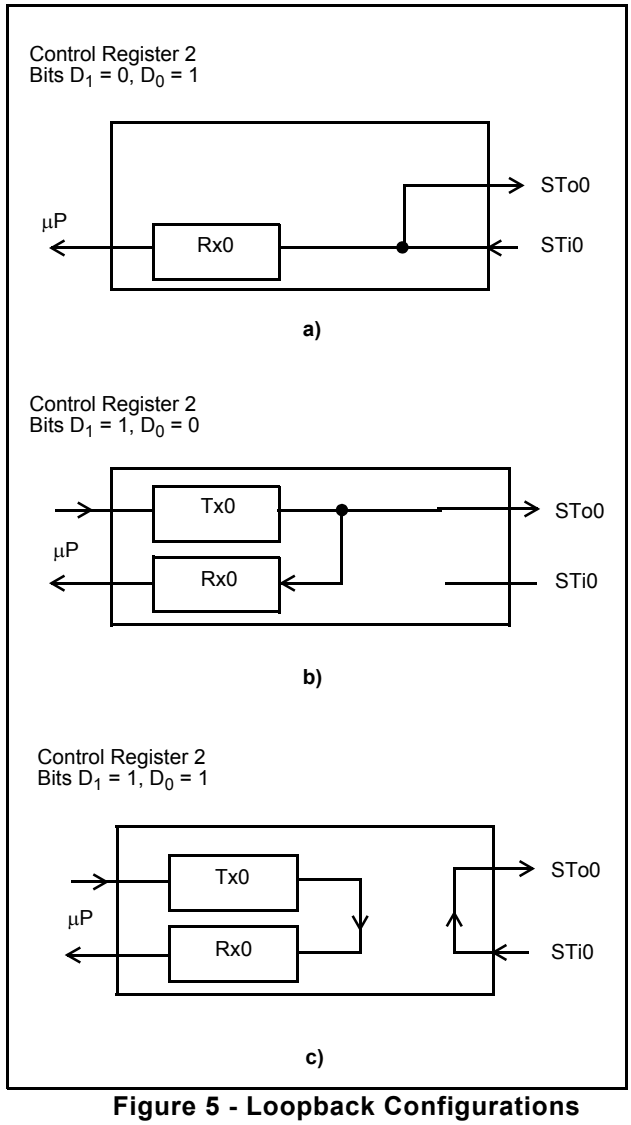


Figure 5 - Loopback Configurations

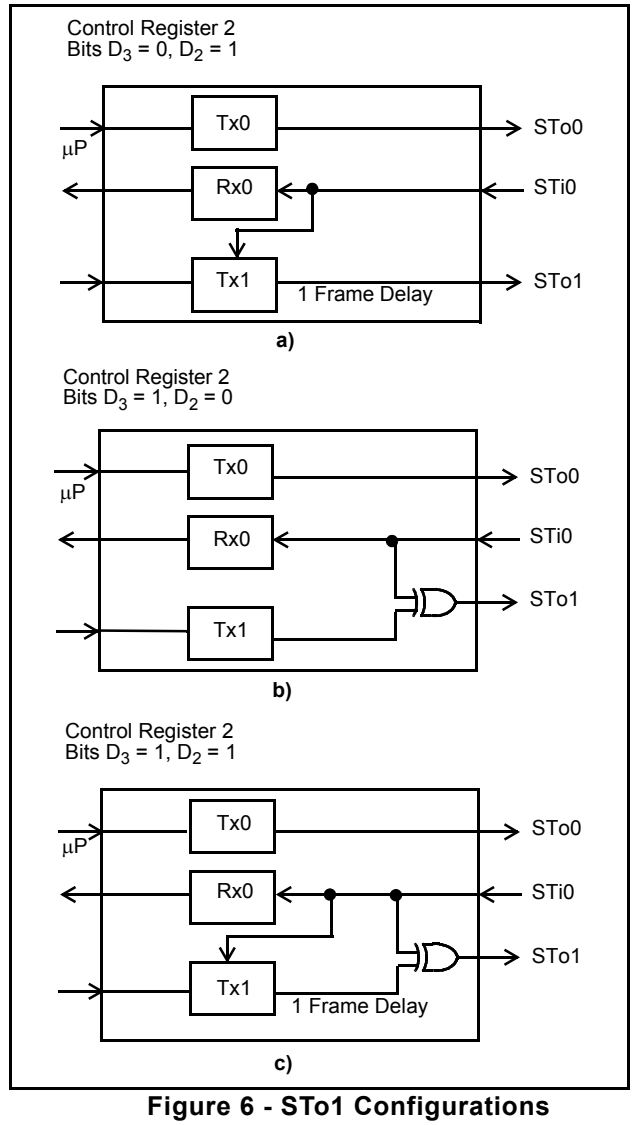


Figure 6 - STo1 Configurations

Interrupt Mask Register (1/2): In static mode the contents of this register masks bits in the Match Byte Register that are 'don't care' bits

1 - bit masked
0 - bit not masked

In dynamic mode, each bit in this register and the corresponding bit in the Match Byte Register define what type of dynamic interrupt is selected. (Refer to Table 5.)

Interrupt Flag Register (1/2): In static mode the least significant bit in this register is set to 1 to flag the corresponding path in which the interrupt occurs.

In dynamic mode this register sets the bits which reflect the position of the bits in the corresponding Interrupt Register which caused the interrupt.

Interrupt Vector Register

This register shown in Figure 7 is common to both interrupt paths and stores an 8 bit vector number which will be output on the data bus when Interrupt Acknowledge ($\overline{IACK}$) is asserted. Bits labelled V_2 - V_7 are stored by the controlling μP. Bits IRQ1 and IRQ2 are set by the STPA to indicate which path caused the interrupt. This creates unique vectors which are used by the μP to vector to interrupt service routines. This feature may be bypassed by simply not asserting $\overline{IACK}$ during interrupt acknowledged.

D7	D6	D5	D4	D3	D2	D1	D0
V_7	V_6	V_5	V_4	V_3	V_2	IRQ2	IRQ1

Figure 7 - Interrupt Vector Registers

Interrupt Modes and Servicing

Static Interrupt Mode

A static interrupt is caused when an incoming byte matches a predefined byte. The incoming byte from a selected channel is stored in Interrupt Image Register (1/2) where it is compared with the contents of the corresponding Match Byte Register. The result of the comparison of individual bits is masked by the contents of the Mask Register (1/2) before it is used to generate an $\overline{IRQ}$. After a static interrupt occurs, information in the Interrupt Image Register is frozen until the μP performs a read operation on this register.

When servicing static interrupts assertion of $\overline{IACK}$ will cause the contents of the Vector Register, with the IRQ1 or IRQ2 bit set, to be output on the data bus. The service routine can subsequently clear $\overline{IRQ}$ by reading the Interrupt Image Register. Alternatively, the IRQRST bit in Control Register 1 can be set to clear the associated interrupt registers.

Static Interrupts are selected using IRQ1MODE and IRQ2MODE bits in Control Register 1. Interrupts are then enabled to the $\overline{IRQ}$ pin with IRQ1EN and IRQ2EN bits of the same register.

Dynamic Interrupt Mode

A dynamic interrupt is generated by a change of state of bits in a selected channel. A 0 to 1 transition or a 1 to 0 transition or a simple change of state from the previous state (toggle) can be detected. The type of transition to be detected is selected using two bits, one from the Match Byte Register (1/2) and one from the Interrupt Mask Register (1/2), in the corresponding bit positions. Table 5 shows how the two registers are programmed.

Match Byte Register bit D_X	Mask Byte Register bit D_X	Transition Type Detected on Incoming bit D_X (x = 0 ....7)
0	0	Mask Bit D_X
0	1	0 to 1 transition
1	0	1 to 0 transition
1	1	Toggle

Table 5 - Dynamic Interrupt Types

For example, the following steps are required to generate an interrupt when bit D_3 of channel 4 changes state from 0 to 1 (all other bits are masked):

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Channel Address Register 1 =	0	0	0	0	0	1	0	0
(channel 4 of STi0 selected)								
Match Byte Register 1 =	0	0	0	0	0	0	0	0
Interrupt Mask Register 1 =	0	0	0	0	1	0	0	0
(When bit D_3 toggles 0 to 1)								

Dynamic interrupts from interrupt path 1 would then be enabled using the Control Register 1.

Control Register 1 =	0	0	0	0	0	1	0	1

This would cause interrupt 1 path to be enabled while interrupt 2 path is disabled.

As with static interrupts, upon serving a dynamic interrupt, assertion of $\overline{IACK}$ will cause the contents of the Vector Register, with the appropriate path bit set, to be output on the data bus. The information contained in the channel is frozen in the Interrupt Image Register. To clear a dynamic interrupt, however, the μP must read the Interrupt Flag Register of the path responsible for the interrupt to determine which bit caused the interrupt. The bit in the corresponding position will be set to 1 and reading this register will clear its contents.

Alternatively, as with static interrupts, the IRQRST bit in Control Register 1 can be set to clear the Image Interrupt Register, Flag Register and path bits in the Vector Register.

Dynamic Interrupts are selected using IRQ1MODE and IRQ2MODE bits in Control Register 1 and are enabled using IRQ1EN and IRQ2EN in the same register.

MMS Pin Reset

The STPA can be RESET in Mode 1 using the MMS pin (27). Applying a low pulse (0V) to MMS after power is applied to the device will reset all control and interrupt registers to 00_{16}. This can be accomplished on power up with a simple R-C circuit as shown in Figure 8.

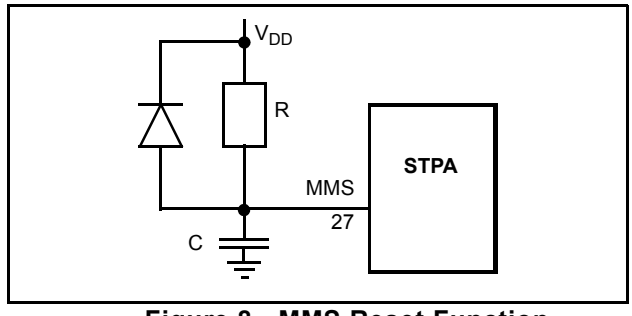


Figure 8 - MMS Reset Function

Mode 2 - Fast RAM Mode

Mode 2 operates as a high speed dual port RAM interface to the ST-BUS. Only the two transmit RAM's, Tx0 and Tx1, and the receive RAM, Rx0 are active in this mode (i.e., control registers and interrupt registers are inactive).

The main feature of this mode is fast access to the dual-port RAM's. Fast access allows high-speed controllers to use this device as a data interface to T1 and CEPT digital links. Timing information is shown in Figure 15.

Mode 2 can also support 24 channel and 32 channel operation. The channel configuration is selected using $\overline{24}$/32 pin. When $\overline{24}$/32=0 the device operates in 24 channel mode and when $\overline{24}$/32=1, it operates in 32 channel mode.

The physical interface in this mode resembles that of a simple RAM device. The signals used to read and write the device are $\overline{CS}$, $\overline{OE}$, R/$\overline{W}$. The pinout of the STPA in this mode is shown in Figure 3. Address decoding for Tx0, Tx1, Rx0 is shown in Table 6.

Contention can arise for access to the dual port RAMS. The occurrence of this is minimized since the ST-BUS serial-to-parallel and parallel-to-serial converters require RAM access for only 1/32 of a channel time (i.e., last half cycle of $\overline{C4i}$ for each channel). For contention to occur the high speed controller must access the same RAM location as that of the ST-BUS. For a parallel read operation this corresponds to the current ST-BUS channel and for a write operation, the next ST-BUS channel. Access contention in Mode 2 is arbitrated with the $\overline{BUSY}$ signal. $\overline{BUSY}$ is intended to hold off any parallel access cycle until it again goes inactive. Figure 16 shows how the access is arbitrated for accesses near the contention window.

Applications using high speed access can easily avoid generating $\overline{BUSY}$ by co-ordinating channel reads and writes with framing and channel boundary information.

Mode 3 - Parallel Bus Controller

In this mode the STPA outputs all necessary signals required to drive devices attached to the parallel port. The STPA can be used to drive devices such as RAM's, FIFO's, latches, A/D and D/A converters, and CODECS, directly from the ST-BUS without an intervening μP. As with the other modes, Mode 3 can operate from 32 channels or 24 channels by connecting $\overline{24}$/32 high or low, respectively. This allows devices to be driven remotely via a T1 or CEPT digital trunk link when used with Zarlink's trunk products.

Referring to Figure 1, the Address Generator block generates and drives the external address lines A4-A0. The STPA also generates $\overline{OE}$ (output enable) and $\overline{WE}$ (write enable) to facilitate data transfers from Rx0 RAM and to Tx0 RAM. Tx1 RAM is unavailable in this mode.

The STPA, in Mode 3, generates external addresses in a particular sequence that minimizes throughput delay through the device. When channel N is present on the ST-BUS, the STPA generates address N+1 on the address bus and asserts $\overline{OE}$ to output data from an external device and latch it into the STPA. During the same channel N, the STPA will generate address N-1 with $\overline{WE}$ asserted to write from the STPA to an external device. Timing for Mode 3 transfers is shown in Figure 17. All parallel bus signals are synchronized to the ST- BUS clock.

The device must be selected using $\overline{CS}$ in order for the parallel bus drivers to be enabled. $\overline{CS}$ should remain active for four ST-BUS bit periods (8 x $\overline{C4i}$ cycles) since a read and a write operation require 2 bit periods each. The STPA generates a signal $\overline{STCH}$ (start of channel) which becomes active at the start of each channel and remains active for 1/2 of the channel time (Figure 18). This signal may be

ADDRESS BITS						REGISTERS	
A_5	A_4	A_3	A_2	A_1	A_0	READ	WRITE
0	0	0	0	0	0	Rx0 - Channel 0	Tx0 - Channel 0
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
0	1	1	1	1	1	Rx0 - Channel 31	Tx0 - Channel 31
1	0	0	0	0	0	Rx0 - Channel 0	Tx1 - Channel 0
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
1	1	1	1	1	1	Rx0 - Channel 31	Tx1 - Channel 31

Table 6. Mode 2 Address Map

connected directly to $\overline{CS}$ to enable the device appropriately.

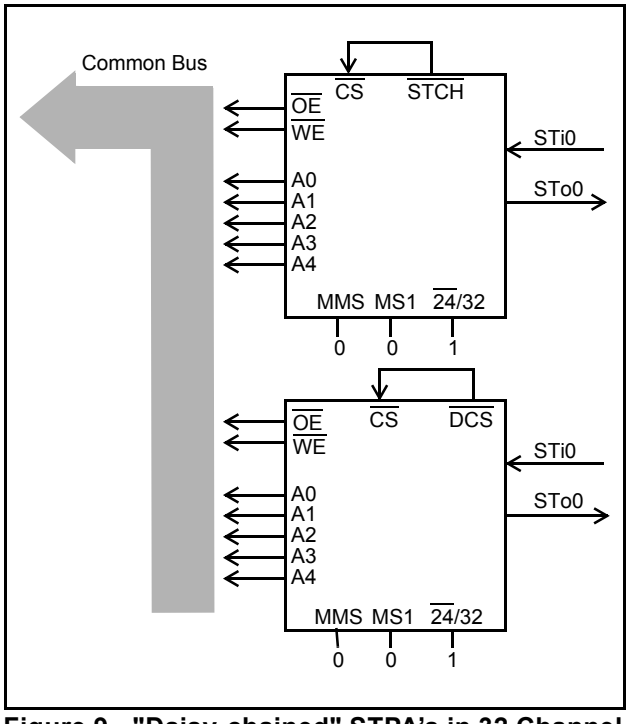


Figure 9 - "Daisy-chained" STPA's in 32 Channel Parallel Bus Controller Mode (Mode 3)

In order to facilitate efficient use of the parallel bus another signal, similar to $\overline{STCH}$, is supplied by the STPA. Delayed Chip Select ($\overline{DCS}$) becomes active for the last half of each channel (Figure 19). This may be connected to a second STPA, residing on the same physical parallel bus, enabling it to perform its read/write operations in the second half of each channel. This allows a large number of devices, connected on a common bus, to be driven by two ST-BUS streams. Figure 9 shows how this "daisy chaining" of STPA's is implemented while Figure 10 illustrates the timing on the shared parallel bus.

Applications

Parallel PBX to Digital Trunk Interface

The STPA is an ideal component for interfacing parallel PBX environments to Zarlink's family of digital trunk devices.

Figure 11 shows a typical interface for both T1/ESF and CRC-4 CEPT digital trunks to a system utilizing a parallel bus architecture. Both the MH89760B T1/ESF and the MH89790B CRC-4 CEPT trunk modules are shown interfaced to a parallel bus structure using two STPAs operating in modes 1 and 2.

The first STPA operating in mode 2 (MMS=0, MS1=1, $\overline{24}$/32=0), routes data and/or voice information between the parallel telecom bus and the T1 or CEPT link via DSTi and DSTo. The second STPA, operating in mode 1 (MMS=1) provides access from the signalling and link control bus to the MH89760B or MH89790B status and control channels. All signalling and link functions may be controlled easily through the STPA transmit RAM's Tx0, Tx1, while status information is read at receive RAM Rx0. In addition, interrupts can be set up to notify the system in case of slips, loss of sync, alarms, violations, etc.

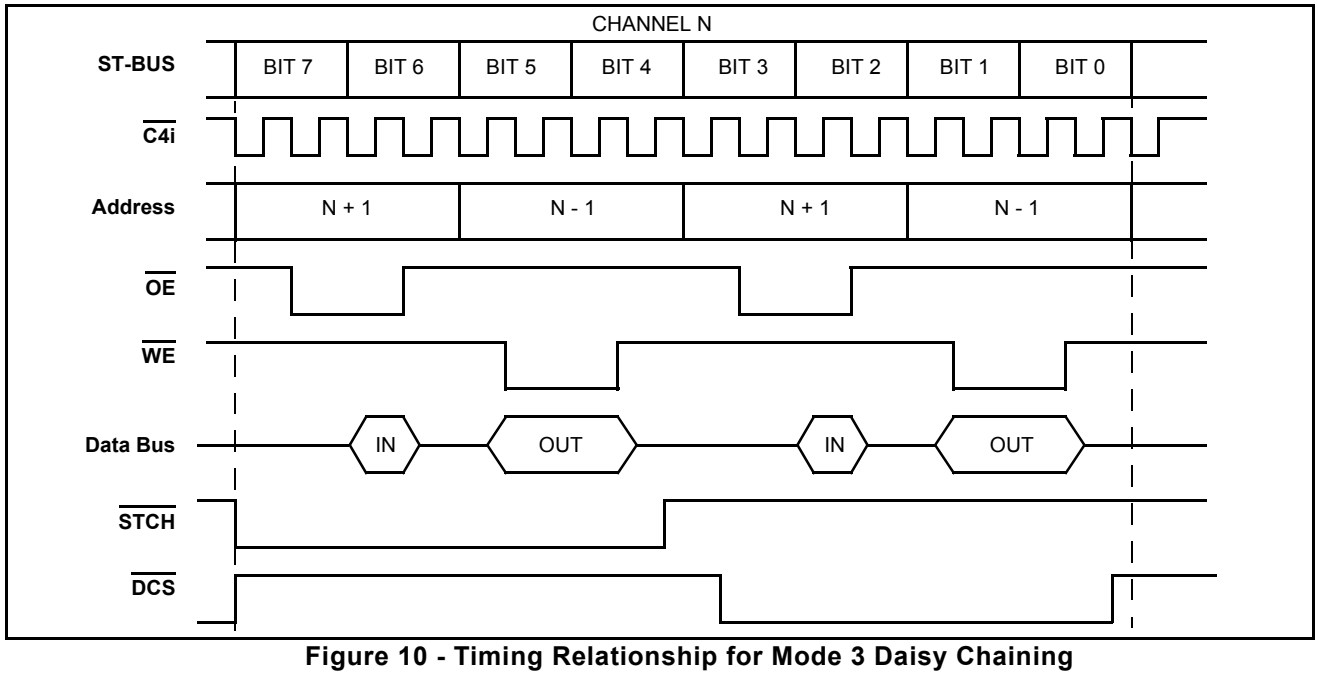
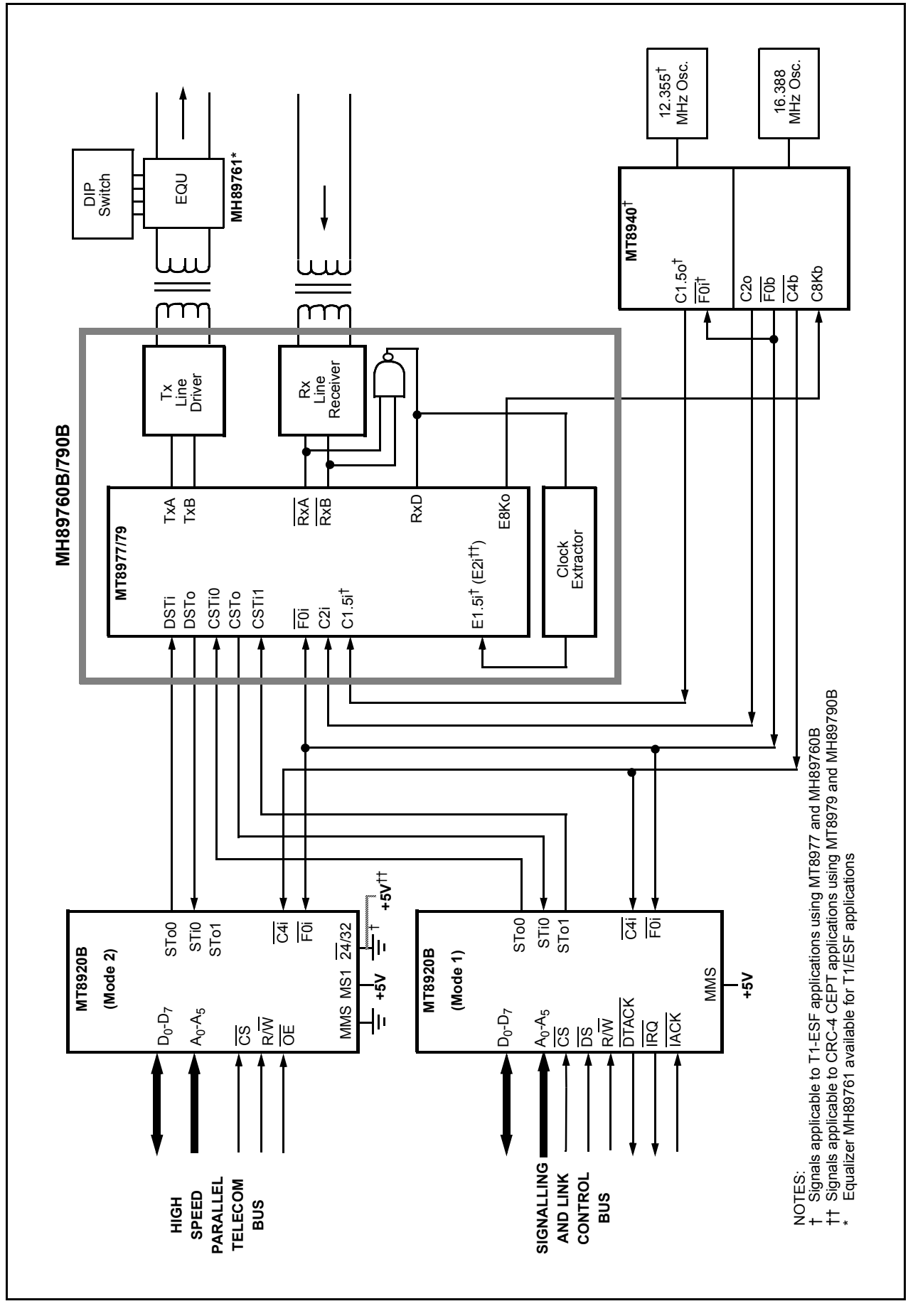


Figure 10 - Timing Relationship for Mode 3 Daisy Chaining



NOTES:
† Signals applicable to T1-ESF applications using MT8977 and MH89760B
†† Signals applicable to CRC-4 CEPT applications using MT8979 and MH89790B
* Equalizer MH89761 available for T1/ESF applications

Figure 11 - Typical T1-ESF / CRC-4 CEPT Digital Trunk Configuration

Digital Signal Processor to ST-BUS Interface

Mode 2 allows many high speed devices to be easily connected to the ST-BUS. Figure 12 shows a TMS32020 digital signal processor interfaced to the ST-BUS through the STPA. This simple interface allows complex functions to be implemented in such systems as PBX's and computer systems. Some of the possible functions include:

- Digital Filtering
- Voice Conferencing
- Speech/Data Compression
- Encryption
- Tone Detection and Generation
- Frequency Spectrum Analysis
- Image Processing
- μ-Law to A-Law Conversion
- Echo Cancellation
- Modulation
- Speech Synthesis and Recognition

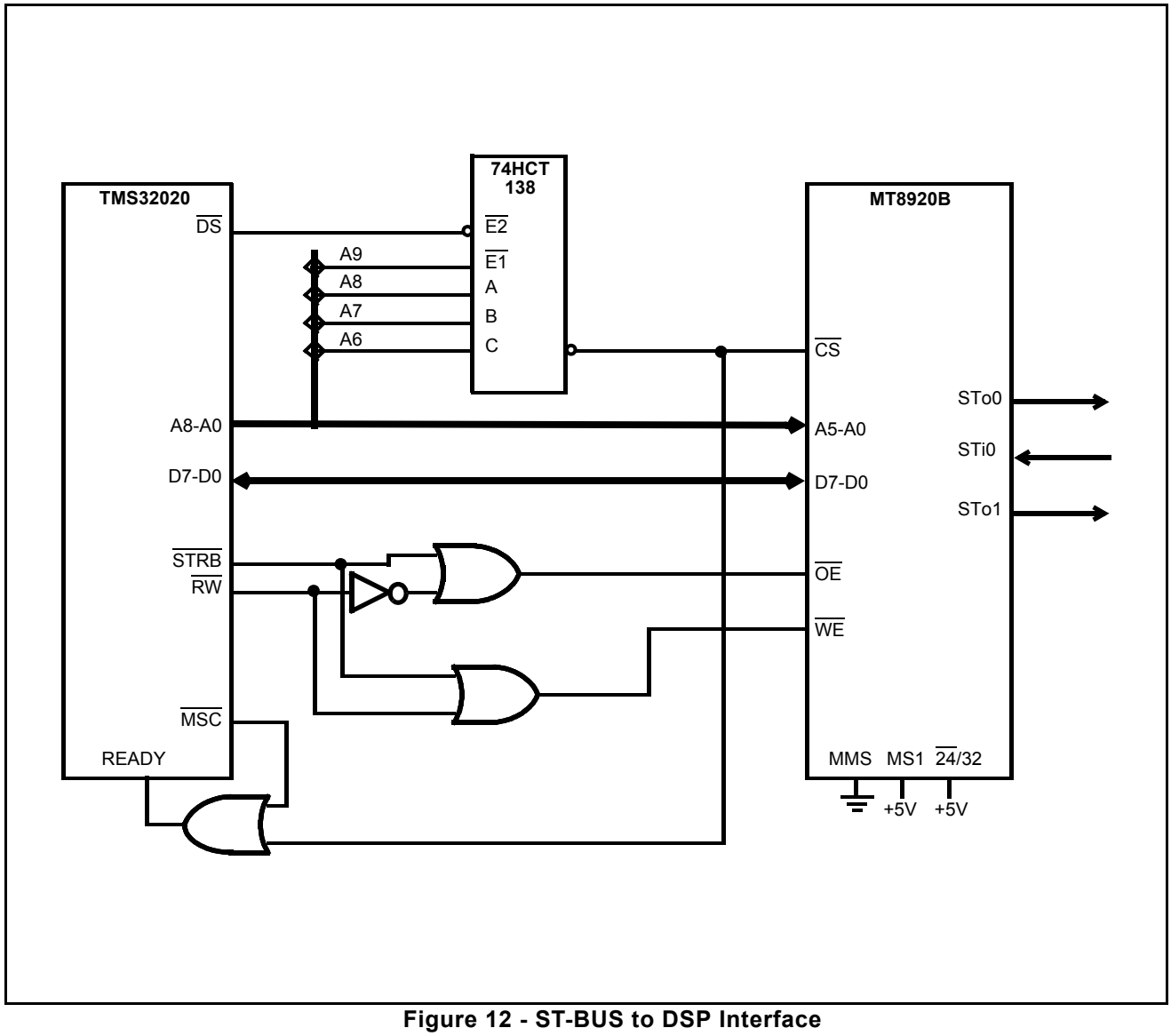


Figure 12 - ST-BUS to DSP Interface

Connecting the STPA to a shared ST-BUS Line

The STPA's STo0 and STo1 outputs cannot be directly forced into a high impedance state. However, with some external logic, the STo0 output can be buffered by a three-state device, controlled by the STo1 output. This application is only possible if the Tx1 RAM and associated STo1 output are not required for some other purpose.

Figure 13 shows an external buffer U1 controlled by the STo1 output and an external Output Data Enable (ODE) signal. When FF (hex) is written to the Tx1 RAM, the corresponding STo1 output channel goes to logic high. This signal, AND-ed together with a logic high at ODE, enables U1, resulting in the STo0 signal transparently passed to the output of U1. When 00 (hex) is written to the Tx1 RAM, the STo1 output goes logic low. This disables U1, resulting in a high impedance state at the output of U1, corresponding to the selected channel.

This method of three-state buffering permits output control on a per-channel or per-bit basis.

The ODE input is used to enable the ST-BUS outputs after all ST-BUS devices are properly configured by software. This eliminates the possibility of contention on the ST-BUS lines during the power-up state.

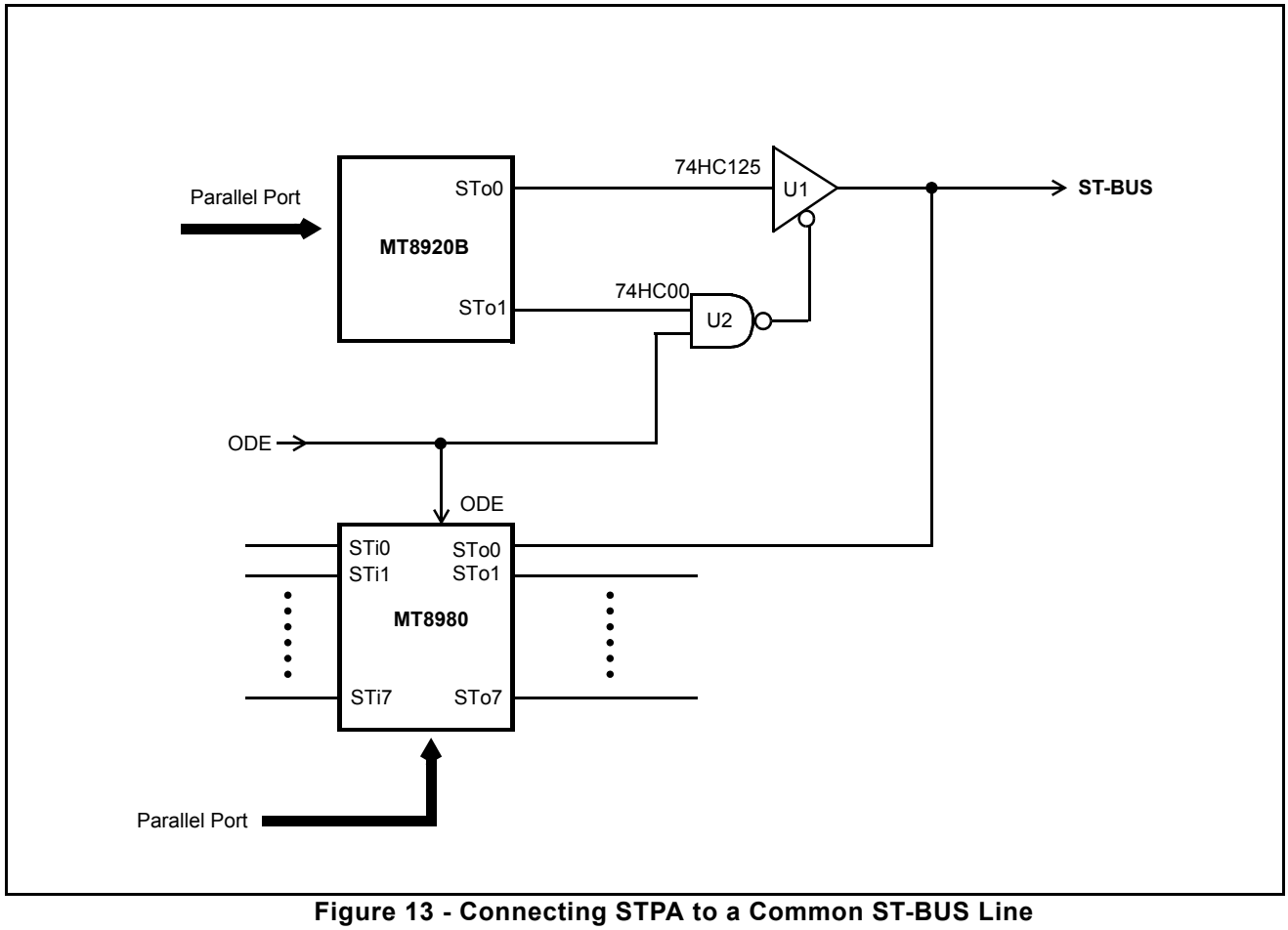


Figure 13 - Connecting STPA to a Common ST-BUS Line

Absolute Maximum Ratings*

- Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Symbol	Min.	Max.	Units
1	Supply Voltage	V_{DD}	-0.3	7.0	V
2	Voltage on any I/O pin		-0.3	V_{DD} + 0.3	V
3	Current on any I/O pin	$I_{I/O}$		±25	mA
4	Storage Temperature	T_{ST}	-55	125	°C
5	Package Power Dissipation Plastic	P_D		600	mW

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions

- Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Supply Voltage	V_{DD}	4.75	5.0	5.25	V	
2	Input High Voltage	V_{IH}	2.4		V_{DD}	V	for 400mV noise margin
3	Input Low Voltage	V_{IL}	0		0.4	V	for 400mV noise margin
4	Operating Temperature	T_A	-40	25	85	°C	
5	Operating Clock Frequency	f_{CK}		4.096		MHz	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics

- Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Supply Current Static Dynamic	I_{CCS} I_{CCD}		10 5	 10	µA mA	outputs unloaded @f_{CK} = 4.096 MHz
2	Input High Voltage	V_{IH}	2.0			V	
3	Input Low Voltage	V_{IL}			0.8	V	
4	Input Leakage Current	I_Z			±10	µA	V_{DD}=5.25V, V_{IN}=V_{SS} to V_{DD}
5	Input capacitance	C_{IN}			10	pF	
6	Schmitt trigger input high (MMS)	V_{T+}	3.8	3.0		V	
7	Schmitt trigger input low (MMS)	V_{T-}		2.0	1.0	V	
8	Schmitt trigger hysteresis (MMS)	V_H	0.8	1.0		V	
9	Output high current (except $\overline{IRQ}$)	I_{OH}	10	15		mA	V_{OH} = 2.4V, V_{DD} = 4.75V
10	Output low current (except $\overline{IRQ}$)	I_{OL}	5	10		mA	V_{OL} = 0.4V, V_{DD} = 4.75V
11	$\overline{IRQ}$, $\overline{DTACK}$, $\overline{BUSY}$ Sink Current	I_{OL}	10	15		mA	V_{OL} = 0.4V, V_{DD} = 4.75V
12	Tristate Leakage A_4-A_0, $\overline{OE}$, $\overline{WE}$ (mode 3)	I_{OZ}		±1	±10	µA	V_{DD} = 5.25V V_{OUT} = V_{SS} to V_{DD}
13	Open drain off-state current $\overline{IRQ}$, $\overline{DTACK}$, $\overline{BUSY}$	I_{OFF}		±1	±20	µA	V_{DD} = 5.25V V_{OUT} = V_{DD}
14	Output capacitance	C_O			15	pF	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Mode 1 Parallel Bus Timing (see Fig. 14)

(V_{CC}=5.0V ±5%,T_A=-40 to 85°C)

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Address to $\overline{DS}$ ($\overline{CS}$) Low††	t_{ARDS}	0			ns	
2	R/$\overline{W}$ to $\overline{DS}$ ($\overline{CS}$) Low††	t_{RWDS}	20			ns	
3	$\overline{DS}$ ($\overline{CS}$) Low to $\overline{DTACK}$ Low††	t_{RDS}[1,2]	t_{cwm}	t_{CLK}	2*t_{CLK}	ns	Load C
4	Valid Data to $\overline{DTACK}$ Low (Read)	t_{RD}	t_{cwm} -30			ns	Load A, C_L=130pF, R_L=740Ω
5	$\overline{DS}$ High to $\overline{DTACK}$ High	t_{DAR}			65	ns	Load C, C_L=50pF
6	$\overline{DS}$ High to Data High Imped.(Read)	t_{DHZ}	0		45	ns	Load A, C_L=130pF, R_L=740Ω
7	$\overline{DS}$ High to $\overline{CS}$ High	t_{CSH}	0			ns	
8	Data Hold Time (Write)	t_{DHT}	0			ns	
9	Input Data Valid after $\overline{DS}$	t_{DST}			t_{cwm} -30	ns	
10	Address Hold Time††	t_{ADHT}	50			ns	

† Timing is over recommended temperature & power supply voltages.

‡ Typical figures are at 25°C, V_{DD}=5V, t_{CLK}=244 ns, t_{CH}=t_{CL}=122 ns and are for design aid only: not guaranteed and not subject to production testing.

††The cycle is initiated by the falling edge of $\overline{CS}$ or $\overline{DS}$, whichever occurs last. Timing is relative to the last falling edge which initiates the cycle.

(1) t_{cwm} is equal to t_{CH} or t_{CL} whichever is smaller (some ST-BUS compatible transceivers may generate C4 clock having t_{CHmin}=70ns or t_{CLmin}=70ns.

(2) Worst case access when memory contention occurs.

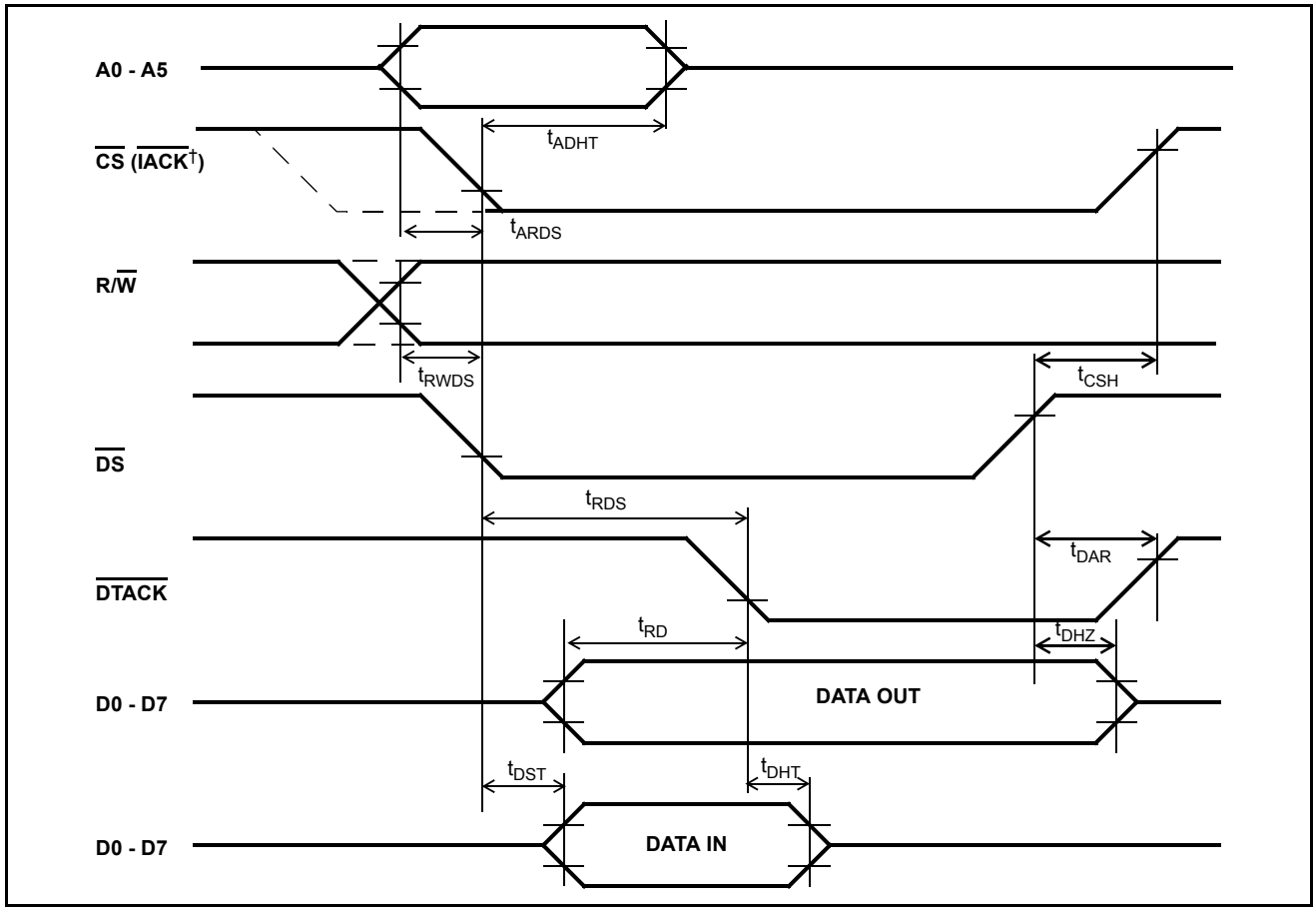


Figure 14 - Mode 1 Parallel Bus Timing

† During Interrupt Acknowledge cycle $\overline{IACK}$ replaces $\overline{CS}$. R/$\overline{W}$ must remain high.

AC Electrical Characteristics† - Mode 2 Parallel Bus Timing - (see Figures 15 and 16)

(V_{CC}=5.0V ±5%,T_A=-40 to 85°C)

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	$\overline{OE}$ Low to Valid Data	t_{EVD}			60	ns	Load A, C_L=130pF, R_L=740Ω
2	Address Access Time	t_{AA}			120	ns	Load A, C_L=130pF, R_L= 740Ω
3	$\overline{CS}$ Low to Valid Data	t_{CSD}			60	ns	Load A, C_L=130pF, R_L=740Ω
4	Output Disable	t_{OHZ}			50	ns	Load A, C_L=130pF, R_L=740Ω
5	Address Setup Time	t_{ASF}	20			ns	
6	Data Setup Time	t_{DST}	30			ns	
7	Data Hold Time	t_{DHT}	5			ns	
8	Address Hold Time	t_{AH}	50			ns	
9	Write Pulse Width	t_{WP}	50			ns	
10	$\overline{OE}$, R/$\overline{W}$ High to $\overline{C4i}$ High	t_{EC4H}		-10		ns	
11	$\overline{OE}$, R/$\overline{W}$ Low to $\overline{C4i}$ Low	t_{EC4L}		10		ns	
12	$\overline{C4i}$ High to $\overline{Busy}$ Low	t_{C4BL}		50		ns	Load C
13	$\overline{C4i}$ Low to $\overline{Busy}$ High	t_{C4BH}		50		ns	Load C
14	$\overline{OE}$, R/$\overline{W}$ High to $\overline{Busy}$ Low	t_{EBL}		40		ns	Load C

† Timing is over recommended temperature & power supply voltages.

‡ Typical figures are at 25°C, V_{DD}=5V, t_{CLK}=244 ns, t_{CH}=t_{CL}=122 ns and are for design aid only: not guaranteed and not subject to production testing.

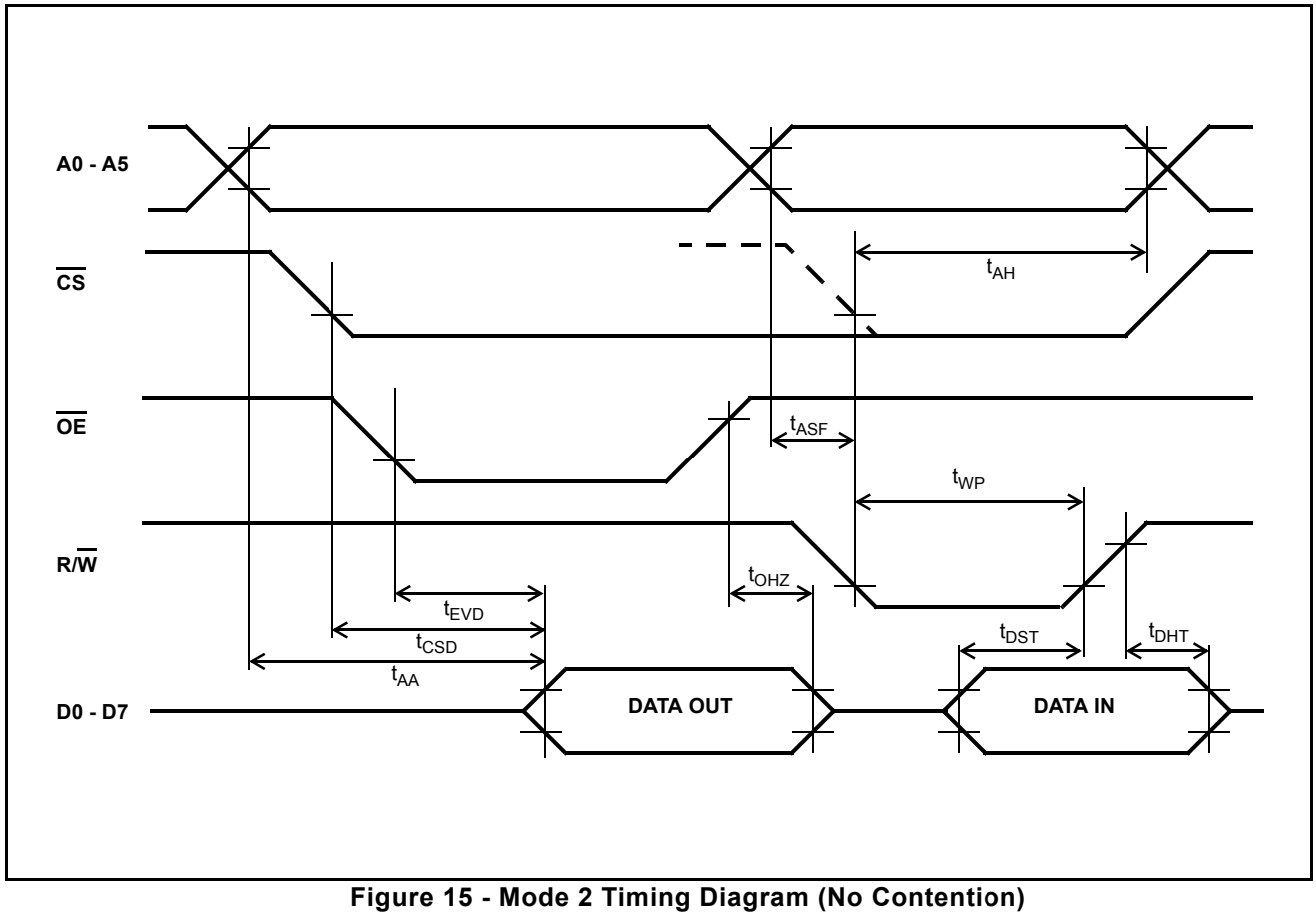


Figure 15 - Mode 2 Timing Diagram (No Contention)

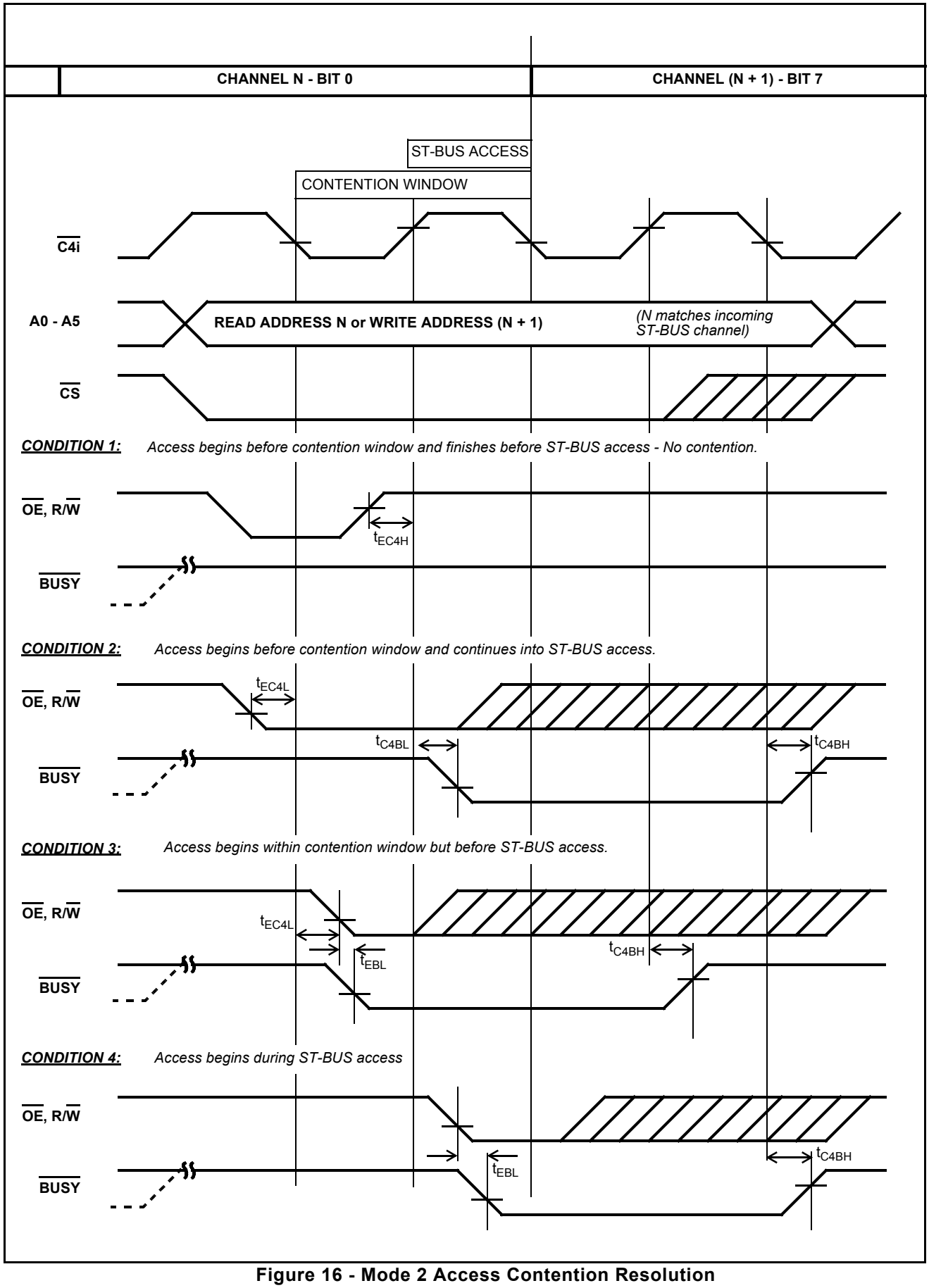


Figure 16 - Mode 2 Access Contention Resolution

AC Electrical Characteristics† - Mode 3 Timing (see Fig.17, 18 and 19)

($(V_{CC}$=5.0V ±5%,TA=-40 to 85°C)

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	$\overline{CS}$ to $\overline{OE}$, $\overline{WE}$, Address Enabled	t_{ZR}			50	ns	Load A, C_L = 130pF, R_L = 740Ω
2	$\overline{C4i}$ Low to Address Change	t_{ACS}			110	ns	Load A, C_L = 130pF, R_L = 740Ω
3	$\overline{CS}$ to $\overline{OE}$, $\overline{WE}$, Address Disabled	t_{RZ}		50		ns	Load A, C_L = 130pF, R_L = 740Ω
4	$\overline{C4i}$ Low to Output Enable Low	t_{OED}			75	ns	Load A, C_L = 130pF, R_L = 740Ω
5	$\overline{C4i}$ Low to Output Enable High	t_{OEH}			75	ns	Load A, C_L = 130pF, R_L = 740Ω
6	$\overline{OE}$, $\overline{WE}$, Pulse Width	t_{ENPW}		$2*t_{CLK}$		ns	Load A, C_L = 130pF, R_L = 740Ω
7	$\overline{C4i}$ Low to Write Enable Low	t_{WED}			75	ns	Load A, C_L = 130pF, R_L = 740Ω
8	$\overline{C4i}$ Low to Write Enable High	t_{WEH}			75	ns	Load A, C_L = 130pF, R_L = 740Ω
9	Read Data Valid from $\overline{OE}$	t_{RST}			$(2*t_{CLK})$ -60	ns	
10	Read Data Hold Time	t_{RHT}	0			ns	
11	Write Data Setup Time	t_{WST}	70	100		ns	Load A, C_L = 130pF, R_L = 740Ω
12	Write Data Hold Time	t_{WHT}	70	100		ns	Load A, C_L = 130pF, R_L = 740Ω
13	$\overline{C4i}$ Transition to $\overline{STCH}$, $\overline{DCS}$ Trans.	t_{STC}			120	ns	Load A, C_L = 70pF, R_L = 1.22KΩ
14	$\overline{STCH}$ Pulse Width	t_{SCPW}		1830		ns	Load A, C_L = 70pF, R_L = 1.22KΩ
15	$\overline{DCS}$ Pulse Width	t_{CSPW}		1830		ns	Load A, C_L = 70pF, R_L = 1.22KΩ

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C, V_{DD}=5V,t_{CLK}=244ns, t_{CH}=t_{CL}=122ns and are for design aid only: not guaranteed and not subject to production testing.

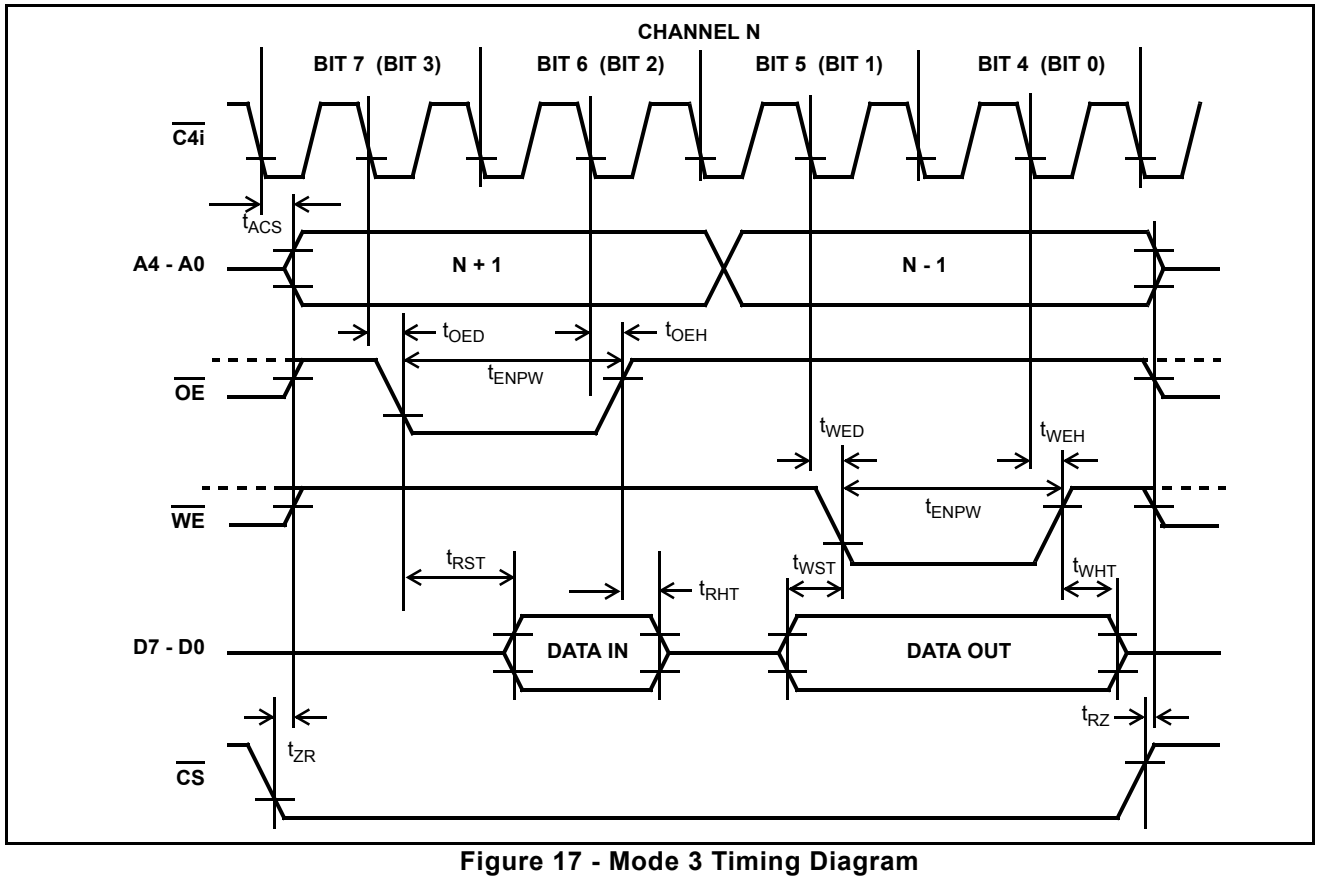


Figure 17 - Mode 3 Timing Diagram

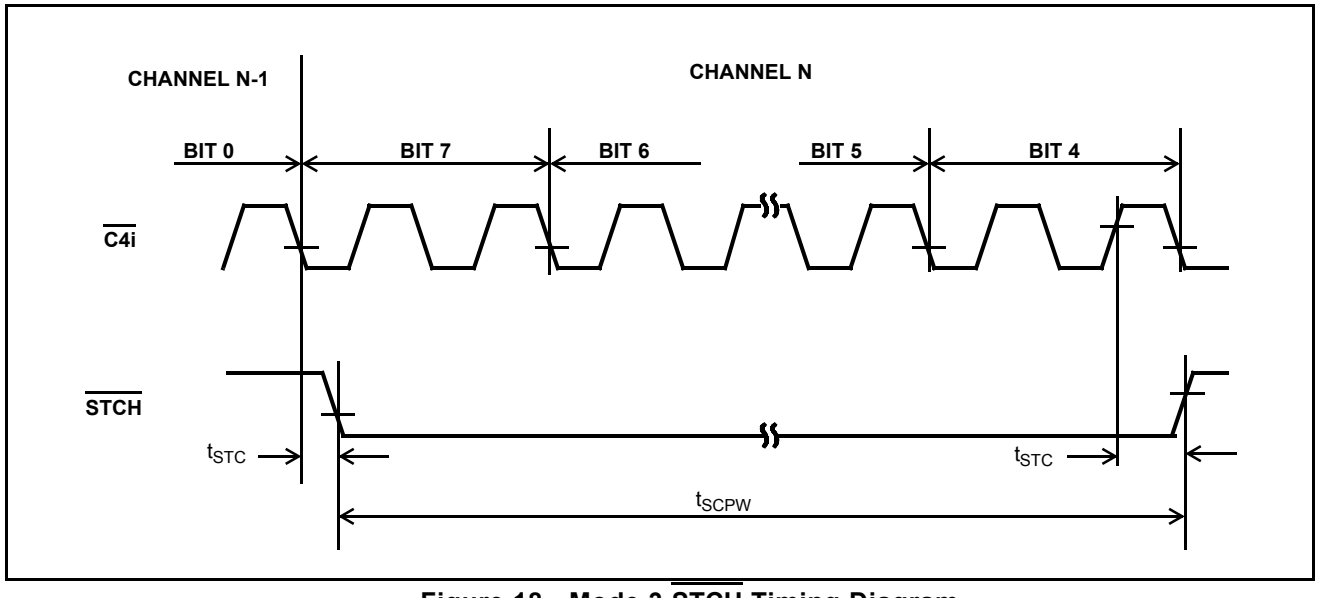


Figure 18 - Mode 3 $\overline{\text{STCH}}$ Timing Diagram

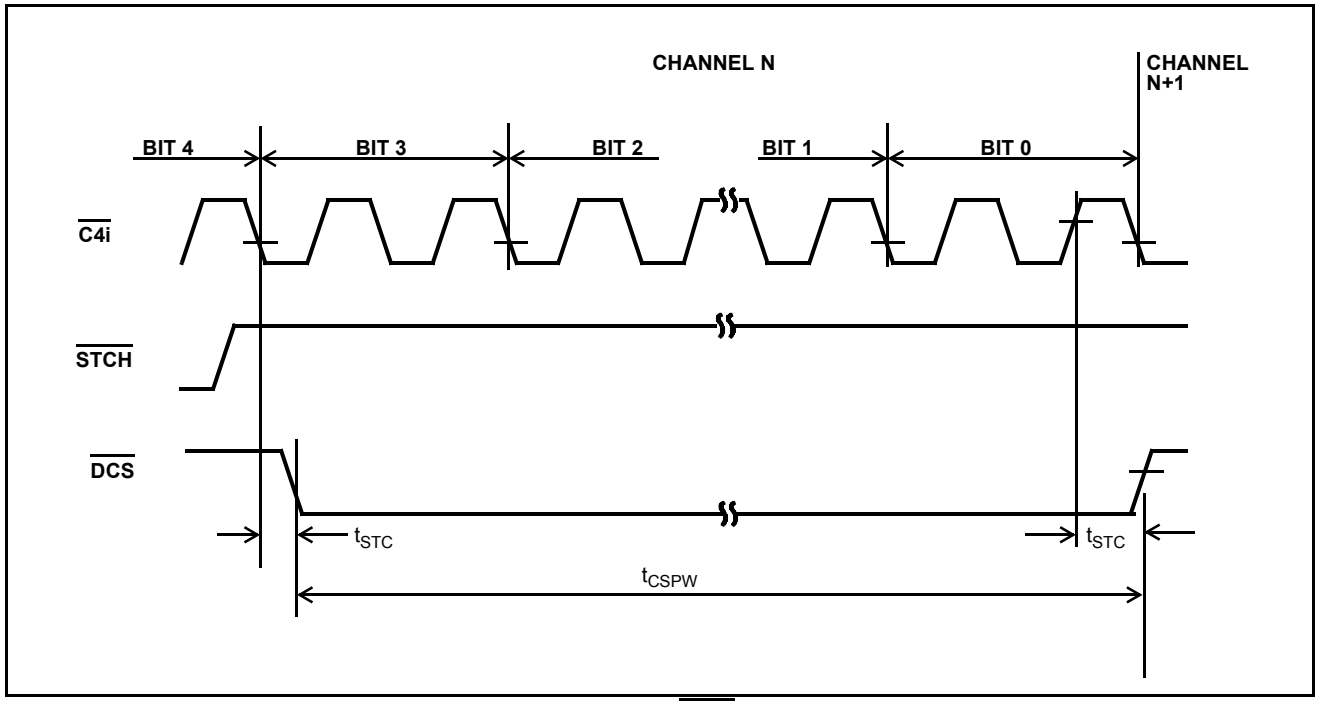


Figure 19 - Mode 3 $\overline{\text{DCS}}$ Timing Diagram

AC Electrical Characteristics† - ST-BUS Timing (see Figure 20)

(V_{CC} = 5.0V ± 5%, T_A = -40 to 85°C)

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Clock $\overline{C4i}$ Period	t_{CLK}		244		ns	
2	Clock $\overline{C4i}$ Period High	t_{CH}	70	122		ns	
3	Clock $\overline{C4i}$ Period Low	t_{CL}	70	122		ns	
4	$\overline{C4i}$ Rise Time	t_R			20	ns	
5	$\overline{C4i}$ Fall Time	t_F			12	ns	
6	Frame Pulse Setup Time	t_{FPS}	20			ns	
7	Frame Pulse Hold Time	t_{FPH}	20			ns	
8	STo0/1 Delay from $\overline{C4i}$	t_{SOD}			100	ns	Load B
9	STi0 Setup Time	t_{STS}	20			ns	
10	STi0 Hold Time	t_{STH}	35			ns	

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C, V_{DD}=5V and are for design aid only: not guaranteed and not subject to production testing.

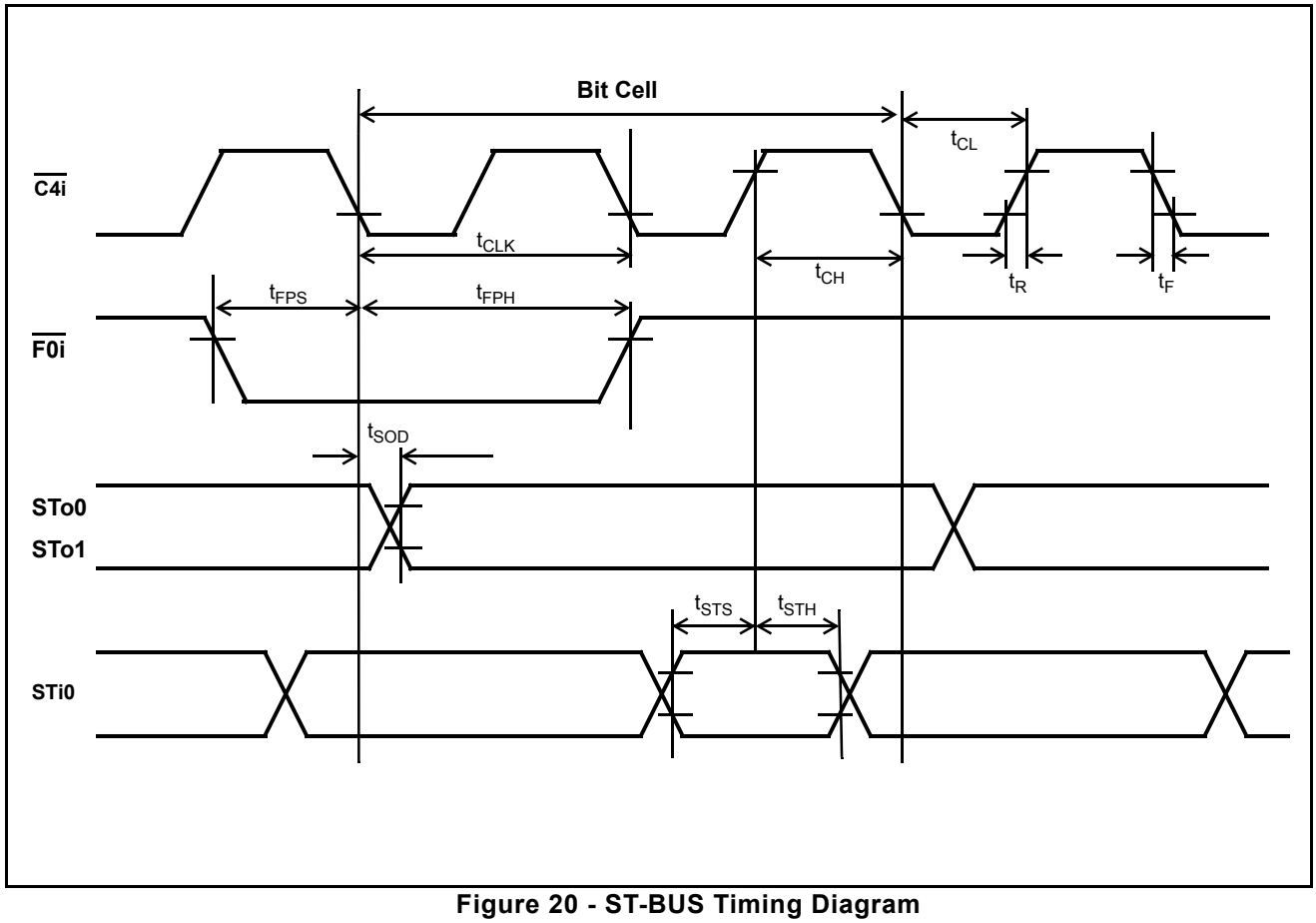


Figure 20 - ST-BUS Timing Diagram

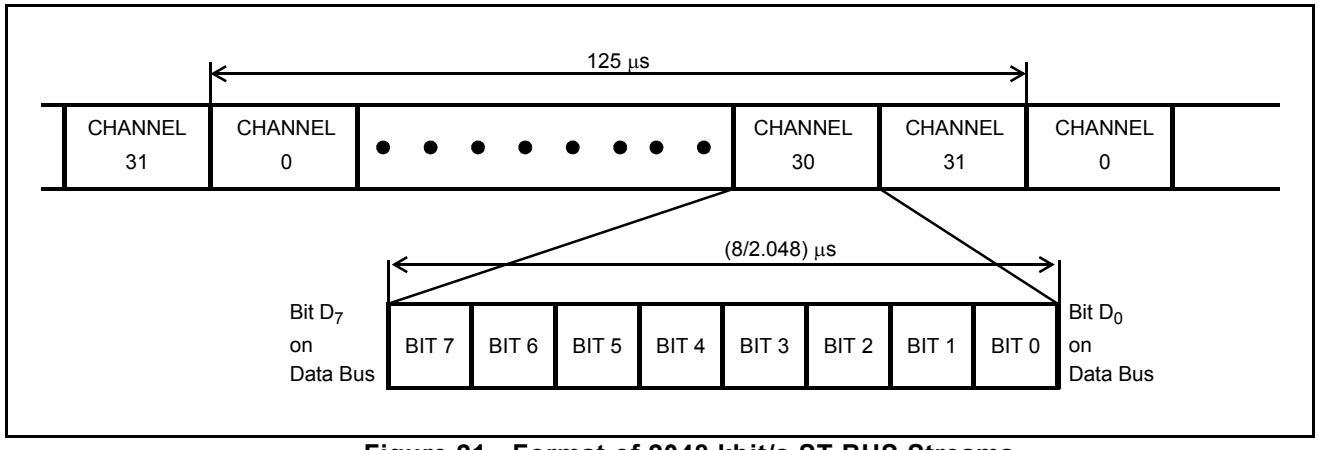


Figure 21 - Format of 2048 kbit/s ST-BUS Streams

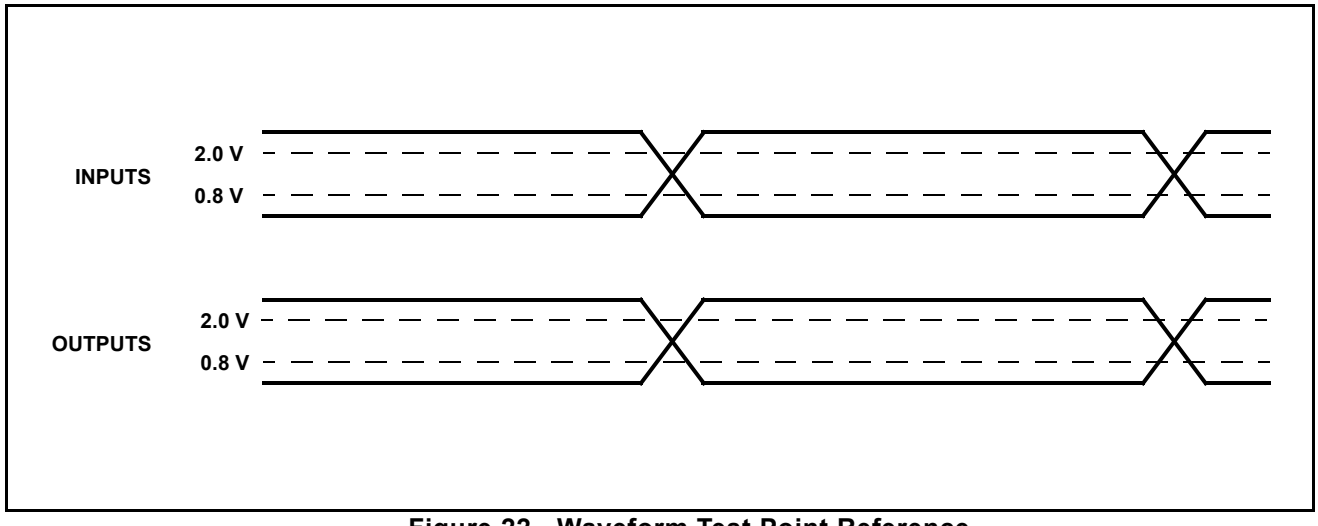


Figure 22 - Waveform Test Point Reference

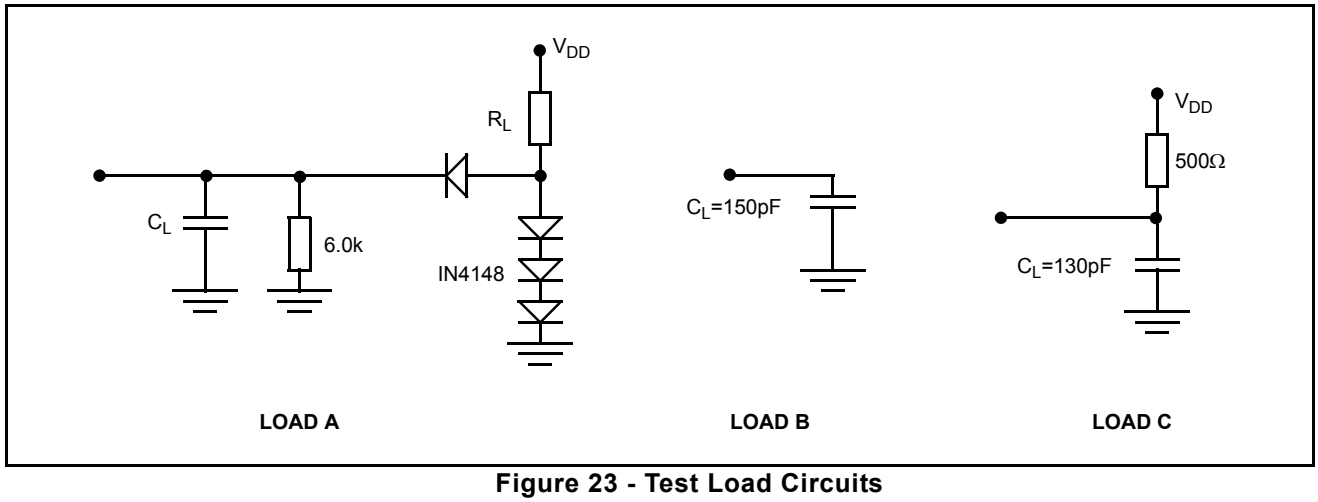
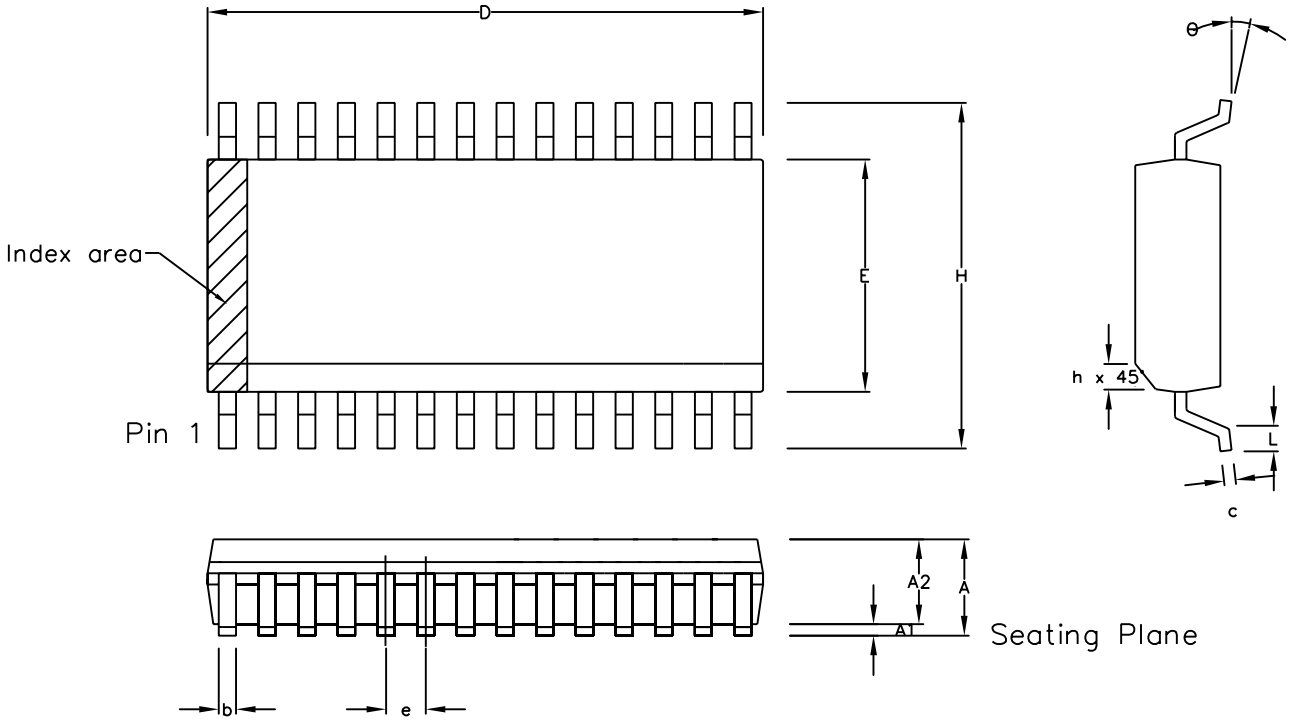


Figure 23 - Test Load Circuits



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	2.35		2.65		0.093		0.104
A1	0.10		0.30		0.004		0.012
A2	2.25		2.35		0.089		0.092
D	17.70		18.10		0.697		0.713
H	10.00		10.65		0.394		0.419
E	7.40		7.60		0.291		0.299
L	0.40		1.27		0.016		0.050
e	1.27 BSC.				0.050 BSC.		
b	0.33		0.51		0.013		0.020
c	0.23		0.32		0.009		0.013
θ	0°		8°		0°		8°
h	0.25		0.75		0.010		0.029
	Pin features						
N	28						
Conforms to JEDEC MS-013AE Iss. C							

Notes:
1. The chamfer on the body is optional. If it not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimension D do not include mould flash, protrusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protrusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.004" total in excess of b dimension.

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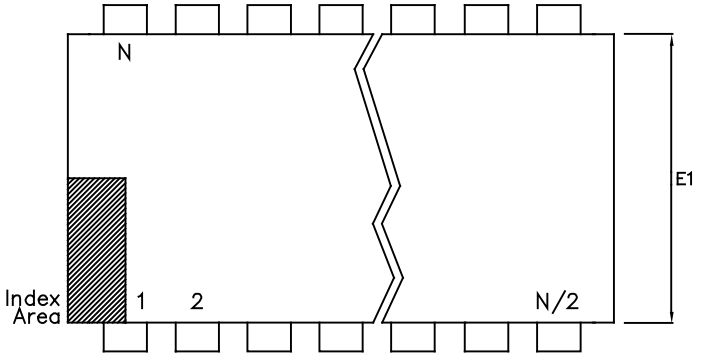
Previous package codes

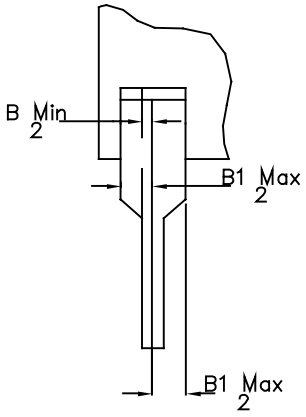
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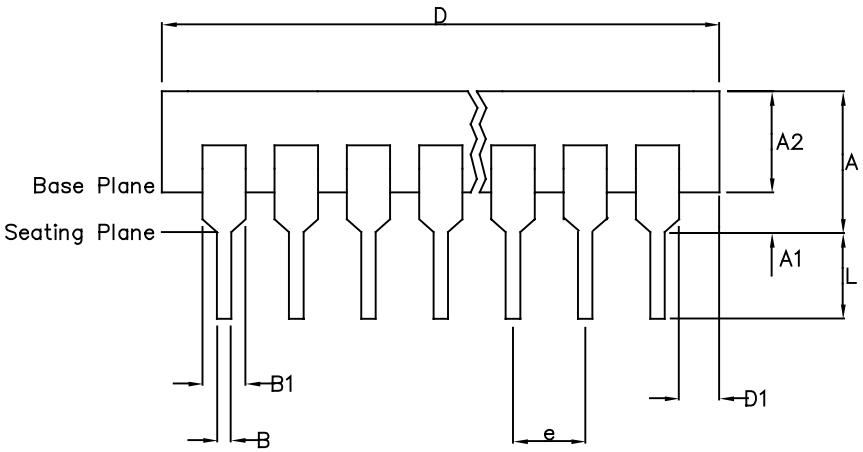
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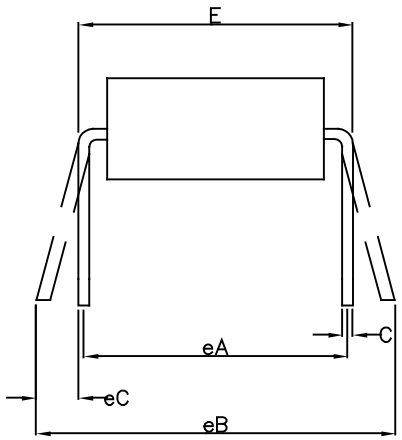
Package Outline for
28 lead SOIC
(0.300" Body Width)

GPD00017









	Min mm	Max mm	Min Inches	Max Inches
A		6.35		0.250
A1	0.38		0.015	
A2	3.18	4.95	0.125	0.195
B	0.36	0.56	0.014	0.022
B1	0.76	1.78	0.030	0.070
C	0.20	0.38	0.008	0.015
D	35.05	39.75	1.380	1.565
D1	0.13		0.005	
E	15.24	15.88	0.600	0.625
E1	12.32	14.73	0.485	0.580
e	2.54 BSC		0.100 BSC	
eA	15.24 BSC		0.600 BSC	
eB		17.78		0.700
L	2.92	5.08	0.115	0.200
N	28		28	
Conforms to Jedec MS-011AB ISS.B				

Notes:
1. Controlling Dimensions are in inches
2. Dimension A, A1 and L are measured with the package seated in the Seating Plane
3. Dimensions D & E1 do not include mould flash or protrusions. Mould flash or protrusion shall not exceed 0.010 inch.
4. Dimensions E & eA are measured with leads constrained to be perpendicular to plane T.
5. Dimensions eB & eC are measured at the lead tips with the leads unconstrained; eC must be zero or greater.

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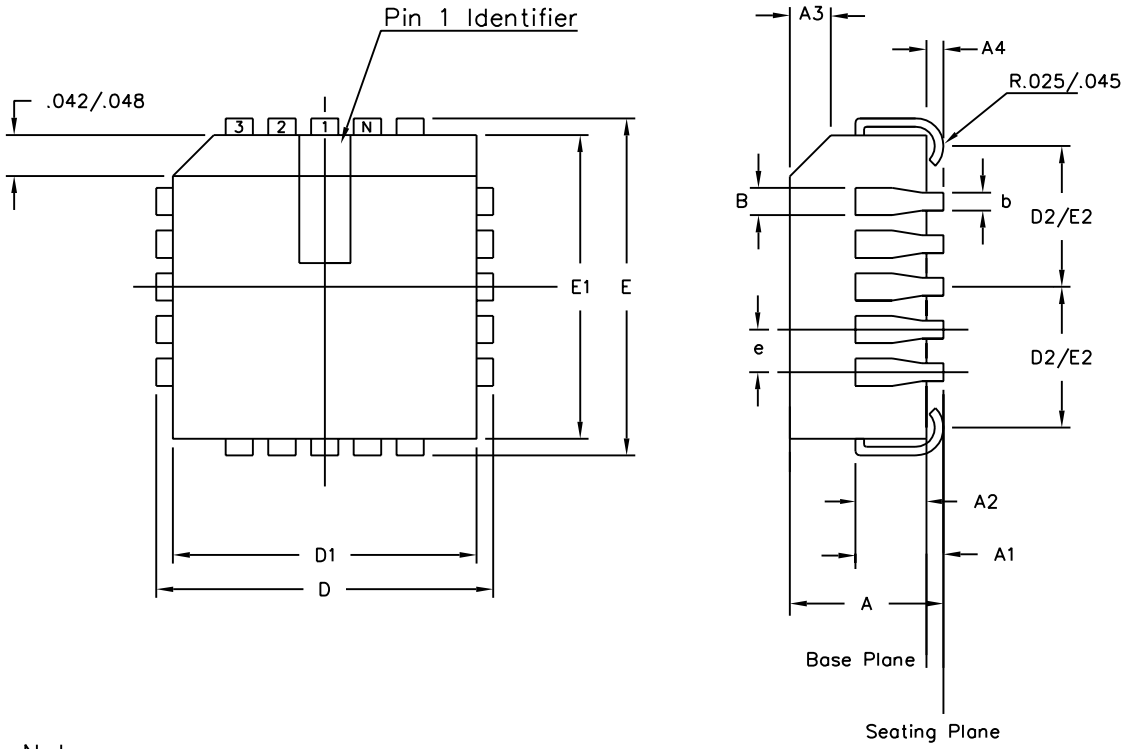
Previous package codes

DP / E

Package Code DA

Package Outline for
28 lead 600mils PDIP

GPD00072



Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.062	0.083	1.57	2.11
A3	0.042	0.056	1.07	1.42
A4	0.020	–	0.51	–
D	0.485	0.495	12.32	12.57
D1	0.450	0.456	11.43	11.58
D2	0.191	0.219	4.85	5.56
E	0.485	0.495	12.32	12.57
E1	0.450	0.456	11.43	11.58
E2	0.191	0.219	4.85	5.56
B	0.026	0.032	0.66	0.81
b	0.013	0.021	0.33	0.53
e	0.050 BSC		1.27 BSC	
	Pin features			
ND	7			
NE	7			
N	28			
Note	Square			
Conforms to JEDEC MS-018AB Iss. A				

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M–1982
2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.

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ZARLINK SEMICONDUCTOR

Previous package codes

HP / P

Package Code QA

Package Outline for 28 lead PLCC

GPD00002



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