THE DATASHEET OF

AFD4400NXN763VB

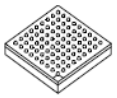
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Freescale Semiconductor
Data Sheet: Technical Data

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AFD4400

AFD4400 Digital Front End Processor Data Sheet



FC PBGA 1152
35 mm x 35 mm

The following list provides an overview of the feature set:

- Flexible radio configurations
  - Up to eight carriers in single or multi-mode combinations
  - LTE(FDD and TDD), WCDMA, N-CDMA, and GSM supported
  - Supported at least 80 MHz total carrier bandwidth
  - Supported at least 100 MHz of instantaneous bandwidth with non-contiguous carriers.
  - Up to eight transmitters, eight receivers, and four observability/sampling receivers
  - Ability to cascade to support multi-sector or distributed antenna systems

- Fully programmable signal processing paths
  - Transmit path: eight vector signal processors
  - Receive path: two vector signal processors
  - Observability Path: one vector signal processor
  - Processor elements sized to support common RF subsystem processing requirements—crest factor reduction, digital pre-distortion (DPD), channel filters, up and down conversion, carrier combining and separation, IQ compensation equalization, interpolation and decimation, and beam forming
  - Transmit/receive processing, busing, and memory system sized for—closed-loop DPD operation up to 491.52 Msps, maximum transmit sample rate of 491.52 Msps, maximum receive sample rate of 245.76 Msps, and maximum observability/sampling rate of 491.52 Msps

- Industry standard interfaces to external components
  - CPRI v4.2 modem interface
  - JESD204B transceiver interface
  - Ethernet OA&M interface
  - AISG antenna accessory interface

- ARM® Cortex®-A9 processor
  - 32 KB L1 instruction cache
  - 32 KB L1 data cache
  - 256 KB L2 cache
  - Neon extension for SIMD and floating point instructions

- Hierarchical memory architecture
  - Local memories within each vector signal processor domain
  - System level shared memory
  - 32-bit DDR3 interface with 500 MHz memory bus speed.
  - External NOR and SPI flash

- Debug – Built around ARM® CoreSight™ architecture
  - JTAG run control interface
  - 32-bit instruction trace port
  - Dedicated JESD204B interface for debug IQ streaming

- Low-power design techniques
  - Clock gating and isolation of clocks
  - Power gating (PG)
  - Power islands

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This figure shows the major functional units.

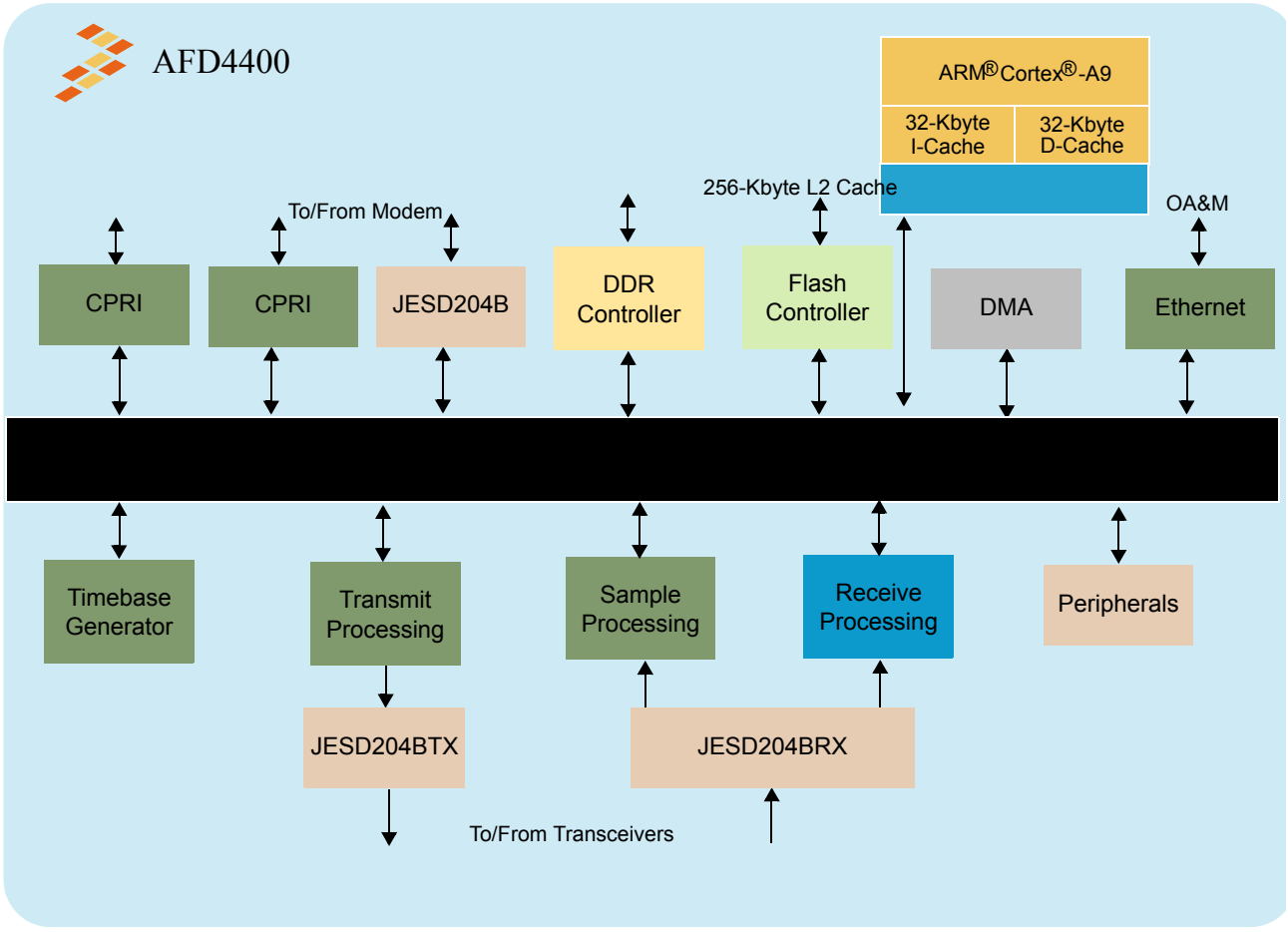


Figure 1. Block diagram

1 Pinout list

This table shows the AFD4400 pin multiplexing.

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
DDR Memory interface				
DDR_DQ0	DDR3 Data	AP29	I/O	MVDD
DDR_DQ1	DDR3 Data	AN29	I/O	MVDD
DDR_DQ2	DDR3 Data	AM26	I/O	MVDD
DDR_DQ3	DDR3 Data	AP30	I/O	MVDD
DDR_DQ4	DDR3 Data	AN28	I/O	MVDD
DDR_DQ5	DDR3 Data	AN26	I/O	MVDD
DDR_DQ6	DDR3 Data	AP25	I/O	MVDD
DDR_DQ7	DDR3 Data	AP26	I/O	MVDD
DDR_DQ8	DDR3 Data	AJ26	I/O	MVDD
DDR_DQ9	DDR3 Data	AG25	I/O	MVDD
DDR_DQ10	DDR3 Data	AH26	I/O	MVDD
DDR_DQ11	DDR3 Data	AG24	I/O	MVDD
DDR_DQ12	DDR3 Data	AK26	I/O	MVDD
DDR_DQ13	DDR3 Data	AF24	I/O	MVDD
DDR_DQ14	DDR3 Data	AL25	I/O	MVDD
DDR_DQ15	DDR3 Data	AH24	I/O	MVDD
DDR_DQ16	DDR3 Data	AP17	I/O	MVDD
DDR_DQ17	DDR3 Data	AP16	I/O	MVDD
DDR_DQ18	DDR3 Data	AN15	I/O	MVDD
DDR_DQ19	DDR3 Data	AM17	I/O	MVDD
DDR_DQ20	DDR3 Data	AL16	I/O	MVDD
DDR_DQ21	DDR3 Data	AM15	I/O	MVDD
DDR_DQ22	DDR3 Data	AK15	I/O	MVDD
DDR_DQ23	DDR3 Data	AL15	I/O	MVDD
DDR_DQ24	DDR3 Data	AK17	I/O	MVDD
DDR_DQ25	DDR3 Data	AH17	I/O	MVDD
DDR_DQ26	DDR3 Data	AF18	I/O	MVDD
DDR_DQ27	DDR3 Data	AJ17	I/O	MVDD
DDR_DQ28	DDR3 Data	AF17	I/O	MVDD
DDR_DQ29	DDR3 Data	AG15	I/O	MVDD
DDR_DQ30	DDR3 Data	AH15	I/O	MVDD
DDR_DQ31	DDR3 Data	AG16	I/O	MVDD
DDR_DM0	DDR3 Data Mask Strobe 0	AM27	Out	MVDD
DDR_DM1	DDR3 Data Mask Strobe 1	AH25	Out	MVDD
DDR_DM2	DDR3 Data Mask Strobe 2	AP15	Out	MVDD
DDR_DM3	DDR3 Data Mask Strobe 3	AG17	Out	MVDD
DDR_DQS0	DDR3 Data Sample Strobe 0	AP27	I/O	MVDD

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
DDR_DQS0_B	DDR3 Data Sample Strobe Complement 0	AP28	I/O	MVDD
DDR_DQS1	DDR3 Data Sample Strobe 1	AJ25	I/O	MVDD
DDR_DQS1_B	DDR3 Data Sample Strobe Complement 1	AK25	I/O	MVDD
DDR_DQS2	DDR3 Data Sample Strobe 2	AM16	I/O	MVDD
DDR_DQS2_B	DDR3 Data Sample Strobe Complement 2	AN16	I/O	MVDD
DDR_DQS3	DDR3 Data Sample Strobe 3	AH16	I/O	MVDD
DDR_DQS3_B	DDR3 Data Sample Strobe Complement 3	AJ16	I/O	MVDD
DDR_BA0	DDR3 Bank Select 0	AN18	Out	MVDD
DDR_BA1	DDR3 Bank Select 1	AM19	Out	MVDD
DDR_BA2	DDR3 Bank Select 2	AP19	Out	MVDD
DDR_A0	DDR3 Address	AJ23	Out	MVDD
DDR_A1	DDR3 Address	AN24	Out	MVDD
DDR_A2	DDR3 Address	AH22	Out	MVDD
DDR_A3	DDR3 Address	AJ22	Out	MVDD
DDR_A4	DDR3 Address	AK23	Out	MVDD
DDR_A5	DDR3 Address	AL23	Out	MVDD
DDR_A6	DDR3 Address	AM24	Out	MVDD
DDR_A7	DDR3 Address	AL22	Out	MVDD
DDR_A8	DDR3 Address	AN23	Out	MVDD
DDR_A9	DDR3 Address	AP23	Out	MVDD
DDR_A10	DDR3 Address	AM23	Out	MVDD
DDR_A11	DDR3 Address	AH21	Out	MVDD
DDR_A12	DDR3 Address	AL21	Out	MVDD
DDR_A13	DDR3 Address	AP22	Out	MVDD
DDR_A14	DDR3 Address	AK21	Out	MVDD
DDR_A15	DDR3 Address	AL20	Out	MVDD
DDR_WE_B	DDR3 Write Enable	AH20	Out	MVDD
DDR_RAS_B	DDR3 Row Address Strobe	AJ20	Out	MVDD
DDR_CAS_B	DDR3 Column Address Strobe	AJ21	Out	MVDD
DDR_CS0_B	DDR3 Chip Select 0	AM20	Out	MVDD
DDR_CS1_B	DDR3 Chip Select 1	AL19	Out	MVDD
DDR_CKE0	DDR3 Clock Enable 0	AK19	Out	MVDD
DDR_CKE1	DDR3 Clock Enable 1	AJ19	Out	MVDD
DDR_CK0	DDR3 Clock 0	AN21	Out	MVDD
DDR_CK0_B	DDR3 Clock 0 Complement	AP21	Out	MVDD
DDR_CK1	DDR3 Clock 1	AN20	Out	MVDD
DDR_CK1_B	DDR3 Clock 1 Complement	AP20	Out	MVDD
DDR_ODT0	DDR3 On Die Termination	AJ18	Out	MVDD
DDR_ODT1	DDR3 On Die Termination	AL18	Out	MVDD

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
DDR_RESET	DDR3 Reset	AH19	Out	MVDD
DDR_ZQ	DDR3 Driver Impedance Calibration	AG19	Out	MVDD
DDR_VREF	DDR3 Reference Voltage	AD24	In	MVDD
FLASH interface				
FLASH_DAT0 GPIOE0	Flash Data	AD29	I/O	FVDD
FLASH_DAT1 GPIOE1	Flash Data	AD34	I/O	FVDD
FLASH_DAT2 GPIOE2	Flash Data	AC33	I/O	FVDD
FLASH_DAT3 GPIOE3	Flash Data	AE29	I/O	FVDD
FLASH_DAT4 GPIOE4	Flash Data	AB27	I/O	FVDD
FLASH_DAT5 GPIOE5	Flash Data	AD31	I/O	FVDD
FLASH_DAT6 GPIOE6	Flash Data	AE30	I/O	FVDD
FLASH_DAT7 GPIOE7	Flash Data	AD32	I/O	FVDD
FLASH_DAT8 GPIOE8	Flash Data	AE31	I/O	FVDD
FLASH_DAT9 GPIOE9	Flash Data	AG32	I/O	FVDD
FLASH_DAT10 GPIOE10	Flash Data	AE34	I/O	FVDD
FLASH_DAT11 GPIOE11	Flash Data	AF33	I/O	FVDD
FLASH_DAT12 GPIOE12	Flash Data	AF30	I/O	FVDD
FLASH_DAT13 GPIOE13	Flash Data	AE33	I/O	FVDD
FLASH_DAT14 GPIOE14	Flash Data	AF32	I/O	FVDD
FLASH_DAT15 GPIOE15	Flash Data	AF29	I/O	FVDD
FLASH_A0 GPIOE16	Flash Address	V32	I/O	FVDD
FLASH_A1 GPIOE17	Flash Address	V25	I/O	FVDD
FLASH_A2 GPIOE18	Flash Address	V29	I/O	FVDD
FLASH_A3 GPIOE19	Flash Address	W26	I/O	FVDD

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
FLASH_A4 GPIOE20	Flash Address	V28	I/O	FVDD
FLASH_A5 GPIOE21	Flash Address	W27	I/O	FVDD
FLASH_A6 GPIOE22	Flash Address	W31	I/O	FVDD
FLASH_A7 GPIOE23	Flash Address	W32	I/O	FVDD
FLASH_A8 GPIOE24	Flash Address	W30	I/O	FVDD
FLASH_A9 GPIOE25	Flash Address	W33	I/O	FVDD
FLASH_A10 GPIOE26	Flash Address	W34	I/O	FVDD
FLASH_A11 GPIOE27	Flash Address	Y34	I/O	FVDD
FLASH_A12 GPIOE28	Flash Address	Y33	I/O	FVDD
FLASH_A13 GPIOE29	Flash Address	Y32	I/O	FVDD
FLASH_A14 GPIOE30	Flash Address	Y30	I/O	FVDD
FLASH_A15 GPIOE31	Flash Address	Y29	I/O	FVDD
FLASH_A16 GPIOD9	Flash Address	AA34	I/O	FVDD
FLASH_A17 GPIOD10	Flash Address	AA29	I/O	FVDD
FLASH_A18 GPIOD11	Flash Address	AA28	I/O	FVDD
FLASH_A19 GPIOD12	Flash Address	AA32	I/O	FVDD
FLASH_A20 GPIOD13	Flash Address	AA30	I/O	FVDD
FLASH_A21 QSPI_CK	Flash Address	AB33	I/O	FVDD
FLASH_A22 QSPI_IO0	Flash Address	AA31	I/O	FVDD
FLASH_A23 QSPI_IO1	Flash Address	AB31	I/O	FVDD
FLASH_A24 QSPI_IO2	Flash Address	AC30	I/O	FVDD
FLASH_A25 QSPI_IO3	Flash Address	AB34	I/O	FVDD
FLASH_CS0_B GPIOD14	Flash Chip Select 0	AC28	I/O	FVDD

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
FLASH_CS1_B GPIOD15	Flash Chip Select 1	AB26	I/O	FVDD
FLASH_CS2_B QSPI_CS_B	Flash Chip Select 2	AB30	Out	FVDD
FLASH_BE0_B GPIOD16	Flash Byte Enable	AA27	I/O	FVDD
FLASH_BE1_B GPIOD17	Flash Byte Enable	AC26	I/O	FVDD
FLASH_OE_B GPIOD18	Flash Output Enable	AC29	I/O	FVDD
FLASH_WE_B GPIOD19	Flash Write Enable	AD28	I/O	FVDD
FLASH_WAIT_B GPIOD20	Flash Busy/Ready/Wait	AC32	I/O	FVDD
FLASH_BCLK GPIOD21	Flash Burst Clock	AC34	I/O	FVDD
FLASH_ADV_B GPIOD22	Flash Address Valid	AB28	I/O	FVDD
SPI-1 interface				
SPI1_MOSI GPIOE0 SPI1_MISO	SPI1 Master Out Slave In	G16	I/O	GVDD3
SPI1_MISO GPIOE1	SPI1 Master In Slave Out	B16	I/O	GVDD3
SPI1_CLK GPIOD22	SPI1 Serial Clock	A15	I/O	GVDD3
SPI1_SS0 GPIOD23	SPI1 Slave Select 0	E16	I/O	GVDD3
SPI1_SS1 GPIOE23	SPI1 Slave Select 1	D16	I/O	GVDD3
SPI-2 interface				
SPI2_MOSI GPIOE2 SPI2_MISO	SPI2 Master Out Slave In Data	A16	I/O	GVDD3
SPI2_MISO GPIOE3	SPI2 Master In Slave Out Data	D17	I/O	GVDD3
SPI2_CLK GPIOD24	SPI2 Serial Clock	H17	I/O	GVDD3
SPI2_SS0 GPIOD25	SPI2 Slave Select 0	G17	I/O	GVDD3
SPI2_SS1 GPIOE24	SPI2 Slave Select 1	F17	I/O	GVDD3
SPI-3 interface				
SPI3_MOSI GPIOE4 SPI3_MISO	SPI3 Master Out Slave In Data	C17	I/O	GVDD3

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
SPI3_MISO GPIOE5	SPI3 Master In Slave Out Data	A17	I/O	GVDD3
SPI3_CLK GPIOD26	SPI3 Serial Clock	E18	I/O	GVDD3
SPI3_SS0 GPIOD27	SPI3 Slave Select 0	G18	I/O	GVDD3
SPI3_SS1 GPIOE25	SPI3 Slave Select 1	F18	I/O	GVDD3
SPI-4 interface				
SPI4_MOSI GPIOE6 SPI4_MISO	SPI4 Master Out Slave In Data	C18	I/O	GVDD3
SPI4_MISO GPIOE7	SPI4 Master In Slave Out Data	B18	I/O	GVDD3
SPI4_CLK GPIOD28	SPI4 Serial Clock	D18	I/O	GVDD3
SPI4_SS0 GPIOD29	SPI4 Slave Select 0	A19	I/O	GVDD3
SPI4_SS1 GPIOE26	SPI4 Slave Select 1	A18	I/O	GVDD3
SPI-5 interface				
SPI5_MOSI GPIOE8 SPI5_MISO	SPI5 Master Out Slave In Data	D20	I/O	GVDD4
SPI5_MISO GPIOE9	SPI5 Master In Slave Out Data	F19	I/O	GVDD4
SPI5_CLK GPIOD29	SPI5 Serial Clock	F20	I/O	GVDD4
SPI5_SS0 GPIOD30	SPI5 Slave Select 0	C21	I/O	GVDD4
SPI5_SS1 GPIOD31	SPI5 Slave Select 1	G20	I/O	GVDD4
SPI-6 interface				
SPI6_MOSI GPIOE10 SPI6_MISO TBGEN_AGC_EN0	SPI6 Master Out Slave In Data	D21	I/O	GVDD4
SPI6_MISO GPIOE11 TBGEN_AGC_EN1	SPI6 Master In Slave Out Data	A21	I/O	GVDD4
SPI6_CLK GPIOE12 TBGEN_AGC_EN2	SPI6 Serial Clock	B21	I/O	GVDD4
SPI6_SS0 GPIOE13 TBGEN_AGC_EN3	SPI6 Slave Select 0	G21	I/O	GVDD4

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
SPI6_SS1 GPIOE27	SPI6 Slave Select 1	E21	I/O	GVDD4
SPI-7 interface				
SPI7_MOSI GPIOE14 SPI7_MISO TBGEN_AGC_EN4	SPI7 Master Out Slave In Data	H21	I/O	GVDD4
SPI7_MISO GPIOE15 TBGEN_AGC_EN5	SPI7 Master In Slave Out Data	A22	I/O	GVDD4
SPI7_CLK GPIOE16 TBGEN_AGC_EN6	SPI7 Serial Clock	F21	I/O	GVDD4
SPI7_SS0 GPIOE17 TBGEN_AGC_EN7	SPI7 Slave Select 0	G22	I/O	GVDD4
SPI7_SS1 GPIOE28	SPI7 Slave Select 1	D22	I/O	GVDD4
SPI-8 interface				
SPI8_MOSI GPIOE18 SPI8_MISO	SPI8 Master Out Slave In Data	D23	I/O	GVDD4
SPI8_MISO GPIOE19	SPI8 Master In Slave Out Data	B22	I/O	GVDD4
SPI8_CLK GPIOE20	SPI8 Serial Clock	E22	I/O	GVDD4
SPI8_SS0 GPIOE21	SPI8 Slave Select 0	C23	I/O	GVDD4
SPI8_SS1 GPIOE22	SPI8 Slave Select 1	A23	I/O	GVDD4
UART1 interface				
UART1_TXD GPIOE23	UART1 Receive Data	C8	I/O	GVDD7
UART1_RXD GPIOE24	UART1 Transmit Data	F11	I/O	GVDD7
UART2 interface				
UART2_TXD GPIOE25	UART2 Receive Data	E10	I/O	GVDD7
UART2_RXD GPIOE26	UART2 Transmit Data	B9	I/O	GVDD7
UART3 interface				
UART3_TXD GPIOE27	UART3 Receive Data	A10	I/O	GVDD7
UART3_RXD GPIOE28	UART3 Transmit Data	G12	I/O	GVDD7
UART4 interface				

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
UART4_TXD GPIOE29 I2C4_SDA	UART4 Receive Data	C10	I/O	GVDD7
UART4_RXD GPIOE30 I2C4_SCL	UART4 Transmit Data	D11	I/O	GVDD7
I2C1 interface				
I2C1_SDA GPIOE0	I2C1 Serial Clock	B3	I/O	GVDD7
I2C1_SCL GPIOE1	I2C1 Serial Data	A6	I/O	GVDD7
I2C2 interface				
I2C2_SDA GPIOE2	I2C2 Serial Clock	C4	I/O	GVDD7
I2C2_SCL GPIOE3	I2C2 Serial Data	H11	I/O	GVDD7
I2C3 interface				
I2C3_SDA GPIOE4	I2C3 Serial Clock	G10	I/O	GVDD7
I2C3_SCL GPIOE5	I2C3 Serial Data	D6	I/O	GVDD7
I2C5 interface				
I2C5_SDA GPIOE31	I2C5 Serial Clock	A7	I/O	GVDD7
I2C5_SCL GPIOD9	I2C5 Serial Data	F9	I/O	GVDD7
I2C6 interface				
I2C6_SDA GPIOD10	I2C6 Serial Clock	G11	I/O	GVDD7
I2C6_SCL GPIOD11	I2C6 Serial Data	C5	I/O	GVDD7
I2C7 interface				
I2C7_SDA GPIOD12	I2C7 Serial Clock	B4	I/O	GVDD7
I2C7_SCL GPIOD13	I2C7 Serial Data	A8	I/O	GVDD7
I2C8 interface				
I2C8_SDA GPIOD14 TBGEN_GP_EVENT0 UART1_RTS_B SPI1_SS3	I2C8 Serial Clock	E8	I/O	GVDD7
I2C8_SCL GPIOD15 TBGEN_GP_EVENT1 UART1_CTS_B SPI2_SS3	I2C8 Serial Data	A3	I/O	GVDD7

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
I2C9 interface				
I2C9_SDA GPIOD16 TBGEN_GP_EVENT2 UART2_RTS_B SPI3_SS3	I2C9 Serial Clock	A4	I/O	GVDD7
I2C9_SCL GPIOD17 TBGEN_GP_EVENT3 UART2_CTS_B SPI4_SS3	I2C9 Serial Data	E9	I/O	GVDD7
I2C10 interface				
I2C10_SDA GPIOD18 TBGEN_GP_EVENT4 UART3_RTS_B SPI5_SS3	I2C10 Serial Clock	C9	I/O	GVDD7
I2C10_SCL GPIOD19 TBGEN_GP_EVENT5 UART3_CTS_B SPI6_SS3	I2C10 Serial Data	F10	I/O	GVDD7
I2C11 interface				
I2C11_SDA GPIOD20 TBGEN_GP_EVENT6 UART4_RTS_B SPI7_SS3	I2C11 Serial Clock	D8	I/O	GVDD7
I2C11_SCL GPIOD21 TBGEN_GP_EVENT7 UART4_CTS_B SPI8_SS3	I2C11 Serial Data	C7	I/O	GVDD7
General purpose IO module A (GPIOA) interface				
GPIOA0 UART4_RTS_B SOC_OBS0	General Purpose IO GPIOA pin 0	H13	I/O	GVDD7
GPIOA1 UART4_CTS_B SOC_OBS1	General Purpose IO GPIOA pin 1	D10	I/O	GVDD7
GPIOA2 SPI8_SS2 EIM_CS4_B SOC_OBS2	General Purpose IO GPIOA pin 2	A20	I/O	GVDD4
GPIOA3 SPI7_SS2 SOC_OBS3	General Purpose IO GPIOA pin 3	B19	I/O	GVDD4

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
GPIOA4 SPI6_RDY TBGEN_GP_TIMESTAMP0 SOC_OBS4	General Purpose IO GPIOA pin 4	C19	I/O	GVDD4
GPIOA5 SPI7_RDY TBGEN_GP_TIMESTAMP1 SOC_OBS5	General Purpose IO GPIOA pin 5	C20	I/O	GVDD4
GPIOA6 SPI8_RDY TBGEN_GP_TIMESTAMP2 SOC_OBS6	General Purpose IO GPIOA pin 6	J9	I/O	GVDD2
GPIOA7 TBGEN_GP_TIMESTAMP3 SOC_OBS7	General Purpose IO GPIOA pin 7	A2	I/O	GVDD2
GPIOA8 SOC_OBS8	General Purpose IO GPIOA pin 8	J10	I/O	GVDD2
GPIOA9 SOC_OBS9	General Purpose IO GPIOA pin 9	J11	I/O	GVDD2
GPIOA10	General Purpose IO GPIOA pin 10	H8	I/O	GVDD2
GPIOA11	General Purpose IO GPIOA pin 11	F4	I/O	GVDD2
GPIOA12 TBGEN_GP_TIMESTAMP0	General Purpose IO GPIOA pin 12	H10	I/O	GVDD2
GPIOA13 TBGEN_GP_TIMESTAMP1	General Purpose IO GPIOA pin 13	E4	I/O	GVDD2
GPIOA14 TBGEN_GP_TIMESTAMP2	General Purpose IO GPIOA pin 14	A5	I/O	GVDD2
GPIOA15 TBGEN_GP_TIMESTAMP3	General Purpose IO GPIOA pin 15	E13	I/O	GVDD3
GPIOA16 TBGEN_GP_TIMESTAMP0 VSP7_GPO0_4	General Purpose IO GPIOA pin 16	A13	I/O	GVDD3
GPIOA17 TBGEN_GP_TIMESTAMP1 VSP7_GPO0_5	General Purpose IO GPIOA pin 17	G14	I/O	GVDD3
GPIOA18 TBGEN_GP_TIMESTAMP2 VSP7_GPO0_6	General Purpose IO GPIOA pin 18	F14	I/O	GVDD3
GPIOA19 SPI5_RDY TBGEN_GP_TIMESTAMP3 VSP7_GPO0_7	General Purpose IO GPIOA pin 19	C13	I/O	GVDD3
GPIOA20 SPI1_RDY TBGEN_GP_EVENT0 VSP7_GPO0_0	General Purpose IO GPIOA pin 20	G15	I/O	GVDD3

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
GPIOA21 SPI2_RDY TBGEN_GP_EVENT1 VSP7_GPO0_1	General Purpose IO GPIOA pin 21	A14	I/O	GVDD3
GPIOA22 SPI3_RDY TBGEN_GP_EVENT2 MC_SYNC_OUT VSP7_GPO0_2	General Purpose IO GPIOA pin 22	B13	I/O	GVDD3
GPIOA23 SPI4_RDY TBGEN_GP_EVENT3 VSP7_GPO0_3	General Purpose IO GPIOA pin 23	F15	I/O	GVDD3
GPIOA24 SPI8_SS3 MC_SYNC_OUT VSP5_GPO0_0	General Purpose IO GPIOA pin 24	F5	I/O	GVDD2
GPIOA25 SPI7_SS3 VSP5_GPO0_1	General Purpose IO GPIOA pin 25	G9	I/O	GVDD2
GPIOA26 SPI6_SS2 VSP5_GPO0_2	General Purpose IO GPIOA pin 26	D3	I/O	GVDD2
GPIOA27 SPI6_SS3 VSP_EXT_GO16 VSP5_GPO0_3	General Purpose IO GPIOA pin 27	F8	I/O	GVDD2
GPIOA28 SPI5_SS2 TBGEN_GP_EVENT4 VSP_EXT_GO17 VSP6_GPO0_0	General Purpose IO GPIOA pin 28	H15	I/O	GVDD2
GPIOA29 SPI5_SS3 TBGEN_GP_EVENT5 VSP_EXT_GO18 VSP6_GPO0_1	General Purpose IO GPIOA pin 29	E6	I/O	GVDD2
GPIOA30 TBGEN_GP_EVENT6 VSP_EXT_GO19 VSP6_GPO0_2	General Purpose IO GPIOA pin 30	D5	I/O	GVDD2
GPIOA31 TBGEN_GP_EVENT7 VSP_EXT_GO20 VSP6_GPO0_3	General Purpose IO GPIOA pin 31	E7	I/O	GVDD2
General purpose IO module B (GPIOB) interface				

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
GPIOB0 TIMED_GPIOB0 VSP_EXT_GO21 VSP1_GPO0_0 VSP2_GPO0_0	General Purpose IO GPIOB pin 0	AP13	I/O	GVDD8
GPIOB1 TIMED_GPIOB1 ARM_EVENTI VSP_EXT_GO22 VSP1_GPO0_1 VSP2_GPO0_1	General Purpose IO GPIOB pin 1	AL13	I/O	GVDD8
GPIOB2 TIMED_GPIOB2 VSP_EXT_GO23 VSP1_GPO0_2 VSP2_GPO0_2	General Purpose IO GPIOB pin 2	AK13	I/O	GVDD8
GPIOB3 TIMED_GPIOB3 VSP1_GPO0_3 VSP2_GPO0_3	General Purpose IO GPIOB pin 3	AJ14	I/O	GVDD8
GPIOB4 TIMED_GPIOB4 VSP3_GPO0_0 VSP4_GPO0_0	General Purpose IO GPIOB pin 4	AP11	I/O	GVDD8
GPIOB5 TIMED_GPIOB5 VSP3_GPO0_1 VSP4_GPO0_1	General Purpose IO GPIOB pin 5	AN10	I/O	GVDD8
GPIOB6 TIMED_GPIOB6 VSP3_GPO0_2 VSP4_GPO0_2	General Purpose IO GPIOB pin 6	AM13	I/O	GVDD8
GPIOB7 TIMED_GPIOB7 VSP3_GPO0_3 VSP4_GPO0_3	General Purpose IO GPIOB pin 7	AM12	I/O	GVDD8
GPIOB8 TIMED_GPIOB8 VSP8_GPO0_0 VSP9_GPO0_0	General Purpose IO GPIOB pin 8	AN11	I/O	GVDD1
GPIOB9 TIMED_GPIOB9 VSP8_GPO0_1 VSP9_GPO0_1	General Purpose IO GPIOB pin 9	AN13	I/O	GVDD1
GPIOB10 TIMED_GPIOB10 VSP8_GPO0_2 VSP9_GPO0_2	General Purpose IO GPIOB pin 10	AL12	I/O	GVDD1

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
GPIOB11 TIMED_GPIOB11 VSP8_GPO0_3 VSP9_GPO0_3	General Purpose IO GPIOB pin 11	AM10	I/O	GVDD1
GPIOB12 TIMED_GPIOB12 VSP10_GPO0_0 VSP11_GPO0_0	General Purpose IO GPIOB pin 12	AM11	I/O	GVDD1
GPIOB13 TIMED_GPIOB13 VSP10_GPO0_1 VSP11_GPO0_1	General Purpose IO GPIOB pin 13	AH13	I/O	GVDD1
GPIOB14 TIMED_GPIOB14 VSP10_GPO0_2 VSP11_GPO0_2	General Purpose IO GPIOB pin 14	AP12	I/O	GVDD1
GPIOB15 TIMED_GPIOB15 VSP10_GPO0_3 VSP11_GPO0_3	General Purpose IO GPIOB pin 15	AL11	I/O	GVDD1
GPIOB16 TIMED_GPIOB16 VSP1_GPO0_4 VSP2_GPO0_4	General Purpose IO GPIOB pin 16	AN9	I/O	GVDD1
GPIOB17 TIMED_GPIOB17 VSP1_GPO0_5 VSP2_GPO0_5	General Purpose IO GPIOB pin 17	AJ12	I/O	GVDD1
GPIOB18 TIMED_GPIOB18 VSP1_GPO0_6 VSP2_GPO0_6	General Purpose IO GPIOB pin 18	AK11	I/O	GVDD1
GPIOB19 TIMED_GPIOB19 VSP1_GPO0_7 VSP2_GPO0_7	General Purpose IO GPIOB pin 19	AN8	I/O	GVDD1
GPIOB20 TIMED_GPIOB20 VSP3_GPO0_4 VSP4_GPO0_4	General Purpose IO GPIOB pin 20	AP10	I/O	GVDD1
GPIOB21 TIMED_GPIOB21 VSP3_GPO0_5 VSP4_GPO0_5	General Purpose IO GPIOB pin 21	AP8	I/O	GVDD1
GPIOB22 TIMED_GPIOB22 VSP_GPI3_15 VSP3_GPO0_6 VSP4_GPO0_6	General Purpose IO GPIOB pin 22	AP7	I/O	GVDD1

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
GPIOB23 TIMED_GPIOB23 VSP_GPI3_16 VSP3_GPO0_7 VSP4_GPO0_7	General Purpose IO GPIOB pin 23	AN7	I/O	GVDD1
GPIOB24 TIMED_GPIOB24 VSP_GPI3_17 VSP8_GPO0_4 VSP9_GPO0_4	General Purpose IO GPIOB pin 24	AM7	I/O	GVDD9
GPIOB25 TIMED_GPIOB25 VSP_GPI3_18 VSP8_GPO0_5 VSP9_GPO0_5	General Purpose IO GPIOB pin 25	AJ11	I/O	GVDD9
GPIOB26 TIMED_GPIOB26 VSP_GPI3_19 VSP8_GPO0_6 VSP9_GPO0_6	General Purpose IO GPIOB pin 26	AH12	I/O	GVDD9
GPIOB27 TIMED_GPIOB27 VSP_GPI3_20 VSP8_GPO0_7 VSP9_GPO0_7	General Purpose IO GPIOB pin 27	AG12	I/O	GVDD9
GPIOB28 TIMED_GPIOB28 VSP_GPI3_21 VSP10_GPO0_4 VSP11_GPO0_4	General Purpose IO GPIOB pin 28	AP9	I/O	GVDD9
GPIOB29 TIMED_GPIOB29 VSP_GPI3_22 VSP10_GPO0_5 VSP11_GPO0_5	General Purpose IO GPIOB pin 29	AG13	I/O	GVDD9
GPIOB30 TIMED_GPIOB30 VSP_GPI3_23 VSP10_GPO0_6 VSP11_GPO0_6	General Purpose IO GPIOB pin 30	AF12	I/O	GVDD9
GPIOB31 TIMED_GPIOB31 VSP_GPI3_24 VSP10_GPO0_7 VSP11_GPO0_7	General Purpose IO GPIOB pin 31	AF13	I/O	GVDD9
General purpose IO module C (GPIOC) interface				

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
GPIOC0 SPI8_SS2 SPI1_SS2 VSP_GPI3_25 TIMED_GPIOC0 TBGEN_T0_CTRL1 VSP2_GPO0_8	General Purpose IO GPIOC pin 0	D26	I/O	GVDD6
GPIOC1 TSEC_1588_CLKIN SPI1_SS3 VSP_GPI3_26 TIMED_GPIOC1 TBGEN_T1_CTRL1 VSP2_GPO0_9	General Purpose IO GPIOC pin 1	A29	I/O	GVDD6
GPIOC2 TSEC_1588_TRIG1 SPI2_SS2 VSP_GPI3_27 TIMED_GPIOC2 TBGEN_T2_CTRL1 VSP4_GPO0_8	General Purpose IO GPIOC pin 2	G25	I/O	GVDD6
GPIOC3 TSEC_1588_TRIG2 SPI2_SS3 TBGEN_GP_TIMESTAMP0 TIMED_GPIOC3 TBGEN_T3_CTRL1 VSP4_GPO0_9	General Purpose IO GPIOC pin 3	A28	I/O	GVDD6
GPIOC4 TSEC_1588_ALARM1 SPI3_SS2 TIMED_GPIOC4 TBGEN_T4_CTRL1 VSP9_GPO0_8	General Purpose IO GPIOC pin 4	E26	I/O	GVDD6
GPIOC5 TSEC_1588_ALARM2 SPI3_SS3 TBGEN_GP_TIMESTAMP1 TIMED_GPIOC5 TBGEN_T5_CTRL1 VSP9_GPO0_9	General Purpose IO GPIOC pin 5	B28	I/O	GVDD6
GPIOC6 TSEC_1588_FIPER1 SPI4_SS2 TBGEN_GP_TIMESTAMP2 TIMED_GPIOC6 TBGEN_T6_CTRL1 VSP11_GPO0_8	General Purpose IO GPIOC pin 6	C29	I/O	GVDD6

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
GPIOC7 TSEC_1588_FIPER2 SPI4_SS3 TBGEN_GP_TIMESTAMP3 TIMED_GPIOC7 TBGEN_T7_CTRL1 VSP11_GPO0_9	General Purpose IO GPIOC pin 7	C28	I/O	GVDD6
GPIOC8 TSEC_1588_FIPER3 SPI5_SS2 TBGEN_AGC_EN0 TIMED_GPIOC8 TBGEN_T0_CTRL2 VSP5_GPO0_8	General Purpose IO GPIOC pin 8	A30	I/O	GVDD6
GPIOC9 TSEC_1588_CLKOUT SPI5_SS3 TBGEN_AGC_EN1 TIMED_GPIOC9 TBGEN_T1_CTRL2 VSP5_GPO0_9	General Purpose IO GPIOC pin 9	B29	I/O	GVDD6
GPIOC10 UART1_RTS_B SPI6_SS2 TBGEN_AGC_EN2 TIMED_GPIOC10 TBGEN_T2_CTRL2 VSP5_GPO0_10	General Purpose IO GPIOC pin 10	D28	I/O	GVDD6
GPIOC11 UART1_CTS_B SPI6_SS3 TBGEN_AGC_EN3 TIMED_GPIOC11 TBGEN_T3_CTRL2 VSP5_GPO0_11	General Purpose IO GPIOC pin 11	A31	I/O	GVDD6
GPIOC12 UART2_RTS_B SPI7_SS3 TBGEN_AGC_EN4 TIMED_GPIOC12 TBGEN_T4_CTRL2 VSP6_GPO0_8	General Purpose IO GPIOC pin 12	A33	I/O	GVDD6
GPIOC13 UART2_CTS_B SPI8_SS3 TBGEN_AGC_EN5 TIMED_GPIOC13 TBGEN_T5_CTRL2 VSP6_GPO0_9	General Purpose IO GPIOC pin 13	C30	I/O	GVDD6

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
GPIOC14 UART3_RTS_B EXT_DMA_REQ1 TBGEN_AGC_EN6 TIMED_GPIOC14 TBGEN_T6_CTRL2 VSP6_GPO0_10	General Purpose IO GPIOC pin 14	D29	I/O	GVDD6
GPIOC15 UART3_CTS_B VSP_GPI3_0 TBGEN_AGC_EN7 TIMED_GPIOC15 TBGEN_T7_CTRL2 VSP6_GPO0_11	General Purpose IO GPIOC pin 15	B32	I/O	GVDD6
GPIOC16 UART4_RTS_B VSP_GPI3_1 TBGEN_T0_CTRL2_B TIMED_GPIOC16 VSP5_GPO0_4 VSP7_GPO0_8	General Purpose IO GPIOC pin 16	B31	I/O	GVDD6
GPIOC17 UART4_CTS_B VSP_GPI3_2 TBGEN_T1_CTRL2_B TIMED_GPIOC17 VSP5_GPO0_5 VSP7_GPO0_9	General Purpose IO GPIOC pin 17	C31	I/O	GVDD6
GPIOC18 VSP_GPI3_3 TBGEN_T2_CTRL2_B TIMED_GPIOC18 VSP6_GPO0_4 VSP7_GPO0_10	General Purpose IO GPIOC pin 18	C32	I/O	GVDD6
GPIOC19 SPI1_RDY VSP_GPI3_4 TBGEN_T3_CTRL2_B TIMED_GPIOC19 VSP6_GPO0_5 VSP7_GPO0_11	General Purpose IO GPIOC pin 19	C33	I/O	GVDD6
GPIOC20 SPI2_RDY VSP_GPI3_5 TBGEN_T4_CTRL2_B TIMED_GPIOC20 VSP5_GPO0_6 VSP7_GPO0_12	General Purpose IO GPIOC pin 20	C34	I/O	GVDD6

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
GPIOC21 SPI3_RDY VSP_GPI3_6 TBGEN_T5_CTRL2_B TIMED_GPIOC21 VSP5_GPO0_7 VSP7_GPO0_13	General Purpose IO GPIOC pin 21	F26	I/O	GVDD6
GPIOC22 SPI4_RDY VSP_GPI3_7 TBGEN_T6_CTRL2_B TIMED_GPIOC22 VSP6_GPO0_6 VSP7_GPO0_14	General Purpose IO GPIOC pin 22	D30	I/O	GVDD6
GPIOC23 SPI5_RDY VSP_GPI3_8 TBGEN_T7_CTRL2_B TIMED_GPIOC23 VSP6_GPO0_7 VSP7_GPO0_15	General Purpose IO GPIOC pin 23	E31	I/O	GVDD6
GPIOC24 TSEC1_RXD1 VSP_GPI3_9 TIMED_GPIOC24 TBGEN_T0_CTRL2_B VSP2_GPO0_10 TBGEN_T0_CTRL1	General Purpose IO GPIOC pin 24	C24	I/O	GVDD5
GPIOC25 TSEC1_RXD2 VSP_GPI3_10 SPI6_RDY TIMED_GPIOC25 TBGEN_T1_CTRL2_B VSP2_GPO0_11 TBGEN_T1_CTRL1	General Purpose IO GPIOC pin 25	H22	I/O	GVDD5
GPIOC26 TSEC1_RXD3 VSP_GPI3_11 SPI7_RDY TIMED_GPIOC26 TBGEN_T2_CTRL2_B VSP4_GPO0_10 TBGEN_T2_CTRL1	General Purpose IO GPIOC pin 26	G23	I/O	GVDD5

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
GPIOC27 TSEC1_RX_ER VSP_GPI3_12 SPI8_RDY TIMED_GPIOC27 TBGEN_T3_CTRL2_B VSP4_GPO0_11 TBGEN_T3_CTRL1	General Purpose IO GPIOC pin 27	D24	I/O	GVDD5
GPIOC28 TSEC1_GTX_CLK VSP_GPI3_13 EIM_CS5_B TIMED_GPIOC28 TBGEN_T4_CTRL2_B VSP9_GPO0_10 TBGEN_T4_CTRL1	General Purpose IO GPIOC pin 28	A25	I/O	GVDD5
GPIOC29 TSEC1_TX_CLK VSP_GPI3_14 EIM_CS3_B TIMED_GPIOC29 TBGEN_T5_CTRL2_B VSP9_GPO0_11 TBGEN_T5_CTRL1	General Purpose IO GPIOC pin 29	E23	I/O	GVDD5
GPIOC30 TSEC1_TXD0 VSP_GPI3_28 EXT_DMA_REQ1 TIMED_GPIOC30 TBGEN_T6_CTRL2_B VSP11_GPO0_10 TBGEN_T6_CTRL1	General Purpose IO GPIOC pin 30	F23	I/O	GVDD5
GPIOC31 TSEC1_TXD1 VSP_GPI3_29 EXT_DMA_REQ2 TIMED_GPIOC31 TBGEN_T7_CTRL2_B VSP11_GPO0_11 TBGEN_T7_CTRL1	General Purpose IO GPIOC pin 31	C25	I/O	GVDD5
General purpose IO module D (GPIOD) interface				
GPIOD0 TSEC1_TXD2 VSP_GPI3_30 SOC_OBS0	General Purpose IO GPIOD pin 0	B25	I/O	GVDD5

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
GPIOD1 TSEC1_TXD3 EXT_DMA_REQ2 VSP_EXT_GO16 SOC_OBS1 TBGEN_T0_CTRL2 TBGEN_GP_EVENT0	General Purpose IO GPIOD pin 1	A26	I/O	GVDD5
GPIOD2 TSEC1_TX_ERVSP_EXT_GO17 SOC_OBS2 TBGEN_T1_CTRL2 TBGEN_GP_EVENT1	General Purpose IO GPIOD pin 2	D25	I/O	GVDD5
GPIOD3 TSEC1_TX_ENVSP_EXT_GO18 SOC_OBS3 TBGEN_T2_CTRL2 TBGEN_GP_EVENT2	General Purpose IO GPIOD pin 3	F24	I/O	GVDD5
GPIOD4 TSEC1_COLVSP_EXT_GO19 SOC_OBS4 TBGEN_T3_CTRL2 TBGEN_GP_EVENT3	General Purpose IO GPIOD pin 4	G24	I/O	GVDD5
GPIOD5 TSEC1_CRS VSP_GPI3_31 VSP_EXT_GO20 SOC_OBS5 TBGEN_T4_CTRL2 TBGEN_GP_EVENT4	General Purpose IO GPIOD pin 5	B26	I/O	GVDD5
GPIOD6 TSEC1_RX_CLK SPI7_SS2 VSP_EXT_GO21 SOC_OBS6 TBGEN_T5_CTRL2 TBGEN_GP_EVENT5	General Purpose IO GPIOD pin 6	C26	I/O	GVDD5
GPIOD7 TSEC1_RX_DV SPI8_SS2 VSP_EXT_GO22 SOC_OBS7 TBGEN_T6_CTRL2 TBGEN_GP_EVENT6	General Purpose IO GPIOD pin 7	F25	I/O	GVDD5

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
GPIOD8 TSEC1_RXD0 MC_SYNC_OUT VSP_EXT_GO23 SOC_OBS8 TBGEN_T7_CTRL2 TBGEN_GP_EVENT7	General Purpose IO GPIOD pin 8	E25	I/O	GVDD5
Ethernet management channel interface				
TSEC_MDC GPIOD9 SOC_OBS9	Ethernet MDC	C27	Out	GVDD5
TSEC_MDIO GPIOD10	Ethernet MDIO	A27	I/O	GVDD5
Reset, Clocks and misc. signals				
RSTIN_B	Hard Reset In	E12	In	JVDD
URST_B	User Reset In (Warm Reset)	D12	In	JVDD
RSTOUT_B	Hard Reset Out	B6	Out	GVDD7
RSTOUT1_B GPIOD22	Hard & Soft Reset Out 1	H19	Out	GVDD4
RSTOUT2_B GPIOD23	Hard & Soft Reset Out 2	G19	Out	GVDD4
RSTOUT3_B GPIOD24	Hard & Soft Reset Out 3	D14	Out	GVDD3
RSTOUT4_B GPIOD25	Hard & Soft Reset Out 4	E15	Out	GVDD3
RSTOUT5_B GPIOD26	Hard & Soft Reset Out 5	B15	Out	GVDD3
RSTOUT6_B GPIOD27	Hard & Soft Reset Out 6	C14	Out	GVDD3
RSTOUT7_B GPIOD28	Hard & Soft Reset Out 7	D15	Out	GVDD3
WDOG_B	WDOG out	B7	Out	GVDD7
DEVCLK1_P	Device Clock used as the main reference to the IC	R25	In	SD3_XCOREVDD
DEVCLK1_N	Device Clock used as the main reference to the IC	R24	In	SD3_XCOREVDD
DEVCLK2_P	Device Clock used as the reference to JESDTX1-8 and JESDRX1-12 SerDes	Y11	In	SD1_XCOREVDD
DEVCLK2_N	Device Clock used as the reference to JESDTX1-8 and JESDRX1-12 SerDes	Y12	In	SD1_XCOREVDD
SYSREF_OUT_N	Sys reference out	N34	Out	LVDD3
SYSREF_OUT_P	Sys reference out	N33	Out	LVDD3
SYSREF_IN_N	Sys reference in	T28	In	LVDD3
SYSREF_IN_P	Sys reference in	T29	In	LVDD3

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
FRMCLK_N	Frame Clock (JESD204A only)	R31	Out	LVDD3
FRMCLK_P	Frame Clock (JESD204A only)	R30	Out	LVDD3
CPRI_REVCLK_P	Differential CPRI Recovered Clock	P33	Out	LVDD3
CPRI_REVCLK_N	Differential CPRI Recovered Clock, LVDS signaling	P34	Out	LVDD3
CPRI_REVCLK	Single ended CPRI Recovered Clock	A32	Out	GVDD6
RGMII_REFCLK_P	Ethernet Reference Clock	U27	In	LVDD3
RGMII_REFCLK_N	Ethernet Reference Clock	U26	In	LVDD3
SGMII_PHY_REFCLK	25 MHz Reference Clock to Ethernet PHYs	A24	Out	GVDD5
MC_SYNC_IN	System Synchronization	C15	In	GVDD3
TG_RF_SYNC_P	10ms Tone Generator Synchronization	T33	Out	LVDD3
TG_RF_SYNC_N	10ms Tone Generator Synchronization	T34	Out	LVDD3
TG_RF_SYNC	10ms Tone Generator Synchronization	B34	Out	GVDD6
BMOD0	Boot Mode 0	F13	In	JVDD
BMOD1	Boot Mode 1	A12	In	JVDD
CKO	Clock Out	E19	Out	GVDD4
TEST	Factory test mode enable	C12	In	JVDD
ANL_TEST	Analog Test	Y27	Out	FVDD
ANL_REFCLK_P_TEST	Analog Test for DEVCLK1 pads	W29	Out	FVDD
ANL_REFCLK_N_TEST	Analog Test for DEVCLK1 pads	W28	Out	FVDD
JTAG interface				
JTAG_TRST_B	JTAG Test Reset	A9	In	JVDD
JTAG_TDO	JTAG Test Data Out	C11	Out	JVDD
JTAG_TDI	JTAG Test Data In	B10	In	JVDD
JTAG_TCK	JTAG Test Clock	B12	In	JVDD
JTAG_TMS	JTAG Test Mode Select	A11	I/O	JVDD
JTAG_VSP_SEL	Select the secondary JTAG multiplexed on HW MUX1 of GPIOD4-8	G13	In	JVDD
SJC_MOD_B	JTAG controller mode	AG30	In	FVDD
TRACE interface				
TRACE_CLK	Trace Clock	AK32	Out	TVDD
TRACE_IN_CLK	Trace Input Clock	AF34	In	FVDD
TRACE_CTL	Trace Control	AL32	Out	TVDD
TRACE_DATA0	Trace Data	AH34	Out	TVDD
TRACE_DATA1	Trace Data	AG34	Out	TVDD
TRACE_DATA2	Trace Data	AH33	Out	TVDD
TRACE_DATA3	Trace Data	AJ34	Out	TVDD

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
TRACE_DATA4	Trace Data	AJ33	Out	TVDD
TRACE_DATA5	Trace Data	AH30	Out	TVDD
TRACE_DATA6	Trace Data	AK34	Out	TVDD
TRACE_DATA7	Trace Data	AJ32	Out	TVDD
TRACE_DATA8	Trace Data	AH29	Out	TVDD
TRACE_DATA9	Trace Data	AL34	Out	TVDD
TRACE_DATA10	Trace Data	AM34	Out	TVDD
TRACE_DATA11	Trace Data	AH31	Out	TVDD
TRACE_DATA12	Trace Data	AG28	Out	TVDD
TRACE_DATA13	Trace Data	AJ30	Out	TVDD
TRACE_DATA14	Trace Data	AL33	Out	TVDD
TRACE_DATA15	Trace Data	AK30	Out	TVDD
TRACE_DATA16	Trace Data	AM30	Out	TVDD
TRACE_DATA17	Trace Data	AN34	Out	TVDD
TRACE_DATA18	Trace Data	AN32	Out	TVDD
TRACE_DATA19	Trace Data	AK31	Out	TVDD
TRACE_DATA20	Trace Data	AJ28	Out	TVDD
TRACE_DATA21	Trace Data	AN31	Out	TVDD
TRACE_DATA22	Trace Data	AM31	Out	TVDD
TRACE_DATA23	Trace Data	AL29	Out	TVDD
TRACE_DATA24	Trace Data	AL30	Out	TVDD
TRACE_DATA25	Trace Data	AK28	Out	TVDD
TRACE_DATA26	Trace Data	AP33	Out	TVDD
TRACE_DATA27	Trace Data	AK29	Out	TVDD
TRACE_DATA28	Trace Data	AH28	Out	TVDD
TRACE_DATA29	Trace Data	AP32	Out	TVDD
TRACE_DATA30	Trace Data	AL28	Out	TVDD
TRACE_DATA31	Trace Data	AG27	Out	TVDD
JESD interface data signals				
TX1_DAT_P	TX Data Out 1	AA4	Out	SD1_XPADVDD
TX1_DAT_N	TX Data Out 1	AA5	Out	SD1_XPADVDD
RX1_DAT_P	Rx/SRX Data In 1	W1	In	SD1_XCOREVDD
RX1_DAT_N	Rx/SRX Data In 1	W2	In	SD1_XCOREVDD
TX2_DAT_P	TX Data Out 2	AB6	Out	SD1_XPADVDD
TX2_DAT_N	TX Data Out 2	AB7	Out	SD1_XPADVDD
RX2_DAT_P	Rx/SRX Data In 2	AA1	In	SD1_XCOREVDD
RX2_DAT_N	Rx/SRX Data In 2	AA2	In	SD1_XCOREVDD
TX3_DAT_P	TX Data Out 3	AC4	Out	SD1_XPADVDD
TX3_DAT_N	TX Data Out 3	AC5	Out	SD1_XPADVDD
RX3_DAT_P	Rx/SRX Data In 3	AC1	In	SD1_XCOREVDD
RX3_DAT_N	Rx/SRX Data In 3	AC2	In	SD1_XCOREVDD
TX4_DAT_P	TX Data Out 4	AD6	Out	SD1_XPADVDD

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
TX4_DAT_N	TX Data Out 4	AD7	Out	SD1_XPADVDD
RX4_DAT_P	Rx/SRX Data In 4	AE1	In	SD1_XCOREVDD
RX4_DAT_N	Rx/SRX Data In 4	AE2	In	SD1_XCOREVDD
TX5_DAT_P	TX Data Out 5	AE4	Out	SD1_XPADVDD
TX5_DAT_N	TX Data Out 5	AE5	Out	SD1_XPADVDD
RX5_DAT_P	Rx/SRX Data In 5	AG1	In	SD1_XCOREVDD
RX5_DAT_N	Rx/SRX Data In 5	AG2	In	SD1_XCOREVDD
TX6_DAT_P	TX Data Out 6	AF6	Out	SD1_XPADVDD
TX6_DAT_N	TX Data Out 6	AF7	Out	SD1_XPADVDD
RX6_DAT_P	Rx/SRX Data In 6	AJ1	In	SD1_XCOREVDD
RX6_DAT_N	Rx/SRX Data In 6	AJ2	In	SD1_XCOREVDD
TX7_DAT_P	TX Data Out 7	AG4	Out	SD1_XPADVDD
TX7_DAT_N	TX Data Out 7	AG5	Out	SD1_XPADVDD
RX7_DAT_P	Rx/SRX Data In 7	AL1	In	SD1_XCOREVDD
RX7_DAT_N	Rx/SRX Data In 7	AL2	In	SD1_XCOREVDD
TX8_DAT_P	TX Data Out 8	AH6	Out	SD1_XPADVDD
TX8_DAT_N	TX Data Out 8	AH7	Out	SD1_XPADVDD
RX8_DAT_P	Rx/SRX Data In 8	AN1	In	SD1_XCOREVDD
RX8_DAT_N	Rx/SRX Data In 8	AN2	In	SD1_XCOREVDD
RX9_DAT_P	SRx. Data In 9	V3	In	SD2_XCOREVDD
RX9_DAT_N	SRx. Data In 9	V4	In	SD2_XCOREVDD
RX10_DAT_P	SRx. Data In 10	U1	In	SD2_XCOREVDD
RX10_DAT_N	SRx. Data In 10	U2	In	SD2_XCOREVDD
RX11_DAT_P	SRx. Data In 11	R1	In	SD2_XCOREVDD
RX11_DAT_N	SRx. Data In 11	R2	In	SD2_XCOREVDD
RX12_DAT_P	SRx. Data In 12	N1	In	SD2_XCOREVDD
RX12_DAT_N	SRx. Data In 12	N2	In	SD2_XCOREVDD
SerDes1 misc ports				
SD1_IC_TX	TX Impedance Calibration	AE11	In	SD1_XPADVDD
SD1_IC_RX	RX Impedance Calibration	W6	In	SD1_XPADVDD
SD1_PLL1_TPA	PLL1 Analog Test Point	Y7	Out	SD1_XPADVDD
SD1_PLL1_TPD	PLL1 Digital Test Point	Y9	Out	SD1_XPADVDD
SD1_PLL2_TPA	PLL2 Analog Test Point	AE9	Out	SD1_XPADVDD
SD1_PLL2_TPD	PLL2 Digital Test Point	AD10	Out	SD1_XPADVDD
JESD204B interface SYNC~ signals				
TX1_SYNC_N	Synchronization for TX1	AK9	In	LVDD1
TX1_SYNC_P	Synchronization for TX1	AL9	In	LVDD1
TX2_SYNC_N	Synchronization for TX2	AL8	In	LVDD1
TX2_SYNC_P	Synchronization for TX2	AK8	In	LVDD1
TX3_SYNC_N	Synchronization for TX3	AP4	In	LVDD1
TX3_SYNC_P	Synchronization for TX3	AN4	In	LVDD1
TX4_SYNC_N	Synchronization for TX4	AN5	In	LVDD1

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
TX4_SYNC_P	Synchronization for TX4	AP5	In	LVDD1
TX5_SYNC_N	Synchronization for TX5	AK6	In	LVDD1
TX5_SYNC_P	Synchronization for TX5	AL6	In	LVDD1
TX6_SYNC_N	Synchronization for TX6	AL5	In	LVDD1
TX6_SYNC_P	Synchronization for TX6	AK5	In	LVDD1
TX7_SYNC_N	Synchronization for TX7	AH9	In	LVDD1
TX7_SYNC_P	Synchronization for TX7	AG9	In	LVDD1
TX8_SYNC_N	Synchronization for TX8	AG10	In	LVDD1
TX8_SYNC_P	Synchronization for TX8	AH10	In	LVDD1
RX1_SYNC_N	Synchronization for RX1	P10	Out	LVDD2
RX1_SYNC_P	Synchronization for RX1	P9	Out	LVDD2
RX2_SYNC_N	Synchronization for RX2	M7	Out	LVDD2
RX2_SYNC_P	Synchronization for RX2	M6	Out	LVDD2
RX3_SYNC_N	Synchronization for RX3	N9	Out	LVDD2
RX3_SYNC_P	Synchronization for RX3	N10	Out	LVDD2
RX4_SYNC_N	Synchronization for RX4	L7	Out	LVDD2
RX4_SYNC_P	Synchronization for RX4	L6	Out	LVDD2
RX5_SYNC_N	Synchronization for RX5	H5	Out	LVDD2
RX5_SYNC_P	Synchronization for RX5	H4	Out	LVDD2
RX6_SYNC_N	Synchronization for RX6	K5	Out	LVDD2
RX6_SYNC_P	Synchronization for RX6	K4	Out	LVDD2
RX7_SYNC_N	Synchronization for RX7	G3	Out	LVDD2
RX7_SYNC_P	Synchronization for RX7	G2	Out	LVDD2
RX8_SYNC_N	Synchronization for RX8	L10	Out	LVDD2
RX8_SYNC_P	Synchronization for RX8	L9	Out	LVDD2
RX9_SYNC_N	Synchronization for RX9	C2	Out	LVDD2
RX9_SYNC_P	Synchronization for RX9	C1	Out	LVDD2
RX10_SYNC_N	Synchronization for RX10	J7	Out	LVDD2
RX10_SYNC_P	Synchronization for RX10	J6	Out	LVDD2
RX11_SYNC_N	Synchronization for RX11	E2	Out	LVDD2
RX11_SYNC_P	Synchronization for RX11	E1	Out	LVDD2
RX12_SYNC_N	Synchronization for RX12	G7	Out	LVDD2
RX12_SYNC_P	Synchronization for RX12	G6	Out	LVDD2
Ethernet interface				
SGMII1_TXDAT_P	Ethernet Data Out	U6	Out	SD2_XPADVDD
SGMII1_TXDAT_N	Ethernet Data Out	U7	Out	SD2_XPADVDD
SGMII1_RXDAT_P	Ethernet Data In	L1	In	SD2_XCOREVDD
SGMII1_RXDAT_N	Ethernet Data In	L2	In	SD2_XCOREVDD
SGMII2_TXDAT_P	Ethernet Data Out	T4	Out	SD2_XPADVDD
SGMII2_TXDAT_N	Ethernet Data Out	T5	Out	SD2_XPADVDD
SGMII2_RXDAT_P	Ethernet Data In	J1	In	SD2_XCOREVDD
SGMII2_RXDAT_N	Ethernet Data In	J2	In	SD2_XCOREVDD

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
SGMII_REFCLK_P	SerDes Reference Clock for SGMII	V11	In	SD2_XCOREVDD
SGMII_REFCLK_N	SerDes Reference Clock for SGMII	V12	In	SD2_XCOREVDD
SerDes2 misc signals				
SD2_IC_TX	TX Impedance Calibration	M4	In	SD2_XPADVDD
SD2_IC_RX	RX Impedance Calibration	W10	In	SD2_XPADVDD
SD2_PLL1_TPA	PLL1 Analog Test Point	U10	Out	SD2_XPADVDD
SD2_PLL1_TPD	PLL1 Digital Test Point	W8	Out	SD2_XPADVDD
SD2_PLL2_TPA	PLL2 Analog Test Point	P7	Out	SD2_XPADVDD
SD2_PLL2_TPD	PLL2 Digital Test Point	P5	Out	SD2_XPADVDD
CPRI interface				
CPRI1_TXDAT1_P	CPRI Data Out	L31	Out	SD3_XPADVDD
CPRI1_TXDAT1_N	CPRI Data Out	L30	Out	SD3_XPADVDD
CPRI1_RXDAT1_P	CPRI Data In	L34	In	SD3_XCOREVDD
CPRI1_RXDAT1_N	CPRI Data In	L33	In	SD3_XCOREVDD
CPRI1_TXDAT2_P	CPRI Data Out	K29	Out	SD3_XPADVDD
CPRI1_TXDAT2_N	CPRI Data Out	K28	Out	SD3_XPADVDD
CPRI1_RXDAT2_P	CPRI Data In	J34	In	SD3_XCOREVDD
CPRI1_RXDAT2_N	CPRI Data In	J33	In	SD3_XCOREVDD
CPRI2_TXDAT1_P BBI_JESD_TXDAT1_P	CPRI or Modem Interface JESD Data Out	J31	Out	SD3_XPADVDD
CPRI2_TXDAT1_N BBI_JESD_TXDAT1_N	CPRI or Modem Interface JESD Data Out	J30	Out	SD3_XPADVDD
CPRI2_RXDAT1_P BBI_JESD_RXDAT1_P	CPRI or Modem Interface JESD Data In	G34	In	SD3_XCOREVDD
CPRI2_RXDAT1_N BBI_JESD_RXDAT1_N	CPRI or Modem Interface JESD Data In	G33	In	SD3_XCOREVDD
CPRI2_TXDAT2_P BBI_JESD_TXDAT2_P	CPRI or Modem Interface JESD Data Out	H29	Out	SD3_XPADVDD
CPRI2_TXDAT2_N BBI_JESD_TXDAT2_N	CPRI or Modem Interface JESD Data Out	H28	Out	SD3_XPADVDD
CPRI2_RXDAT2_P BBI_JESD_RXDAT2_P	CPRI or Modem Interface JESD Data In	E34	In	SD3_XCOREVDD
CPRI2_RXDAT2_N BBI_JESD_RXDAT2_N	CPRI or Modem Interface JESD Data In	E33	In	SD3_XCOREVDD
SerDes3 misc signals				
SD3_IC_TX	TX Impedance Calibration	J24	In	SD3_XPADVDD
SD3_IC_RX	RX Impedance Calibration	N31	In	SD3_XPADVDD
SD3_PLL1_TPA	PLL1 Analog Test Point	N26	Out	SD3_XPADVDD
SD3_PLL1_TPD	PLL1 Digital Test Point	M28	Out	SD3_XPADVDD
SD3_PLL2_TPA	PLL2 Analog Test Point	J26	Out	SD3_XPADVDD
SD3_PLL2_TPD	PLL2 Digital Test Point	L26	Out	SD3_XPADVDD
BBI JESD204B interface SYNC~ signals				
BBI_TXSYNC_P	Modem Interface JESD Tx. Synchronization	U31	In	LVDD3

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
BBI_TXSYNC_N	Modem Interface JESD Tx. Synchronization	U30	In	LVDD3
BBI_RXSYNC_P	Modem Interface JESD Rx. Synchronization	U33	Out	LVDD3
BBI_RXSYNC_N	Modem Interface JESD Rx. Synchronization	U34	Out	LVDD3
Debug JESD204B interface				
TX10_DAT1_P	Debug JESD Tx. Data Out	G31	Out	SD3_XPADVDD
TX10_DAT1_N	Debug JESD Tx. Data Out	G30	Out	SD3_XPADVDD
TX10_DAT2_P	Debug JESD Tx. Data Out	F29	Out	SD3_XPADVDD
TX10_DAT2_N	Debug JESD Tx. Data Out	F28	Out	SD3_XPADVDD
TX10_SYNC_N	Debug JESD Synchronization	P29	In	LVDD3
TX10_SYNC_P	Debug JESD Synchronization	P28	In	LVDD3
Thermal diode and FA				
ANODE	Thermal Diode Anode	AF14	—	LVDD3
CATHODE	Thermal Diode Cathode	AH14	—	LVDD3
FA_ANALOG_PIN	Leakage Measurement	AE28	Gnd	TVDD1_8
FA_ANALOG_G_V	Transistor Gate Voltage	AE27	Gnd	TVDD1_8
FAVDD	FA supply	AF26	Power	—
SENSE_DVDD1	Voltage sense	K10	Power	—
SENSE_DVSS1	Voltage sense	K9	Gnd	—
SENSE_DVDD2	Voltage sense	AK27	Power	—
SENSE_DVSS2	Voltage sense	AJ27	Gnd	—
Supply and Ground balls				
DVDD	Digital supply	AA14,AA16,AA18,AA20,AA22,AA24,AB15,AB17,AB19,AB21,AB23,AC14,AC16,AC18,AC20,AC22,AC24,L12,L14,L16,L22,M13,M15,M17,M19,M21,N12,N14,N16,N18,N20,N22,P13,P15,P17,P19,P21,R14,R16,R18,R20,R22,T15,T17,T19,T21,U14,U16,U18,U20,U22,V15,V17,V19,V21,V23,W14,W16,W18,W20,W22,Y15,Y17,Y19,Y21,Y23		

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
DVSS	Ground	AA15,AA17,AA19,AA21,AA23,AA33,AB14,AB16,AB18,AB20,AB22,AB24,AB29,AB32,AC15,AC17,AC19,AC21,AC23,AC27,AC31,AD19,AD21,AD23,AD30,AD33,AE20,AE22,AE24,AE26,AE32,AF15,AF16,AF19,AF21,AF23,AF25,AF31,AG11,AG14,AG18,AG20,AG23,AG26,AG29,AG31,AG33,AH11,AH18,AH23,AH27,AH32,AJ10,AJ13,AJ15,AJ24,AJ29,AJ31,AJ9,AK10,AK12,AK14,AK16,AK24,AK33,AK4,AK7,AL10,AL14,AL17,AL26,AL27,AL31,AL4,AL7,AM14,AM18,AM25,AM28,AM29,AM32,AM33,AM4,AM5,AM6,AM8,AM9,AN12,AN14,AN17,AN25,AN27,AN30,AN33,AN6,AP14,AP18,AP31,AP6,B1,B11,B14,B17,B2,B20,B23,B24,B27,B30,B33,B5,B8,C16,C22,C3,C6,D1,D13,D19,D2,D27,D31,D7,D9,E11,E14,E17,E20,E24,E3,E5,F1,F12,F16,F2,F22,F3,F6,F7,G1,G26,G4,G5,G8,H12,H14,H16,H18,H20,H6,H7,H9,J22,J4,J5,J8,K11,K6,K7,K8,L13,L15,L17,L18,L21,L8,M12,M14,M16,M18,M20,M22,M8,M9,N13,N15,N17,N19,N21,P12,P14,P16,P18,P20,P22,R15,R17,R19,R21,R28,R29,R32,R33,R34,T14,T16,T18,T20,T22,T30,T31,T32,U15,U17,U19,U21,U23,U25,U32,V14,V16,V18,V20,V22,V27,V30,V31,V33,V34,W15,W17,W19,W21,W23,Y14,Y16,Y18,Y20,Y22,Y24,Y26,Y28,Y31		
P1OVDD	Fusebox supply	AF27		
P2OVDD	Fusebox supply	AF28		
APVDD1	System PLL supply	V26		
APVDD2	DDR PLL supply	U29		
APVDD3	TbGen PLL supply	U28		
FVDD	Flash supply	AA25,AA26,W25,Y25		
GVDD1	Supply group GVDD1	AD16,AE16		
GVDD2	Supply group GVDD2	J12,J13,K12,K13		
GVDD3	Supply group GVDD3	J17,J18,K17,K18		
GVDD4	Supply group GVDD4	J19,K19,L19		
GVDD5	Supply group GVDD5	J20,K20,L20		
GVDD6	Supply group GVDD6	J21,K21,K22		
GVDD7	Supply group GVDD7	J14,J15,K14,K15		
GVDD8	Supply group GVDD8	AD17,AE17		
GVDD9	Supply group GVDD9	AD15,AE15		
JVDD	Supply group JVDD	J16,K16		
LVDD1	Supply group LVDD1	AD14,AE13,AE14		
LVDD2	Supply group LVDD2	L11,M10,M11,N11,P11		
LVDD3	Supply group LVDD3	U24,V24,W24		

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
MVDD	Supply group MVDD	AD18,AD20,AD22,AE19,AE21,AF20,AF22,AG21,AG22,AK18,AK20,AK22,AL24,AM21,AM22,AN19,AN22,AP24		
MVDD1_8	Supply group MVDD1_8	AE18,AE23		
SD1_XCOREVDD	Supply group SD1_XCOREVDD	AA13,AB13,AC13,AD13,Y13		
SD1_XCOREVSS	Supply group SD1_XCOREVSS	AA10,AA3,AB1,AB10,AB11,AB12,AB2,AB3,AB9,AC10,AC3,AD1,AD11,AD12,AD2,AD3,AE10,AE12,AE3,AF1,AF10,AF11,AF2,AF3,AF9,AG3,AH1,AH2,AH3,AJ3,AK1,AK2,AK3,AL3,AM1,AM2,AM3,AN3,AP2,AP3,W3,W4,W5,W7,Y1,Y10,Y2,Y3		
SD1_XPADVDD	Supply group SD1_XPADVDD	AA8,AB8,AC8,AD8,AE8,AF8,AG8,AH8,AJ8		
SD1_XPADVSS	Supply group SD1_XPADVSS	AA6,AA7,AB4,AB5,AC6,AC7,AD4,AD5,AE6,AE7,AF4,AF5,AG6,AG7,AH4,AH5,AJ4,AJ5,AJ6,AJ7,Y4,Y5,Y6		
SD1_AVDD_PLL1	PLL1 Supply	AA9		
SD1_AVSS_PLL1	PLL1 Supply	Y8		
SD1_AVDD_PLL2	PLL2 supply	AD9		
SD1_AVSS_PLL2	PLL2 supply	AC9		
SD2_XCOREVDD	Supply group SD2_XCOREVDD	R13,T13,U13,V13,W13		
SD2_XCOREVSS	Supply group SD2_XCOREVSS	H1,H2,H3,J3,K1,K2,K3,L3,L4,L5,M1,M2,M3,M5,N3,N4,N5,N6,N7,N8,P1,P2,P3,P4,P8,R10,R11,R12,R3,R9,T1,T10,T2,T3,T9,U11,U12,U3,U4,V1,V10,V2,V5,W11,W12,W9		
SD2_XPADVDD	Supply group SD2_XPADVDD	R8,T8,U8,V8		
SD2_XPADVSS	Supply group SD2_XPADVSS	R4,R5,R6,T6,T7,U5,V6,V7		
SD2_AVDD_PLL1	PLL1 Supply	U9		
SD2_AVSS_PLL1	PLL1 Supply	V9		
SD2_AVDD_PLL2	PLL2 supply	P6		
SD2_AVSS_PLL2	PLL2 supply	R7		
SD3_XCOREVDD	Supply group SD3_XCOREVDD	K23,L23,M23,N23,P23,R23,T23		
SD3_XCOREVSS	Supply group SD3_XCOREVSS	D32,D33,D34,E32,F32,F33,F34,G32,H23,H24,H25,H26,H32,H33,H34,J23,J25,J32,K24,K32,K33,K34,L24,L25,L32,M26,M32,M33,M34,N24,N25,N28,N29,N30,N32,P26,P27,P30,P31,P32,R26,R27,T24,T25,T26,T27		
SD3_XPADVDD	Supply group SD3_XPADVDD	E27,F27,G27,H27,J27,K27,L27		
SD3_XPADVSS	Supply group SD3_XPADVSS	E28,E29,E30,F30,F31,G28,G29,H30,H31,J28,J29,K30,K31,L28,L29,M29,M30,M31		
SD3_AVDD_PLL1	PLL1 Supply	M27		
SD3_AVSS_PLL1	PLL1 Supply	N27		
SD3_AVDD_PLL2	PLL2 supply	K25		
SD3_AVSS_PLL2	PLL2 supply	K26		
TVDD	Supply group TVDD	AB25,AC25,AD25,AE25		
TVDD1_8	Supply group TVDD1_8	AD26,AD27		

Table 1. AFD4400 Pinout

Signal	Description	Package Pin	Pin Type	Power Supply
NC	Not connected	AA11,AA12,AC11,AC12,D4,M24,M25,P24,P25,T11,T12		

2 AFD4400 ball map

This figure shows the AFD4400 ball map.

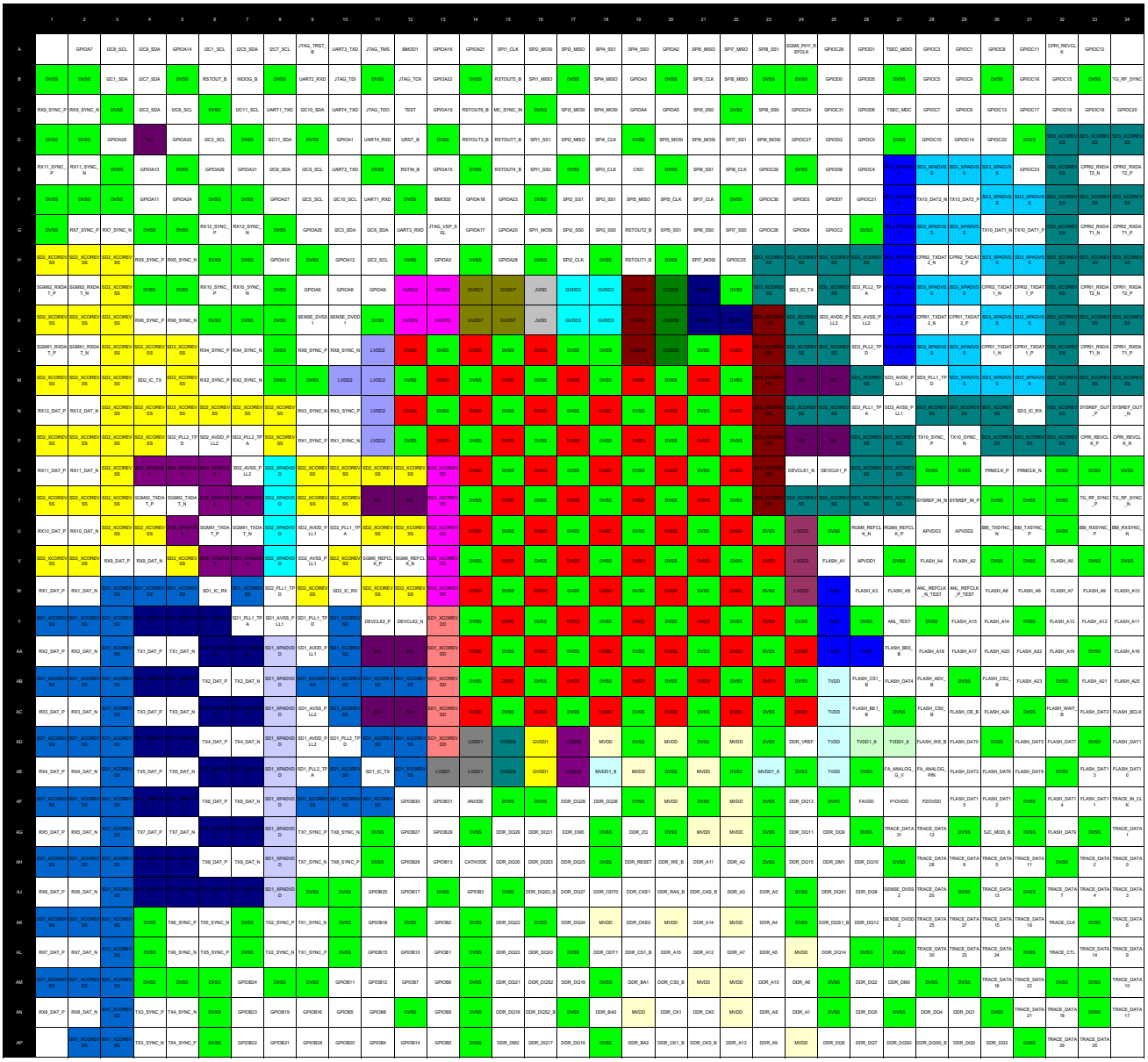


Figure 2. AFD4400 ball map

3 Electrical characteristics

This section provides the AC and DC electrical specifications. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference.

3.1 Overall DC electrical characteristics

This section covers the ratings, conditions and other characteristics.

3.1.1 Absolute maximum ratings

Table 2 shows the absolute maximum operating ratings.

CAUTION

Stress beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 2. Absolute maximum operating ratings

Parameter Symbol	Symbol	Min	Max	Unit	Note
Core supply voltage DVDD	V_{DD}	–0.3	1.1	V	—
PLL supply voltage APVDD1 APVDD2 APVDD3	V_{DPLL}	–0.3	1.98	V	—
SerDes PLL supply voltage SD1_AVDD_PLL1 SD1_AVDD_PLL2 SD2_AVDD_PLL1 SD2_AVDD_PLL2 SD3_AVDD_PLL1 SD3_AVDD_PLL2	VDD_{SDP}	–0.3	1.65	V	1
SerDes transceiver Core power supply for receivers SD1_XCOREVDD SD2_XCOREVDD SD3_XCOREVDD	VDD_{SDX}	–0.3	1.1	V	—
SerDes transceiver pad power supply for transmitter SD1_XPADVDD SD2_XPADVDD SD3_XPADVDD	VDD_{SDIO}	–0.3	1.65	V	1
JTAG supply voltage JVDD	VDD_{GPIO}	–0.3	3.6	V	—

Table 2. Absolute maximum operating ratings (continued)

Parameter Symbol		Symbol	Min	Max	Unit	Note
LVCMOS Input/output supply voltage FVDD GVDD1 GVDD2 GVDD3 GVDD4 GVDD5 GVDD6 GVDD7 GVDD8 GVDD9		VDD_{GPIO}	–0.3	3.6	V	2
DDR pad supply voltage MVDD TVDD		VDD_{DDR}	–0.3	1.65	V	—
DDR pad 1.8V supply voltage MVDD1_8 TVDD1_8		VDD_{DDR1p8}	–0.3	1.98	V	—
LVDS Input/output supply voltage LVDD1 LVDD2 LVDD3		VDD_{LVDS}	–0.3	1.98	V	—
Fuse programming Supply P1OVDD P2OVDD		VDD_{EFUSE_PGM}	–0.3	1.98	V	—
Input voltage range	DDR input signal	MV_{IN}	–0.3	0.3 + VDD_{DDR}	V	—
	LVCMOS input	V_{IN_GPIO}	–0.3	0.3 + VDD_{GPIO}	V	—
	LVDS input	V_{IN_LVDS}	–0.3	0.3 + VDD_{LVDS}	V	—
	DDR reference	DDR_{REF}	–0.3	0.3 + (0.5 x VDD_{DDR1p8})	V	—
	SerDes input	V_{IN_SerDes}	–0.3	0.3 + VDD_{SDIO}	V	—
Storage temperature range		$T_{storage}$	–40	125	°C	—

Note:
1. Supply can be configured for two different nominal voltage settings. Refer AFD4400 Reference Manual for details.
2. The LVCMOS IO voltage is configured through VSEL bits. Refer AFD4400 Reference Manual for details.

3.1.2 Recommended operating conditions

Table 3 provides the recommended operating conditions.

Table 3. Recommended operating conditions

Supply		Symbol	Min	Typ	Max	Unit	Notes
Digital logic voltage DVDD	At initial startup	V_{DD}	(VID or 1.025)-30mV	(VID or 1.025)	(VID or 1.025)+30mV	V	2,3,4,5,8
	During normal operation	V_{DD}	VID-30mV	VID	VID+30mV	V	

Table 3. Recommended operating conditions (continued)

Supply		Symbol	Min	Typ	Max	Unit	Notes
PLL voltage	Analog supply • APVDD1 • APVDD2 • APVDD3	V_{DPLL}	1.71	1.8	1.89	V	—
SerDes	SerDes transceiver core supply for receiver • SD1_XCOREVDD • SD2_XCOREVDD • SD3_XCOREVDD	VDD_{SDX}	0.95	1	1.05	V	—
	SerDes PLL supply • SD1_AVDD_PLL1 • SD1_AVDD_PLL2 • SD2_AVDD_PLL1 • SD2_AVDD_PLL2 • SD3_AVDD_PLL1 • SD3_AVDD_PLL2	VDD_{SDP}	1.425	1.5	1.575	V	—
	SerDes transceiver pad supply for transmitter • SD1_XPADVDD • SD2_XPADVDD • SD3_XPADVDD	VDD_{SDIO}	1.425	1.5	1.575	V	—
JTAG power supply • JVDD		VDD_{GPIO}	2.85	3.0 3.3	3.465	V	1
LVCMOS power supply • FVDD • GVDD1 • GVDD2 • GVDD3 • GVDD4 • GVDD5 • GVDD6 • GVDD7 • GVDD8 • GVDD9		VDD_{GPIO}	1.71 2.85	1.8 3.0 3.3	1.89 3.465	V	1
DDR pad supply voltage range • MVDD • TVDD		VDD_{DDR}	1.425	1.5	1.575	V	—
DDR pad 1.8V supply • MVDD1_8 • TVDD1_8		VDD_{DDR1p8}	1.71	1.8	1.89	V	—
DDR pad Reference Voltage • DDR_VREF		DDR_{REF}	(0.5 x VDD_{DDR}) – 2%	0.5 x VDD_{DDR}	(0.5 x VDD_{DDR}) + 2%	V	—
LVDS power supply • LVDD1 • LVDD2 • LVDD3		VDD_{LVDS}	1.71	1.8	1.89	V	1

Table 3. Recommended operating conditions (continued)

Supply	Symbol	Min	Typ	Max	Unit	Notes
Fuse program voltage • P1OVDD • P2OVDD	V_{EFUSE_PGM}	1.71	1.8	1.89	V	6,7
Operating temperature range (Junction)	T_J	–40	—	105	°C	—

Note:

1. Overshoot and undershoot conditions (transitions above max IO supply and below ground) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle.
2. Refer to Section 4.2.1, “Voltage ID (VID) controllable supply and Section 4.2.2, “Core supply voltage (VDD) filtering for additional information
3. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin. Refer to Section 4.2.6, “Remote power-supply sense recommendations” for more detail.
4. Operation at 1.1V is allowable for up to 25ms at initial power on.
5. Voltage ID (VID) operating range is between 0.975V to 1.025V. Regulator selection should be based on Vout range wider than VIDmin to VIDmax with resolution of 12.5mV or better.
6. P1OVDD should be tied to ground during functional applications.This supply is needed in the factory for programming of memory repair fuses.
7. P2OVDD should be tied to ground during functional applications. It can be driven to the specified supply during functional fuse programming.
8. If VID is known at initial start-up, set V_{DD}=VID else if VID is not known at initial start-up, set V_{DD} to 1.025V and change it immediately, to V_{DD}=VID after reading the VID at the beginning of software.

3.1.3 LVCMOS DC parameters

Table 4 provides the DC operating characteristics for LVCMOS pads.

Table 4. LVCMOS DC electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	Notes
V_{OH}	High-level output voltage	Ioh = –1mA	VDD_{GPIO}–0.15		—	V	—
V_{OL}	Low-level output voltage	Iol = 1mA	—		0.15	V	—
V_{IH}	High-level DC input voltage	—	$0.7 \times VDD_{GPIO}$		VDD_{GPIO}	V	1
V_{IL}	Low-level DC input voltage	—	0	—	$0.2 \times VDD_{GPIO}$	V	
I_{IN}	Input current (no pull-up/down)	Vin = VDD_{GPIO} or 0	—	—	1	µA	2
Iin_33pu	Input current (33 KΩ PU)	Vin = 0 Vin = VDD_{GPIO}	—	—	220 1	µA	2,4
Iin_50pu	Input current (50 KΩ PU)	Vin = 0 Vin = VDD_{GPIO}	—	—	100 1	µA	2,4
Iin_100pu	Input current (100 KΩ PU)	Vin = 0 Vin = VDD_{GPIO}	—	—	50 1	µA	2,4
Iin_100pd	Input current (100 KΩ PD)	Vin = 0 Vin = VDD_{GPIO}	—	—	1 50	µA	2,4
Rkeep	Pad keeper resistance	—	105	135	175	KΩ	3,4

Table 4. LVCMOS DC electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	Notes
Rod_keep	Maximum external resistor value that is guaranteed to overdrive the pad keeper	—	—	—	47	KΩ	4

Note:

1. To maintain a valid level, the transitioning edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, V_{IL} or V_{IH}. monotonic input transition time is from 0.1ns to 1s.
2. Max condition: with best case process corner, 3.6 V supply, and 105 °C temperature.
3. Typ condition: Typical conditions: typical process corner, 1.8 V supply, and 25 °C temperature, max condition: worst case process conditions, 1.71 V supply, and 105 °C temperature, min condition: best case process conditions, 3.6 V supply, and –40 °C temperature. These values are for I/O buffers. Pad keeper resistance is weak to save power in special cases when after reset pad keeper is enabled and external resistor is connected to pad to overwrite keeper value.
4. Values are based on simulated numbers and are not measured on silicon.

Table 5. LVCMOS Schmitt trigger operation

Symbol	Parameter	Test conditions	Supply voltage	Min	Typ	Max	Unit	Notes
V_{T+}	Positive going threshold voltage	V_{OUT} >= (V_{OH})min	1.8V	0.4 x VDD_{GPIO}	—	—	V	1
V_{T-}	Negative going threshold voltage	V_{OUT} =< (V_{OL})max	1.8V	—	—	0.6 x VDD_{GPIO}	V	1
V_{HYS}	Hysteresis voltage	V_{T+} - V_{T-}	1.8V	0.17	—	—	V	1
			3.3V	0.12	—	—	V	1

Note:

1. Values are based on simulated numbers and are not measured on silicon.

3.1.3.1 Output driver impedance

The tables below shows the average impedance at different operating points.

Table 6. Output driver average impedance (1.8 V voltage mode)

Parameter	Symbol	Drive strength setting	Min	Typ	Max	Unit	Note
Output driver impedance	Rdrv	0 0 1	170	220	300	Ω	—
		0 1 0	65	85	115	Ω	—
		0 1 1	45	60	80	Ω	—
		1 0 0	55	75	100	Ω	—
		1 0 1	40	55	75	Ω	—
		1 1 0	30	40	52	Ω	—
		1 1 1	25	33	44	Ω	—

Note:

1. Drive strength value 000 sets the pad at high Z.

Table 8. Output driver average impedance (3.3 V voltage mode)

Parameter	Symbol	Drive strength setting	Min	Typ	Max	Unit	Note
Output driver impedance	Rdrv	0 0 1	180	250	400	Ω	—
		0 1 0	65	90	145	Ω	—
		0 1 1	45	65	90	Ω	—
		1 0 0	60	80	115	Ω	—
		1 0 1	45	55	80	Ω	—
		1 1 0	30	40	55	Ω	—
		1 1 1	25	34	45	Ω	—

Note:
1. Drive strength value 000 sets the pad at high Z.

3.1.4 LVDS DC parameters

The DC operating characteristics are provided in the table below for LVDS pads.

Table 9. LVDS DC electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	Notes
V_{od}	Output differential voltage	Resistive load = 100 Ω between padp and padn	250	350	450	mV	|Vpadp–Vpadn|
V_{oh}	High-level output voltage		1.25	1.375	1.6	V	—
V_{ol}	Low-level output voltage		0.9	1.025	1.25		—
V_{os}	Offset voltage		1.125	1.2	1.375		—
V_{id}	Input Differential Voltage	—	100	—	600	mV	|Vpadp–Vpadn|
V_{icm}	Input common mode voltage	—	50mV	—	1.57	V	—
ICC	Power supply current (VDD_{LVDS})	Resistive load = 100 Ω between padp and padn	—	—	5	mA	—
R_T	RX Termination resistor	—	—	100	—	Ω	1

Note:
1. Values are based on simulated numbers and are not measured on silicon.

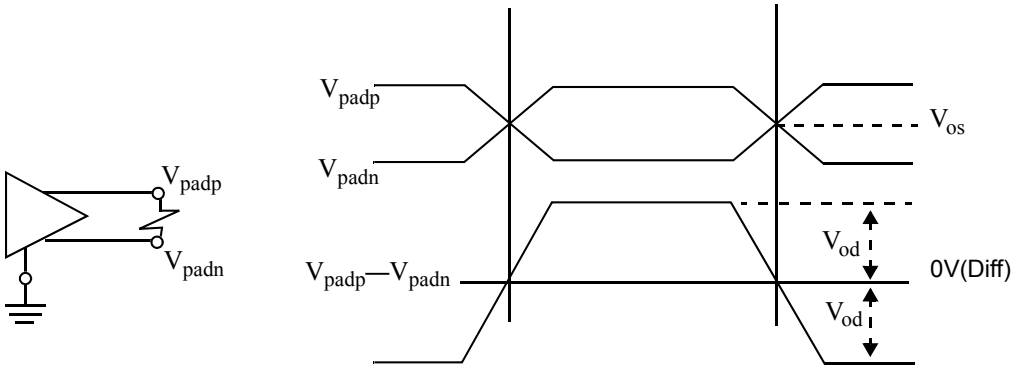


Figure 3. LVDS parameters

3.1.5 DDR DC parameters

Table 10 provides DC electrical characteristics for DDR.

Table 10. DDR DC electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	Notes
Vih	Input high voltage	—	DDR_{REF} + 0.100	—	VDD_{DDR}	V	—
Vil	Input low voltage	—	GND	—	DDR_{REF} – 0.100	—	—
Voh	High-level output voltage	Ioh = –1 mA	$0.8 \times VDD_{DDR}$	—	—	V	—
Vol	Low-level output voltage	Iol = 1 mA	—	—	$0.2 \times VDD_{DDR}$		—
Vref	Input reference voltage	—	$0.49 \times VDD_{DDR}$	$0.5 \times VDD_{DDR}$	$0.51 \times VDD_{DDR}$		1
Iin	Input current for the IO cell (no internal pullup/pulldown resistor)	Vi = 0 or VDD_{DDR}	—	—	50	µA	2
MMpupd	Pullup/pulldown driver impedance mismatch	34 Ω full strength driver	–10	—	+10	%	4

Table 10. DDR DC electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	Notes
Rres	Driver 240 Ω unit calibration resolution	—	—	—	10	Ω	4
Rkeep	Pad keeper resistance	—	105	135	175	kΩ	3,4
Rod_keep	Maximum external resistor value that is guaranteed to overdrive the pad keeper	—	—	—	47	kΩ	4

Note:

1. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to Vref with a min value of Vref - 0.04 and a max value of Vref + 0.04. V_{TT} should track variations in the DC level of Vref.
2. Typ condition: typ model, VDD_{DDR} 1.5 V, and 25 °C. Max condition: bcs model, VDD_{DDR}1.575 V, and –40 °C. Min condition: wcs model, VDD_{DDR} 1.425 V, and 125 °C.
3. Typ condition: typ model, VDD_{DDR} 1.5 V, and 25 °C, max condition: wcs model, VDD_{DDR} 1.425 V, and 125 °C, min condition: bcs model, VDD_{DDR} 1.575 V, and –40 °C. These values are for digital IO buffers.
4. Values are based on simulated numbers and are not measured on silicon.

3.1.6 SerDes DC parameters

The following subsections define the DC-level requirements for the CPRI, SGMII and JESD204B data lines.

3.1.6.1 DC-level requirements for CPRI configurations

This section provide various DC-level requirements for CPRI configurations.

This table provides the CPRI-LV-XAUI based transmitter DC specifications.

Table 11. Transmitter DC specifications (LV: 1.2288, 2.4576 and 3.072 Gbps)(SDn_XPADVDD=1.5)

Symbol	Characteristic	Min	Nom	Max	Unit	Note
V_{DIFF_P-P}	Differential Output Voltage	800		1600	mV p–p	—
R_D	Differential resistance	80	100	120	Ω	—

This table provides the CPRI-LV-XAUI based receiver DC specifications.

Table 12. Receiver DC specifications (LV: 1.2288, 2.4576 and 3.072 Gbps) (SDn_XPADVDD=1.5)

Symbol	Characteristic	Min	Nom	Max	Unit	Note
V_{IN}	Differential input voltage	200		1600	mV p–p	—
R_{IN}	Differential resistance	80		120	Ω	—

This table provides the CPRI-LV-II and LV_III transmitter DC specifications.

Table 13. CPRI transmitter DC specifications (LV-II: 1.2288, 2.4576, 3.072, 4.9152, and 6.144 Gbps, LV-III: 9.8304 Gbps) (SDn_XPADVDD=1.5)

Symbols	Parameter	Min	Nom	Max	Unit	Note
V_{ODIFF}	Output differential voltage into floating load Rload=100 Ω	800	—	1200	mV	—
$V_{TX\text{-}DE\text{-}RATIO–1.14\ dB}$	De-emphasized differential output voltage (Ratio)	0.6	1.1	1.6	dB	—
$V_{TX\text{-}DE\text{-}RATIO–3.5\ dB}$	De-emphasized differential output voltage (Ratio)	3	3.5	4	dB	—
$V_{TX\text{-}DE\text{-}RATIO–4.66\ dB}$	De-emphasized differential output voltage (Ratio)	4.1	4.6	5.1	dB	—
$V_{TX\text{-}DE\text{-}RATIO–6.0\ dB}$	Tx De-emphasized level	5.5	6.0	6.5	dB	—
$V_{TX\text{-}DE\text{-}RATIO–9.5\ dB}$	De-emphasized differential output voltage (Ratio)	9	9.5	10	dB	—
T_Rd	Differential resistance	80	100	120	Ω	—

This table provides the CPRI LV-II and LV-III receiver DC timing specifications.

Table 14. CPRI receiver DC specifications (LV-II: 1.2288, 2.4576, 3.072, 4.9152, and 6.144 Gbps, LV-III: 9.8304 Gbps) (SDn_XPADVDD=1.5)

Symbols	Parameter	Min	Nom	Max	Unit	Note
V_{IN_DIFF}	Input differential voltage	N/A	—	1200	mV	—
R_{DIN}	Differential resistance	80	—	120	Ω	—

NOTE

It is assumed that for the V_{IN_DIFF} Min spec, the eye can be closed at the receiver after passing the signal through a CEI/CPRI Level II LR compliant Channel.

3.1.6.2 DC-level requirements for SGMII configurations

This table describes the SGMII SerDes transmitter DC specifications.

Table 15. SGMII transmitter DC specifications (SDn_XPADVDD=1.5)

Symbol	Parameter	Min	Nom	Max	Unit	Note
V_{OH}	Output high voltage	—	—	1.5 x |Vod|,max	mV	1
V_{OL}	Output low voltage	|Vod|,min/2	—	—	mV	1

Table 15. SGMII transmitter DC specifications (continued)(SDn_XPADVDD=1.5)

$\|V_{OD}\|$	Output differential voltage	320	500	725	mV	—
		293.8	459	665.6		—
		266.9	417	604.7		—
		240.6	376	545.2		—
		213.1	333	482.9		—
		186.9	292	423.4		—
		160.0	250	362.5		—
Z0	Output impedance (single ended)	40	50	60	Ω	—

Note:

1. This does not align to DC-coupled SGMII.
2. $|V_{OD}|= |V_{SD_TXn} - V_{SD_TXn_B}|$. $|V_{OD}|$ is also referred to as output differential peak voltage. $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$
3. The $|V_{OD}|$ value shown in the Typ column is based on the condition of SD*n*_XCOREVDD-Typ = 1.35 V or 1.5 V, no common mode offset variation. SerDes transmitter is terminated with 100- differential load between differential pins.
4. For recommended operating conditions, see Table 3.

This table describes the SGMII SerDes receiver DC timing specifications.

Table 16. SGMII receiver DC specifications (SDn_XPADVDD=1.5)

Symbols	Parameter	Min	Nom	Max	Unit	Note
$V_{RX_DIFFp-p}$	Input differential voltage	100	—	1200	mV	—
		175	—	1200	mV	—
V_{LOS}	Loss of signal threshold	30	—	100	mV	—
		65	—	175	mV	—
Z_{RX_DIFF}	Receiver differential input impedance	80	—	120	Ω	—

3.1.6.3 DC-level requirements for JESD204B configurations

This table provides the JESD204B transmitter DC specifications.

Table 17. JESD204B transmitter DC specifications(SDn_XPADVDD=1.5)

Symbols	Parameter	Min	Nom	Max	Unit	Note
V_{TX_DIFF}	Output differential voltage (into floating load Rload = 100 Ω)	360	—	770	mV	—
R_D	Differential resistance	80	100	120	Ω	—

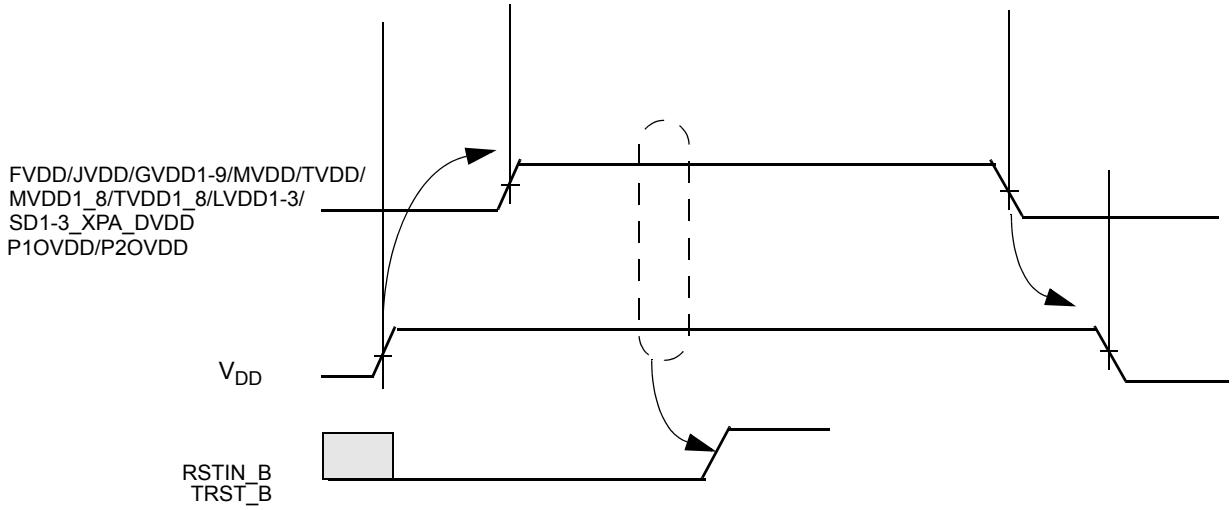
This table below provides the JESD204B receiver DC timing specifications.

Table 18. JESD204B receiver DC specifications (SDn_XPADVDD=1.5)

Symbols	Parameter	Min	Nom	Max	Unit	Note
V_{RX_DIFF}	Input differential voltage	110	—	1050	mV	—
R_{IN}	Differential resistance	80	—	120	Ω	—

3.2 Power sequencing

The following figure depicts the power-up sequencing requirements.There is no timing parameters associated with it; board designers need to ensure the sequence.



Note :
1. The Core VDD should come first. Other supplies can be in any order once the core supply is up and stable.
2. RSTIN_B and TRST_B should remain asserted till the power supplies get stable.
3. Refer to DC operating condition for supply specification.
4. During power off VDD should be the last supply to get turned off.

Figure 4. Power-up sequencing

3.2.1 Power-on ramp rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid falsely triggering the ESD circuitry. Table 19 provides the power supply ramp rate specifications.

Table 19. Power supply ramp rate

Parameter	Min	Max	Unit	Note
Required ramp rate for all voltage supplies	—	25	V/mS	3,4
Required ramp rate for P1OVDD and P2OVDD	—	25	V/mS	1, 2,3,4

Note:
1. P1OVDD should be tied to ground during functional applications.This supply is needed in the factory for programming of memory repair fuses.
2. P2OVDD should be tied to ground during functional applications. It can be driven to the specified supply during functional fuse programming.
3. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.
4. Over full recommended operating temperature range (see Table 3).

3.3 RESET initialization

This section describes the electrical specifications for the RESET initialization timing requirements.

The figure below shows reset timing diagram.

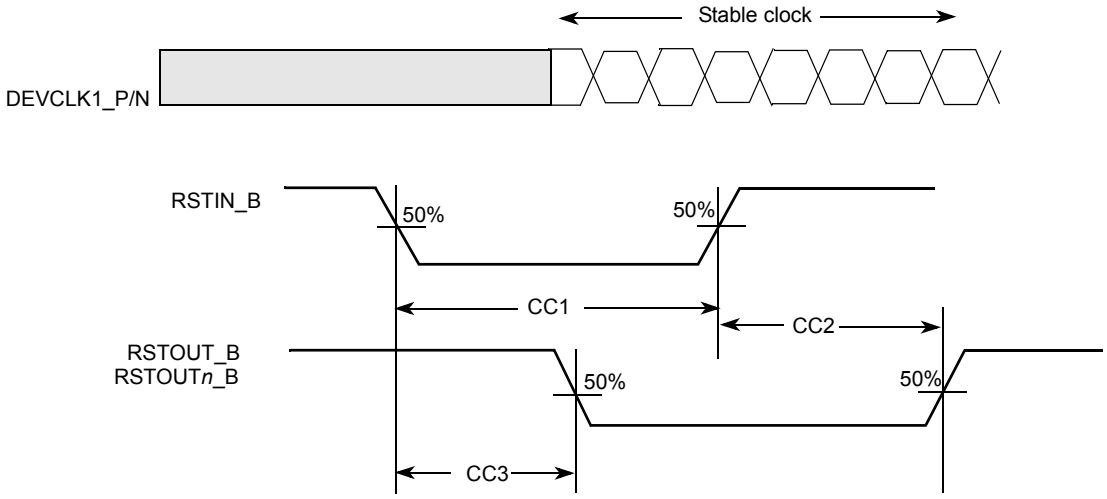


Figure 5. Reset timing diagram

NOTE

As shown in Figure 5, a stable DEVCLK1_P/N is required (at least one DEVCLK period before) to AFD4400 before releasing the RSTIN_B pin.

This table provides RESET initialization timing specifications.

Table 20. Reset initialization timing specifications

ID	Parameter	Symbol	Min	Max	Unit	Note
CC1	Duration of RSTIN_B to be qualified as valid (assumption: Input slope = 5 ns)	T_{RSTINV}	50	—	ns	—
CC2	Duration of RSTOUT_B, RSTOUT*n*_B assertion after de-assertion of RSTIN_B	$T_{RSTOUTW}$	200	—	µs	2
CC3	Delay from RSTIN_B to RSTOUT_B, RSTOUT*n*_B assertion	$T_{ROUTLRINV}$	—	35	ns	2
CC4	Duration of RSTOUT*n*_B for software bit based assertion	$T_{RSTOUTnW}$	45	—	µs	1,2

Note:
1. RSTOUT1_B to RSTOUT7_B can be asserted by writing into corresponding register bits in System Reset Controller module. Refer AFD4400 Reference Manual for details.
2. RSTOUT1_B to RSTOUT7_B pulse width matches RSTOUT_B timing in case of power on reset, cold reset and warm reset assertion.

3.4 Power characteristics

3.4.1 Power specifications

3.4.1.1 Device AFD4400NXN763VB power specification

This table defines the frequency settings used for specifying power consumption. All power states are specified at 105°C junction temperature.

Table 21. Frequency definition for power consumption measurement

Parameter	Symbol	Value	Unit
ARM® Cortex-A9 core clock	f_{mcu}	614.4	MHz
VSP clock	f_{VSP}	614.4	MHz
AXI clock	f_{axi}	307.2	MHz
AHB clock	f_{ahb}	153.6	MHz
IPG clock	f_{ip}	76.8	MHz
CPRI baud rate	f_{cpri}	9830.4	Mbps
JESD204 baud rate	f_{jesd}	9830.4	Mbps
Ethernet (SGMII) baud rate	f_{etsec}	1250	Mbps
DDR clock rate	f_{ddr}	500	MHz

This table provides the current consumption in various operating modes.

Table 22. Power numbers

Characteristic	Condition	Power mode	Junction Temp (°C)	V_{DD} (V)	V_{DD} Power (Core+ platform)	SoC Power (IO + V_{DD})(Watts)	Notes
Full run mode	• All VSPA running FIR with 100% utilization • ARM running code with 100% utilization. • ARM Data accesses from DDR memory • 8 JESD TX and 8 JESD RX at 9.8G rate, 1 lane per interface • 2 JESD RX for SRx function at 9.8G rate • 4 CPRI running at 9.8G, 2 links in RE mode, 2 links in REC mode • 2 Ethernet ports running at 1.25G	Maximum	105	VID	33.2	37.1	1,3,4
	• All VSPA running FIR 70% with 10% control code • ARM running code with 75% utilization • 8 JESD TX and 8 JESD RX at 9.8G rate, 1 lane per interface • 2 JESD RX for SRx function at 9.8G rate • 4 CPRI running at 9.8G, 2 links in RE mode, 2 links in REC mode	Thermal	105	VID	26.2	30.1	2,3,4
		Typical	70	VID	22.4	26.3	2,3,4,5

Preliminary

Table 22. Power numbers (continued)

Characteristic	Condition	Power mode	Junction Temp (°C)	V_{DD} (V)	V_{DD} Power (Core+ platform)	SoC Power (IO + V_{DD})(Watts)	Notes
Half run mode	• Six VSPA running FIR with 100% utilization. Remaining five power gated. • ARM running code with 100% utilization. • ARM Data accesses from DDR memory • 4 JESD TX and 4 JESD RX at 9.8G rate, 1 lane per interface • 2 JESD RX for SRx function at 9.8G rate • 2 CPRI running at 9.8G, one link in RE mode, one link in REC mode • Single Ethernet lane running at 1.25G	Maximum	105	VID	19.1	21.9	1,3,4
	• Six VSPA running FIR 70% with 10% control code. Remaining five power gated. • ARM running code with 75% utilization • 4 JESD TX and 4 JESD RX at 9.8G rate, 1 lane per interface • 2 JESD RX for SRx function at 9.8G rate • 2 CPRI running at 9.8G, one link in RE mode, one link in REC mode	Thermal	105	VID	15.3	18.1	2,3,4
		Typical	70	VID	12.9	15.7	2,3,4,5
4T4R 40 MHz bandwidth	• 4 Tx Antenna (153.6 MSPS) • 4 Rx Antenna (76.8 MSPS) • 2 SRx (153.6 MSPS) • 40 MHz Occupied Bandwidth • (8 - 5MHz LTE carriers per antenna) • 40 MHz Instantaneous Bandwidth • 153.6 MHz DPD Bandwidth • 2 CPRI links at 9.8304Gbps rate	Thermal	105	VID	16.2	18.2	5
Full Standby (CPRI active, antenna paths configured but not active)	• All VSPA in partial powerdown waiting for go event. Clocks enabled but gated. • ARM in stop mode. Clocks enabled but gated. Servicing only CPRI C&M messages • 8 JESD TX and 8 JESD RX at 9.8G rate, 1 lane per interface. Links active but no data transfer (zeros sent, receive data ignored) • 2 JESD RX for SRx function at 9.8G rate. Link active but receive data ignored. • 4 CPRI running at 9.8G, 2 links in RE mode, 2 links in REC mode	Typical	70	VID	3.4	7.2	5

Preliminary

Table 22. Power numbers (continued)

Characteristic	Condition	Power mode	Junction Temp (°C)	V_{DD} (V)	V_{DD} Power (Core+ platform)	SoC Power (IO + V_{DD})(Watts)	Notes
Half Standby (CPRI active, antenna paths configured but not active)	• 6 VSPA in partial powerdown waiting for go event. Clocks enabled but gated. Remaining VSPA in full powerdown. • ARM in stop mode. Clocks enabled but gated. Servicing only CPRI C&M messages • 4 JESD TX and 4 JESD RX at 9.8G rate, 1 lane per interface. Links active but no data transfer (zeros sent, receive data ignored). Remaining links inactive with SerDes powered down or disabled. • 2 JESD RX for SRx function at 9.8G rate. Link active but receive data ignored. • 2 CPRI running at 9.8G, 1 link in RE mode, 1 link in REC mode	Typical	70	VID	2.8	5.7	5
Sleep (CPRI active, no antenna paths configured or active)	• All VSPA in full powerdown. Clocks disabled. • ARM in stop mode. Clocks enabled but gated. Servicing only CPRI C&M messages. • All JESD disabled. Links inactive with SerDes powered down or disabled. • 2 CPRI running at 9.8G, 1 link in RE mode, 1 link in REC mode	Typical	70	VID	1.5	2.3	5

Note:
1. The maximum power is the peak power to be used for power supply sizing.
2. The thermal power is the average power of a worse case device running the defined use case.
3. The full run mode max power is tested (excluding IO power) using correlated static leakage limits. All other power modes are based on estimation and not guaranteed.
4. IO power is estimated based on typical design. It is highly dependent on board design and use case.
5. Typical power based on nominal process distribution for this device.
6. Voltage ID (VID) operating range is between 0.975V to 1.025V.

Preliminary

3.4.1.2 Device AFD4400NXN752VB power specification

This table defines the frequency settings used for specifying power consumption. All power states are specified at 105°C junction temperature.

Table 23. Frequency definition for power consumption measurement

Parameter	Symbol	Value	Unit
ARM® Cortex-A9 core clock	f_{mcu}	553	MHz
VSP clock	f_{VSP}	553	MHz
AXI clock	f_{axi}	276.5	MHz
AHB clock	f_{ahb}	138.3	MHz
IPG clock	f_{ip}	69.1	MHz
CPRI baud rate	f_{cpri}	9830.4	Mbps

Table 23. Frequency definition for power consumption measurement (continued)

Parameter	Symbol	Value	Unit
JESD204 baud rate	f_{jesd}	9830.4	Mbps
Ethernet (SGMII) baud rate	f_{etsec}	1250	Mbps
DDR clock rate	f_{ddr}	500	MHz

This table provides the current consumption in various operating modes.

Table 24. Power numbers

Characteristic	Condition	Power mode	Junction Temp (°C)	V_{DD} (V)	V_{DD} Power (Core+ platform)	SoC Power (IO + V_{DD})(Watts)	Notes
Full run mode	• All VSPA running FIR with 100% utilization • ARM running code with 100% utilization. • ARM Data accesses from DDR memory • 8 JESD TX and 8 JESD RX at 9.8G rate, 1 lane per interface • 2 JESD RX for SRx function at 9.8G rate • 4 CPRI running at 9.8G, 2 links in RE mode, 2 links in REC mode • 2 Ethernet ports running at 1.25G	Maximum	105	VID	34.9	38.8	1,3,4
	• All VSPA running FIR 70% with 10% control code • ARM running code with 75% utilization • 8 JESD TX and 8 JESD RX at 9.8G rate, 1 lane per interface • 2 JESD RX for SRx function at 9.8G rate • 4 CPRI running at 9.8G, 2 links in RE mode, 2 links in REC mode	Thermal	105	VID	28.2	32.1	2,3,4
		Typical	70	VID	22.6	26.5	2,3,4,5
Half run mode	• Six VSPA running FIR with 100% utilization. Remaining five power gated. • ARM running code with 100% utilization. • ARM Data accesses from DDR memory • 4 JESD TX and 4 JESD RX at 9.8G rate, 1 lane per interface • 2 JESD RX for SRx function at 9.8G rate • 2 CPRI running at 9.8G, one link in RE mode, one link in REC mode • Single Ethernet lane running at 1.25G	Maximum	105	VID	20.4	23.2	1,3,4
	• Six VSPA running FIR 70% with 10% control code. Remaining five power gated. • ARM running code with 75% utilization • 4 JESD TX and 4 JESD RX at 9.8G rate, 1 lane per interface • 2 JESD RX for SRx function at 9.8G rate • 2 CPRI running at 9.8G, one link in RE mode, one link in REC mode	Thermal	105	VID	16.7	19.5	2,3,4
		Typical	70	VID	13.2	16.0	2,3,4,5

Preliminary

Table 24. Power numbers (continued)

Characteristic	Condition	Power mode	Junction Temp (°C)	V_{DD} (V)	V_{DD} Power (Core+ platform)	SoC Power (IO + V_{DD})(Watts)	Notes
4T4R 40 MHz bandwidth	• 4 Tx Antenna (153.6 MSPS) • 4 Rx Antenna (76.8 MSPS) • 2 SRx (153.6 MSPS) • 40 MHz Occupied Bandwidth • (8 - 5MHz LTE carriers per antenna) • 40 MHz Instantaneous Bandwidth • 153.6 MHz DPD Bandwidth • 2 CPRI links at 9.8304Gbps rate	Thermal	105	VID	19.0	21.0	5
Full Standby (CPRI active, antenna paths configured but not active)	• All VSPA in partial powerdown waiting for go event. Clocks enabled but gated. • ARM in stop mode. Clocks enabled but gated. Servicing only CPRI C&M messages • 8 JESD TX and 8 JESD RX at 9.8G rate, 1 lane per interface. Links active but no data transfer (zeros sent, receive data ignored) • 2 JESD RX for SRx function at 9.8G rate. Link active but receive data ignored. • 4 CPRI running at 9.8G, 2 links in RE mode, 2 links in REC mode	Typical	70	VID	4.3	8.3	5
Half Standby (CPRI active, antenna paths configured but not active)	• 6 VSPA in partial powerdown waiting for go event. Clocks enabled but gated. Remaining VSPA in full powerdown. • ARM in stop mode. Clocks enabled but gated. Servicing only CPRI C&M messages • 4 JESD TX and 4 JESD RX at 9.8G rate, 1 lane per interface. Links active but no data transfer (zeros sent, receive data ignored). Remaining links inactive with SerDes powered down or disabled. • 2 JESD RX for SRx function at 9.8G rate. Link active but receive data ignored. • 2 CPRI running at 9.8G, 1 link in RE mode, 1 link in REC mode	Typical	70	VID	3.5	6.4	5
Sleep (CPRI active, no antenna paths configured or active)	• All VSPA in full powerdown. Clocks disabled. • ARM in stop mode. Clocks enabled but gated. Servicing only CPRI C&M messages. • All JESD disabled. Links inactive with SerDes powered down or disabled. • 2 CPRI running at 9.8G, 1 link in RE mode, 1 link in REC mode	Typical	70	VID	1.9	2.7	5

Preliminary

Table 24. Power numbers (continued)

Characteristic	Condition	Power mode	Junction Temp (°C)	V_{DD} (V)	V_{DD} Power (Core+ platform)	SoC Power (IO + V_{DD})(Watts)	Notes

Note:
1. The maximum power is the peak power to be used for power supply sizing.
2. The thermal power is the average power of a worse case device running the defined use case.
3. The full run mode max power is tested (excluding IO power) using correlated static leakage limits. All other power modes are based on estimation and not guaranteed.
4. IO power is estimated based on typical design. It is highly dependent on board design and use case.
5. Typical power based on nominal process distribution for this device.
6. Voltage ID (VID) operating range is between 0.975V to 1.025V.

3.5 Input clocks

AFD4400 has four sets of reference input clocks : DEVCLK1_P/N, DEVCLK2_P/N, SGMII_REFCLK_P/N, and RGMII_REFCLK_P/N.The DEVCLK1 is the default system clock and must be present for the device to come out of reset.

Refer to Section 3.6.11.2, "SerDes reference clocks" for DEVCLK*n*_P/N and SGMII_REFCLK_P/N electrical specification.

This table provides the RGMII_REFCLK_P/N clock parameters. This clock is an optional source of reference clock to PLLs.

Table 25. SGMII_REFCLK/RGMII_REFCLK AC parameters

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
Clock frequency	f_{RGMII}	66	125	167	MHz	—
SGMII clock duty cycle	—	40	50	60	%	—
Period Jitter (Short + Long)	T_{J_PERIOD}	—	—	150	ps	—
Jitter phase noise at -56 dBc	—	—	—	500	KHz	—

Note:
1. Refer LVDS IO timing spec for pulse skew requirement.

3.6 Module electrical characteristics

This section describes the electrical information including timing specification for the various modules.

3.6.1 Configurable serial peripheral interface (CSPI)

This section describes the electrical information of the CSPI.

Table 26. SPI master mode timing characteristics

ID	Parameter Description	Symbol	Min	Max	Unit	Note
CSM1	SPI*n*_CLK Cycle Time	T_{SPK}	38.5	—	ns	—
CSM2	SPI*n*_CLK High or Low Time	T_{SPKLH}	17	—	ns	—

Table 26. SPI master mode timing characteristics (continued)

ID	Parameter Description	Symbol	Min	Max	Unit	Note
CSM4	SPI*n*_SS*m* negated pulse width	T_{SPOW}	30	—	ns	—
CSM5	SPI*n*_SS*m* Lead Time (CS setup time)	T_{SPKHOH}	5	—	ns	—
CSM6	SPI*n*_SS*m* Lag Time (CS hold time)	T_{SPKLOL}	5	—	ns	—
CSM10	SPI*n*_DI Setup Time	T_{SPIVKL}	5	—	ns	—
CSM11	SPI*n*_DI Hold Time	T_{SPIXKL}	5	—	ns	—
CSM12	SPI*n*_DO Output Delay	T_{SPKHOV}	—	6	ns	—
CSM13	SPI*n*_RDY Setup Time	T_{SPOHIH}	5	—	ns	—

Table 27. SPI slave timing characteristics

Ref. Num	Parameter Description	Symbol	Min	Max	Unit	Note
CSS1	SPI*n*_CLK Cycle Time	T_{SPK2}	55.5	—	ns	—
CSS2	SPI*n*_CLK High or Low Time	T_{SPKLH2}	25.5	—	ns	—
CSS4	SPI*n*_SS*m* negated pulse width	T_{SPIW2}	47	—	ns	—
CSS5	SPI*n*_SS*m* Lead Time (CS setup time)	T_{SPIHKH}	5	—	ns	—
CSS6	SPI*n*_SS*m* Lag Time (CS hold time)	T_{SPILKL}	5	—	ns	—
CSS7	SPI*n*_DI Setup Time	$T_{SPIVKL2}$	5	—	ns	—
CSS8	SPI*n*_DI Hold Time	$T_{SPIXKL2}$	5	—	ns	—
CSS9	SPI*n*_DO Output Delay	$T_{SPKHOV2}$	—	17	ns	—

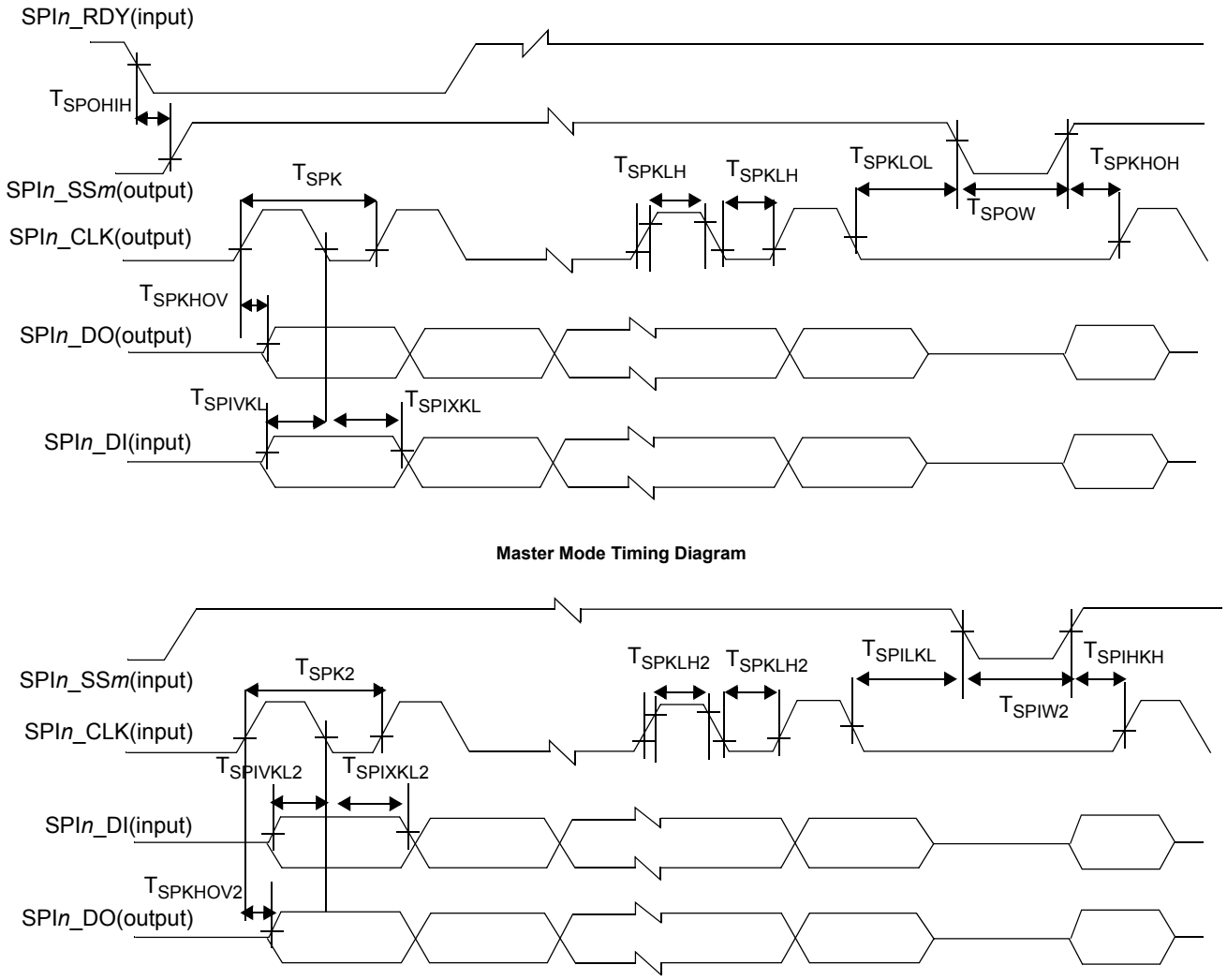


Figure 6. CSPI Timing Diagram

3.6.2 IO electrical characteristics

3.6.2.1 LVCMOS pads

This section describes the electrical specifications for the LVCMOS interface.

3.6.2.1.1 AC characteristics conditions

AC electrical characteristics are not applicable for output open drain pulldown driver.

This table provides the AC electical characteristics at 1.8 V.

Table 28. AC electrical characteristics (1.8 V voltage mode)

Parameter	Symbol	Drive strength (dse2,des1,dse0)	Slew rate	Test conditions	Min	Max	Unit	Notes
IO output transition time , (Rise/Fall)	T_{TLH} T_{THL}	High (011)	Slow	15 pF capacitive load on pad		1.89/1.84	ns	—
			Fast			1.97/2.20		—
		Low (100)	Slow			2.99/2.96		—
			fast			2.44/2.58		—
		Medium (101)	Slow			2.56/2.42		—
			fast			1.84/1.96		—
		Max (111)	Slow			1.82/1.67		—
			fast			1.13/1.24		—

Note:
1. Refer AFD4400 Reference Manual for drive strength setting (dse2,dse1 and dse0) configuration register.

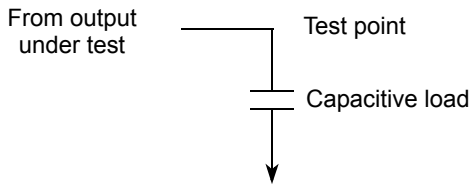
This table provides the AC electrical characteristics at 3.3 V.

Table 29. AC electrical characteristics (3.3 V voltage mode)

Parameter	Symbol	Drive strength (dse2,des1,dse0)	Slew rate	Test conditions	Min	Max	Unit	Notes
IO output transition time , (Rise/Fall)	T_{TLH} T_{THL}	High (011)	Slow	15 pF capacitive load on pad		3.00/3.16	ns	—
			Fast			2.17/2.73		—
		Low (100)	Slow			3.37/3.58		—
			fast			2.64/3.07		—
		Medium (101)	Slow			2.98/3.00		—
			fast			2.04/2.37		—
		Max (111)	Slow			2.19/2.18		—
			fast			1.28/1.57		—

Note:
1. Refer AFD4400 Reference Manual for drive strength setting (dse2,dse1 and dse0) configuration register.

This figure provides the pad load circuit.



Capacitive load includes package, die and equivalent lumped load, external to pad

Figure 7. Pad load circuit

The output pad propagation and transition time waveform is shown below in the figure.

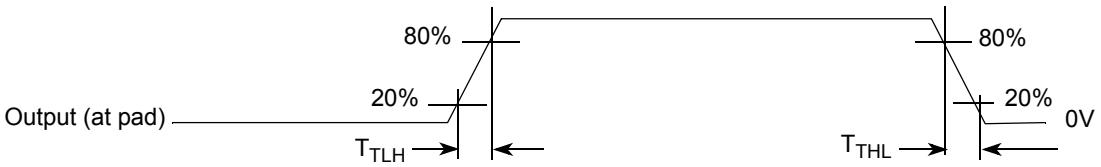


Figure 8. Output pad transition time waveform

3.6.2.2 LVDS pads

3.6.2.2.1 AC characteristics conditions

The AC operating characteristics are provided in Table 30 for LVDS pads.

Table 30. AC electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	Notes
Tskd	Differential pulse skew	Resistive load = 100 Ω between padp and padn, capacitive load = 2 pF	0.01	—	0.25	ns	
Ttlh	Output transition time low to high		0.12	—	0.58		1,2
Tthl	Output transition time high to low		0.10	—	0.73		
F	Operating frequency	—	—	125	600	MHz	—
Vos	Offset voltage imbalance	—	—	—	150	mV	—

Note:
1. TIA/EIA-644-A Spec, section 4.1.4.
2. Measurement levels are 20–80% from output voltage

This figure shows differential LVDS driver propagation delay and transition time waveforms.

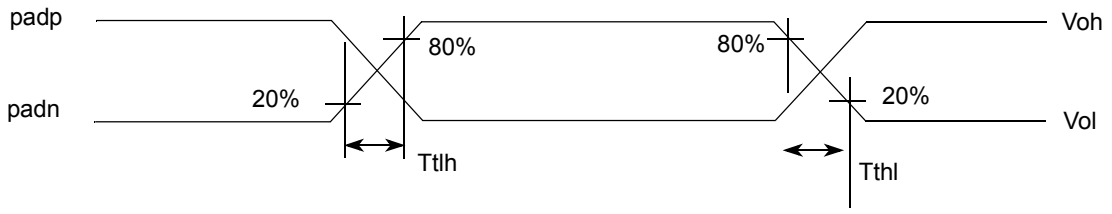


Figure 9. Differential LVDS driver transition time waveforms

3.6.2.3 DDR IOs

This section provides AC electrical specifications for the DDR IOs.

3.6.2.3.1 AC electrical characteristics

This table provides the AC characteristics for the DDR IO.

Table 31. DDR AC electrical characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Single output slew rate	tsr	0.4	2	V/ns	—
Skew between pad rise/fall asymmetry + skew caused by simultaneous switching noise (SSN)	tskd	—	70	ps	—

This figure shows the AC pad load circuit.

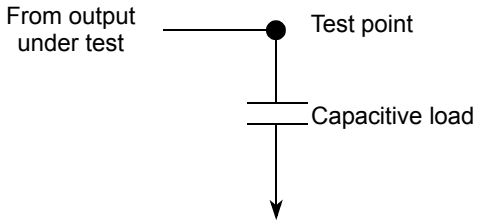


Figure 10. Pad load circuit

This figure shows output pad propagation and transition time waveform.

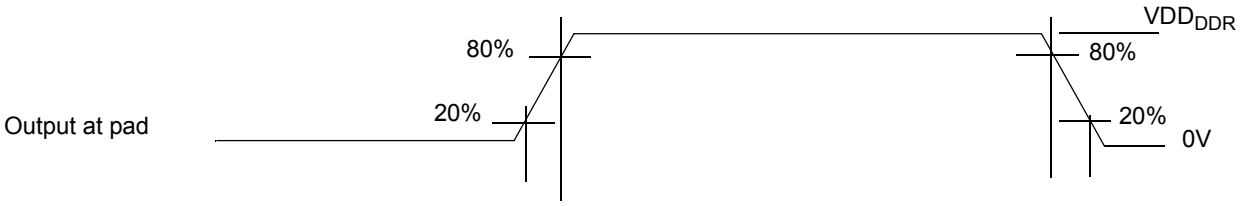


Figure 11. Output pad transition time waveform

3.6.3 DDR controller

This table provides the timing parameters for DDR3 controller.

Table 32. DDR3 timing parameter

ID	Parameter	Symbol	Min	Max	Unit	Note
DDR0	Clock Period	T_{MMKW}	2	—	ns	—
DDR1	CK clock high-level width	T_{MMKH}	0.47	0.53	T_{MMKW}	—
DDR2	CK clock low-level width	T_{MMKL}	0.47	0.53	T_{MMKW}	—
DDR4	CS, RAS, CAS, CKE, WE, ODT setup time	T_{MMKHOV}	440	—	ps	—
DDR5	CS, RAS, CAS, CKE, WE, ODT hold time	T_{MMKHOX}	315	—	ps	—
DDR6	Address output setup time	$T_{MMKHOV2}$	440	—	ps	—
DDR7	Address output hold time	$T_{MMKHOX2}$	315	—	ps	—

Note:

1. All measurements are in reference to Vref level.
2. Measurements are done using balanced load and 25 Ω resistor from outputs to VDD_REF.

This table provides the write timing parameters for DDR3 write cycle.

Table 33. DDR3 write cycle

ID	Parameter	Symbol	Min	Max	Unit	Note
DDR17	DQ and DQM setup time to DQS (differential strobe)	T_{MMDHDV}	215	—	ps	—
DDR18	DQ and DQM hold time to DQS (differential strobe)	T_{MMDHDX}	215	—	ps	—
DDR21	DQS latching rising transitions to associated clock edges	T_{MMKHDH}	–0.25	+0.25	T_{MMKW}	—
DDR22	DQS high level width	T_{MMDQSH}	0.45	0.55	T_{MMKW}	—
DDR23	DQS low level width	T_{MMDQSL}	0.45	0.55	T_{MMKW}	—

Note:

1. To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.
2. All measurements are in reference to Vref level.
3. Measurements are done using balanced load and 25 Ω resistor from outputs to VDD_REF.

This table provides the timing parameters for DDR3 read cycle.

Table 34. DDR3 read cycle

ID	Parameters	Symbol	Min	Max	Unit	Note
DDR27	Tolerated skew for DDR_DQS - DDR_DQ	$T_{MMDSKEW}$	-150	150	ps	—

Note:

1. To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.
2. All measurements are in reference to Vref level.
3. Measurements are done using balanced load and 25 Ω resistor from outputs to VDD_REF.

This figure shows the basic timing parameters of DDR3.

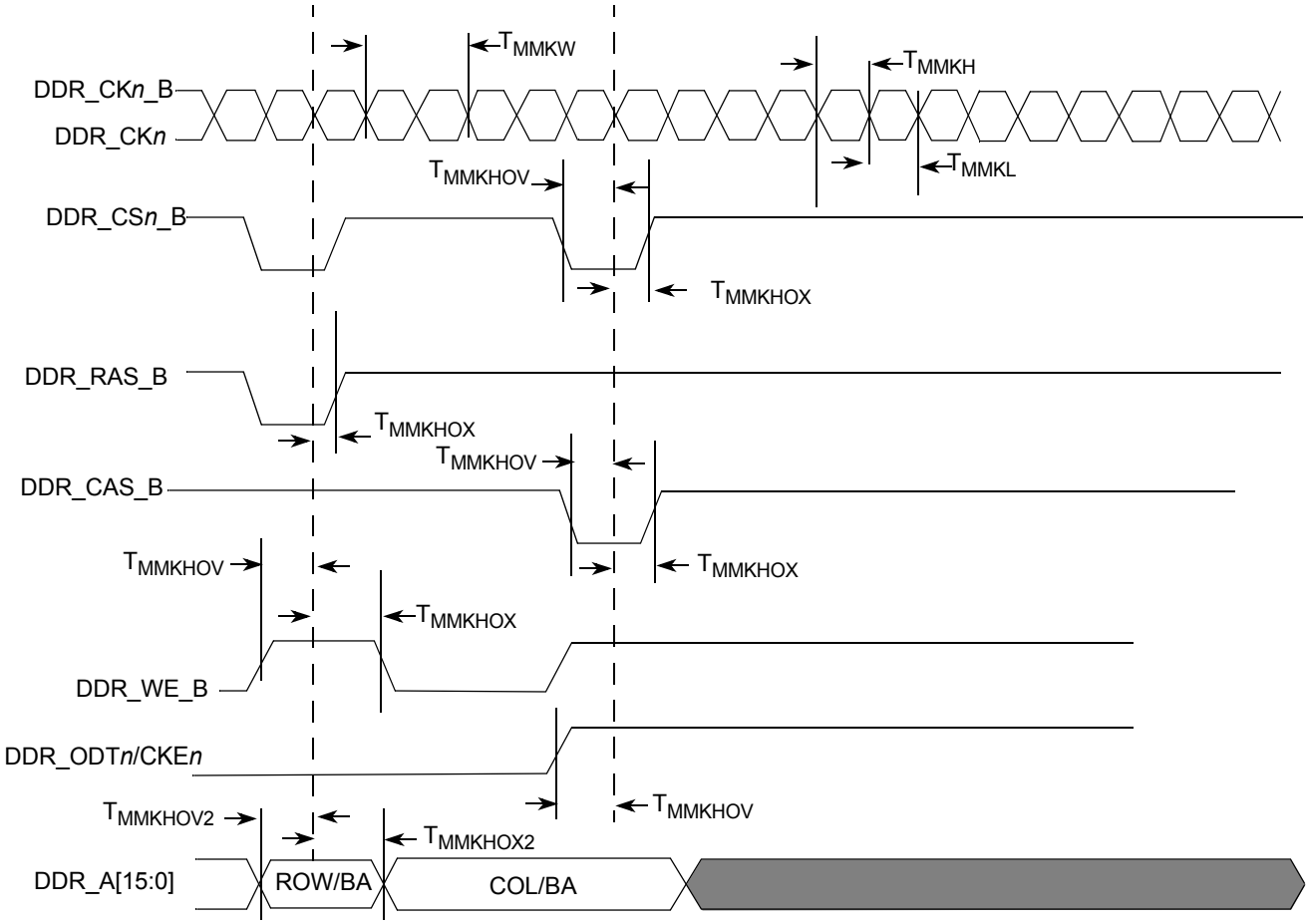


Figure 12. DDR3 command and address parameters

This figure shows the write timing parameters.

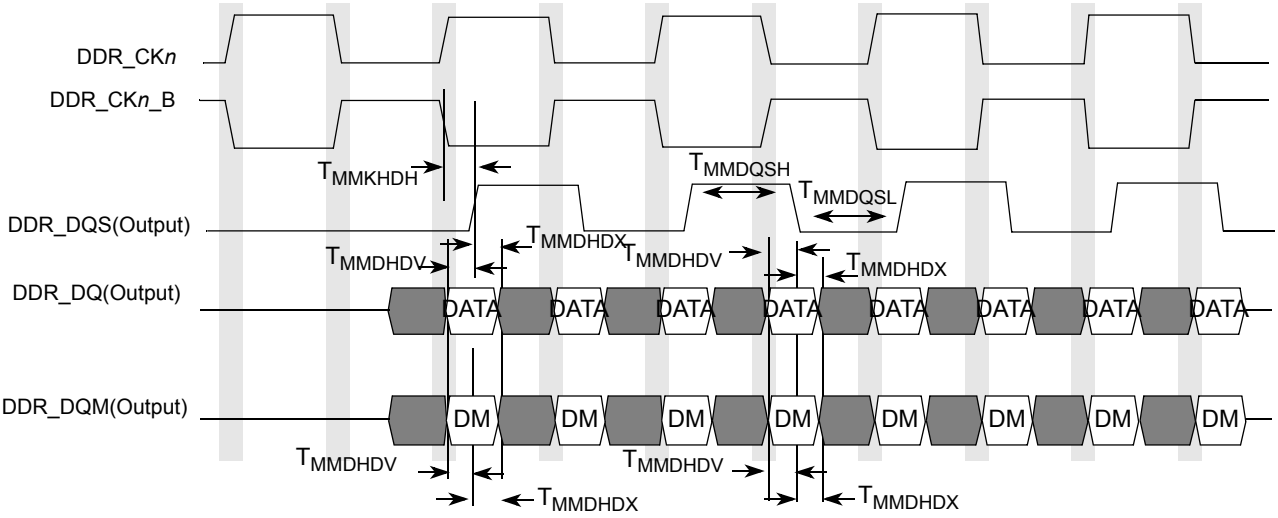


Figure 13. DDR3 write cycle

This figure shows the read timing parameters.

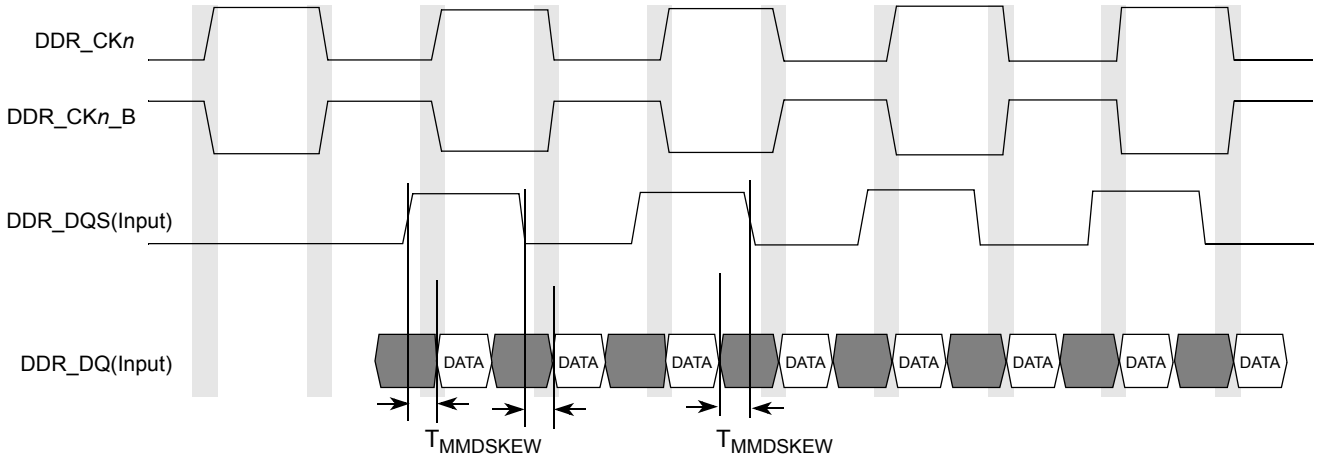


Figure 14. DDR3 read cycle

3.6.4 Digital phase lock loop (DPLL)

This table lists the DDR PLL, System PLL and TbGen PLL electrical characteristics.

Table 35. DPLL electrical characteristics

Parameter	Min	Max	Unit	Note
Reference clock frequency range	66.67	166	MHz	—
Output clock frequency range	491.52	2000	MHz	1
PLL lock time	—	100	μs	—
Period jitter (peak-to-peak) for PLL output	—	±(40 + clock out period × 1%)	ps	—
Phase jitter (peak-to-peak) for PLL output	—	±(75 + ref_clock_period × 1%)	ps	—

Note:
1. The maximum PLL output frequency should be programmed based on the maximum operating limit.

3.6.5 Ethernet: Enhanced three-speed ethernet (eTSEC)

This section provides the AC electrical characteristics for the enhanced three-speed Ethernet 10/100/1000 controller and MII management interface.

3.6.5.1 MII AC timing specifications

This section describes the MII transmit and receive AC timing specifications.

This table provides the MII transmit AC timing specifications.

Table 36. MII transmit AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Note
TSEC1_TX_CLK clock period 10 Mbps	t_{MTX}	399.96	400	400.04	ns	—
TSEC1_TX_CLK clock period 100 Mbps	t_{MTX}	39.996	40	40.004	ns	—
TSEC1_TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%	—
TSEC1_TX_CLK to MII data TSEC1_TXD[3:0], TSEC1_TX_ER, TSEC1_TX_EN delay	t_{MTKHDX}	0	—	25	ns	—
TSEC1_TX_CLK data clock rise (20%–80%)	t_{MTXR}	1.0	—	4.0	ns	—
TSEC1_TX_CLK data clock fall (80%–20%)	t_{MTXF}	1.0	—	4.0	ns	—

This figure shows the MII transmit AC timing diagram.

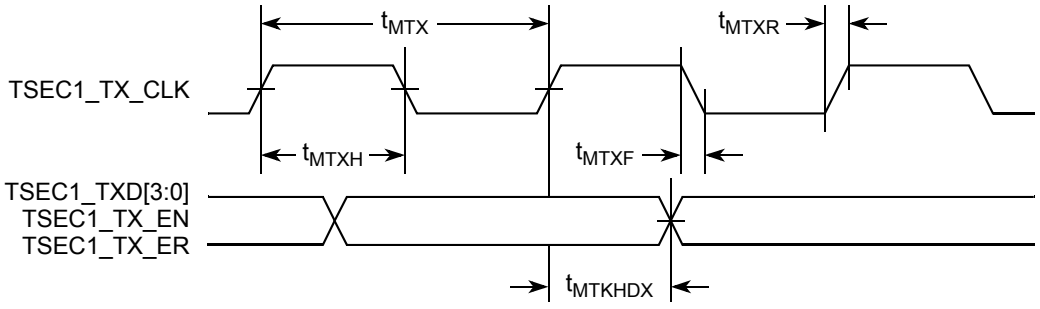


Figure 15. MII transmit AC timing diagram

This table provides the MII receive AC timing specifications.

Table 37. MII receive AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Note
TSEC1_RX_CLK clock period 10 Mbps	t_{MRX}	399.96	400	400.04	ns	—
TSEC1_RX_CLK clock period 100 Mbps	t_{MRX}	39.996	40	40.004	ns	—
TSEC1_RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%	—
TSEC1_RXD[3:0], TSEC1_RX_DV, TSEC1_RX_ER setup time to TSEC1_RX_CLK	t_{MRDVKH}	10.0	—	—	ns	—
TSEC1_RXD[3:0], TSEC1_RX_DV, TSEC1_RX_ER hold time to TSEC1_RX_CLK	t_{MRDXKH}	10.0	—	—	ns	—

Note: The frequency of TSEC1_RX_CLK (input) should not exceed the frequency of TSEC1_TX_CLK (input) by more than 300 ppm.

This figure shows the MII receive AC timing diagram.

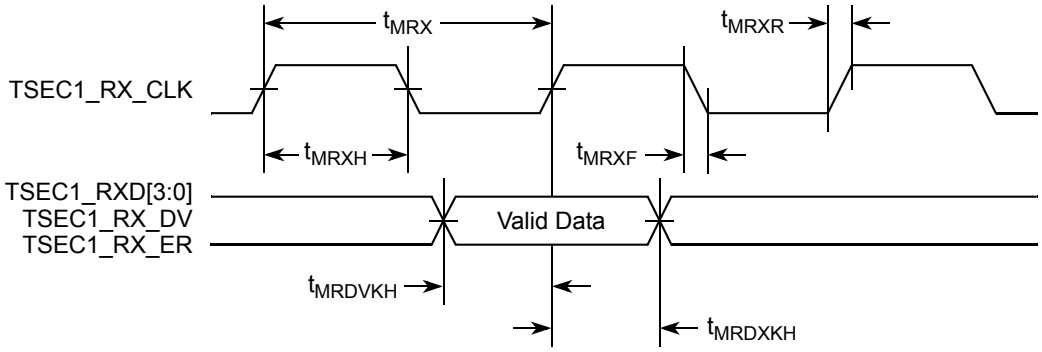


Figure 16. MII receive AC timing diagram

3.6.5.2 RGMII AC timing specifications

This table presents the RGMII AC timing specifications.

Table 38. RGMII AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	–770	0	950	ps	5
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.3	—	2.6	ns	2

Table 38. RGMII AC timing specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3,4
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45	50	55	%	—

Note:

2. This implies that the PC board design requires clocks to be routed such that an additional trace delay greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their chip. If so, additional PCB delay is probably not needed.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. The frequency of TSEC1_RX_CLK (input) should not exceed the frequency of TSEC1_GTX_CLK (output) by more than 300 ppm.

This figure shows the RGMII AC timing and multiplexing diagrams.

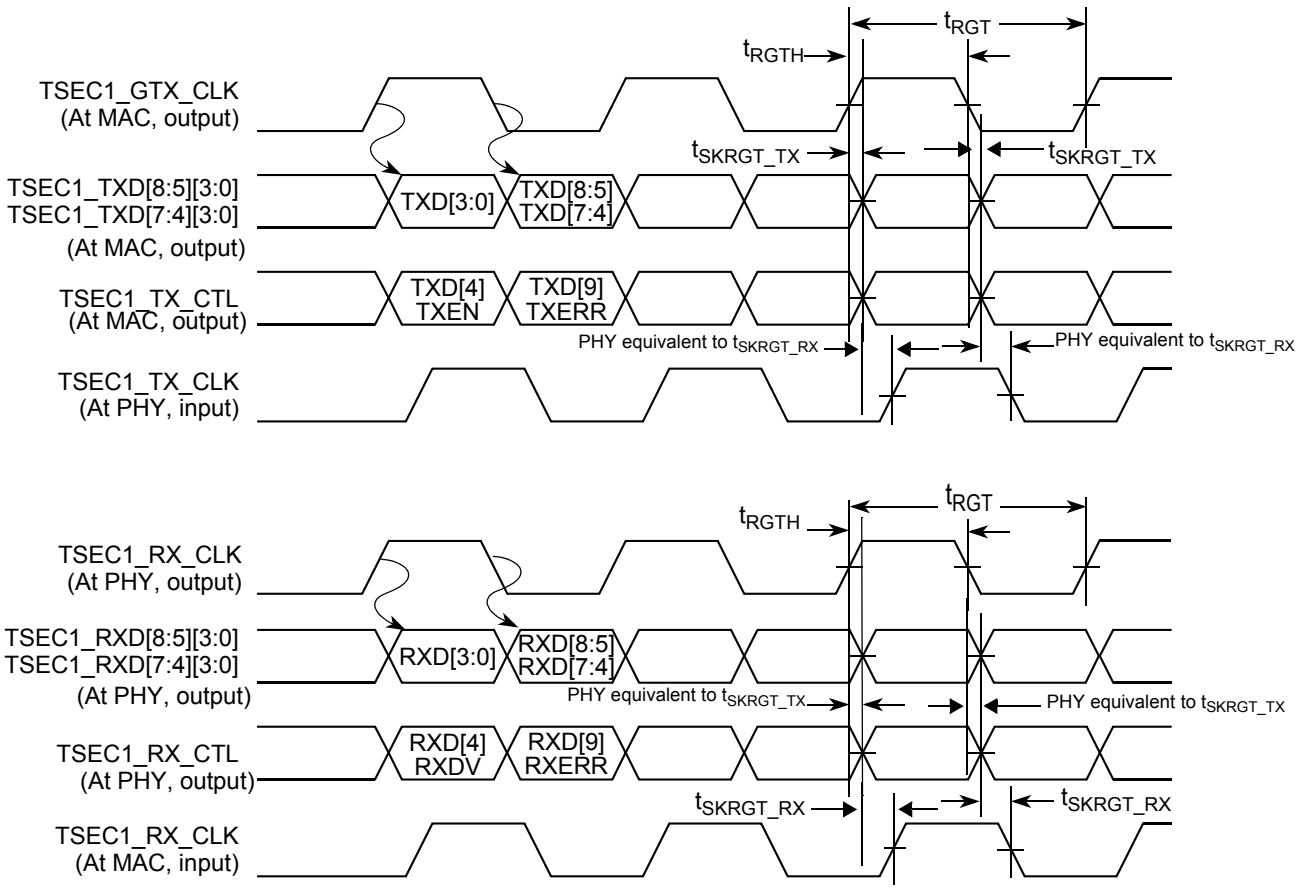


Figure 17. RGMII timing and multiplexing diagrams

WARNING

Freescale guarantees timings generated from the MAC. Board designers must ensure delays needed at the PHY or the MAC.

3.6.5.3 RMII AC timing specifications

In RMII mode, the reference clock should be fed to TSEC1_TX_CLK. This section describes the RMII transmit and receive AC timing specifications.

This table lists the RMII transmit AC timing specifications.

Table 39. RMII transmit AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Typ
TSEC1_TX_CLK clock period	t_{RMT}	—	20.0	—	ns	—
TSEC1_TX_CLK duty cycle	t_{RMTH}	35	—	65	%	—
TSEC1_TX_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps	—
TSEC1_TX_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	2.0	—	10.0	ns	—

This figure shows the RMII transmit AC timing diagram.

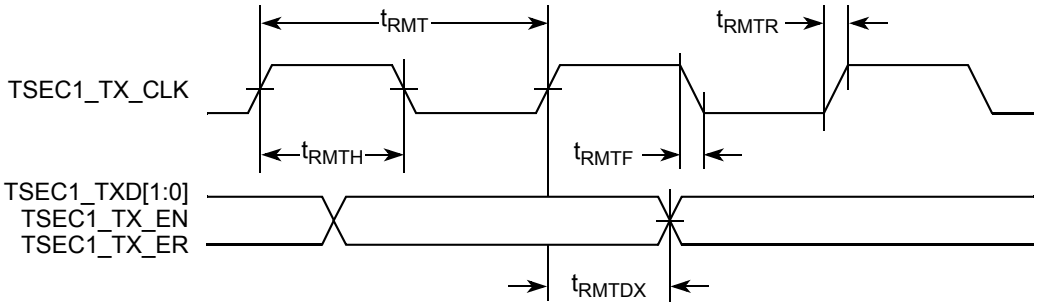


Figure 18. RMII transmit AC timing diagram

This table lists the RMII receive AC timing specifications.

Table 40. RMII receive AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Note
TSEC1_TX_CLK clock period	t_{RMR}	—	20.0	—	ns	—
TSEC1_TX_CLK duty cycle	t_{RMRH}	35	—	65	%	—
TSEC1_TX_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps	—
RXD[1:0], CRS_DV, RX_ER set-up time to TSEC1_TX_CLK rising edge	t_{RMRDV}	4.0	—	—	ns	—
RXD[1:0], CRS_DV, RX_ER hold time to TSEC1_TX_CLK rising edge	t_{RMRDX}	2.0	—	—	ns	—

This figure shows the RMII receive AC timing diagram.

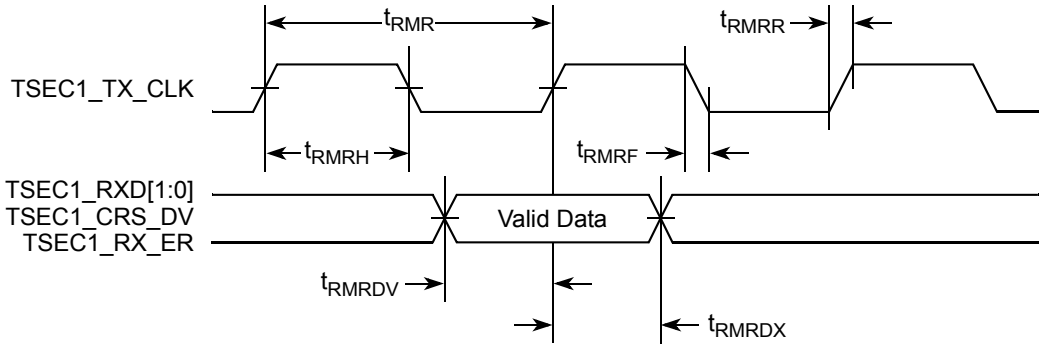


Figure 19. RMII receive AC timing diagram

3.6.5.4 MII management AC timing specifications

This table provides the MII management AC timing specifications.

Table 41. MII management AC timing specifications

At recommended operating conditions with VDD_{GPIO} = 3.3 V ± 5%.

Parameter	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	—	2.5	MHz	1
MDC period	t_{MDC}	400	—	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	$(8 \times t_{axi}) - 3$	—	$(8 \times t_{axi}) + 3$	ns	2, 3
MDIO to MDC setup time	t_{MDDVKH}	15	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—

Notes:

1. This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock MDC).
2. This parameter is dependent on the platform (AXI) clock frequency (f_{axi}). The delay is equal to 8 platform clock periods ±3 ns. For example, with a platform clock of 307.2 MHz, the min/max delay is 26 ns ± 3 ns.
3. t_{axi} is the platform AXI bus clock.

The figure below shows the MII management interface timing diagram.

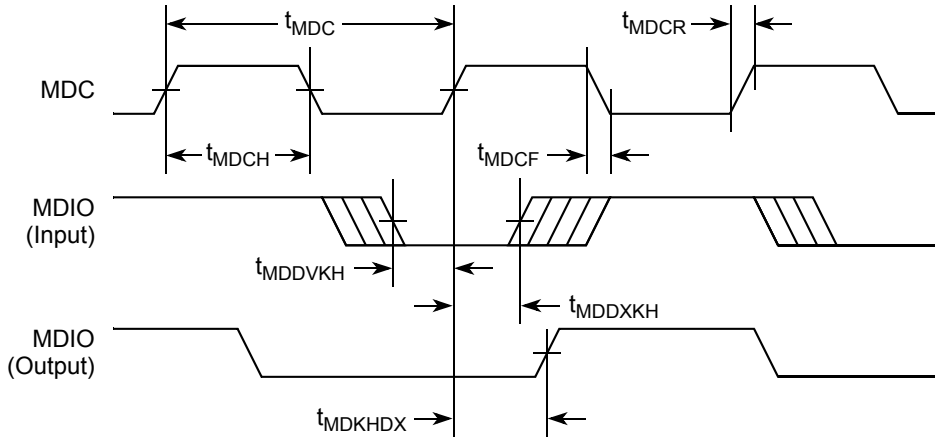


Figure 20. MII management interface timing diagram

3.6.5.5 Ethernet controller IEEE Std 1588 AC timing specifications

This table provides the IEEE 1588 AC timing specifications.

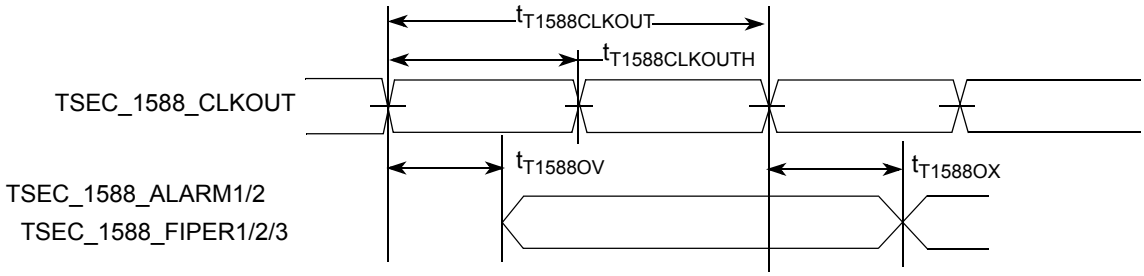
Table 42. Ethernet controller IEEE 1588 AC timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Clock period	$t_{T1588CLK}$	3.3	—	$T_{RX_CLK} \times 7$	ns	1, 3
Duty cycle	$t_{T1588CLKH}$/ $t_{T1588CLK}$	40	50	60	%	2
Peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time TSEC_1588_CLKIN (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—
Fall time TSEC_1588_CLKIN (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
TSEC_1588_CLKOUT clock period	$t_{T1588CLKOUT}$	$2 \times t_{T1588CLK}$	—	—	ns	4
TSEC_1588_CLKOUT duty cycle	$t_{T1588CLKOUTH}$/ $t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_ALARM*n*, TSEC_1588_FIPER*n* hold time	$t_{T1588OX}$	0.5	—	—	ns	5
TSEC_1588_ALARM*n*, TSEC_1588_FIPER*n* delay	$t_{T1588OV}$	—	—	3.0	ns	—
TSEC_1588_TRIG*n* pulse width	$t_{T1588TRIGH}$	$2 \times t_{T1588CLK_MAX}$	—	—	ns	3

Notes:

1. T_{RX_CLK} is the maximum clock period of TSEC receiving clock selected by TMR_CTRL[CKSEL]. See the *AFD4400 Reference Manual* for a description of TMR_CTRL registers.
2. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the *AFD4400 Reference Manual* for a description of TMR_CTRL registers.
3. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ is 2800, 280, and 56 ns, respectively.
4. For 1588, there are three input clock sources: TSEC_1588_CLKIN, RTC and AXI clock. When using TSEC_1588_CLKIN, the minimum clock period is $2 \times t_{T1588CLK}$.
5. The parameter has been characterized at highest slew rate and drive strength.

This figure shows the data and command output AC timing diagram.



Note: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is counted starting at the falling edge.

Figure 21. Ethernet controller IEEE 1588 output AC timing

This figure shows the data and command input AC timing diagram.

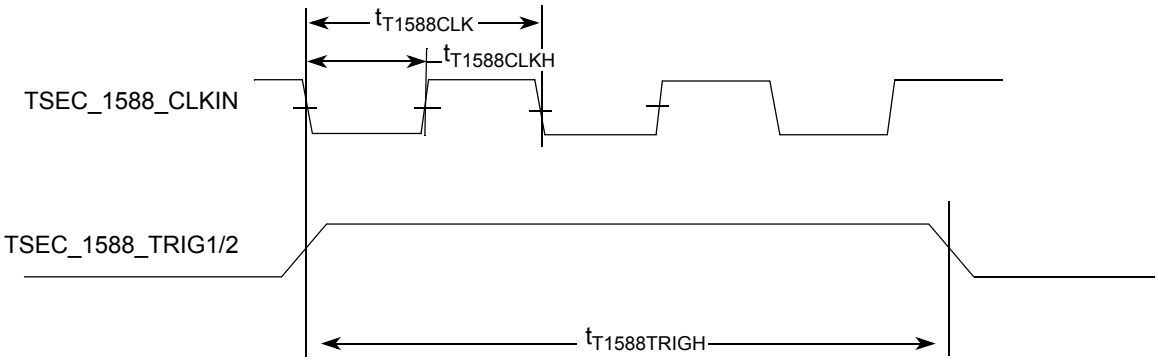


Figure 22. Ethernet controller IEEE 1588 input AC timing

3.6.5.6 SGMII interface electrical characteristics

For SGMII interface electrical characteristics, see Section 3.6.11, “SerDes”.

3.6.6 Fusebox

This section describes the fusebox electrical characteristics.

The table below shows the fusebox supply current parameters. These parameters are validated through characterization.

Table 43. Fusebox supply current parameters

Parameter	Symbol	Min	Typ	Max	Unit	Note
The V_{EFUSE_PGM} current flow when not programming	I_{VPGM_UNPROG}	0.35	0.41	1.76	mA	—
The V_{EFUSE_PGM} current flow during programming	I_{VPGM_PROG}	87.2	87.3	96.09	mA	—
Programming time	T_{PGM}	11	12	13	µs	—

3.6.7 JTAG

This section describes the AC electrical specifications for the IEEE Std 1149.1™/1149.6™ (JTAG) interface. This section applies to both the ARM and VSP JTAG ports.

NOTE

The VSP JTAG cannot be used for boundary scan (BSR). The BSR TAP is connected to main JTAG port (ARM JTAG).

3.6.7.1 JTAG AC timing specifications

This table provides the JTAG AC timing specifications as defined in Figure 23 through Figure 26.

Table 44. JTAG AC timing specifications

For recommended operating conditions see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	—	20	MHz	—
JTAG external clock cycle time	t_{JTG}	50	—	ns	—
JTAG external clock pulse width	t_{JTKHKL}	25	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} and t_{JTGF}	—	2	ns	—
JTAG_TRST_B/JTAG_VSP_TRST_B assert time	t_{TRST}	125	—	ns	1
Input setup times	t_{JTDVKH}	4	—	ns	—
Input hold times	t_{JTDXKH}	21	—	ns	—
Output valid times	t_{JTKLDV}	—	25	ns	2
Output hold times	t_{JTKLDX}	0	—	ns	2
JTAG external clock to output high impedance	t_{JTKLDZ}	4	10	ns	—

Note:

1. JTAG_TRST_B/JTAG_VSP_TRST_B is an asynchronous level sensitive signal.
2. All the output timings are measured from the midpoint voltage of the falling/rising edge of JTAG clock to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

This figure shows the AC test load for TDO and the boundary-scan outputs.

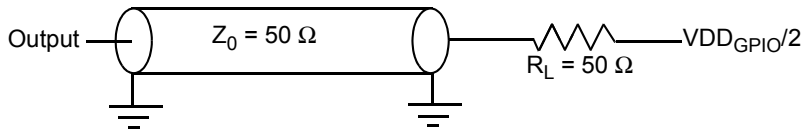


Figure 23. AC test load for the JTAG interface

This figure provides the JTAG clock input timing diagram.

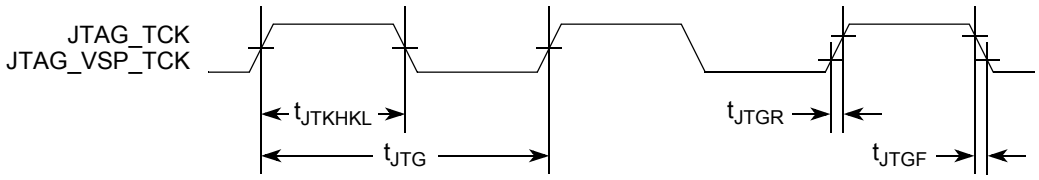


Figure 24. JTAG clock input timing diagram

This figure provides the TRST_B timing diagram.

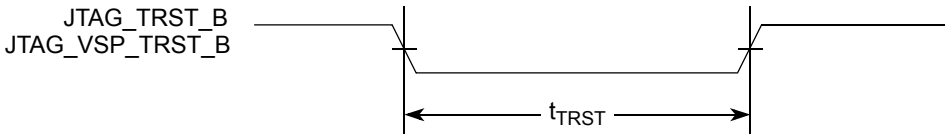


Figure 25. TRST_B timing diagram

This figure provides the boundary-scan timing diagram.

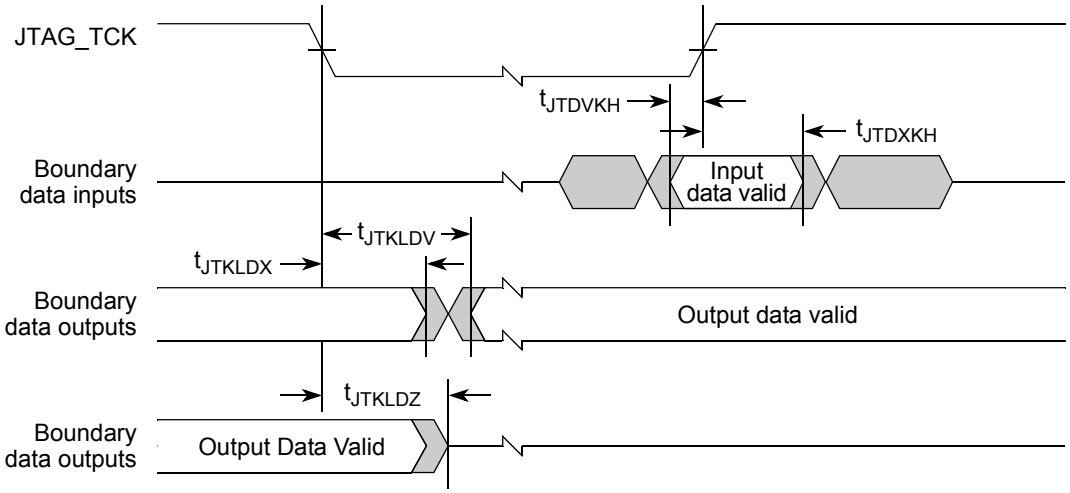


Figure 26. Boundary-scan timing diagram

3.6.8 GPIO signals

This section describes the AC electrical specifications for the GPIO pins.

3.6.8.1 GPIO AC timing specifications

This table provides the GPIO input and output AC timing specifications.

Table 45. GPIO pin input AC timing specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Unit	Notes
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	1

Note:

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} to ensure proper operation.

This figure provides the AC test load for the GPIO pin.

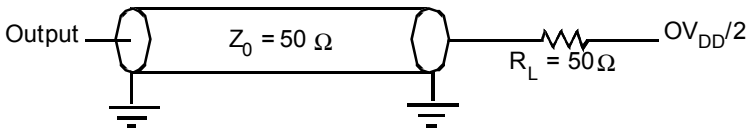


Figure 27. GPIO pin AC test load

3.6.9 I^2C

This section describes the electrical information of the I^2C interface.

3.6.9.1 I^2C module timing

This table provides the timing characteristics for the I^2C module.

Table 46. I^2C module timing characteristics

ID	Parameter	Symbol	Standard Mode		Fast Mode		Unit	Note
			Min	Max	Min	Max		
IC0	I2C*n*_SCL frequency	f_{I2C}	—	100	—	400	KHz	—
IC1	I2C*n*_SCL cycle time	t_{I2C}	10	—	2.5	—	µs	—
IC6	LOW Period of the I2C*n*_SCL Clock	t_{I2CL}	4.7	—	1.3	—	µs	—
IC5	HIGH Period of I2C*n*_SCL Clock	t_{I2CH}	4.0	—	0.6	—	µs	—
IC2	Hold time (repeated) START condition	t_{I2SXKL}	4.0	—	0.6	—	µs	—
IC3	Set-up time for STOP condition	t_{I2PVKH}	4.0	—	0.6	—	µs	—
IC4	Data hold time	t_{I2DXKL}	0	3.45	0	0.9	µs	1,2

Table 46. I²C module timing characteristics (continued)

ID	Parameter	Symbol	Standard Mode		Fast Mode		Unit	Note
			Min	Max	Min	Max		
IC8	Data set-up time	t_{I2DVKH}	0.25	—	0.1	—	µs	3
IC7	Set-up time for a repeated START condition	t_{I2DLKH}	4.7	—	0.6	—	µs	—
IC9	Bus free time between a STOP and START condition	t_{I2KHDX}	4.7	—	1.3	—	µs	—

Note:

1. A device must internally provide a hold time of at least 300 ns for I2C*n*_SDA signal in order to bridge the undefined region of the falling edge of I2C*n*_SCL. The "*n*" is the instance number of the I2C module.
2. The maximum hold time has only to be met if the device does not stretch the LOW period (ID # IC6) of the I2C*n*_SCL signal.
3. Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (IC8) of 250 ns must be met. This will automatically be the case if the device does not stretch the LOW period of the I2C*n*_SCL. If such a device does stretch the LOW period of the I2C*n*_SCL signal, it must output the next data bit to the I2C*n*_SDA line (IO max rise time + data_setup_time(IC8) time (according to the Standard-mode I2C-bus specification) before the I2C*n*_SCL line is released.
4. C_b = total capacitance of one bus line in pF. Assumed to be ~400 pF (max).

This figure below depicts the timing of I²C module.

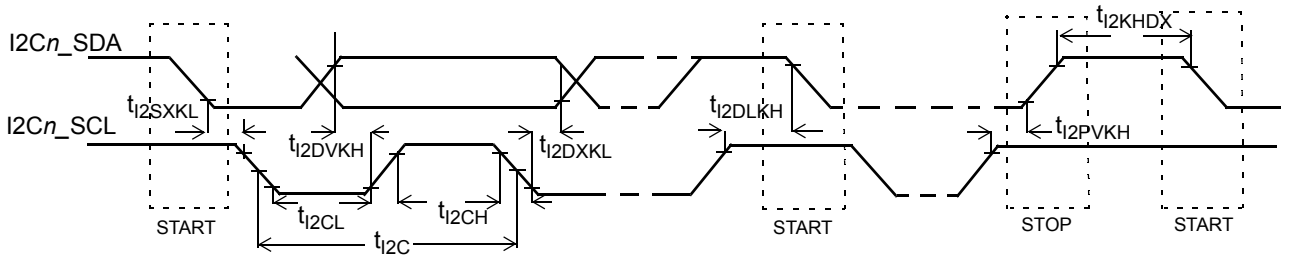


Figure 28. I²C bus timing

3.6.10 Quad-SPI

This table provides Quad-SPI timing characteristics.

Table 47. Quad-SPI module timing characteristics

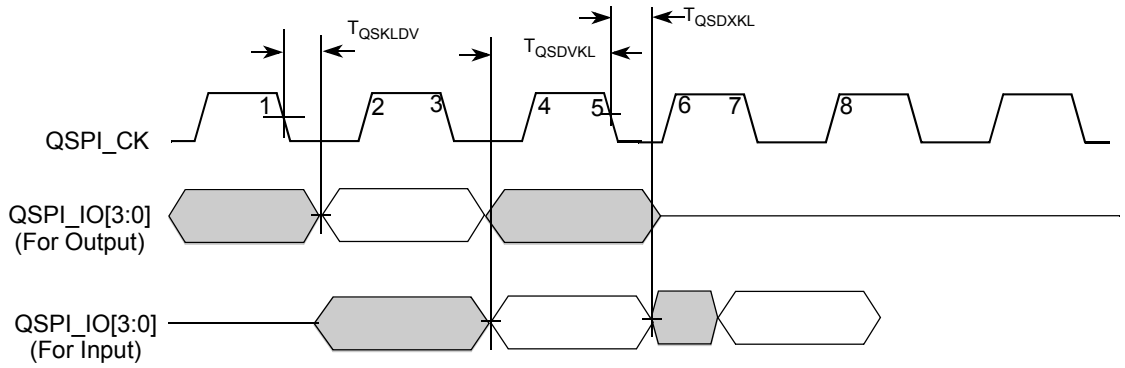
Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Frequency	f_{QSK}	—	—	52	Mhz	—
Clock to Q delay	T_{QSKLDV}	—	—	5.0	ns	—
Setup time for incoming data	T_{QSDVKL}	10.5	—	—	ns	—

Table 47. Quad-SPI module timing characteristics (continued)

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Hold time requirement for incoming data	T_{QSDXKL}	1.0	—	—	ns	—

Note:
1. All data are based on a negative edge data launch from AFD4400 and a negative edge data capture as shown in the timing diagrams.
2. Timings correspond to QSPI_SMPR = 0x0000_000x.
3. A negative value of hold is an indication of pad delay on the clock pad (delay between the edge capturing data inside device and the edge appearing at the pin).
4. 15 pF load has been assumed on the pads.

The figure below depicts Quad-SPI timing.



1. Last address out
2. Address captured at flash
3. Data out from Flash
4. This is SPI protocol defined Ideal Data Capture edge.The capture edge can be programmed as shown in 5,6,7,8.
5. Delayed data captured edge with QSPI_SMPR=0000_000x
6. Delayed data captured edge with QSPI_SMPR=0000_002x
7. Delayed data captured edge with QSPI_SMPR=0000_004x
8. Delayed data captured edge with QSPI_SMPR=0000_006x

Figure 29. Quad-SPI input timing

3.6.11 SerDes

The following subsections define the AC-level specifications for the CPRI, SGMII and JESD204B data lines.

3.6.11.1 Signal terms definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines the terms that are used in the description and specification of differential signals.

This figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. This figure shows the waveform for either a transmitter output (SD_TX*n*_P and SD_TX*n*_N) or a receiver input (SD_RX*n*_P and SD_RX*n*_N). Each signal swings between A volts and B volts where A > B.

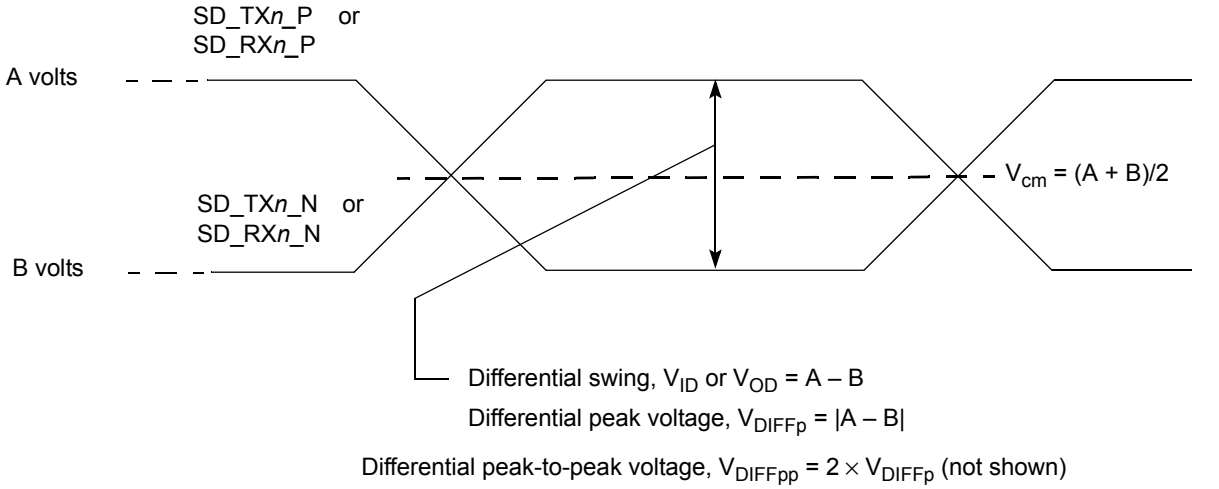


Figure 30. Differential voltage definitions for transmitter or receiver

Using this waveform, the definitions are as shown in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing — The transmitter output signals and the receiver input signals SD_TX*n*, SD_TX*n*_B, SD_RX*n,* and SD_RX*n*_B each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's single-ended swing.

Differential Output Voltage, V_{OD} (or **Differential Output Swing**)

The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SD_TXn} - V_{SD_TXn_B}$. The V_{OD} value can be either positive or negative.

Differential Input Voltage, V_{ID} (or **Differential Input Swing**)

The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SD_RXn} - V_{SD_RXn_B}$. The V_{ID} value can be either positive or negative.

Differential Peak Voltage, V_{DIFFp}

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, $V_{DIFFp} = |A - B|$ volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice the differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-to-peak voltage can also be calculated as $V_{TX\text{-}DIFFp-p} = 2 \times |V_{OD}|$.

Differential Waveform

The differential waveform is constructed by subtracting the inverting signal (SD_TX*n*_B, for example) from the non-inverting signal (SD_TX*n*_B, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. See Figure 35 as an example for differential waveform.

Common Mode Voltage, V_{cm}

The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = (V_{SD_TXn} + V_{\overline{SD_TXn}}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and TD_B. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or TD_B) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV. In other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

3.6.11.2 SerDes reference clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes.

The following sections describe the SerDes reference clock requirements and provide application information.

3.6.11.2.1 SerDes reference clock receiver characteristics

This figure shows a receiver reference diagram of the SerDes reference clocks.

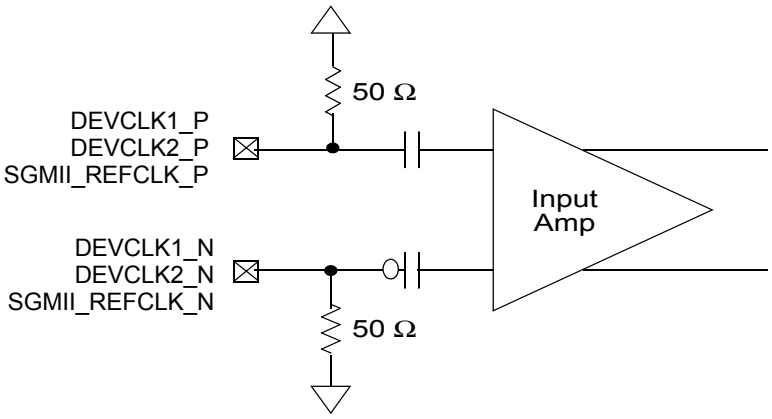


Figure 31. Receiver of SerDes reference clocks

The characteristics of the clock signals are as follows:

- The SerDes transceivers core power supply voltage requirements (VDD_{SDX}) are as specified in Section 3.1.2, "Recommended operating conditions."
- The SerDes reference clock receiver reference circuit structure is as follows:
  - Pins are internally AC-coupled differential inputs as shown in Figure 31. Each differential clock input has on-chip 50-Ω termination to SD*n*_XCOREVSS followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.

- The SerDes reference clock input can be either differential or single-ended. See the differential mode and single-ended mode descriptions below for detailed requirements.

- The maximum average current requirement also determines the common mode voltage range.
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V ÷ 50 = 8 mA) while the minimum common mode input level is 0.1 V above SD*n*_XCOREVSS. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the clock inputs cannot drive 50 Ω to SD*n*_XCOREVSS DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled off-chip.
- The input amplitude requirement is described in detail in the following sections.

3.6.11.2.2 DC-level requirement for SerDes reference clocks

The DC level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- Differential Mode
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-to-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For an external DC-coupled connection, as described in Section 3.6.11.2.1, "SerDes reference clock receiver characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. Figure 32 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

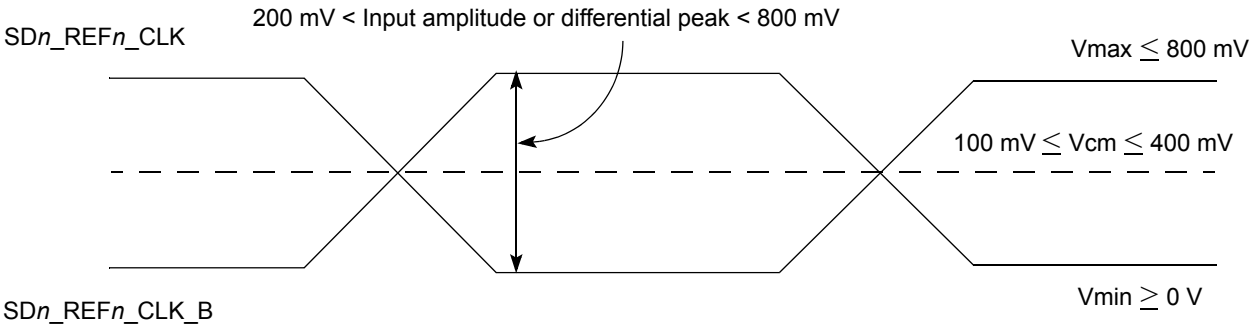


Figure 32. Differential reference clock input DC requirements (external DC-coupled)

  - For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different common mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SD*n*_XCOREVSS. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (SD*n*_XCOREVSS). Figure 33 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

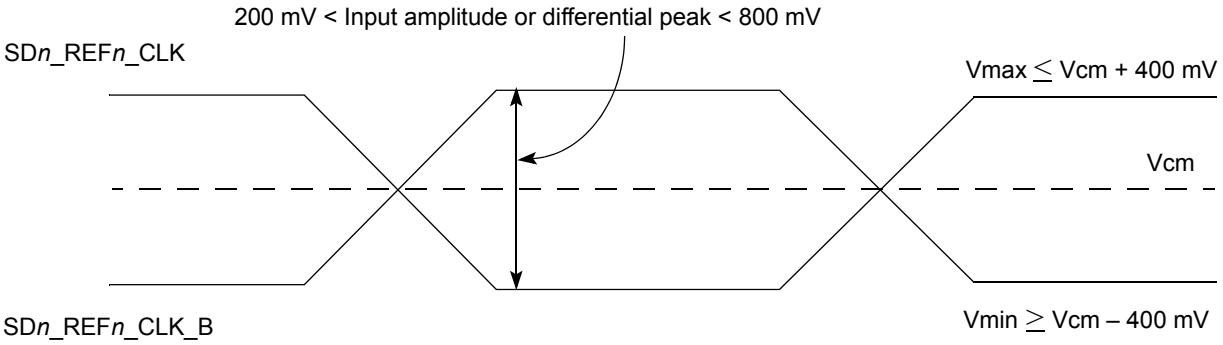


Figure 33. Differential reference clock input DC requirements (external AC-coupled)

- Single-Ended Mode
  - The reference clock can also be single-ended. The DEVCLK1_P/DEVCLK2_P/SGMII_REFCLK_P input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-to-peak (from V_{MIN} to V_{MAX}) with DEVCLK1_N/DEVCLK2_N/SGMII_REFCLK_N either left unconnected or tied to ground.
  - The DEVCLK1_P/DEVCLK2_P/SGMII_REFCLK_P input average voltage must be between 200 and 400 mV. Figure 34 shows the SerDes reference clock input requirement for single-ended signaling mode.
  - To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase (DEVCLK1_N/DEVCLK2_N/SGMII_REFCLK_N) through the same source impedance as the clock input (DEVCLK1_P/DEVCLK2_P/SGMII_REFCLK_P) in use.

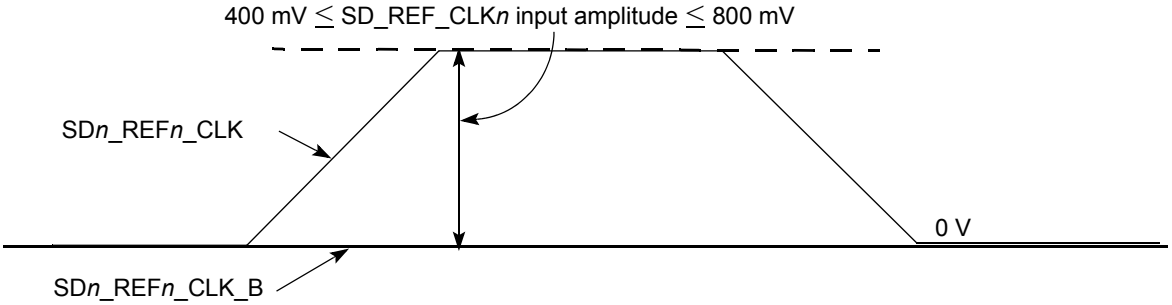


Figure 34. Single-ended reference clock input DC requirements

3.6.11.2.3 AC requirements of reference clock

The table below lists the AC requirements for SerDes reference clock SGMII_REFCLK_P/SGMII_REFCLK_N.

Table 48. SGMII_REFCLK_P/SGMIIREFCLK_N requirement

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SGMII_REFCLK_P/SGMIIREFCLK_N frequency range	f_{SGMII}	—	125	—	MHz	1
SGMII_REFCLK_P/SGMIIREFCLK_N clock frequency tolerance	t_{CLK_TOL}	–100	—	100	ppm	—
SGMII_REFCLK_P/SGMIIREFCLK_N reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	—
SGMII_REFCLK_P/SGMIIREFCLK_N max deterministic peak-to-peak jitter at 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	—

Table 48. SGMII_REFCLK_P/SGMIIREFCLK_N (continued)requirement

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SGMII_REFCLK_P/SGMIIREFCLK_N total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at refClk input)	t_{CLK_TJ}	—	—	86	ps	—
SGMII_REFCLK_P/SGMIIREFCLK_N rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	2
Differential input high voltage	V_{IH}	V_{CM}+200 mV	—	—	mV	3
Differential input low voltage	V_{IL}	—	—	V_{CM} –200 mV	mV	3
Rising edge rate (SGMII_REFCLK_P) to falling edge rate (SGMII_REFCLK_N) matching	Rise-Fall Matching	—	—	20	%	4, 5

Notes:
1. **Caution:** Only 125 have been tested. In-between values do not work correctly with the rest of the system.
2. Measured from –200 mV to +200 mV on the differential waveform (derived from SGMII_REFCLK_P minus SGMII_REFCLK_N). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 35.
3. Measurement taken from differential waveform
4. Measurement taken from single-ended waveform
5. Matching applies to rising edge for SGMII_REFCLK_P and falling edge rate for SGMII_REFCLK_N. It is measured using a 200 mV window centered on the median cross point where SGMII_REFCLK_P rising meets SGMII_REFCLK_N falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SGMII_REFCLK_P must be compared to the fall edge rate of SGMII_REFCLK_N, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 36.

This table lists the AC requirements for SerDes reference clock DEVCLK*n*_P/DEVCLK*n*_N.

Table 49. DEVCLK*n*_P/DEVCLK*n*_N input clock requirements

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Frequency range	t_{CLK_REF}	—	122.88	—	MHz	1
Clock frequency tolerance	t_{CLK_TOL}	–100	—	100	ppm	—
Reference clock duty cycle (measured at 1.6 V)	t_{CLK_DUTY}	45	50	55	%	—
Single side band noise at 1 KHz	t_{SSN_1K}	—	—	–85	dBC/Hz	—
Single side band noise at 10 KHz	t_{SSN_10K}	—	—	–108	dBC/Hz	—
Single side band noise at 100 KHz	t_{SSN_100K}	—	—	–128	dBC/Hz	—
Single side band noise at 1 MHz	t_{SSN_1M}	—	—	–138	dBC/Hz	—
Single side band noise at 10 MHz	t_{SSN_10M}	—	—	–138	dBC/Hz	—
Random jitter (1.2 MHz to 15 MHz)	t_{J_RANDOM}	—	—	0.8	ps	—

Table 49. DEVCLK*n*_P/DEVCLK*n*_N input clock requirements (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Total reference clock jitter at 10^{-12} BER (1.2 MHz to 15 MHz)	t_{J_TOTAL}	—	—	11	ps	—
Spurious noise (1.2 MHz to 15 MHz)	t_{J_NOISE}	—	—	–75	dBC	—
Jitter phase noise at -56 DBc	—	—	—	500	KHz	—

Notes:
1. **Caution:** Only 122.88 have been tested. In-between values do not work correctly with the rest of the system.

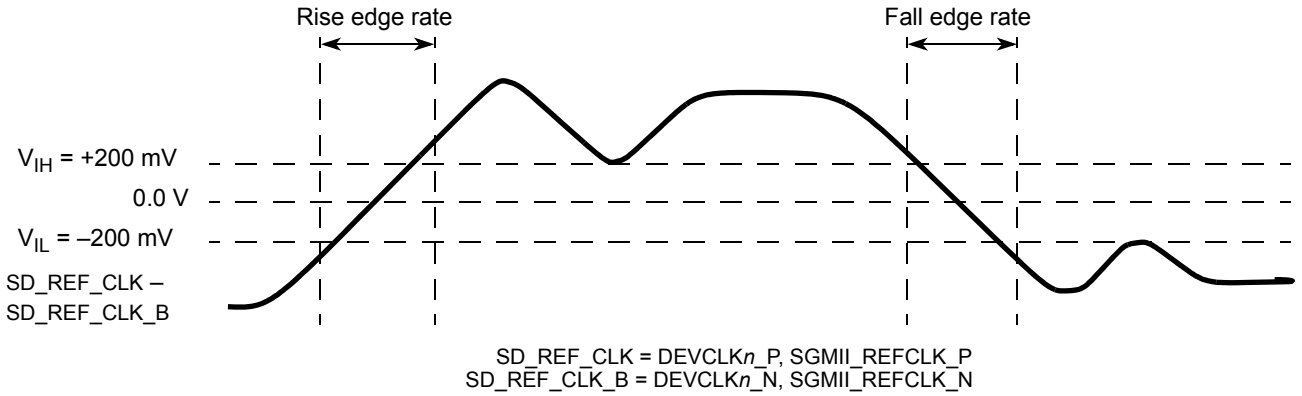


Figure 35. Differential measurement points for rise and fall time

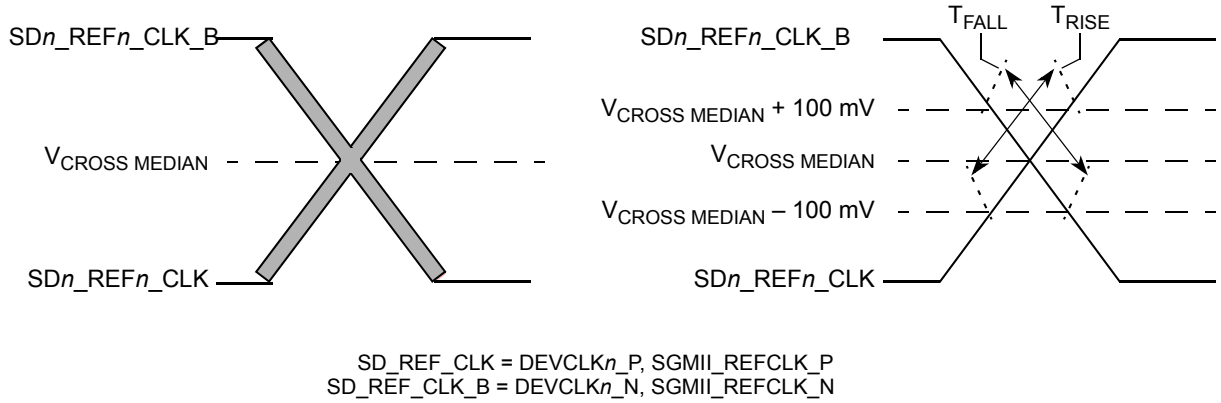


Figure 36. Single-ended measurement points for rise and fall time matching

3.6.11.3 SerDes transmitter and receiver reference circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

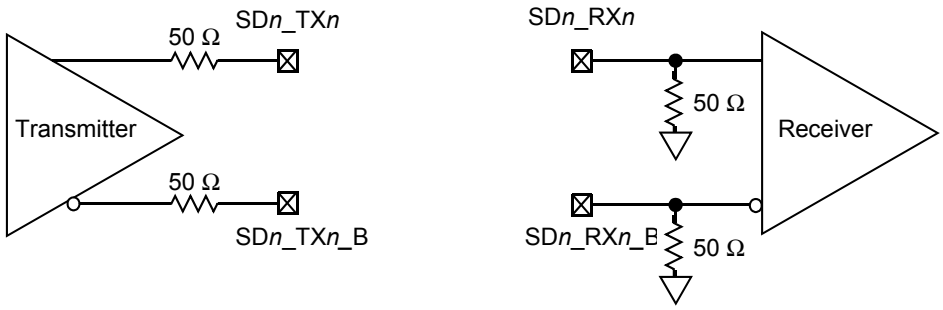


Figure 37. SerDes transmitter and receiver reference circuits

The AC specification of SerDes data lanes are defined in each interface protocol section below based on the application usage:

- Section 3.6.11.4, "CPRI AC timing specifications"
- Section 3.6.11.5, "SGMII interface"
- Section 3.6.11.6, "JESD204B"

Note that external AC-coupling capacitor is required for the above serial transmission protocols with the capacitor value defined in the specification of each protocol section.

3.6.11.4 CPRI AC timing specifications

Lynx supports following CPRI electrical variants to the limited extent described below:-

- Low Voltage (LV) variant guided by XAUI electrical interface (IEEE 802.3-2005) for data rates: 1.2288, 2.4576 and 3.072 Gb/s +/- 100ppm is supported.
- Low Voltage-II (LV-II) guided by guided by OIF-CEI-02.0 for data rates: 1.2288, 2.4576, 3.072, 4.9152 and 6.144Gb/s, +/- 100ppm is supported.
- The LV-III variant is supported for CPRI line bit rates: 2.4576, 3.072, 4.9152, 6.144 and 9.8304Gb/s +/- 100ppm.

This table below defines the AC specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 50. CPRI transmitter AC timing specifications (LV-I: 1.2288, 2.4576, and 3.072 Gbps)

Characteristic	Symbol	Min	Nom	Max	Unit	Note
Deterministic Jitter	JD	—	—	0.17	UI p–p	—
Total Jitter	JT	—	—	0.35	UI p–p	—
Unit Interval: 1.2288 Gbaud	UI	1/1228.8 – 100ppm	1/1228.8	1/1228.8 + 100ppm	µs	—
Unit Interval: 2.4576 Gbaud	UI	1/2457.6 – 100ppm	1/2457.6	1/2457.6 + 100ppm	µs	—
Unit Interval: 3.072 Gbaud	UI	1/3072.0 – 100ppm	1/3072.0	1/3072.0 + 100ppm	µs	—

NOTE

The AC specifications do not include Refclk jitter.

This table defines the AC specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 51. CPRI receiver AC timing specifications (LV-I: 1.2288, 2.4576, and 3.072 Gbps)

Characteristic	Symbol	Min	Nom	Max	Unit	Condition	Notes
Deterministic jitter tolerance	JD	—	—	0.37	UI p–p	Measured at receiver	—
Combined deterministic and random jitter tolerance	JDR	—	—	0.55	UI p–p	Measured at receiver	—
total jitter tolerance	JT	—	—	0.65	UI p–p	Measured at receiver	1,2
Unit interval: 1.2288 Gbaud	UI	1/1228.8 – 100ppm	1/1228.8	1/1228.8 + 100ppm	ps	—	—
Bit error ratio	BER			10^{-12}		—	—
Unit interval: 2.4576 Gbaud	UI	1/2457.6 – 100ppm	1/2457.6	1/2457.6 + 100ppm	ps	—	—
Unit interval: 3.072 Gbaud	UI	1/3072.0 – 100ppm	1/3072.0	1/3072.0 + 100ppm	ps	—	—

Note:

1. Total random jitter is composed of deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter's amplitude and frequency is defined in agreement with XAUI specification IEEE 802.3-2005 [1], clause 47.
2. The AC specifications do not include Refclk jitter.

This table provides the CPRI-LV-II/LV_III transmitter AC specifications.

Table 52. CPRI transmitter AC timing specifications (LV-II: 1.2288, 2.4576, 3.072, 4.9152, and 6.144 Gbps, LV-III: 9.8304 Gbps)

Parameter	Symbols	Min	Nom	Max	Condition	Unit	Notes
Uncorrelated high probability jitter/random jitter	T_UHPJ/T_RJ	—	—	0.18	—	UI p–p	—
Total jitter	T_TJ	—	—	0.30	—	UI p–p	—
Unit interval: 1.2288 Gbaud	UI	1/1228.8-100ppm	1/1228.8	1/1228.8+100ppm	—	µs	—
Unit interval: 2.4576 Gbaud	UI	1/2457.6-100ppm	1/2457.6	1/2457.6+100ppm	—	µs	—
Unit interval: 3.072 Gbaud	UI	1/3072.0-100ppm	1/3072.0	1/3072.0+100ppm	—	µs	—
Unit interval: 4.9152 Gbaud	UI	1/4915.2-100ppm	1/4915.2	1/4915.2+100ppm	—	µs	—
Unit interval: 6.144 Gbaud	UI	1/6144.0-100ppm	1/6144.0	1/6144.0+100ppm	—	µs	—
Unit interval: 9.8304 Gbaud	UI	1/9830.4-100ppm	1/9830.4	1/9830.4+100ppm	—	µs	—

This table provide the CPRI LV-II receiver AC timing specifications. The AC specifications do not include Refclk jitter.

Table 53. CPRI receiver AC timing specifications (LV-II: 1.2288, 2.4576, 3.072, 4.9152, and 6.144 Gbps)

Parameter	Symbols	Min	Nom	Max	Unit	Notes
Gaussian jitter	R_GJ	—	—	0.2	UI p–p	—
Uncorrelated bounded high probability jitter	R_UBHPJ	—	—	0.12	UI p–p	—
Correlated bounded high probability jitter	R_CBHPJ	—	—	0.63	UI p–p	—
Bounded high probability jitter	R_BHPJ	—	—	0.75	UI p–p	—
Sinusoidal jitter, maximum	R_SJ-max	—	—	5.000	UI p–p	—
Sinusoidal jitter, high frequency	R_SJ-hf	—	—	0.050	UI p–p	—
Total jitter does not include sinusoidal jitter	R_Tj	—	—	0.950	UI p–p	—
Unit Interval: 1.2288 Gbaud	UI	1/1228.8-100ppm	1/1228.8	1/1228.8+100ppm	µs	—
Unit interval: 2.4576 Gbaud	UI	1/2457.6-100ppm	1/2457.6	1/2457.6+100ppm	µs	—
Unit interval: 3.072 Gbaud	UI	1/3072.0-100ppm	1/3072.0	1/3072.0+100ppm	µs	—
Unit interval: 4.9152 Gbaud	UI	1/4915.2-100ppm	1/4915.2	1/4915.2+100ppm	µs	—
Unit interval: 6.144 Gbaud	UI	1/6144.0-100ppm	1/6144.0	1/6144.0+100ppm	µs	—

The intended application is as a point-to-point interface of approximately 100 cm and up to two connectors. The maximum allowed total loss (channel + interconnect + other loss) is 20.4 dB at 6.144 Gb/s.

This table provides the LV-III receiver parameters guided by 10 GBase-KR electrical interface (IEEE 802.3 [22], clause 72.7.2).

Table 54. CPRI receiver AC timing specifications (LV-III: 9.8304 Gbps)

Parameter	Symbols	Min	Nom	Max	Unit	Notes
Random jitter	R_GJ	—	—	0.130	UI p–p	—
Sinusoidal jitter, maximum	R_SJ-max	—	—	0.115	UI p–p	—
DCD	R_dcd	—	—	0.035	UI p–p	—
Total jitter	R_Tj	—	—	See Note 1	UI p–p	1
Unit Interval: 9.8304 Gbaud	UI	1/9830.4-100pm	1/9830.4	1/9830.4+100ppm	µs	—

Note:

1. The R_Tj is per Interference Tolerance Test IEEE Std 802.3ap-2007 specified in Annex 69A.
2. The AC specifications do not include Refclk jitter.
3. The maximum channel insertion loss is achieved by manual tuning TX equalization.

3.6.11.5 SGMII interface

This section provides AC electrical characteristics of SGMII interface.

This table provides the SGMII transmitter AC specifications. The AC specifications do not include Refclk jitter.

Table 55. SGMII transmitter AC specifications

Parameter	Symbols	Min	Nom	Max	Condition	Unit	Note
Unit interval	UI	800-100 ppm	800	800+100 ppm	±100 ppm	ps	—
Deterministic jitter	JD	—	—	0.17	—	UI p–p	—

Table 55. SGMII transmitter AC specifications (continued)

Parameter	Symbols	Min	Nom	Max	Condition	Unit	Note
Total jitter JT	JT	—	—	0.35	—	UI p–p	—
AC coupling capacitor	CTX	75	—	200	All transmitters shall be AC coupled	nF	—

This table provide the SGMII receiver AC timing specifications. The source-synchronous clocking is not supported and the clock is recovered from the data.

Table 56. SGMII receiver AC specifications

Parameter	Symbol	Min	Nom	Max	Condition	Unit	Note
Unit interval	UI	800 – 100 ppm	800	800 + 100 ppm	± 100 ppm	ps	—
Deterministic jitter tolerance	JD	—	—	0.37	Measured at receiver	UI p–p	—
Combined deterministic and random Jitter tolerance	JDR	—	—	0.55	Measured at receiver	UI p–p	—
Total jitter tolerance	JT	—	—	0.65	Measured at receiver	UI p–p	—
Bit error ratio	BER	—	—	10^{-12}	—	—	—

Note:
1. The AC specifications do not include Refclk jitter.
2. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of Figure 38

This figure shows the single frequency sinusoidal jitter limits.

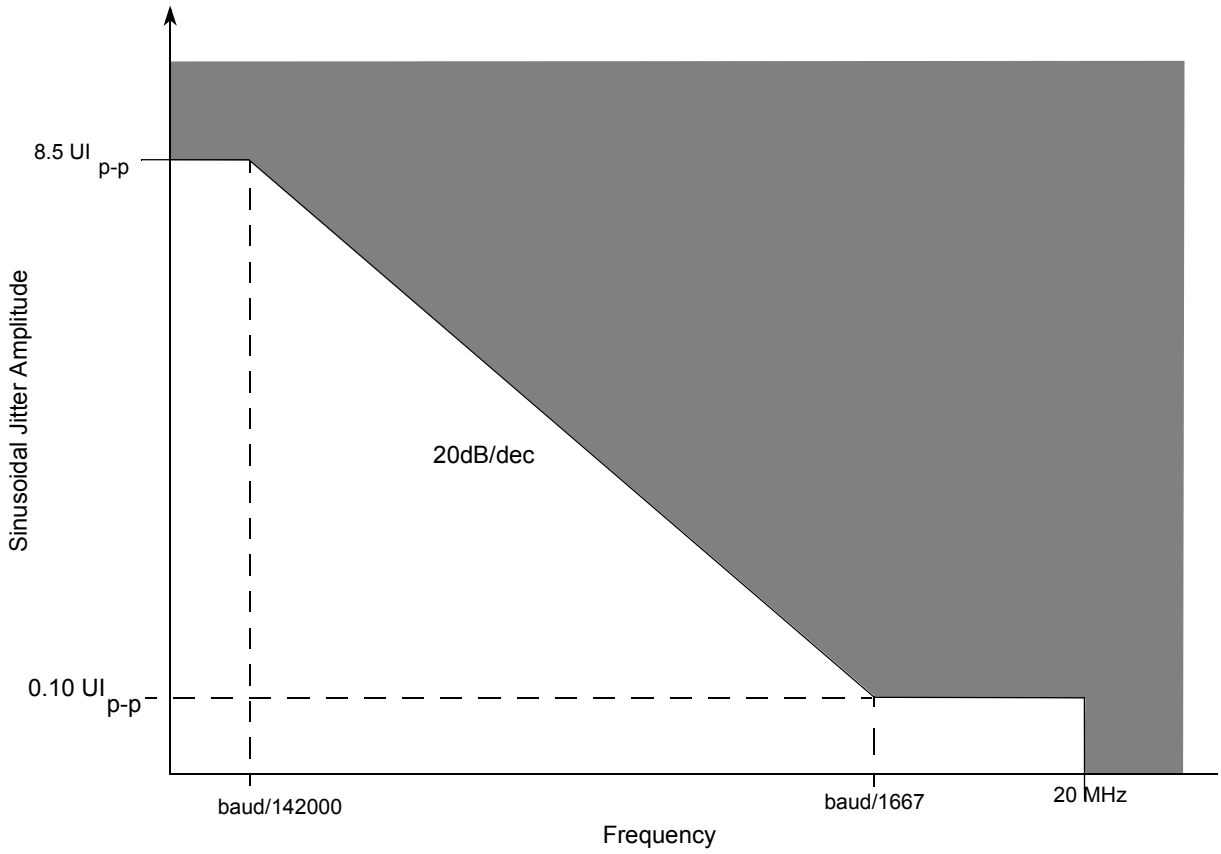


Figure 38. Single frequency sinusoidal jitter limits

3.6.11.6 JESD204B

This section presents JESD204B specification at 4.9152 Gb/s, 6.144 Gb/s, and 9.8304 Gb/s data rates. The link is required to operate with a BER 10^{-12}.

This table provides the JESD204B transmitter AC specifications.

Table 57. JESD204B transmitter AC specifications

Symbols	Parameter	Min	Nom	Max	Unit	Condition	Note
T_UHPJ	Uncorrelated high probability jitter/Random jitter	—	—	0.18	UI p–p	—	—
T_TJ	Total jitter JT	—	—	0.30	UI p–p	—	—

This table provides the JESD204B receiver AC timing specifications for speeds 1.288, 2.4576, 4.9152, and 6.144 Gbps.

Table 58. JESD204B(1.2288/2.4576/4.9152/6.144 Gbps) receiver AC specifications

Symbols	Parameter	Min	Nom	Max	Unit	Condition	Note
UI_JD1.2	Unit interval for 1.2288 GBaud	1/1228.8 - 100 ppm	1/1228.8	1/1228.8 + 100 ppm	µs	—	—
UI_JD2.4	Unit interval for 2.4576 GBaud	1/2457.6 - 100 ppm	1/2457.6	1/2457.6 + 100 ppm	µs	—	—
UI_JD3.1	Unit interval for 3.072 GBaud	1/3072.0 - 100 ppm	1/3072.0	1/3072.0 + 100 ppm	µs	—	—
UI_JD4.9	Unit interval for 4.9152 GBaud	1/4915.2 - 100 ppm	1/4915.2	1/4915.2 + 100 ppm	µs	—	—
UI_JD6.1	Unit interval for 6.144 GBaud	1/6144.0 - 100 ppm	1/6144.0	1/6144.0 + 100 ppm	µs	—	—
R_UBHPJ	Uncorrelated bounded high probability jitter	—	—	0.15	UI p–p	—	—
R_CBHPJ	Correlated bounded high probability jitter	—	—	0.3	UI p–p	—	—
R_BHPJ	Bounded high probability jitter	—	—	0.45	UI p–p	—	—
R_SJ-max	Sinusoidal jitter, maximum	—	—	5	UI p–p	—	—
R_SJ-hf	Sinusoidal jitter, high frequency	—	—	0.05	UI p–p	—	—
R_Tj	Total jitter does not include sinusoidal jitter	—	—	0.6	UI p–p	—	—

Note:
1. The AC specifications do not include Refclk jitter.
2. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency.
3. The ISI jitter (R_CBHPJ) and amplitude have to correlated for example by a PCB trace.

This table provides the JESD204B receiver AC timing specifications for 9.8304 Gbps speed.

Table 59. JESD204B(9.8304 Gbps) receiver AC specifications

Symbols	Parameter	Min	Nom	Max	Unit	Condition	Note
UI_JD9.8	Unit interval for 9.8304 GBaud	1/9830.4 - 100 ppm	1/9830.4	1/9830.4 + 100 ppm	µs	—	—
Tj	Total jitter	—	—	0.7	UI p–p	—	—

Note:
1. The AC specifications do not include Refclk jitter.
2. Total jitter (Tj) includes high frequency sinusodial jitter.

3.6.12 Special timed signals

3.6.12.1 SYSREF signal

This table provides the values of timing parameters.

Table 60. SYSREF_IN and SYSREF_OUT timing specification

Parameter	Symbols	Min	Nom	Max	Unit	Notes
Device Clock Period	t_{DEVCLK}	—	8.138	—	ns	1
SYSREF_OUT(10ms pulse) Pulse high Period	$t_{SYSOUTW}$	2	—	—	t_{DEVCLK}	2
SYSREF_OUT delay with respect to DEVCLK	t_{KSYSD}	—	—	3.5	ns	—
SYSREF_IN setup time	t_{SYSHKH}	2.5	—	—	ns	—
SYSREF_IN hold time	t_{SYSXKH}	0.5	—	—	ns	—

Note:
1. Refer to Table 20 for DEVCLK characteristics.
2. The signal is generated counting 16 TbGen ref clocks. The pulse width will change based on the ref_clk frequency.

The figure below shows SYSREF_IN and SYSREF_OUT timings with respect to DEVCLK input pin.

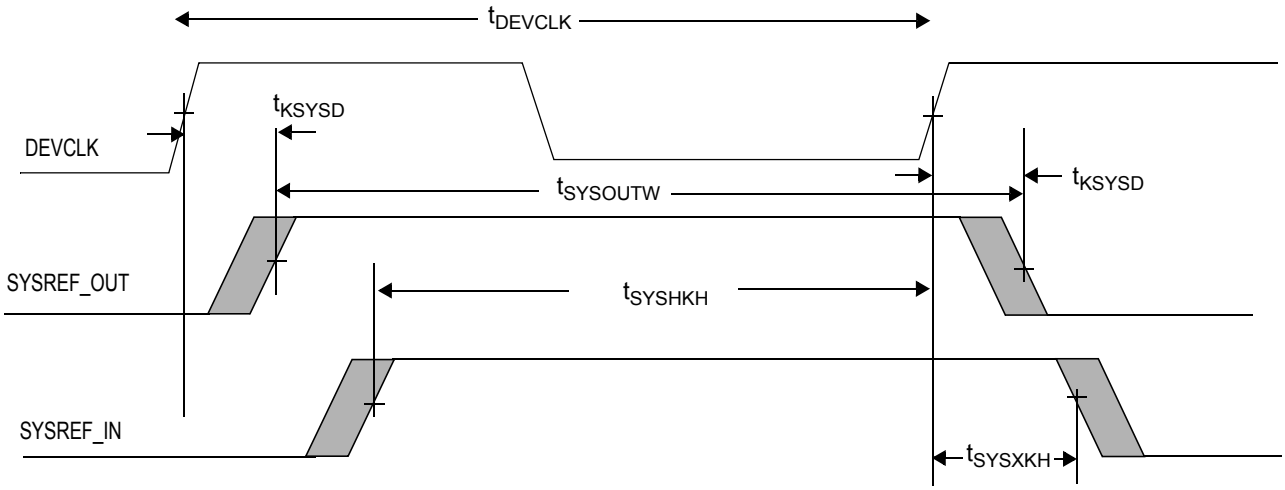


Figure 39. SYSREF timing parameters

3.6.12.2 Timed GPIO, AGC_EN, GP_EVENTs

This table provides the values of timing parameters.

Table 61. Timed GPIO, AGC_EN, GP_EVENTs timing specification

Parameter	Symbols	Min	Nom	Max	Unit	Notes
Delay with respect to Device clock (DEVCLK) input pin	$t_{TIMEDIOVKH}$	—	—	9.63	ns	1

Note:

1. Refer Table 20 for DEVCLK characteristics.
2. Pulse width of these signals can be programmed in the multiple of DEVCLK through TbGen module register.

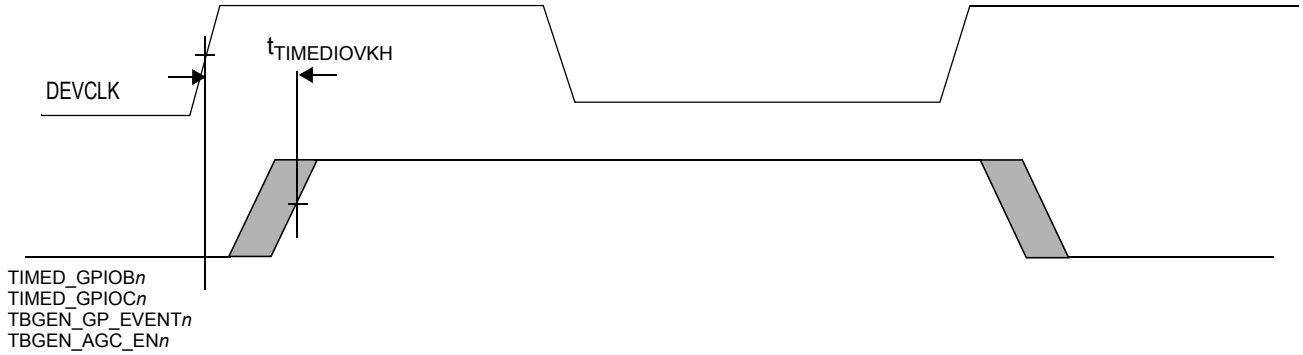


Figure 40. Timed GPIO, AGC_EN and GP_EVENTs Timing parameters

3.6.12.3 MC_SYNC_OUT and MC_SYNC_IN timings

Table 62 and Table 63 below provides the values of timing parameters.

Table 62. MC_SYNC_OUT timing specification

Parameter	Symbols	Min	Nom	Max	Unit	Notes
Delay with respect to DEVCLK input pin	$t_{MCOUTVKH}$	—	—	9.63	ns	1

Note:

1. Refer Table 20 for DEVCLK characteristics.

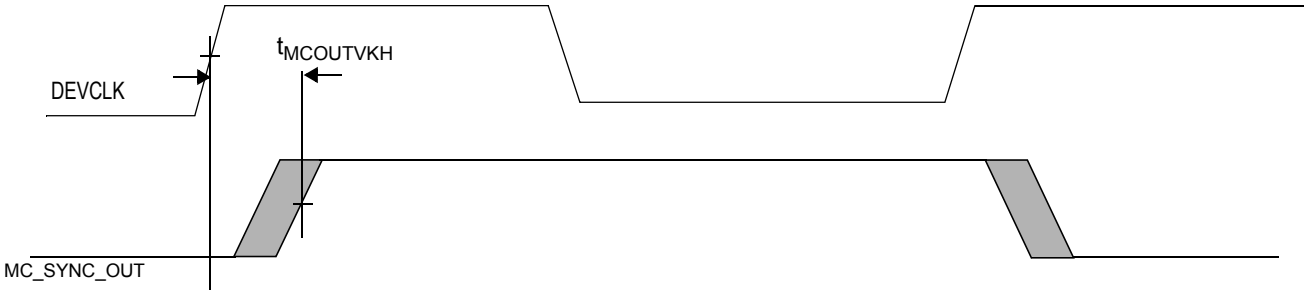


Figure 41. MC_SYNC_OUT Timing parameters

Table 63. MC_SYNC_IN timing specification

Parameter	Symbols	Min	Nom	Max	Unit	Notes
Minimum pulse width	t_{MCINW}	2	—	—	DEVCLK1 period	—

3.6.13 Trace port timing (TPIU)

Table 64 and Table 65 provides the Trace port timing specifications.

Table 64. Trace port timing

Parameter	Symbol	Min	Max	Unit	Notes
TRACE_CLK frequency	t_{TRK}	—	156	MHz	—
Data setup time	t_{TRKHDV},t_{TRKLDV}	1.2	—	ns	—
Data hold time	t_{TRKHDX},t_{TRKLDX}	0.2	—	ns	—

Table 65. Trace_clk_in port timing

Parameter	Symbol	Min	Max	Unit	Notes
TRACE_CLK_IN frequency	t_{TRKIN}	—	200	MHz	—

This figure below shows trace port interface timing.

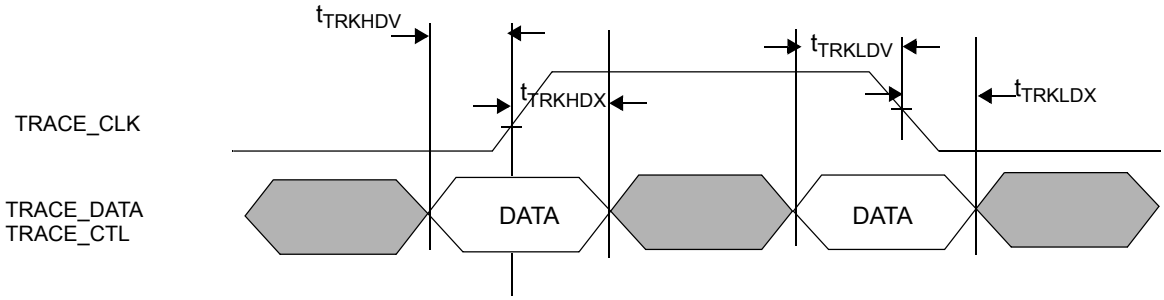


Figure 42. Trace port timing

3.6.14 Universal asynchronous receiver/transmitter (UART)

This section provides the universal asynchronous receiver/transmitter (UART) timing parameters.

NOTE

In the following tables, the maximum value of the ipg_perclk frequency is 78 MHz. The UART generates the baud clock based on “ipg_perclk” which comes from clock controller module (CCM).

3.6.14.1 UART serial mode timing

This section provides the transmit and receive timings of the UART serial mode.

3.6.14.1.1 Transmitter

This figure shows the transmit timing of the UART in serial mode. Note that the below figure only shows 8 data bits and 1 stop bit format.

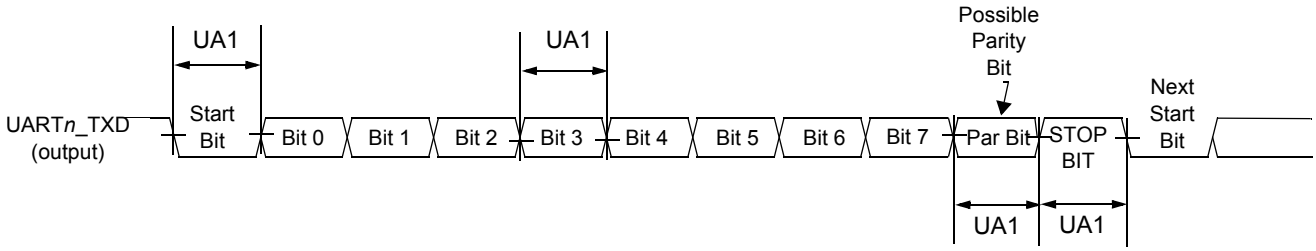


Figure 43. UART serial mode transmit timing diagram

This table lists the UART serial mode transmit timing parameters.

Table 66. UART serial mode transmit timing parameters

ID	Parameter	Symbol	Min	Max	Notes
UA1	Transmit bit time	t_{UATBW}	$1/F_{baud_rate} - T_{ref_clk}$	$1/F_{baud_rate} + T_{ref_clk}$	1,2,3

Note:

1. UA1 applies to all bits.
2. F_{baud_rate}: baud rate frequency. The maximum baud rate the UART can support is (ipg_perclk frequency)/16 or 4 mbps whichever is less.
3. Tref_clk: The period of UART reference clock (ipg_perclk after RFDIV divider).

3.6.14.1.2 Receiver

This figure shows the receive timing of the UART in serial mode. Note that the below figure only shows 8 data bits and 1 stop bit format.

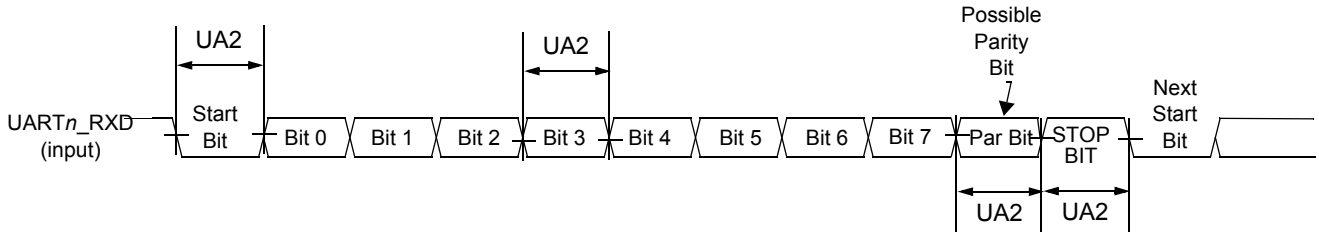


Figure 44. UART serial mode receive timing diagram

This table lists the UART serial mode receive timing parameters.

Table 67. UART serial mode receive timing parameters

ID	Parameter	Symbol	Min	Max	Notes
UA2	Receive bit time	t_{UARBW}	$1/F_{baud_rate} - 1/(16 \times F_{baud_rate})$	$1/F_{baud_rate} + 1/(16 \times F_{baud_rate})$	1,2,3

Note:

1. UA2 applies to all bits
2. The UART receiver can tolerate $1/(16 \times F_{baud_rate})$ tolerance in each bit, however, accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud_rate})$.
3. F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16 or 4 Mbaud whichever is less.

3.6.15 External flash interface module (EIM)

This section provides the parallel Flash interface module (EIM) timing parameters.

All EIM output control signals may be asserted and de-asserted by internal clock related to BCLK rising edge according to corresponding assertion/negation control fields.

This table show the maximum flash clock frequency.

Table 68. EIM (flash controller) timing parameters

Parameter	Symbol	Max	Unit	Notes
Operating frequency	f_{FLK}	104	Mhz	—

NOTE

BCD,WSC,WBEA,WADVN,BCS,SRD,ADVA,ADVN,ADH,RADVN,OEA are register configuration bits. Refer AFD4400 Reference Manual for details.

In synchronous mode, all output signal timings are relative to the falling edge of any BCLK. The external circuit must use the rising edge of the BCLKs to latch the data.All input timings are relative to the rising edge of BCLKs.

This table show the bus timing parameters.

Table 69. EIM timing specifications

Parameter	Symbol[1]	Min	Max	Unit	Notes
BCLK cycle time	t_{EMK}	9.6	—	ns	—
BCLK duty cycle	t_{EMKH}/t_{EMK}	45	55	%	—
Sync mode Input setup	$t_{EMIVKH1}$	2.9	—	ns	—
Sync mode Input hold	$t_{EMIXKH1}$	1	—	ns	—
Sync mode Output delay	$t_{EMKLOV1}$	—	1.5	ns	—
Sync Output hold	$t_{EMKLOX1}$	-2	—	ns	1
Async mode Input setup time	$t_{EMIVKH2}$	1	—	t_{EIM_CLK}	2,3
Async mode input hold time	$t_{EMIXKH2}$	1	—	t_{EIM_CLK}	2,3
Async mode outmode skew	$t_{EMKLOV2}$	-1.5	1.5	ns	—

Note:

1. Here, the negative sign means output transit happens earlier than the falling edge of BCLK.
2. t_{EIM_CLK} is 104 MHz maximum.This is module internal clock and not visible outside the chip.Refer AFD4400 reference manual for details.
3. RWSC is a register configurable parameter. Refer AFD4400 Reference Manual for details.Module has different register bits for different timing parameters.

Figures below show the AC timing diagram for input/output signals of EIM NOR interface. The timing specs have been illustrated here by taking timings among few input/output signals. The timing parameters can be configured through programmable register bits in the WEIM module. Refer AFD4400 Reference Manual for details.

Figure 45. EIM synchronous mode input timing

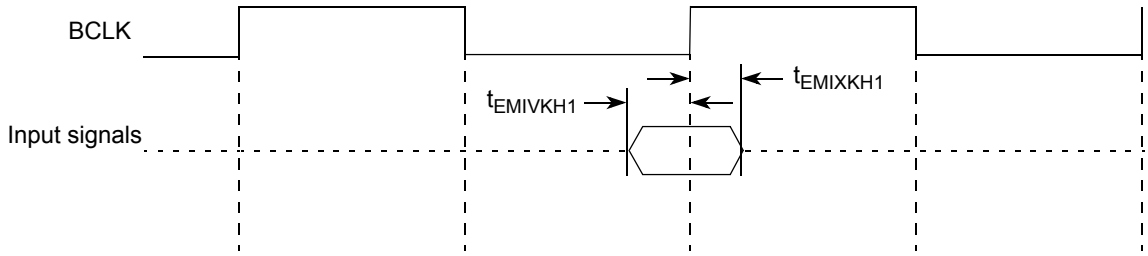


Figure 46. EIM synchronous mode output timing

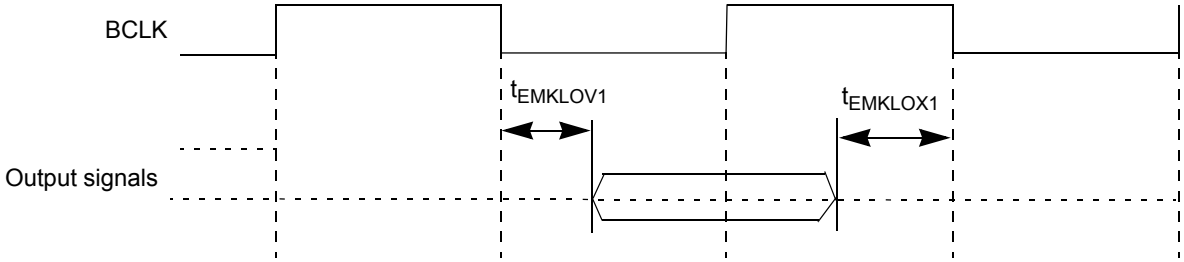
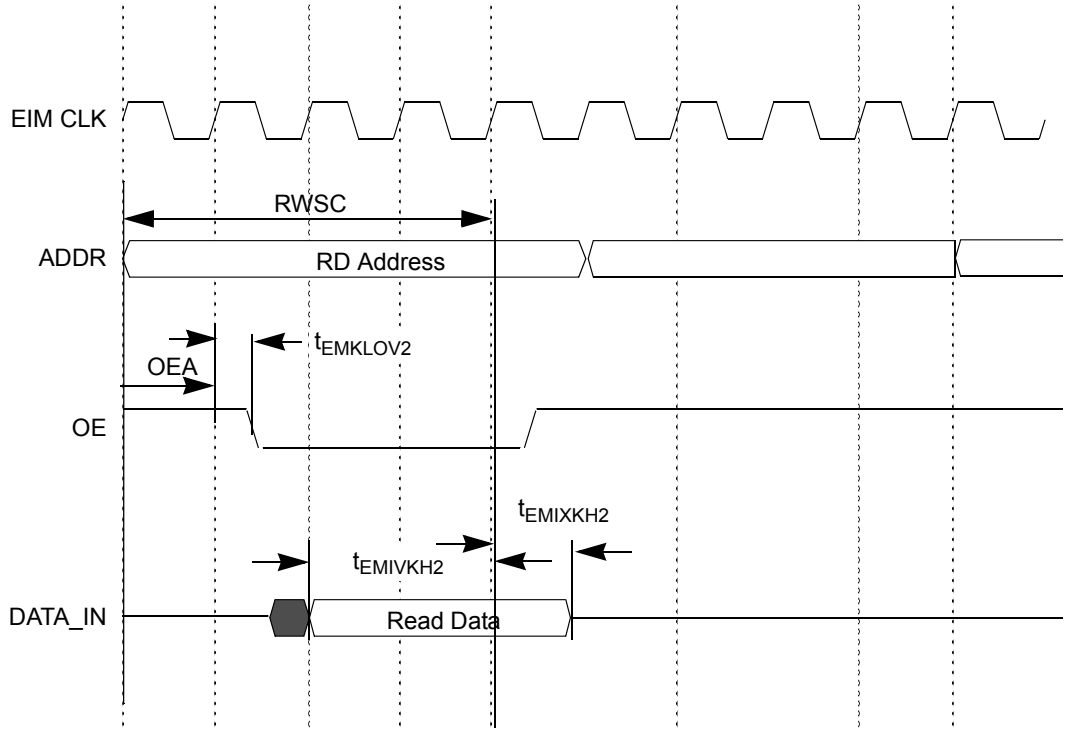


Figure 47. EIM Async interface timing



4 Hardware design considerations

4.1 System clocking

This section describes the PLL configuration of the chip.

4.1.1 PLL characteristics

Characteristics of the chip's PLLs include the following:

- There are a total of nine PLLs on the chip.
- There are three PLLs to supply operating clocks for different modules. All the three PLLs can get DEVCLK or RGMII_REFCLK as reference clock. SYSPLL output drives clock to ARM® Cortex-A9, VSP and system buses. The DDR PLL is source to DDR controller. It can also provide clock to VSP7 (dual precision). The TbGen_PLL supplies clock to RF interface modules like JESD controllers and time base generator (TbGen).
- Each of the three SerDes blocks has two PLLs which generate a core clock from their respective externally supplied reference clock inputs. The frequency ratio is selected using the SerDes PLL ratio configuration bits.

4.1.2 Maximum operating frequencies

This table provides the clocking specifications for the ARM® Cortex-A9 core, VSP core and memory.

Table 70. Processor clocking specifications

Characteristic	AFD4400NXN763VB	AFD4400NXN752VB	Unit
	Frequency (Max)	Frequency (Max)	
ARM® Cortex-A9 Core frequency	614.4	553	MHz
VSP 1, 2, 3, 4, 5, 6, 8, 9, 10, 11 Core frequency	614.4	553	MHz
VSP 7 Core frequency	307.2	276.5	MHz
System bus frequency	307.2	276.5	MHz
DDR interface frequency	500	500	MHz

4.2 Power supply design

4.2.1 Voltage ID (VID) controllable supply

To guarantee performance and power specifications, a specific method of selecting the optimum voltage-level must be implemented when the chip is used. The software must read the VID efuse values stored in the eFuse and then configure the external voltage regulator based on this information. (Refer AFD4400 Reference Manual for fuse definition and mapping) This method requires a point of load voltage regulator for each chip.

The default voltage regulator setting that is safe for the system to boot is the recommended operating V_{DD} at initial start-up of 1.025V. It is highly recommended to select a regulator with a Vout range of at least 0.9 V to 1.1 V, with a resolution of 12.5 mV or better, when implementing a VID solution.If the VID for a specific part is already known at initial start up, it is acceptable to program the voltage regulator to that VID value.The device does not require an initial voltage of 1.025V at start-up.

Table 71 lists the valid VID efuse values that will be programmed at the factory for this chip.

Table 71. VID fuse settings

VID fuse value (in binary)	V_{DD} voltage (in volt)
00001	0.9875
00010	0.9750
10000	1.0000
10001	1.0125
10010	1.0250
All other values	Reserved
Note: 1. If VID_ALT is not all zeros, the software must use VID_ALT fuses for voltage ID configuration.	

4.2.2 Core supply voltage (V_{DD}) filtering

The V_{DD} supply is normally derived from a high current capacity linear or switching power supply which can regulate its output voltage very accurately despite changes in current demand from the chip within the regulator's relatively low bandwidth. Several bulk decoupling capacitors must be distributed around the PCB to supply transient current demand above the bandwidth of the voltage regulator.

These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. However, customers should work directly with their power regulator vendor for best values and types of bulk capacitors.

As a guideline for customers and their power regulator vendors, Freescale recommends that these bulk capacitors be chosen to maintain the transient power surges to less than VID+50 mV (negative transient undershoot should comply with specification of VID-30mV) with a slew rate of 12 A/us.

These bulk decoupling capacitors ideally supply a stable voltage for current transients into the megahertz range. Above that, see Section 4.3, "Decoupling recommendations for further decoupling recommendations.

4.2.3 PLL power supply filtering

Each of the PLLs described in Section 4.1, "System clocking," is provided with power through independent power supply pins (APVDD*n*,SD*x*_AVDD_PLL*n)*. APVDD*n* voltages must be derived directly from a 1.8 V voltage source through a low frequency filter scheme. SD*x*_AVDD_PLL*n* must be derived directly from the SD*x*_XPADVDD voltage source through a low frequency filter scheme. The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, as illustrated in Figure 48, one for each of the APVDD pins. By providing independent filters to each PLL, the opportunity to cause noise injection from one PLL to the other is reduced. This circuit is intended to filter noise in the PLL's resonant frequency range from a 500 kHz to 10 MHz range.

Each circuit should be placed as close as possible to the specific APVDD pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the APVDD pin, which is on the periphery of the footprint, without the inductance of vias.

This figure shows the PLL power supply filter circuit.

Where:

R = 5 Ω ± 5%
C1 = 10 µF ± 10%, 0603, X5R, with ESL ≤ 0.5 nH
C2 = 1.0 µF ± 10%, 0402, X5R, with ESL ≤ 0.5 nH

NOTE

A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change (0402 body, X5R, ESL ≤ 0.5 nH).

Voltage for APVDD is defined at the input of the PLL supply filter and not the pin of APVDD.

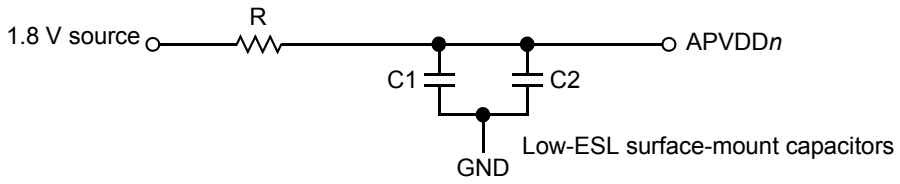


Figure 48. PLL power supply filter circuit

The SD*x*_AVDD_PLL*n* signals provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following Figure 49. For maximum effectiveness, the filter circuit is placed as closely as possible to the SD*x*_AVDD_PLL*n* balls to ensure it filters out as much noise as possible. Prior to release of PLL reset, and start of PLL lock, the PLL supply must be at a stable and quiescent value. The ground connection should be near the SD*x*_AVSS_PLL*n* balls. The 0.003-µF capacitors closest to the balls, followed by a 4.7-µF and 47-µF capacitor, and finally the 0.33 Ω resistor to the board supply plane. The capacitors are connected from SD*x*_AVDD_PLL*n* to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.

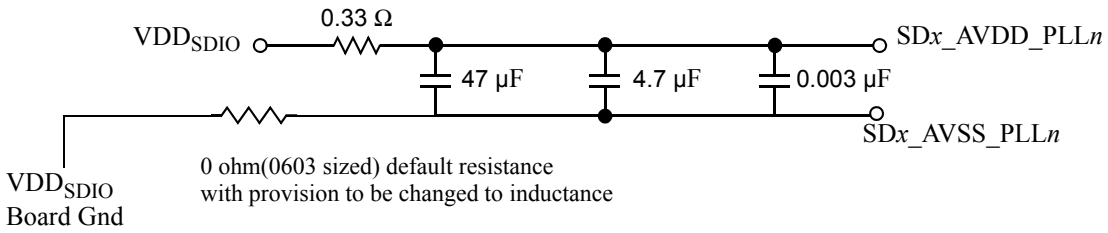


Figure 49. SerDes PLL power supply filter circuit

Note the following:

- SD*x*_AVDD_PLL*n* should be a filtered version of VDD_{SDIO}.
- Signals on the SerDes interface are fed from the VDD_{SDIO} power plane.
- Voltage for SD*x*_AVDD_PLL*n* is defined at the PLL supply filter and not the pin of SD*x*_AVDD_PLL*n*.
- A 47-µF 0805 XR5 or XR7, 4.7-µF 0603, and 0.003-µF 0402 capacitor are recommended. The size and material type are important. A 0.33-Ω ± 1% resistor is recommended.
- There needs to be dedicated analog ground, SD*x*_AVSS_PLL*n* for each SD*x*_AVDD_PLL*n* pin up to the physical local of the filters themselves.
- The noise level on the SerDes PLL power supplies must be less than 10 mV Pk-Pk.

4.2.4 SerDes transceiver core supply filtering

VDD_{SDX} should be supplied by a dedicated linear regulator. Systems may design to allow flexibility to address system noise dependencies.

NOTE

For initial system bring-up, the linear regulator option is highly recommended.

An example solution for VDD_{SDX} filtering, where VDD_{SDX} is sourced from linear regulator, is illustrated in Figure 50. The component values in this example filter are system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

- C1 = 0.003 µF ± 10%, X5R, with ESL ≤ 0.5 nH
- C2 and C3 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH
- F1 to F4 are 0603 sized Ferrite SMD, like the Murata part BLM18PG121SH1. Its maximum DC resistance is 0.05Ω, or 0.0125Ω for the parallel resultant, and each has about a 120Ω ± 25% of AC impedance at 100 MHz, which will be quarter valued for the parallel resultant, with individual maximum DC current carrying capacity of 2Amps. Bulk and decoupling capacitors are added, as needed, per power supply design.

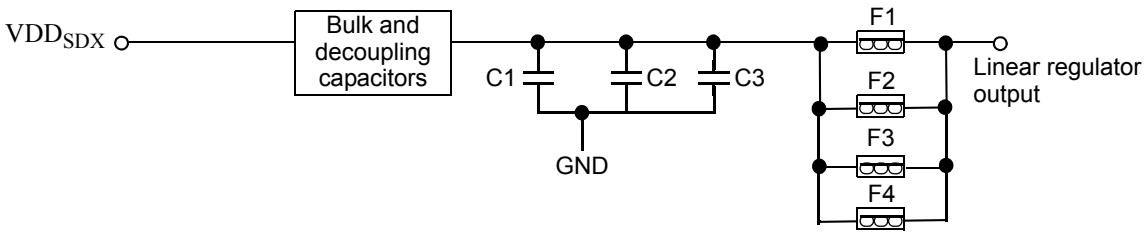


Figure 50. VDD_{SDX} power supply filter circuit

Note the following:

- Refer to Section 3.2.1, "Power-on ramp rate, for maximum VDD_{SDX} power-up ramp rate.
- There needs to be enough output capacitance or a soft start feature to assure ramp rate requirement is met.
- The ferrite beads should be placed in parallel to reduce voltage droop.
- Besides a linear regulator, a low noise dedicated switching regulator can also be used. 10 mVp-p, 50kHz - 500MHz is the noise goal.

4.2.5 SerDes transceiver pad supply filtering

VDD_{SDIO} must be supplied by a linear regulator or sourced by a filtered VDD_{DDR}. Systems may design in both options to allow flexibility to address system noise dependencies.

NOTE

For initial system bring-up, the linear regulator option is highly recommended.

An example solution for VDD_{SDIO} filtering, where VDD_{SDIO} is sourced from a linear regulator, is illustrated in Figure 51. The component values in this example filter are system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

- C1 = 0.003 µF ± 10%, X5R, with ESL ≤ 0.5 nH
- C2 and C3 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH
- F1 to F4 are 0603 sized Ferrite SMD, like the Murata part BLM18PG121SH1. Its maximum DC resistance is 0.05Ω, or 0.0125Ω for the parallel resultant, and each has about a 120Ω ± 25% of AC impedance at 100 MHz, which will be quarter valued for the parallel resultant, with individual maximum DC current carrying capacity of 2Amps.Bulk and decoupling capacitors are added, as needed, per power supply design.

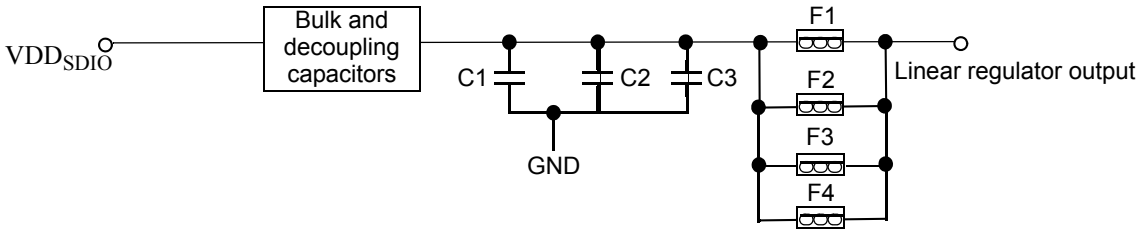


Figure 51. VDD_{SDIO} power supply filter circuit

Note the following:

- Refer to Section 3.2.1, "Power-on ramp rate, for maximum VDD_{SDIO} power-up ramp rate.
- There needs to be enough output capacitance or a soft-start feature to assure ramp rate requirement is met.
- The ferrite beads should be placed in parallel to reduce voltage droop.
- Besides a linear regulator, a low-noise, dedicated switching regulator can be used. 10mVp-p, 50 kHz - 500 MHz is the noise goal.

4.2.6 Remote power-supply sense recommendations

It is common practice to connect remote sense pin of on-board power supply with one of the supply pin of the connected IC. This arrangement helps to compensate for the slow components of the IR droop caused by the resistive supply current path from the power supply to the IC pins.

Following AFD4400 SENSE pins can be connected to the on-board power supply remote sense pins:

- Sense Pins pair 1: SENSE_DVDD1, SENSE_DVSS1
- Sense Pins pair 2: SENSE_DVDD2, SENSE_DVSS2

Either of the two pairs (with other pair unconnected) or both the pairs can be connected to power supply. It is recommended to use both the sense pairs on the board. An example circuit with both the sense pins has been illustrated in Figure 53.

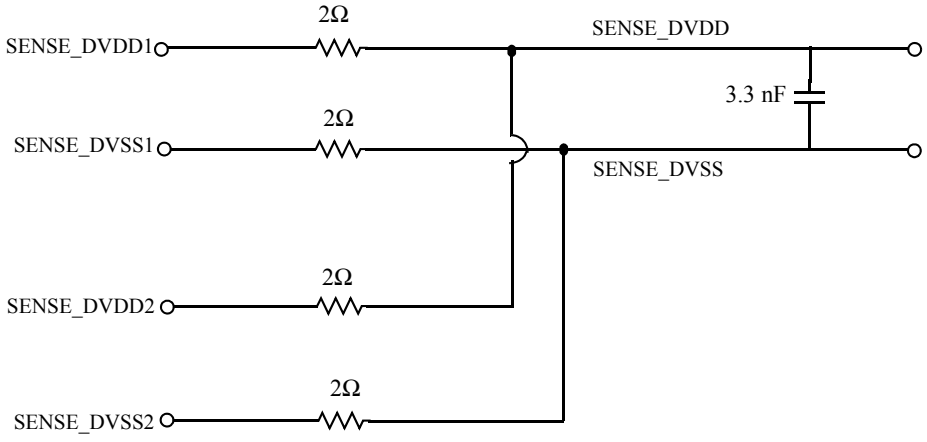


Figure 52. Power supply sense circuit

4.3 Decoupling recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the chip system, and the chip itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place decoupling capacitors at each V_{DD},VDD_{GPIO},VDD_{DDR},VDD_{LVDS} and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

As presented in Section 4.2.2, "Core supply voltage (VDD) filtering," it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} and other planes, to enable quick recharging of the smaller chip capacitors.

4.4 SerDes block power supply decoupling recommendations

The SerDes block requires a clean, tightly regulated source of power (VDD_{SDX} and VDD_{SDIO}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

NOTE

Only SMT capacitors should be used to minimize inductance.Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

1. The board should have at least 1 x 0.1-uF SMT ceramic chip capacitor placed as close as possible to each supply ball of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
2. Between the device and any SerDes voltage regulator there should be a lower bulk capacitor (for example a 10-uF, low ESR SMT tantalum or ceramic) and a higher bulk capacitor (for example a 100uF - 300-uF low ESR SMT tantalum or ceramic capacitor).

4.5 Guidelines for high-speed interface termination

4.5.1 SerDes interface entirely unused

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section.

Note that SDn_AVDD_PLLn, SDn_XCOREVDD,SDn_XPADVDD must remain powered.

For SDn_AVDD_PLLn, it must be connected to SDn_XPADVDD through a zero ohm resistor (instead of filter circuit shown in Figure 57).

The following pins must be left unconnected:

- CPRIm_TXDATn_P
- CPRIm_TXDATn_N
- TX_DATn_P
- TX_DATn_N
- SGMIIn_TXDAT_P
- SGMIIn_TXDAT_N

- SDn_IC_TX
- SDn_IC_RX

The following pins must be connected to SDn_XCOREVSS :

- SGMII_REFCLK_P
- SGMII_REFCLK_N

It is recommended for the following pins to be connected to SDn_XCOREVSS:

- CPRIm_RXDATn_P
- CPRIm_RXDATn_N
- RX_DATn_P
- RX_DATn_N
- SGMIIn_RXDAT_P
- SGMIIn_RXDAT_N

Refer to AFD4400 reference manual for SerDes PLL/Lane programming model.

4.5.2 SerDes interface partly unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

Note that both SDn_XCOREVDD and SDn_XPADVDD must remain powered.

If any of the PLLs are unused, the corresponding SDn_AVDD_PLLn must be connected to SDn_XPADVDD through a zero ohm resistor (instead of filter circuit shown in Figure 57).

The following unused pins must be left unconnected:

- CPRIm_TXDATn_P
- CPRIm_TXDATn_N
- TX_DATn_P
- TX_DATn_N
- SGMIIn_TXDAT_P
- SGMIIn_TXDAT_N

The following pins must be connected to SDn_XCOREVSS :

- SGMII_REFCLK_P
- SGMII_REFCLK_N

It is recommended that the following unused pins be connected to SDn_XCOREVSS:

- CPRIm_RXDATn_P
- CPRIm_RXDATn_N
- RX_DATn_P
- RX_DATn_N
- SGMIIn_RXDAT_P
- SGMIIn_RXDAT_N

For details on the SerDes PLL/Lane programming model, refer to the AFD4400 Digital Front End Processor Reference Manual.

4.6 Temperature diode

The chip has temperature diodes that can be used to monitor its temperature using external temperature monitoring devices (such as analog devices, ADT7461A™). These on-chip temperature diodes have pins that may be connected to test points, or left as a no connect when they are not used.

The following are specifications of the chip temperature diodes:

- Operating range: 10-230µA
- The Non-ideality factor over the temperature range 85C to 105C, n = 1.006 ± 0.003 with approximate error ±1°C
- Temperature range 0°C to 85°C, the error in measurement is ±3°C.
- Temperature range -40°C to 0°C, the error in measurement is ±5°C.

4.7 Thermal characteristics

This table shows the thermal characteristics for the chip. Note that these numbers are based on design estimates and are preliminary.

Table 72. Package thermal characteristics

Rating	Board	Symbol	Value	Unit	Notes
Junction to Ambient, natural Convection	Single layer board (1s)	$R_{\theta JA}$	15	°C/W	1,2
Junction to Ambient, natural Convection	Four layer board (2s2p)	$R_{\theta JA}$	11	°C/W	1,3
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	10	°C/W	1,2
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	7	°C/W	1,2
Junction to Board	—	$R_{\theta JB}$	2.8	°C/W	3
Junction to Case (Top)	—	$R_{\theta JCtop}$	0.4	°C/W	4
Junction to Lid Top	—	$R_{\theta JClid}$	0.17	°C/W	5

Note:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-3 and JESD51-6 with the board (JESD51-9) horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measure on the top surface of the board near the package.
4. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Junction-to-Lid-Top thermal resistance determined using the using MIL-STD 883 Method 1012.1. However, instead of the cold plate, the lid top temperature is used here for the reference case temperature. Reported value does not include the thermal resistance of the interface layer between the package and cold plate.

5 Package information

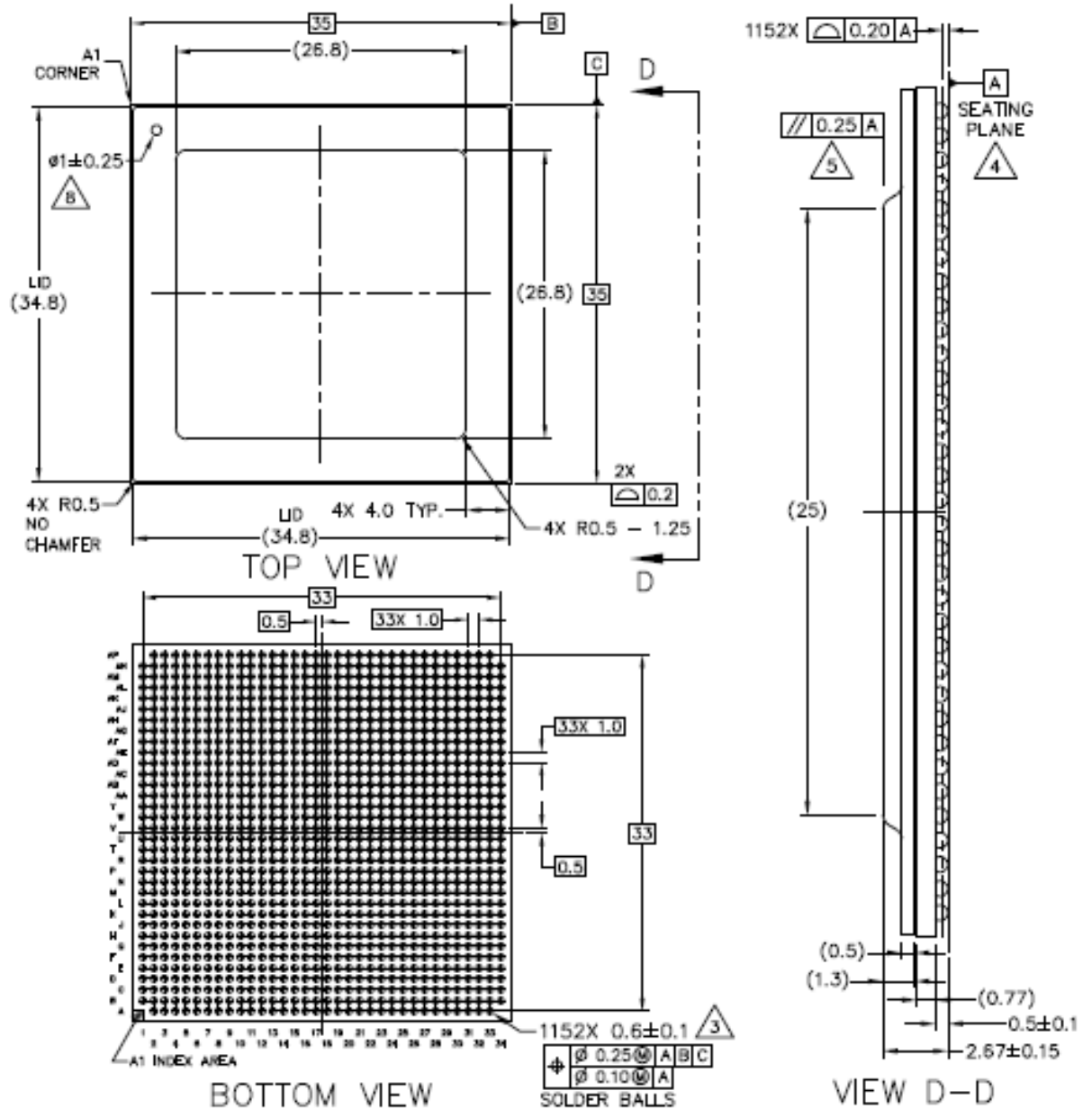
5.1 Package parameters for the FC-PBGA

The package parameters are as provided in the following list. The package type is 35 mm × 35 mm, 1152 flip-chip, plastic-ball, grid array (FC-PBGA). The AFD4400part is designed to be RoHS and Pb-free compliant.

Package outline	35 mm × 35 mm
Interconnects	1152
Ball Pitch	1.0 mm
Ball Diameter (typical)	0.60 mm
Solder Balls	96.5% Sn, 3% Ag, 0.5% Cu
Module height (typical)	2.52 mm to 2.82 mm (maximum)

5.2 Mechanical dimensions of AFD4400FC-PBGA

This figure shows the mechanical dimensions and bottom surface nomenclature of the chip.



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TITLE: FCPBGA WITH LID, 35 X 35 PKG X 2.67 PKG, 1.0 MM PITCH, 1152 I/O	DOCUMENT NO: 98ASA00464D	REV: C
	STANDARD: NON-JEDEC	
	12 FEB 2015	

Figure 53. Mechanical dimensions

Note:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. All dimensions are symmetric across the package center lines unless dimensioned otherwise.
4. Maximum solder ball diameter measured parallel to datum A.
5. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
6. Parallelism measurement excludes any effect of mark on top surface of package.

5.3 Revision history

This table summarizes revisions to this document.

Table 73. Revision History

Rev. Number	Date	Substantive change(s)
0	10/2015	• Initial public release

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