FS6500-FS4500-ASILD

Safety power system basis chip with CAN FD and LIN transceivers

Rev. 9.0 — 15 July 2026 Product data sheet



1 General description

The FS6500/FS4500 SMARTMOS devices are a multi-output, power supply, integrated circuit, including CAN Flexible Data (FD) and/or LIN transceivers, dedicated to the automotive market.

Multiple switching and linear voltage regulators, including low-power mode (32 µA) are available with various wake-up capabilities. An advanced power management scheme is implemented to maintain high efficiency over a wide range of input voltages (down to 2.7 V) and output current ranges (up to 2.2 A).

The FS6500/FS4500 includes configurable fail-safe/fail silent safety behavior and features, with two fail-safe outputs, becoming a full part of a safety oriented system partitioning, to reach a high integrity safety level (up to ASIL D).

The built-in CAN FD interface fulfills the ISO 11898-2[(12)] and -5[(13)] standards. The LIN interface fulfills LIN protocol specifications 2.0, 2.1[(22)], 2.2[(23)], and SAE J2602-2[(24)].

High temperature capability up to T_A = 125 °C and T_J = 150 °C, compliant with AEC-Q100 Grade 1 automotive qualification.

2 Features and benefits

- Battery voltage sensing and MUX output pin
- Highly flexible SMPS pre-regulator, allowing two topologies: non-inverting buck-boost and standard buck
- Family of devices to supply MCU core from 1.0 V to 5.0 V, with SMPS (0.8 A, 1.5 A or 2.2 A, 1.5 A or 2.2 A) or LDO (0.5 A)
- Linear voltage regulator dedicated to auxiliary functions, or to sensor supply (V_{CCA} tracker or independent), 5.0 V, or 3.3 V
- Linear voltage regulator dedicated to MCU Analog/Digital (A/D) reference voltage or I/Os supply (V_{CCA}), 5.0 V, or 3.3 V
- 3.3 V keep alive memory supply available in low-power mode
- Long duration timer, counting up to 6 months with 1.0 s resolution
- Multiple wake-up sources in low-power mode: CAN, LIN, IOs, LDT
- Five configurable I/Os

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

3 Applications

- Drive Train Electrification (BMS, Hybrid EV and HEV, Inverter, DC-DC, Alterno Starter)
- Drive Train - Chassis and Safety (Active Suspension, Steering, Safety Domain Gateway)
- Power Train (EMS, TCU, Gear Box)
- ADAS (LDW, Radar, Sensor Fusion Safety area)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

4 Simplified application diagrams

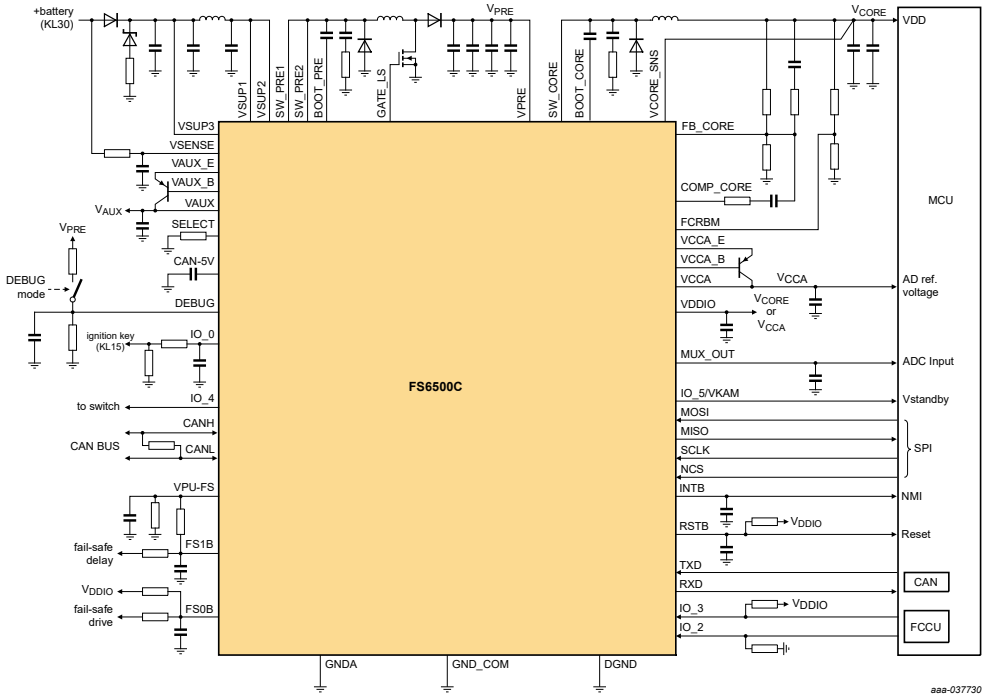


Figure 1. FS6500C simplified application diagram - buck boost configuration - FS1B

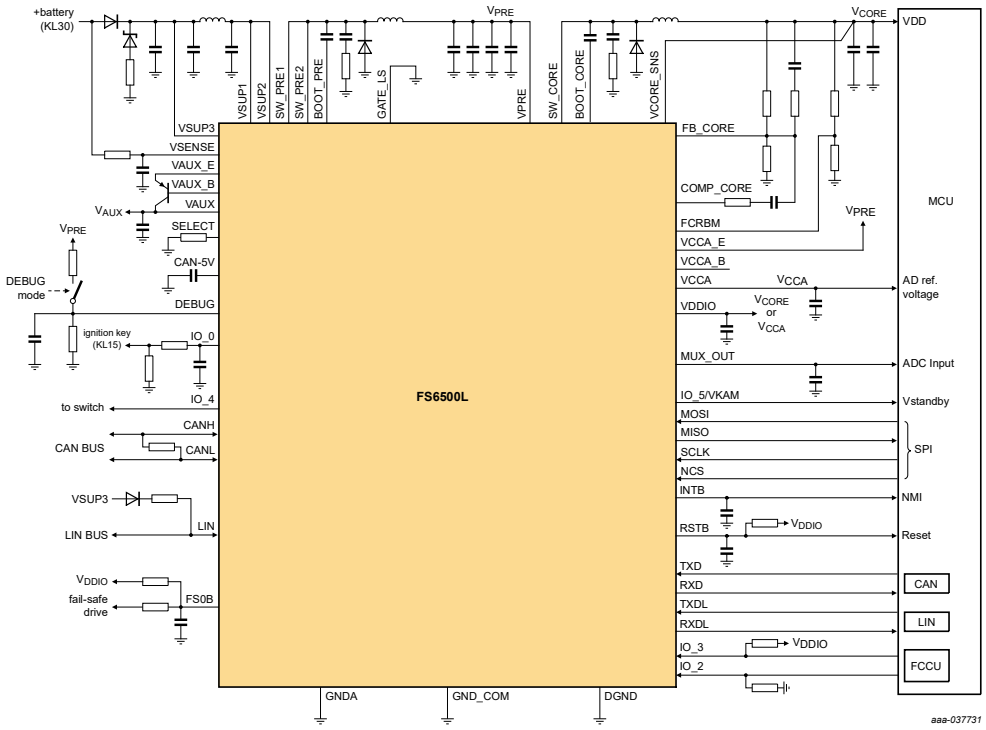


Figure 2. FS6500L simplified application diagram - buck configuration - LIN - V_{CCA} = 100 mA

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

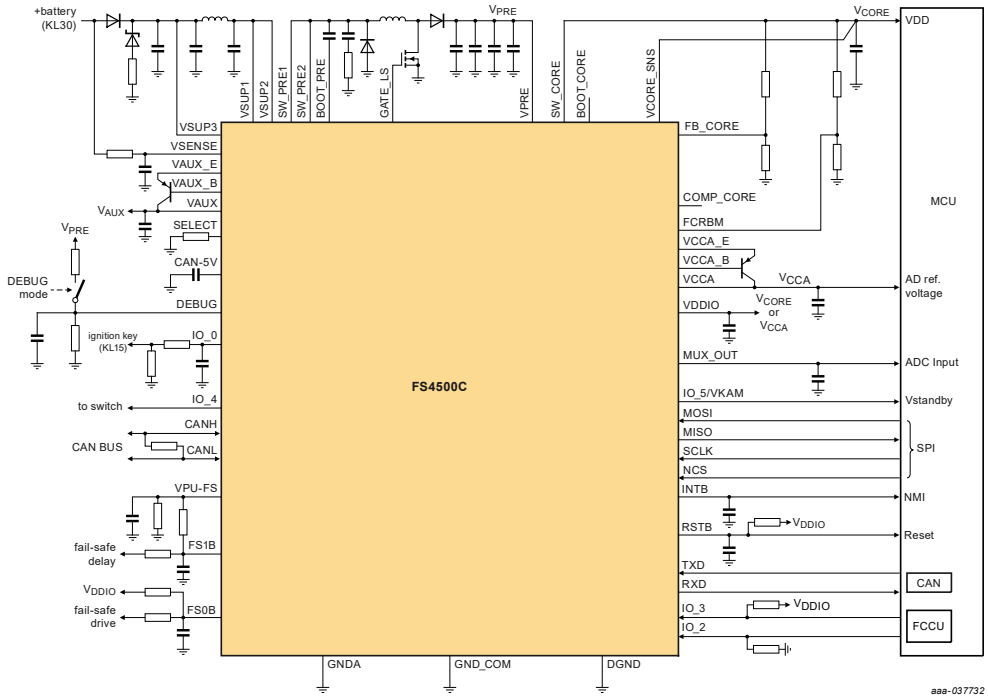


Figure 3. FS4500C simplified application diagram - buck boost configuration - FS1B

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

5 Ordering information

5.1 Part number definition

MC33FS **c** 5 **x** **y** **z** AE[1](KE)[2]/R2

[1] Parts with AE suffix (China manufacturing)
[2] Parts with KE suffix (Malaysia manufacturing)

Table 1. Part number breakdown

Code	Option	Variable	Description
c	4 series	V_{CORE} type	Linear
	6 series		DC-DC
x	0	V_{CORE} current	0.5 A or 0.8 A
	1		1.5 A
	2		2.2 A
y	0	Functions	None
	1		FS1B
	2		LDT
	3		FS1B, LDT
	4		LDT, VKAM ON by default
z	N	Physical interface	None
	C		CAN FD
	L		CAN FD and LIN

5.2 Part numbers list

Table 2. Orderable part variations

Part Number	Temperature (T_A)	Package	FS1B	LDT	VCORE	VCORE type	VKAM on	CAN FD	LIN	Notes
MC33FS4500CAE MC33FS4500CKE	–40 °C to 125 °C	48-pin LQFP exposed pad	0	0	0.5 A	Linear	by SPI	1	0	[1][2]
MC33FS4500LAE MC33FS4500LKE			0	0	0.5 A	Linear	by SPI	1	1	
MC33FS4500NAE MC33FS4500NKE			0	0	0.5 A	Linear	by SPI	0	0	
MC33FS4501CAE MC33FS4501CKE			1	0	0.5 A	Linear	by SPI	1	0	
MC33FS4501NAE MC33FS4501NKE			1	0	0.5 A	Linear	by SPI	0	0	
MC33FS4502CAE MC33FS4502CKE			0	1	0.5 A	Linear	by SPI	1	0	
MC33FS4502LAE MC33FS4502LKE			0	1	0.5 A	Linear	by SPI	1	1	

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 2. Orderable part variations*...continued*

Part Number	Temperature (T_A)	Package	FS1B	LDT	VCORE	VCORE type	VKAM on	CAN FD	LIN	Notes
MC33FS4502NAE MC33FS4502NKE			0	1	0.5 A	Linear	by SPI	0	0	
MC33FS4503CAE MC33FS4503CKE			1	1	0.5 A	Linear	by SPI	1	0	
MC33FS4503NAE MC33FS4503NKE			1	1	0.5 A	Linear	by SPI	0	0	
MC33FS6500CAE MC33FS6500CKE			0	0	0.8 A	DC-DC	by SPI	1	0	
MC33FS6500LAE MC33FS6500LKE			0	0	0.8 A	DC-DC	by SPI	1	1	
MC33FS6500NAE MC33FS6500NKE			0	0	0.8 A	DC-DC	by SPI	0	0	
MC33FS6501CAE MC33FS6501CKE			1	0	0.8 A	DC-DC	by SPI	1	0	
MC33FS6501NAE MC33FS6501NKE			1	0	0.8 A	DC-DC	by SPI	0	0	
MC33FS6502CAE MC33FS6502CKE			0	1	0.8 A	DC-DC	by SPI	1	0	
MC33FS6502LAE MC33FS6502LKE			0	1	0.8 A	DC-DC	by SPI	1	1	
MC33FS6502NAE MC33FS6502NKE			0	1	0.8 A	DC-DC	by SPI	0	0	
MC33FS6503CAE MC33FS6503CKE			1	1	0.8 A	DC-DC	by SPI	1	0	
MC33FS6503NAE MC33FS6503NKE			1	1	0.8 A	DC-DC	by SPI	0	0	
MC33FS6504LAE MC33FS6504LKE			0	1	0.8 A	DC-DC	by default	1	1	
MC33FS6510CAE MC33FS6510CKE			0	0	1.5 A	DC-DC	by SPI	1	0	
MC33FS6510LAE MC33FS6510LKE			0	0	1.5 A	DC-DC	by SPI	1	1	
MC33FS6510NAE MC33FS6510NKE			0	0	1.5 A	DC-DC	by SPI	0	0	
MC33FS6511CAE MC33FS6511CKE			1	0	1.5 A	DC-DC	by SPI	1	0	
MC33FS6511NAE MC33FS6511NKE			1	0	1.5 A	DC-DC	by SPI	0	0	
MC33FS6512CAE MC33FS6512CKE			0	1	1.5 A	DC-DC	by SPI	1	0	
MC33FS6512LAE MC33FS6512LKE			0	1	1.5 A	DC-DC	by SPI	1	1	
MC33FS6512NAE MC33FS6512NKE			0	1	1.5 A	DC-DC	by SPI	0	0	
MC33FS6513CAE MC33FS6513CKE			1	1	1.5 A	DC-DC	by SPI	1	0	
MC33FS6513NAE MC33FS6513NKE			1	1	1.5 A	DC-DC	by SPI	0	0	
MC33FS6514LAE MC33FS6514LKE			0	1	1.5 A	DC-DC	by default	1	1	
MC33FS6520CAE MC33FS6520CKE			0	0	2.2 A	DC-DC	by SPI	1	0	

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 2. Orderable part variations...*continued*

Part Number	Temperature (T_A)	Package	FS1B	LDT	VCORE	VCORE type	VKAM on	CAN FD	LIN	Notes
MC33FS6520LAE MC33FS6520LKE			0	0	2.2 A	DC-DC	by SPI	1	1	
MC33FS6520NAE MC33FS6520NKE			0	0	2.2 A	DC-DC	by SPI	0	0	
MC33FS6521CAE MC33FS6521CKE			1	0	2.2 A	DC-DC	by SPI	1	0	
MC33FS6521NAE MC33FS6521NKE			1	0	2.2 A	DC-DC	by SPI	0	0	
MC33FS6522CAE MC33FS6522CKE			0	1	2.2 A	DC-DC	by SPI	1	0	
MC33FS6522LAE MC33FS6522LKE			0	1	2.2 A	DC-DC	by SPI	1	1	
MC33FS6522NAE MC33FS6522NKE			0	1	2.2 A	DC-DC	by SPI	0	0	
MC33FS6523CAE MC33FS6523CKE			1	1	2.2 A	DC-DC	by SPI	1	0	
MC33FS6523NAE MC33FS6523NKE			1	1	2.2 A	DC-DC	by SPI	0	0	

[1] To order parts in tape and reel, add the R2 suffix to the part number.
[2] LIN and FS1B functions are exclusive. The differentiation is made by part numbers. When LIN is available, FS1B is not, and vice versa. VKAM on by default is available on certain part numbers only.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

6 Block diagram

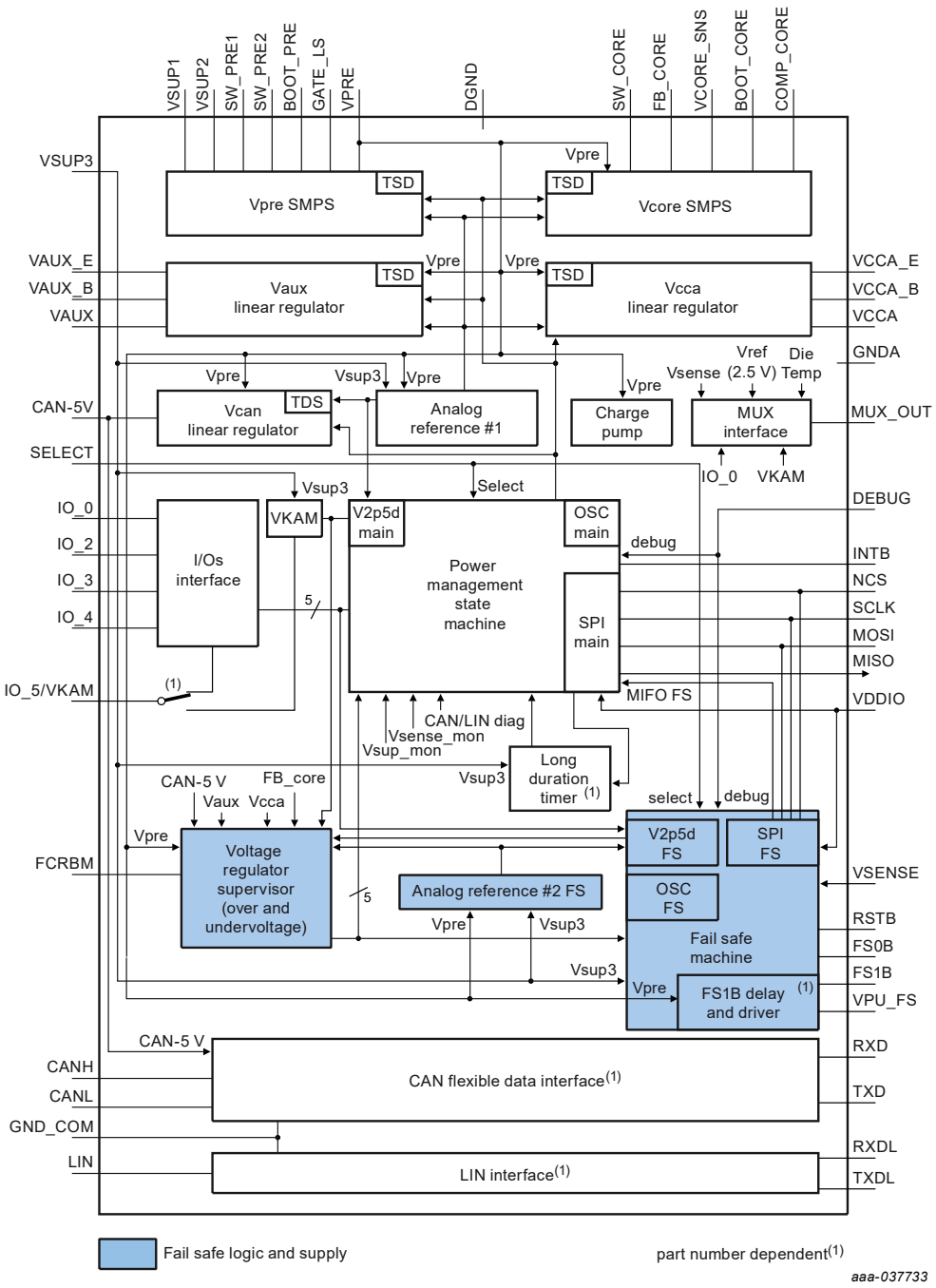


Figure 4. FS6500/FS4500 with CAN and LIN simplified internal block diagram

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

7 Pinning information

7.1 Pinning information

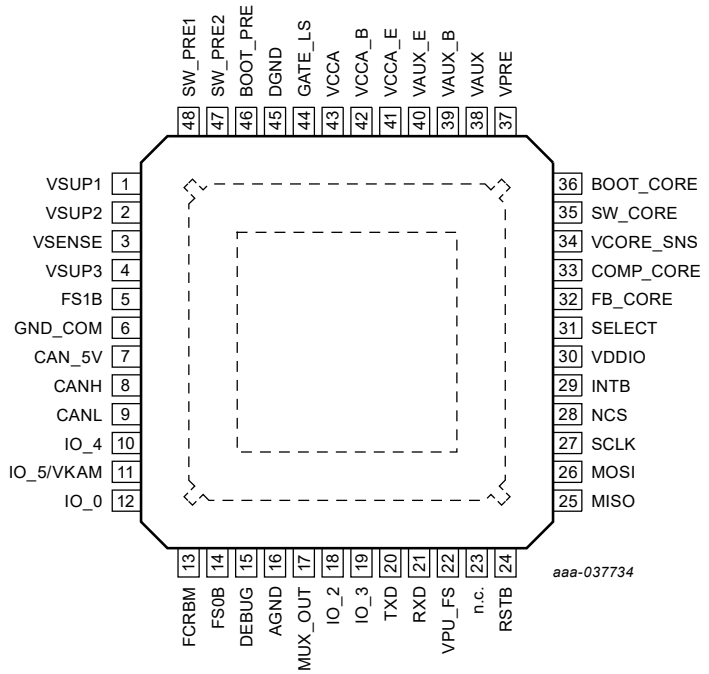


Figure 5. FS6500 pinout with CAN and FS1B

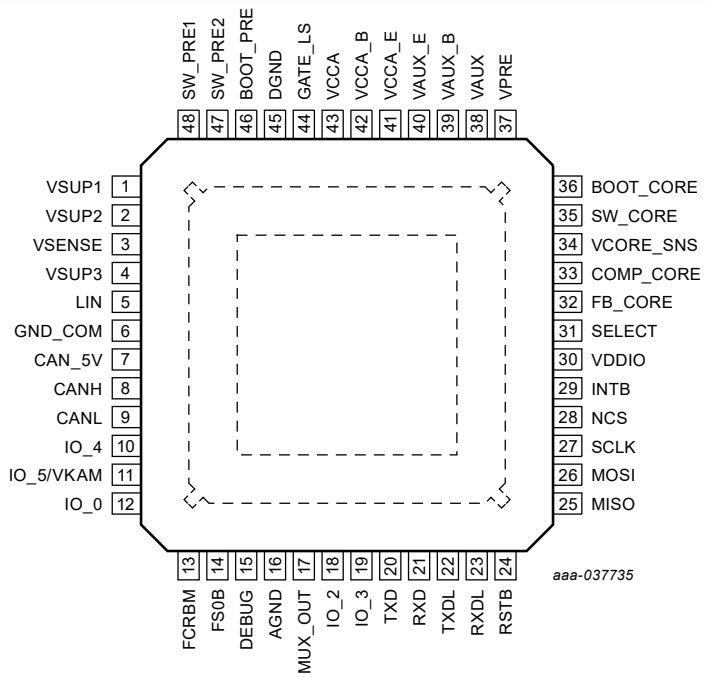


Figure 6. FS6500 pinout with CAN and LIN

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

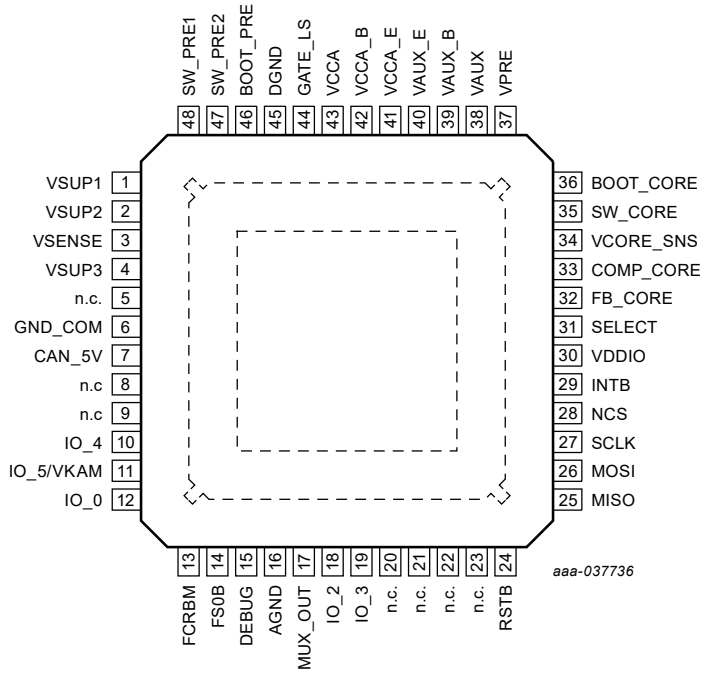


Figure 7. FS6500 pinout without CAN, without LIN

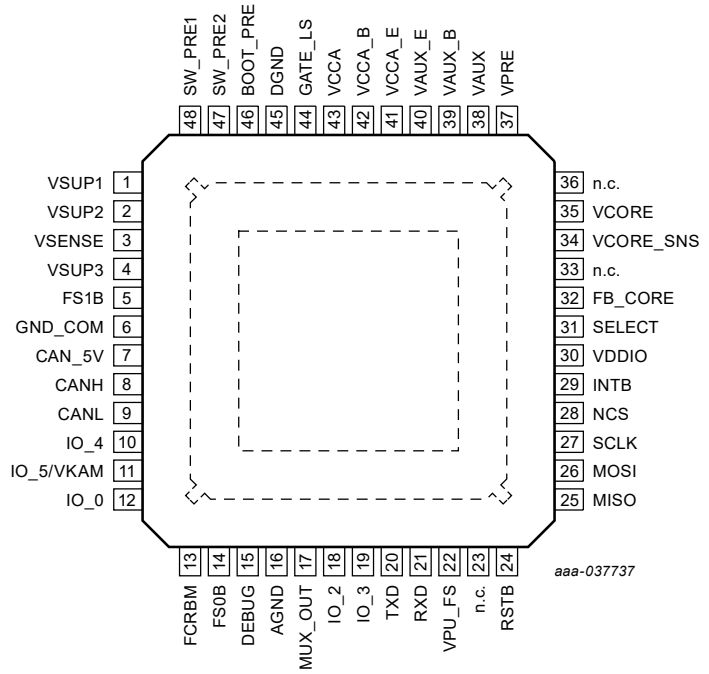


Figure 8. FS4500 pinout with CAN and FS1B

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

7.2 Pin description

A functional description of each pin can be found in Section 11.

Table 3. FS6500/FS4500 pin definition

Pin number	Pin name	Type	Definition
1	VSUP1	A_IN	Power supply of the device. An external reverse battery protection diode in series is mandatory
2	VSUP2	A_IN	Second power supply. Protected by the external reverse battery protection diode used for VSUP1. VSUP1 and VSUP2 must be connected together externally.
3	VSENSE	A_IN	Sensing of the battery voltage. Must be connected prior to the reverse battery protection diode.
4	VSUP3	A_IN	Third power supply dedicated to the device supply. Protected by the external reverse battery protection diode used for VSUP1. Must be connected between the reverse protection diode and the input PI filter.
5	LIN	A_IN/OUT	LIN single-wire bus transmitter and receiver.
	or FS1B	D_OUT	Second output of the safety block (active low). The pin is asserted low at start-up and when a fault condition is detected, with a configurable delay or duration versus FS0B output terminal. Open drain structure.
	LIN and FS1B functions are exclusive. The differentiation is made by part numbers. When LIN is available, FS1B is not, and vice versa. If neither LIN, nor FS1B functions are used, this pin must be left open.		
6	GND_COM	GROUND	Dedicated ground for physical layers
7	CAN_5V	A_OUT	Output voltage for the embedded CAN FD interface
8	CANH	A_IN/OUT	CAN output high. If CAN function is not used, this pin must be left open.
9	CANL	A_IN/OUT	CAN output low. If CAN function is not used, this pin must be left open.
10	IO_4	D_IN A_OUT	Can be used as digital input (load dump proof) with wake-up capability or as an output gate driver **Digital input**: Pin status can be read through the SPI. Can be used to monitor error signals from another IC for safety purposes (when used with IO_5). **Wake-up capability:** Can be selectable to wake-up on edges or levels. **Output gate driver:** Can drive a logic level low-side NMOS transistor. Controlled by the SPI.
11	IO_5/VKAM	A_IN D_IN A_OUT	Can be used as digital input with wake-up capability or as an analog output providing keep alive memory supply in low-power mode. **Analog input**: Pin status can be read through the MUX output terminal **Digital input**: Pin status can be read through the SPI. Can be used to monitor error signals from another IC for safety purposes (when used with IO_4). **Wake-up capability:** Can be selectable to wake-up on edges or levels. **Supply output:** Provide keep alive memory supply in low-power mode
	VKAM can be enabled or disabled by default at power up. The differentiation is made by part numbers.		
12	IO_0	A_IN D_IN	Can be used as analog or digital input (load dump proof) with wake-up capability (selectable) **Analog input**: Pin status can be read through the MUX output terminal **Digital input:** Pin status can be read through the SPI. **Wake-up capability:** Can be selectable to wake-up on edges or levels.
13	FCRBM	A_IN	Feedback core resistor bridge monitoring: For safety purposes, this pin is used to monitor the middle point of a redundant resistor bridge connected on V_{CORE} (in

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 3. FS6500/FS4500 pin definition*...continued*

Pin number	Pin name	Type	Definition
			parallel to the one used to set the V_{CORE} voltage). If not used, this pin must be connected directly to FB_CORE.
14	FS0B	D_OUT	First output of the safety block (active low). The pin is asserted low at start-up and when a fault condition is detected. Open drain structure.
15	DEBUG	D_IN	Debug mode entry input
16	AGND	GROUND	Analog ground connection
17	MUX_OUT	A_OUT	Multiplexed output to be connected to a MCU ADC. Selection of the analog parameter is available at MUX-OUT through the SPI.
18 19	IO_2:3	D_IN	Digital input pin with wake-up capability (logic level compatible) **Digital input**: Pin status can be read through the SPI. Can be used to monitor FCCU error signals from MCU for safety purposes. **Wake-up capability:** Can be selectable to wake-up on edges or levels.
20	TXD	D_IN	Transceiver input from the MCU which controls the state of the CAN-bus. Internal pull-up to VDDIO. If CAN function is not used, this pin must be left open.
21	RXD	D_OUT	Receiver output which reports the state of the CAN-bus to the MCU If CAN function is not used, this pin must be left open.
22	TXDL	D_IN	Transceiver input from the MCU controlling the state of the LIN bus. Internal pull-up to VDDIO.
	or VPU_FS	A_OUT	Pull-up output for FS1B function.
	LIN and FS1B functions are exclusive. The differentiation is made by part numbers. When LIN is available, FS1B is not, and vice versa. If neither LIN, nor FS1B functions are used, this pin must be left open.		
23	RXDL	D_OUT	Receiver output reporting the state of the LIN bus to the MCU. If LIN function is not used, this pin must be left open.
24	RSTB	D_OUT	This output is asserted low when the safety block reports a failure. The main function is to reset the MCU. Reset input voltage is also monitored in order to detect external reset and fault condition. Open drain structure.
25	MISO	D_OUT	SPI bus. primary input secondary output
26	MOSI	D_IN	SPI bus. primary output secondary input
27	SCLK	D_IN	SPI Bus. Serial clock
28	NCS	D_IN	Not chip select (active low)
29	INTB	D_OUT	This output pin generates a low pulse when an Interrupt condition occurs. Pulse duration is configurable. Internal pull-up to VDDIO.
30	VDDIO	A_IN	Input voltage for MISO output buffer. Allows voltage compatibility with MCU I/Os.
31	SELECT	D_IN	Hardware selection pin for VAUX and VCCA output voltages
32	FB_CORE	A_IN	VCORE voltage feedback. Input of the error amplifier.
33	COMP_CORE	A_OUT	Compensation network. Output of the error amplifier. For FS4500 series, this pin must be left open (NC).
34	VCORE_SNS	A_IN	VCORE input voltage sense

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 3. FS6500/FS4500 pin definition*...continued*

Pin number	Pin name	Type	Definition
35	SW_CORE	A_OUT	VCORE output switching point for FS6500 series
	or VCORE	A_OUT	VCORE output voltage for FS4500 series
36	BOOT_ CORE	A_IN/OUT	Bootstrap capacitor for VCORE internal NMOS gate drive For FS4500 series, this pin must be left open (NC).
37	VPRE	A_IN	VPRE input voltage sense
38	VAUX	A_OUT	VAUX output voltage. External PNP ballast transistor. Collector connection
39	VAUX_B	A_OUT	VAUX voltage regulator. External PNP ballast transistor. Base connection
40	VAUX_E	A_OUT	VAUX voltage regulator. External PNP ballast transistor. Emitter connection
41	VCCA_E	A_OUT	VCCA voltage regulator. External PNP ballast transistor. Emitter connection
42	VCCA_B	A_OUT	VCCA voltage regulator. External PNP ballast transistor. Base connection
43	VCCA	A_OUT	VCCA output voltage. External PNP ballast transistor. Collector connection
44	GATE_LS	A_OUT	Low-side MOSFET gate drive for non-inverting buck-boost configuration
45	DGND	GROUND	Digital ground connection
46	BOOT_PRE	A_IN/OUT	Bootstrap capacitor for the VPRE internal NMOS gate drive
47	SW_PRE2	A_OUT	Second pre-regulator output switching point
48	SW_PRE1	A_OUT	First pre-regulator output switching point

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

8 Maximum ratings

Table 4. Maximum ratings

All voltages are with respect to ground, unless otherwise specified. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Electrical ratings				
$V_{SUP1/2/3}$	DC voltage at power supply pins	–1.0 to 40	V	[1]
V_{SENSE}	DC voltage at battery sense pin (with ext R in series mandatory)	–14 to 40	V	
$V_{SW1,2}$	DC voltage at SW_PRE1 and SW_PRE2 Pins	–1.0 to 40	V	
V_{PRE}	DC voltage at VPRE Pin	–0.3 to 8	V	
V_{GATE_LS}	DC voltage at Gate_LS pin	–0.3 to 8	V	
V_{BOOT_PRE}	DC voltage at BOOT_PRE pin	–1.0 to 50	V	
V_{SW_CORE}	DC voltage at SW_CORE pin	–1.0 to 8	V	
V_{CORE_SNS}	DC voltage at VCORE_SNS pin	0.0 to 8	V	
V_{BOOT_CORE}	DC voltage at BOOT_CORE pin	0.0 to 15	V	
V_{FB_CORE}	DC voltage at FB_CORE pin	–0.3 to 2.5	V	
V_{COMP_CORE}	DC voltage at COMP_CORE pin	–0.3 to 2.5	V	
V_{FCRBM}	DC voltage at FCRBM pin	–0.3 to 8	V	
$V_{AUX_B,E}$	DC voltage at VAUX_B, VAUX_E pins	–0.3 to 40	V	
V_{AUX}	DC voltage at VAUX pin	–2.0 to 40	V	
$V_{CCA_B,E}$	DC voltage at VCCA_B, VCCA_E pins	–0.3 to 8	V	
V_{CCA}	DC voltage at VCCA pin	–0.3 to 8	V	
V_{DDIO}	DC voltage at VDDIO pin	–0.3 to 8	V	
V_{CAN_5V}	DC voltage on CAN_5V pin	–0.3 to 8	V	
V_{PU_FS}	DC voltage at VPU_FS pin	–0.3 to 8	V	
V_{FSxB}	DC voltage at FS0B, FS1B pins (with ext R in series mandatory)	–0.3 to 40	V	
V_{DEBUG}	DC voltage at DEBUG pin	–0.3 to 40	V	
$V_{IO_0,4}$	DC voltage at IO_0, IO_4 pins (with ext R in series mandatory)	–0.3 to 40	V	
V_{IO_5}	DC voltage at IO_5 pin	–0.3 to 20	V	
V_{KAM}	DC voltage at VKAM pin	–0.3 to 8	V	
V_{DIG}	DC voltage at INTB, RSTB, MISO, MOSI, NCS, SCLK, MUX_OUT, RXD, TXD, RXDL, TXDL, IO_2, IO_3 pins	–0.3 to 8	V	
V_{SELECT}	DC voltage at SELECT pin	–0.3 to 8	V	
V_{BUS_CAN}	DC voltage on CANL, CANH pins	–27 to 40	V	
V_{BUS_LIN}	DC voltage on LIN pin	–18 to 40	V	
I_Isense	V_{SENSE} maximum current capability	–5.0 to 5.0	mA	
$I_IO_{0,4,5}$	IOs maximum current capability (IO_0, IO_4, IO_5)	–5.0 to 5.0	mA	
ESD voltage				
Human body model (JESD22/A114)[(19)] – 100 pF, 1.5 kΩ				
$V_{ESD-HBM1}$	• All pins	±2.0	kV	[2]
$V_{ESD-HBM2}$	• VSUP1, 2, 3, VSENSE, VAUX, IO_0,4, FS0B, FS1B, DEBUG	±4.0	kV	
$V_{ESD-HBM3}$	• CANH, CANL	±6.0	kV	

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 4. Maximum ratings *...continued*

All voltages are with respect to ground, unless otherwise specified. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
$V_{ESD-HBM4}$	• LIN	±8.0	kV	
Charge device model (JESD22/C101)[20]:				
$V_{ESD-CDM1}$	• All pins	±500	V	
$V_{ESD-CDM2}$	• Corner pins	±750	V	
System level ESD (gun test)				
	• VSUP1, 2, 3, VSENSE, VAUX, IO_0, 4, 5, FS0B, FS1B			
$V_{ESD-GUN1}$	330 Ω/150 pF unpowered according to IEC 61000-4-2:[16]	±8.0	kV	
$V_{ESD-GUN2}$	330 Ω/150 pF unpowered according to OEM LIN, CAN, FlexRay Conformance	±8.0	kV	
$V_{ESD-GUN3}$	2.0 kΩ/150 pF unpowered according to ISO 10605[15]	±8.0	kV	
$V_{ESD-GUN4}$	2.0 kΩ/330 pF powered according to ISO 10605[15]	±8.0	kV	
	• CANH, CANL			
$V_{ESD-GUN5}$	330 Ω/150 pF unpowered according to IEC 61000-4-2:[16]	±15.0	kV	
$V_{ESD-GUN6}$	330 Ω/150 pF unpowered according to OEM LIN, CAN, FlexRay Conformance	±12.0	kV	
$V_{ESD-GUN7}$	2.0 kΩ/150 pF unpowered according to ISO 10605[15]	±15.0	kV	
$V_{ESD-GUN8}$	2.0 kΩ/330 pF powered according to ISO 10605[15] • LIN	±12.0	kV	
	• LIN			
$V_{ESD-GUN9}$	330 Ω/150 pF unpowered according to IEC 61000-4-2:[16]	±12.0	kV	
$V_{ESD-GUN10}$	330 Ω/150 pF unpowered according to OEM LIN, CAN, FlexRay conformance	±12.0	kV	
$V_{ESD-GUN11}$	2.0 kΩ/150 pF unpowered according to ISO 10605[15]	±12.0	kV	
$V_{ESD-GUN12}$	2.0 kΩ/330 pF powered according to ISO 10605[15]	±12.0	kV	
Thermal ratings				
T_A	Ambient temperature	–40 to 125	°C	
T_J	Junction temperature	–40 to 150	°C	
T_{STG}	Storage temperature	–55 to 150	°C	
Thermal resistance				
$R_{\theta JA}$	Thermal resistance junction to ambient	30	°C/W	[3]
$R_{\theta JCTOP}$	Thermal resistance junction to case top	23.8	°C/W	[4]
$R_{\theta JCBOTTOM}$	Thermal resistance junction to case bottom	0.9	°C/W	[5]

[1] All V_{SUPS} ($V_{SUP1/2/3}$) must be connected to the same supply (Figure 73).
[2] Compared to AGND.
[3] Per JEDEC JESD51-6[17] with the board (JESD51-7)[18] horizontal.
[4] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC - 883 Method 1012.1)[21].
[5] Thermal resistance between the die and the solder pad on the bottom of the packaged based on simulation without any interface resistance.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

9 Static electrical characteristics

Table 5. Static electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP_UV_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 36 V, thermal dissipation must be considered (see Figure 32).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Power supply						
I_{SUP123}	Power supply current in normal mode	—	—	15.0	mA	
I_{SUP3}	Power supply current for VSUP3 in normal mode	—	3.5	5.0	mA	
I_{SUP_LPOFF1}	Power supply current in LPOFF (V_{SUP} = 14 V at T_A = 25 °C)	—	32	—	µA	[1]
I_{SUP_LPOFF2}	Power supply current in LPOFF (V_{SUP} = 18 V at T_A = 80 °C)	—	42	60	µA	
V_{SNS_UV}	Power supply undervoltage warning	7.0	8.0	9.0	V	
$V_{SNS_UV_HYST}$	Power supply undervoltage warning hysteresis	0.1	—	0.5	V	
V_{SUP_IPFF}	I_{PFF} input voltage detection	21	—	27	V	
$V_{SUP_IPFF_HYST}$	I_{PFF} input voltage hysteresis	0.2	—	—	V	
$V_{SUP_UV_7}$	Power supply undervoltage lockout (power up)	7.0	—	8.0	V	
$V_{SUP_UV_5}$	Power supply undervoltage lockout (power up)	—	—	5.6	V	
$V_{SUP_UV_L}$	Power supply undervoltage lockout (falling — boost configuration)	—	—	2.7	V	
$V_{SUP_UV_L_B}$	Power supply undervoltage lockout (falling — buck configuration)	—	—	4.5	V	[2]
$V_{SUP_UV_LPOFF}$	Power supply undervoltage lockout in LPOFF	—	—	4.5	V	[3]
$V_{SUP_UV_HYST}$	Power supply undervoltage lockout hysteresis	—	0.1	—	V	[4]
V_{PRE} voltage pre-regulator						
V_{PRE}	V_{PRE} output voltage				V	
	• Buck mode (V_{SUP} > $V_{SUP_UV_7}$)	6.25	—	6.75		
	• Buck mode ($V_{SUP_UV_7}$ ≥ V_{SUP} ≥ 4.5 V)	$V_{PRE_UV_4P3}$	V_{SUP} – $R_{DS(on)_PRE}$ * I_{PRE}	—		
	• Boost mode (V_{SUP} ≥ 2.7 V)	6.0	—	7.0		
I_{PRE}	V_{PRE} maximum output current capability				A	[4]
	• Buck or boost with V_{SUP} > $V_{SUP_UV_7}$	2.0	—	—		
	• Buck with $V_{SUP_UV_7}$ ≥ V_{SUP} ≥ 4.5 V	0.5	2.0	—		
	• Boost with $V_{SUP_UV_7}$ ≥ V_{SUP} ≥ 6.0 V	2.0	—	—		
	• Boost with 6.0 V ≥ V_{SUP} ≥ 4.0 V	1.0	—	—		
	• Boost with 4.0 V ≥ V_{SUP} ≥ 2.7 V	0.3	—	—		
I_{PRE_LIM1}	SW_PRE output current limitation in buck–boost mode (V_{SUP} ≤ 28 V)	3.5	—	—	A	
I_{PRE_LIM2}	SW_PRE output current limitation in buck mode (V_{SUP} ≤ 28 V)	2.5	—	—	A	
I_{PRE_OC}	SW_PRE overcurrent detection threshold in buck mode (V_{SUP} ≤ 28 V)	4.5	—	—	A	
V_{PRE_UV}	V_{PRE} undervoltage detection threshold (falling)	5.5	—	6.0	V	
$V_{PRE_UV_HYST}$	V_{PRE} undervoltage hysteresis	0.05	—	0.15	V	[5]
$V_{PRE_UV_4P3}$	V_{PRE} shut-off threshold (falling – buck and buck/boost)	4.1	—	4.5	V	

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 5. Static electrical characteristics *...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP_UV_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 36 V, thermal dissipation must be considered (see Figure 32).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
$V_{PRE_UV_4P3_HYST}$	V_{PRE} shut-off hysteresis	0.05	—	0.15	V	[5]
R_{DSON_PRE}	V_{PRE} pass transistor on resistance with V_{SUP} ≤ 28 V	—	—	200	mΩ	
L_{IR_VPRE}	V_{PRE} line regulation	—	20	—	mV	[5]
LOR_{VPRE_BUCK}	V_{PRE} load regulation for C_{OUT_VPRE} = 57 µF • I_{PRE} from 50 mA to 2.0 A - buck mode	—	100	—	mV	[5]
LOR_{VPRE_BOOST}	V_{PRE} load regulation for C_{OUT_VPRE} = 57 µF • I_{PRE} from 50 mA to 2.0 A - boost mode	—	500	—	mV	[5]
$V_{PRE_LL_H}$ $V_{PRE_LL_L}$	V_{PRE} pulse skipping thresholds	— —	200 180	— —	mV	
T_{WARN_PRE}	V_{PRE} thermal warning threshold	—	125	—	°C	
T_{SD_PRE}	V_{PRE} thermal shutdown threshold	160	—	—	°C	
$T_{SD_PRE_HYST}$	V_{PRE} thermal shutdown hysteresis	—	10	—	°C	[5]
$V_{G_LS_OH}$	LS gate driver high output voltage (I_{OUT} = 50 mA)	V_{PRE} – 1	—	V_{PRE}	V	
$V_{G_LS_OL}$	LS gate driver low level (I_{OUT} = 50 mA)	—	—	0.5	V	
I_{G_LS}	LS gate driver current capability	—	300	—	mA	
R_{G_SHORT}	GATE_LS pin short to GND resistance to detect buck mode only	—	—	10	Ω	
V_{core} voltage regulator						
V_{CORE_FB}	V_{CORE} feedback input voltage	0.784	0.8	0.816	V	
I_{PD_CORE}	V_{CORE} internal pull-down current (active when $V_{COR\ E}$ is enabled)	5.0	12	25	mA	
I_{CORE}	V_{CORE} output current capability in normal mode • FS450x • FS650x • FS651x • FS652x	 — — — —	 — — — —	 0.5 0.8 1.5 2.2	 A	
I_{CORE_LIM}	V_{CORE} output current limitation • FS450x • FS650x • FS651x • FS652x	 0.55 1 1.8 2.5	 — — — —	 1.7 2 2.8 3.5	 A	
R_{DSON_CORE}	V_{CORE} pass transistor on resistance	—	—	200	mΩ	
FS65_ $LOR_{VCORE_1.2}$	V_{CORE} transient load regulation – 1.2 V range C_{OUT_VCORE} = 40 µF, I_{CORE} = 10 mA to 2.2 A, dI_{CORE}/dt ≤ 2.0 A/µs	–60	—	60	mV	[4]
FS65_ $LOR_{VCORE_3.3}$	V_{CORE} transient load regulation – 3.3 V range C_{OUT_VCORE} = 40 µF, I_{CORE} = 10 mA to 1.5 A, dI_{CORE}/dt ≤ 2.0 A/µs	–100	—	100	mV	[4]
FS65_ LOR_{VCORE_5}	V_{CORE} transient load regulation – 5.0 V range C_{OUT_VCORE} = 20 µF, I_{CORE} = 10 mA to 0.8 A, dI_{CORE}/dt ≤ 2.0 A/µs	–150	—	150	mV	[4]
FS45_ $LOR_{VCORE_1.2}$	V_{CORE} transient load regulation – 1.2 V range C_{OUT_VCORE} = 20 µF, I_{CORE} = 10 mA to 0.2 A, dI_{CORE}/dt ≤ 0.5 A/µs	–60	—	60	mV	[4]

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 5. Static electrical characteristics *...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP_UV_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 36 V, thermal dissipation must be considered (see Figure 32).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
FS45_ $LOR_{VCORE_3.3}$	V_{CORE} transient load regulation – 3.3 V range C_{OUT_VCORE} = 20 µF, I_{CORE} = 10 mA to 0.35 A, dI_{CORE}/dt ≤ 0.5 A/µs	–100	—	100	mV	[4]
FS45_ LOR_{VCORE_5}	V_{CORE} transient load regulation – 5 V range C_{OUT_VCORE} = 20 µF, I_{CORE} = 10 mA to 0.5 A, dI_{CORE}/dt ≤ 0.5 A/µs	–150	—	150	mV	[4]
$V_{CORE_LL_H}$ $V_{CORE_LL_L}$	V_{CORE} pulse skipping thresholds	— —	180 160	— —	mV	
T_{WARN_CORE}	V_{CORE} thermal warning threshold	—	125	—	°C	
T_{SD_CORE}	V_{CORE} thermal shutdown threshold	160	—	—	°C	
$T_{SD_CORE_HYST}$	V_{CORE} thermal shutdown hysteresis	—	10	—	°C	[4]
V_{CCA} voltage regulator						
V_{CCA}	V_{CCA} output voltage • 5.0 V configuration with Internal ballast at 100 mA • 5.0 V configuration with external ballast at 200 mA • 5.0 V configuration with external ballast at 300 mA • 3.3 V configuration with Internal ballast at 100 mA • 3.3 V configuration with external ballast at 200 mA • 3.3 V configuration with external ballast at 300 mA	 4.95 4.9 4.85 3.267 3.234 3.201	 5.0 5.0 5.0 3.3 3.3 3.3	 5.05 5.1 5.15 3.333 3.366 3.399	V	[6]
I_{CCA_IN}	V_{CCA} output current (int. MOSFET)	—	—	100	mA	
I_{CCA_OUT}	V_{CCA} output current (external PNP)	—	—	300	mA	
$I_{CCA_LIM_INT}$	V_{CCA} output current limitation (int. MOSFET)	100	—	675	mA	
$I_{CCA_LIM_OUT}$	V_{CCA} output current limitation (external PNP)	300	—	675	mA	
$I_{CCA_LIM_FB}$	V_{CCA} output current limitation foldback	60	—	240	mA	
$V_{CCA_LIM_FB}$	V_{CCA} output voltage foldback threshold	0.6	—	1.2	V	
$V_{CCA_LIM_HYST}$	V_{CCA} output voltage foldback hysteresis	0.03	—	0.3	V	
$I_{CCA_BASE_SC}$ $I_{CCA_BASE_SK}$	V_{CCA} base current capability	— 20	–20 65	–30 —	mA	
T_{WARN_CCA}	V_{CCA} thermal warning threshold (int. MOSFET only)	—	125	—	°C	
TSD_{CCA}	V_{CCA} thermal shutdown threshold (int. MOSFET only)	160	—	—	°C	
TSD_{CCA_HYST}	V_{CCA} thermal shutdown hysteresis	—	10	—	°C	[5]
LOR_{VCCA}	V_{CCA} static load regulation • I_{CCA} = 10 mA to 100 mA (internal MOSFET) • I_{CCA} = 10 mA to 300 mA (external ballast)	—	15	—	mV	[5]
$LORT_{VCCA}$	V_{CCA} transient load regulation • I_{CCA} = 10 mA to 100 mA (internal MOSFET) • I_{CCA} = 10 mA to 300 mA (external ballast)	—	—	1.0	%	[5]
R_{PD_CCA}	V_{CCA} internal pull-down resistor (active when V_{CCA} is disabled)	50	—	170	Ω	
V_{AUX} voltage regulator						
V_{AUX_5}	V_{AUX} output voltage (5.0 V configuration)	4.85	5.0	5.15	V	
V_{AUX_33}	V_{AUX} output voltage (3.3 V configuration)	3.2	3.3	3.4	V	
V_{AUX_TRK}	V_{AUX} tracking error (V_{AUX_5} and V_{AUX_33})	–15	—	+15	mV	
I_{AUX_OUT}	V_{AUX} output current	—	—	400	mA	

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 5. Static electrical characteristics *...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP_UV_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 36 V, thermal dissipation must be considered (see Figure 32).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
I_{AUX_LIM}	V_{AUX} output current limitation	400	—	800	mA	
$I_{AUX_LIM_FB}$	V_{AUX} output current limitation foldback	60	—	240	mA	
$V_{AUX_LIM_FB}$	V_{AUX} output voltage foldback threshold	0.6	—	1.2	V	
$V_{AUX_LIM_HYST}$	V_{AUX} output voltage foldback hysteresis	0.03	—	0.3	V	
$I_{AUX_BASE_SC}$ $I_{AUX_BASE_SK}$	V_{AUX} base current capability	— 7.0	–15 30	–7.0 —	mA	
TSD_{AUX}	V_{AUX} thermal shutdown threshold	160	—	—	°C	
TSD_{AUX_HYST}	V_{AUX} thermal shutdown hysteresis	—	10	—	°C	[5]
LOR_{VAUX}	V_{AUX} static load regulation (I_{AUX_OUT} = 10 mA to 400 mA)	—	15	—	mV	[5]
$LORT_{VAUX}$	V_{AUX} transient load regulation • I_{AUX_OUT} = 10 mA to 400 mA	—	—	1.0	%	[5]
R_{PD_AUX}	V_{AUX} internal pull-down resistor (active when V_{AUX} is disabled)	50	—	170	Ω	
CAN_5V voltage regulator						
V_{CAN}	V_{CAN} output voltage V_{SUP} > 6.0 V in buck mode V_{SUP} > $V_{SUP_UV_L}$ in boost mode	4.8	5.0	5.2	V	
I_{CAN_OUT}	V_{CAN} output current	—	—	100	mA	
I_{CAN_LIM}	V_{CAN} output current limitation	100	—	250	mA	
TSD_{CAN}	V_{CAN} thermal shutdown threshold	160	—	—	°C	
TSD_{CAN_HYST}	V_{CAN} thermal shutdown hysteresis	—	10	—	°C	[5]
V_{CAN_UV}	V_{CAN} undervoltage detection threshold	4.25	—	4.8	V	
$V_{CAN_UV_HYST}$	V_{CAN} undervoltage hysteresis	0.07	—	0.22	V	
V_{CAN_OV}	V_{CAN} overvoltage detection threshold (rising)	5.2	—	5.85	V	
$V_{CAN_OV_HYST}$	V_{CAN} overvoltage hysteresis	0.07	—	0.22	V	
LOR_{VCAN}	V_{CAN} transient load regulation • I_{CAN_OUT} = 0 mA to 50 mA	—	100	—	mV	[5]
VKAM voltage regulator						
V_{KAM}	V_{KAM} output voltage	3.0	3.5	4.0	V	
I_{KAM_OUT}	V_{KAM} output current	—	—	3.0	mA	
I_{KAM_LIM}	V_{KAM} output current limitation	4.0	—	10.0	mA	
I_{SUP_KAM}	V_{KAM} current consumption from V_{SUP3} • I_{KAM_OUT} = 0 mA • I_{KAM_OUT} < 1.0 mA • 1.0 mA < I_{KAM_OUT} < 3.0 mA	 — — —	 — — —	 25 150 2.15	 µA µA mA	
Long duration timer						
I_{LDT}	Timer current consumption (from V_{SUP3})	—	5.0	10	µA	
Fail-safe machine voltage supervisor						
V_{PRE_OV}	V_{PRE} overvoltage detection threshold	7.2	—	8.0	V	
$V_{PRE_OV_HYST}$	V_{PRE} overvoltage hysteresis	—	0.1	—	V	[5]
$V_{CORE_FB_UV}$	V_{CORE} FB undervoltage detection threshold	0.67	—	0.773	V	
$V_{CORE_FB_UV_D}$	V_{CORE} FB undervoltage detection threshold - degraded mode	0.45	—	0.58	V	

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 5. Static electrical characteristics *...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP_UV_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 36 V, thermal dissipation must be considered (see Figure 32).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
$V_{CORE_FB_UV_HYST}$	V_{CORE} FB undervoltage hysteresis	10	—	27	mV	[5]
$V_{CORE_FB_OV}$	V_{CORE} FB overvoltage detection threshold	0.84	—	0.905	V	
$V_{CORE_FB_OV_HYST}$	V_{CORE} FB overvoltage hysteresis	10	—	30	mV	[5]
$V_{CORE_FB_DRIFT}$	V_{CORE_FB} drift versus FCRBM	50	100	150	mV	
$V_{CCA_UV_5}$	V_{CCA} undervoltage detection threshold (5.0 V configuration)	4.5	—	4.75	V	
$V_{CCA_UV_5D}$	V_{CCA} undervoltage detection threshold (degraded 5.0 V)	3.0	—	3.2	V	
$V_{CCA_UV_33}$	V_{CCA} undervoltage detection threshold (3.3 V configuration)	3.0	—	3.2	V	
$V_{CCA_OV_5}$	V_{CCA} overvoltage detection threshold (5.0 V configuration)	5.25	—	5.5	V	
$V_{CCA_OV_33}$	V_{CCA} overvoltage detection threshold (3.3 V configuration)	3.4	—	3.6	V	
$V_{CCA_5_HYST}$	V_{CCA} undervoltage and overvoltage hysteresis (5.0 V configuration)	—	0.105	—	V	[5]
$V_{CCA_33_HYST}$	V_{CCA} undervoltage and overvoltage hysteresis (3.3 V configuration)	—	0.07	—	V	[5]
$V_{AUX_UV_5}$	V_{AUX} undervoltage detection threshold (5.0 V configuration)	4.5	—	4.75	V	
$V_{AUX_UV_5D}$	V_{AUX} undervoltage detection threshold (degraded 5.0 V)	3.0	—	3.2	V	
$V_{AUX_UV_33}$	V_{AUX} undervoltage detection threshold (3.3 V configuration)	3.0	—	3.2	V	
$V_{AUX_OV_5}$	V_{AUX} overvoltage detection threshold (5.0 V configuration)	5.25	—	5.5	V	
$V_{AUX_OV_33}$	V_{AUX} overvoltage detection threshold (3.3 V configuration)	3.4	—	3.6	V	
$V_{AUX_5_HYST}$	V_{AUX} undervoltage and overvoltage hysteresis (5.0 V configuration)	—	0.105	—	V	[5]
$V_{AUX_33_HYST}$	V_{AUX} undervoltage and overvoltage hysteresis (3.3 V configuration)	—	0.07	—	V	[5]
Fail-safe outputs						
V_{RSTB_OL}	Reset low output level (I_RSTB = 2.0 mA)	—	—	0.5	V	
I_{RSTB_LIM}	Reset output current limitation	12	—	25	mA	
V_{RSTB_IL}	Reset low level detection threshold (falling)	1.0	—	—	V	
V_{RSTB_IH}	Reset high level detection threshold (rising)	—	—	2.0	V	
V_{RSTB_HYST}	Reset hysteresis	200	—	—	mV	
$RSTB_{PULL\text{-}DOWN}$	RSTB pull-down resistor	—	1.0	—	MΩ	
V_{FS0B_OL}	FS0B low output level (I_FS0B = 2.0 mA)	—	—	0.5	V	
I_{FS0B_LIM}	FS0B output current limitation	4.0	—	16	mA	
V_{FS0B_IL}	FS0B low level detection threshold (falling)	1.0	—	—	V	
V_{FS0B_IH}	FS0B high level detection threshold (rising)	—	—	2.0	V	
V_{FS0B_HYST}	FS0B hysteresis	100	—	—	mV	
$FS0B_{PULL\text{-}DOWN}$	FS0B pull-down resistor	—	4.0	—	MΩ	
V_{FS1B_OL}	FS1B low output level (I_FS1B = 2.0 mA)	—	—	0.5	V	
I_{FS1B_LIM}	FS1B output current limitation	4.0	—	16	mA	
V_{FS1B_IL}	FS1B low level detection threshold (falling)	1.0	—	—	V	
V_{FS1B_IH}	FS1B high level detection threshold (rising)	—	—	2.0	V	

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 5. Static electrical characteristics *...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP_UV_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 36 V, thermal dissipation must be considered (see Figure 32).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{FS1B_HYST}	FS1B hysteresis	100	—	—	mV	
$FS1B_{PULL\text{-}DOWN}$	FS1B pull-down resistor	—	4.0	—	MΩ	
Fail-safe pull-up						
I_{VPU_FS}	VPU_FS circuitry consumption	—	5.0	10	µA	
$V_{VPU_FS_TH}$	VPU_FS falling threshold to assert FS1B (FS1B_trig)	2.9	3.2	3.5	V	
R_{VPU_FS}	Resistor between VPRE and VPU_FS	—	1.0	1.5	kΩ	[5]
Digital input						
V_{IO_IH}	Digital high input voltage level (IO_0, IO_4, IO_5)	2.6	—	—	V	
V_{IO23_IH}	Digital high input voltage level (IO_2, IO_3)	2.0	—	—	V	
V_{IO_IL}	Digital low input voltage level (IO_0, IO_4, IO_5)	—	—	2.1	V	
V_{IO_HYST}	Input voltage hysteresis (IO_0, IO_4, IO_5)	50	120	500	mV	[5]
V_{IO23_IL}	Digital low input voltage level (IO_2, IO_3)	—	—	0.9	V	
V_{IO23_HYST}	Input voltage hysteresis (IO_2, IO_3)	200	450	700	mV	[5]
$I_{IO_IN_2:4}$	Input current for IO_2, IO_3 and IO_4	–5.0	—	5.0	µA	
$I_{IO_IN_LPOFF}$	Input current for IO_0:5 in LPOFF	–1.0	—	1.0	µA	
Analog input - multi-purpose IOs						
$V_{IO_ANA_WD}$	Measurable input voltage (wide range)	3.0	—	19	V	
$V_{IO_ANA_TG}$	Measurable input voltage (tight range)	3.0	—	9.0	V	
$I_{IO_IN_ANA}$	Input current for IO_0 and IO_5	–5.0	—	100	µA	[7]
Output gate driver (IO_4)						
V_{IO4_OH}	High output level at I_{IO4_OUT} = –2.0 mA	V_{PRE} – 1.5	—	V_{PRE}	V	
V_{IO4_OL}	Low output level at I_{IO4_OUT} = +2.0 mA	0.0	—	1.0	V	
$V_{IO4_OUT_SK}$ $V_{IO4_OUT_SC}$	Output current capability	2.0 —	— —	— –2.0	mA	
Analog multiplexer						
V_{AMUX_ACC}	Voltage sense accuracy (V_{SNS}, IO_0, IO_5) using 5.1 kΩ resistor	–5.0	—	5.0	%	[8]
$V_{AMUX_WD_5}$	Divider ratio (wide input voltage range) at V_{DDIO} = 5.0 V	—	5.0	—		[9]
$V_{AMUX_WD_3P3}$	Divider ratio (wide input voltage range) at V_{DDIO} = 3.3 V	—	7.0	—		20[9]
$V_{AMUX_TG_5}$	Divider ratio (tight input voltage range) at V_{DDIO} = 5.0 V	—	2.0	—		
$V_{AMUX_TG_3P3}$	Divider ratio (tight input voltage range) at V_{DDIO} = 3.3 V	—	3.0	—		
V_{AMUX_REF1}	Internal voltage Reference with 6.0 V < V_{SUP} < 19 V	2.475	2.5	2.525	V	
V_{AMUX_REF2}	Internal voltage reference with V_{SUP} ≤ 6.0 V, or V_{SUP} ≥ 19 V	2.468	2.5	2.532	V	
$V_{AMUX_TP_CO}$	Internal temperature sensor coefficient	—	9.9	—	mV/°C	[5]
V_{AMUX_TP}	Temperature sensor MUX_OUT output voltage (at T_J = 165 °C)	2.08	2.15	2.22	V	
Interrupt						
V_{INTB_OL}	Low output level (I_{INT} = 2.5 mA)	—	—	0.5	V	
R_{PU_INT}	Internal pull-up resistor (connected to VDDIO)	—	10	—	KΩ	
I_{INT_LK}	Input leakage current	—	—	1.0	µA	

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 5. Static electrical characteristics *...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP_UV_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 36 V, thermal dissipation must be considered (see Figure 32).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Digital interface						
$MISO_H$	High output level on MISO (I_{MISO} = 1.5 mA)	V_{DDIO} – 0.4	—	—	V	
$MISO_L$	Low output level on MISO (I_{MISO} = 2.0 mA)	—	—	0.4	V	
I_{MISO}	Tri-state leakage current (V_{DDIO} = 5.0 V)	–5.0	—	5.0	µA	
V_{DDIO}	Supply voltage for MISO output buffer	3.0	—	5.5	V	
IV_{DDIO}	Current consumption on VDDIO	—	1.0	3.0	mA	
SPI_{LK}	SCLK, NCS, MOSI input current	–1.0	—	1.0	µA	
V_{SPI_IH}	SCLK, NCS, MOSI high input threshold	2.0	—	—	V	
V_{SPI_IL}	SCLK, NCS, MOSI low input threshold	—	—	0.8	V	
R_{SPI}	NCS, MOSI internal pull-up (pull-up to VDDIO)	200	400	800	KΩ	
Debug						
V_{DEBUG_IL}	Low input voltage threshold	2.1	2.35	2.8	V	
V_{DEBUG_IH}	High input voltage threshold	4.35	4.6	4.97	V	
I_{DEBUG_LK}	Input leakage current	–10	—	10	µA	
CAN transceiver (FD 2.0 Mbit/s)						
CAN logic input pin (TXD)						
V_{TXD_IH}	TXD high input threshold	0.7 x V_{DDIO}	—	—	V	
V_{TXD_IL}	TXD low input threshold	—	—	0.3 x V_{DDIO}	V	
$TXD_{PULL-UP}$	TXD main device pull-up	20	33	50	KΩ	
TXD_{LK}	TXD input leakage current, V_{TXD} = V_{DDIO}	–1.0	—	1.0	µA	
CAN logic output pin (RXD)						
V_{RXD_OL1}	Low level output voltage (I_{RXD} = 250 µA)	—	—	0.4	V	
V_{RXD_OL2}	Low level output voltage (I_{RXD} = 1.5 mA)	—	—	0.9	V	
$VOUT_{HIGH}$	High level output voltage (I_{RXD} = –250 µA, V_{DDIO} = 3.0 V to 5.5 V)	V_{DDIO} – 0.4	—	—	V	
CAN output pins (CANH, CANL)						
$V_{DIFF_COM_MODE}$	Differential input comparator common mode range in normal mode	–20	—	20	V	
V_{IN_DIFF}	Differential input voltage threshold in normal mode	0.5	—	0.9	V	
$V_{DIFF_COM_SLEEP}$	Differential input comparator common mode range in sleep mode	–12	—	12	V	
$V_{IN_DIFF_SLEEP}$	Differential input voltage threshold in sleep mode	0.4	—	1.1	V	
V_{IN_HYST}	Differential input hysteresis (in TX, RX mode)	50	—	—	mV	
R_{IN_CHCL}	CANH, CANL input resistance	5.0	—	50	kΩ	
R_{IN_DIFF}	CAN differential input resistance	10	—	100	kΩ	
$R_{INSLEEP}$	CANH, CANL input resistance device supplied and in CAN sleep mode	5.0	—	50	kΩ	
R_{IN_MATCH}	Input resistance matching	–3.0	—	3.0	%	

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 5. Static electrical characteristics *...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP_UV_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 36 V, thermal dissipation must be considered (see Figure 32).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
C_{IN_CM}	Common mode input capacitance	—	20	—	pF	[5]
C_{IN_DIFF}	Differential input capacitance	—	10	—	pF	
V_{CANH}	CANH output voltage (45 Ω < R_{BUS} < 65 Ω) • TX dominant state • TX recessive state	 2.75 2.0	 — 2.5	 4.5 3.0	 V	
V_{CANL}	CANL output voltage (45 Ω < R_{BUS} < 65 Ω) • TX dominant state • TX recessive state	 0.5 2.0	 — 2.5	 2.25 3.0	 V	
V_{CAN_SYM}	CAN dominant voltage symmetry (V_{CANL} + V_{CANH})	4.5	5.0	5.5	V	
V_{OH}-V_{OL}	Differential output voltage • TX dominant state (45 Ω < R_{BUS} < 65 Ω) • TX recessive state	 1.5 –50	 2.0 0.0	 3.0 50	 V mV	
$I_{CANL\text{-}SK}$	CANL sink current under short-circuit condition (V_{CANL} ≤ 12 V, CANL driver ON, TXD low)	40	—	100	mA	
$I_{CANH\text{-}SC}$	CANH source current under short-circuit condition (V_{CANH} = –2.0 V, CANH driver ON, TXD low)	–100	—	–40	mA	
V_{CANLP}	CANL, CANH output voltage in sleep modes. No termination load.	–0.1	0.0	0.1	V	
I_{CAN}	CANH, CANL input current, device unsupplied, (V_{CANH}, V_{CANL} = 5.0 V) • V_{SUP} and V_{CAN} connected to GND • V_{SUP} and V_{CAN} connected to GND via 47 kΩ resistor	 –10 –10	 — —	 10 10	 µA µA	[10]
T_{OT}	Overtemperature detection	160	—	—	°C	
T_{HYST}	Overtemperature hysteresis	—	—	20	°C	
LIN transceiver (when 7.0 V < V_{SUP}1,2,3 < 18 V, unless otherwise specified)						
LIN logic input pin (TXDL)						
V_{TXDL_IH}	TXDL high input threshold	2.0	—	—	V	
V_{TXDL_IL}	TXDL low input threshold	—	—	0.8	V	
$TXDL_{PULL\text{-}UP}$	TXDL internal pull-up (to VDDIO)	20	33	50	kΩ	
$TXDL_{LK}$	TXD input leakage current, V_{TXDL} = VDDIO	–1.0	—	1.0	µA	
LIN logic input pin (RXDL)						
V_{RXDL_OL1}	Low level output voltage (I_{RXDL} = 250 µA)	—	—	0.4	V	
V_{RXDL_OL2}	Low level output voltage (I_{RXDL} = 1.5 mA)	—	—	0.9	V	
$V_{RXDL_OUT_HIGH}$	High level output voltage (I_{RXDL} = –250 µA, V_{DDIO} = 3.0 V to 5.5 V)	V_{DDIO} – 0.4	—	—	V	
LIN output pin						
$I_{BUS_PAS_DOM}$	Input leakage current at the receiver. dominant state (Driver OFF, V_{BAT} = 12 V, V_{BUS} = 0 V)	–1.0	—	—	mA	[11]
$I_{BUS_PAS_REC}$	Input leakage current at the receiver. recessive state (Driver OFF, 8.0 V < V_{BAT} < 18 V, 8.0 V < V_{BUS} < 18 V, V_{BUS} ≥ V_{BAT})	—	—	20	µA	
V_{DRIVER_DOM}	Driver dominant voltage	—	—	0.251 × V_{SUP}	V	
V_{BUS_DOM}	Receiver dominant state	—	—	0.4 × V_{SUP}	V	

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 5. Static electrical characteristics *...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP_UV_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 36 V, thermal dissipation must be considered (see Figure 32).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{BUS_REC}	Receiver recessive state	0.6 × V_{SUP}	—	—	V	
V_{BUS_WU}	LIN wake-up detection threshold (7.0 V < V_{SUP} < 18 V)	0.4 × V_{SUP}	—	0.6 × V_{SUP}	V	
V_{LIN_UV}	V_{SUP} undervoltage threshold	—	—	7.0	V	
V_{SER_DIODE}	Series diode voltage drop ($D_{SER_COMMANDER}$ and D_{SER_INT} in pull-up path)	0.4	0.7	1.0	V	
I_{BUS_LIM}	Current limitation for driver dominant state (V_{BUS} = 18 V)	40	—	200	mA	[12]
$R_{RESPONDER}$	LIN pull-up resistor	20	—	60	kΩ	
V_{SHIFT_GND}	Ground shift (V_{SHIFT_GND} = V_{GND_ECU} – $V_{GND_BATTERY}$)	0.0	—	11.5 % V_{BAT}	V	
V_{SHIFT_BAT}	Battery voltage shift (V_{SHIFT_BAT} = $V_{BATTERY}$ – V_{SHIFT_GND}– V_{BAT})	0.0	—	11.5 % V_{BAT}	V	[13]
V_{SHIFT_DIF}	Difference between battery shift and ground shift (V_{SHIFT_DIF} = V_{SHIFT_BAT} – V_{SHIFT_GND})	0.0	—	8.0 % V_{BAT}	V	[14]
V_{BUS_CNT}	V_{BUS_CNT} = (V_{TH_REC} + V_{TH_DOM})/2	0.475 × V_{SUP}	—	0.525 × V_{SUP}	V	[15]
V_{HYST}	V_{HYST} = V_{TH_REC} – V_{TH_DOM}	—	—	0.175 × V_{SUP}	V	
$I_{BUS_NO_GND}$	Ground disconnection. GND = V_{SUP}, 0 V < V_{BUS} < 18 V, V_{BAT} = 12 V. Loss of local GND does not affect communication in the remaining network	–1.0	—	1.0	mA	[16]
$I_{BUS_NO_BAT}$	VBAT disconnection. V_{SUP} = GND, 0 V < V_{BUS} < 18 V. Node sustains the current which can flow under this condition. BUS remains operational.	—	—	30	µA	
LIN_{TSD}	LIN thermal shutdown	150	175	—	°C	[5]
LIN_{TSD_HYST}	LIN thermal shutdown hysteresis		20		°C	
C_{LIN}	LIN internal capacitor	—	—	10	pF	[5]

[1] Long duration timer and VKAM disable.
[2] $V_{SUP_UV_L_B}$ = $V_{PRE_UV_4P3}$ + R_{DSON_PRE} × I_{PRE}.
[3] V_{SUP} min to guarantee V_{KAM} and main logic supply in LPOFF.
[4] Guaranteed by characterization.
[5] Guaranteed by design.
[6] External PNP gain within 150 to 450.
[7] Valid for V_{SUP3} ≥ IO_5.
[8] If a higher resistor value than recommended is used, the accuracy degrades.
[9] Wide range accuracy for input voltage from 9.0 V to 19 V.
[10] Guaranteed by design and characterization.
[11] V_{BAT} is the voltage at the input of the control unit.
[12] Current flowing inside the pin. A transceiver must be capable to sink at least 40 mA.
[13] V_{BAT}: voltage across the battery connectors of the vehicle. V_{GND_ECU}: voltage on the local ECU ground connector with respect to battery ground of the vehicle ($V_{GND_BATTERY}$).
[14] This constraint refers to duty cycle D1 and D2 only.
[15] V_{TH_DOM}: receiver threshold of the recessive to dominant LIN bus edge. V_{TH_REC} receiver threshold of the dominant to recessive LIN bus edge.
[16] V_{SUP} is the voltage at the input of the device (different from V_{BAT} when a reverse current protection diode is implemented.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

10 Dynamic electrical characteristics

Table 6. Dynamic electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP_UV_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 36 V, thermal dissipation must be considered (see Figure 32).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Digital interface timing						
f_{SPI}	SPI operation frequency (50 % DC)	0.5	—	8.0	MHz	
t_{MISO_TRANS}	MISO transition speed, 20 – 80 % • V_{DDIO} = 5.0 V, C_{LOAD} = 50 pF • V_{DDIO} = 5.0 V, C_{LOAD} = 150 pF	 5.0 5.0	 — —	 30 50	ns	
t_{CLH}	Minimum time SCLK = HIGH	62	—	—	ns	
t_{CLL}	Minimum time SCLK = LOW	62	—	—	ns	
t_{PCLD}	Propagation delay (SCLK to data at 10 % of MISO rising edge)	—	—	30	ns	
t_{CSDV}	NCS = low to data at MISO active	—	—	75	ns	
t_{SCLCH}	SCLK low before NCS low (setup time SCLK to NCS change H/L)	75	—	—	ns	
t_{HCLCL}	SCLK change L/H after NCS = low	75	—	—	ns	
t_{SCLD}	SDI input setup time (SCLK change H/L after MOSI data valid)	40	—	—	ns	
t_{HCLD}	SDI input hold time (MOSI data hold after SCLK change H/L)	40	—	—	ns	
t_{SCLCL}	SCLK low before NCS high	100	—	—	ns	
t_{HCLCH}	SCLK high after NCS high	100	—	—	ns	
t_{PCHD}	NCS L/H to MISO at high-impedance	—	—	75	ns	
t_{ONNCS}	NCS min. high time	500	—	—	ns	
t_{NCS_MIN}	NCS filter time	10	—	40	ns	
Functional state machine						
t_{WU_GEN}	General wake-up signal deglitch time (for any wake-up signal on IOs)	60	70	80	µs	
Fail-safe state machine						
CLK_{FS}	Fail-safe oscillator	406	—	495	kHz	
CLK_{FS_MON}	Fail-safe oscillator monitoring	200	—	950	kHz	
t_{IC_ERR}	IO_4:5 Ext. IC filter time	4.0	—	20	µs	
t_{ACK_FS}	Acknowledgment counter (used for IC error handling IO_5)	7.0	—	9.7	ms	
t_{FCCU_ERR}	IO_2:3 FCCU filter time	4.0	—	8.0	us	
$t_{DFS_RECOVERY}$	IO_0 filter time to recover from deep reset and fail state	0.8	—	1.3	ms	
$t_{CORE_DRIFT_MON}$	FCRBM filter time	1.0	—	2.0	ms	
Fail-safe output						
t_{RSTB_FB}	RSTB feedback filter time	8.0	—	15	µs	
t_{FS0B_FB}	FS0B feedback filter time	8.0	—	15	µs	
t_{FS1B_FB}	FS1B feedback filter time	8.0	—	15	µs	
t_{RSTB_BLK}	RSTB feedback blanking time	180	—	320	µs	
t_{FS0B_BLK}	FS0B feedback blanking time	180	—	320	µs	
t_{FS1B_BLK}	FS1B feedback blanking time	180	—	320	µs	
t_{RSTB_POR}	Reset delay time (after a power-on reset or from LPOFF)	12.5	16.5	24.3	ms	[1]

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 6. Dynamic electrical characteristics *...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP_UV_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 36 V, thermal dissipation must be considered (see Figure 32).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
t_{RSTB_LG}	Reset duration (long pulse)	8.0	—	10	ms	
t_{RSTB_ST}	Reset duration (short pulse)	1.0	—	1.3	ms	
t_{RSTB_IN}	External reset delay time	8.0	—	15	µs	
t_{DIAG_SC}	Fail-safe output diagnostic counter (RSTB, FS0B, FS1B)	500	—	800	µs	
V_{SENSE} voltage supply						
t_{VSNS_UV}	V_{SNS} undervoltage filtering time	1.0	—	3.0	µs	
V_{SUP} voltage supply						
t_{VSUP_IPFF}	I_{PFF} input voltage filtering time	1.0	—	5.0	µs	
C_{SUP}	Minimum capacitor on V_{SUP}	47	—	—	µF	
V_{PRE} voltage pre-regulator						
f_{SW_PRE}	V_{PRE} switching frequency	412	437.5	463	kHz	
t_{SW_PRE}	V_{SW_PRE} on and off switching time	—	—	30	ns	[2]
t_{PRE_SOFT}	V_{PRE} soft start duration (C_{OUT_VPRE} ≤ 100 µF)	500	—	700	µs	
$t_{PRE_BLK_LIM}$	V_{PRE} current limitation blanking time	200	—	600	ns	
t_{IPRE_OC}	V_{PRE} overcurrent filtering time	30	—	120	ns	[2]
t_{PRE_UV}	V_{PRE} undervoltage filtering time	20	—	40	µs	
$t_{PRE_UV_4p3}$	V_{PRE} shutoff filtering time	3.0	—	7.0	µs	
$d_{IPRE/DT}$	V_{PRE} load regulation variation	—	—	25	A/ms	[2]
t_{PRE_WARN}	V_{PRE} thermal warning filtering time	30	—	40	µs	
t_{PRE_TSD}	V_{PRE} thermal detection filtering time	1.0	—	3.0	µs	
$t_{LS_RISE/FALL}$	LS gate voltage switching time (I_{OUT} = 300 mA)	—	—	50	ns	
t_{BBTO}	GATE_LS boost transistor timeout detection	—	120	—	us	
V_{core} voltage regulator						
$t_{CORE_BLK_LIM}$	V_{CORE} current limitation blanking time	20	—	40	ns	
f_{SW_CORE}	V_{CORE} switching frequency	2.2	2.34	2.48	MHz	
t_{SW_CORE}	V_{SW_CORE} on and off switching time	—	—	12	ns	
V_{CORE_SOFT}	V_{CORE} soft start (C_{OUT_VCORE} = 100 µF max)	—	—	10	V/ms	
t_{CORE_WARN}	V_{CORE} thermal warning filtering time	30	—	40	µs	
t_{CORE_TSD}	V_{CORE} thermal detection filtering time	1.0	—	3.0	µs	
V_{CCA} voltage regulator						
t_{CCA_LIM}	V_{CCA} output current limitation filter time	1.0	—	3.0	µs	
$t_{CCA_LIM_OFF1}$ $t_{CCA_LIM_OFF2}$	V_{CCA} output current limitation duration	10 50	— —	15 60	ms	
t_{CCA_WARN}	V_{CCA} thermal warning filtering time (int. MOSFET)	30	—	40	µs	
t_{CCA_TSD}	V_{CCA} thermal detection filter time (int. MOSFET)	1.0	—	3.0	µs	
dI_{LOAD}/dt	V_{CCA} load transient	—	2.0	—	A/ms	[2]
V_{CCA_SOFT}	V_{CCA} soft start (5.0 V and 3.3 V)	—	—	50	V/ms	
V_{AUX} voltage regulator						
t_{AUX_LIM}	V_{AUX} output current limitation filter time	1.0	—	3.0	µs	

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 6. Dynamic electrical characteristics *...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP_UV_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 36 V, thermal dissipation must be considered (see Figure 32).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
$t_{AUX_LIM_OFF1}$ $t_{AUX_LIM_OFF2}$	V_{AUX} output current limitation duration	10 50	— —	15 60	ms	
t_{AUX_TSD}	V_{AUX} thermal detection filter time	1.0	—	3.0	µs	
dI_{AUX}/dt	V_{AUX} load transient	—	2.0	—	A/ms	[2]
V_{AUX_SOFT}	V_{AUX} soft start (5.0 V and 3.3 V)	—	—	50	V/ms	
CAN_5V voltage regulator						
t_{CAN_LIM}	Output current limitation filter time	2.0	—	4.0	µs	
t_{CAN_TSD}	V_{CAN} thermal detection filter time	1.0	—	3.0	µs	
t_{CAN_UV}	V_{CAN} undervoltage filtering time	4.0	—	7.0	µs	
t_{CAN_OV}	V_{CAN} overvoltage filtering time	100	—	200	µs	
dI_{CAN}/dt	V_{CAN} load transient	—	100	—	A/ms	[2]
Fail-safe machine voltage supervisor						
t_{PRE_OV}	V_{PRE} overvoltage filtering time	128	—	234	µs	
$t_{PRE_OV_R}$	V_{PRE} overvoltage reaction time	—	—	314	µs	
t_{CORE_UV}	V_{CORE} FB undervoltage filtering time	4.0	—	10	µs	
$t_{CORE_UV_R}$	V_{CORE} FB undervoltage reaction time	—	—	15	µs	
t_{CORE_OV}	V_{CORE} FB overvoltage filtering time	128	—	234	µs	
$t_{CORE_OV_R}$	V_{CORE} FB overvoltage reaction time	—	—	314	µs	
t_{CCA_UV}	V_{CCA} undervoltage filtering time	4.0	—	10	µs	
$t_{CCA_UV_R}$	V_{CCA} undervoltage reaction time	—	—	15	µs	
t_{CCA_OV}	V_{CCA} overvoltage filtering time	128	—	234	µs	
$t_{CCA_OV_R}$	V_{CCA} overvoltage reaction time	—	—	314	µs	
t_{AUX_UV}	V_{AUX} undervoltage filtering time	4.0	—	10	µs	
$t_{AUX_UV_R}$	V_{AUX} undervoltage reaction time	—	—	15	µs	
t_{AUX_OV}	V_{AUX} overvoltage filtering time	128	—	234	µs	
$t_{AUX_OV_R}$	V_{AUX} overvoltage reaction time	—	—	314	µs	
Digital input – multi-purpose IOs						
F_{IO_IN}	Digital input frequency range	0.0	—	100	kHz	
Analog multiplexer						
t_{MUX_READY}	SPI selection to data ready to be sampled on Mux_out • V_{DDIO} = 5.0 V, C_{MUX_OUT} = 1.0 nF	—	—	10	µs	
Interrupt						
t_{INTB_LG}	INTB pulse duration (long)	90	100	—	µs	
t_{INTB_ST}	INTB pulse duration (short)	20	25	—	µs	
Long duration timer						
CLK_{LDT}	Long duration timer oscillator	31129	32768	34407	Hz	
$CLK_{LDT_\%}$	Long duration timer oscillator accuracy • from –40 °C to 125 °C • from –20 °C to 85 °C and calibration	 –5.0 –2.0	 — —	 5.0 2.0	%	

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 6. Dynamic electrical characteristics *...continued*

T_A = –40 °C to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP_UV_L}$ to 36 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 36 V, thermal dissipation must be considered (see Figure 32).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
CAN dynamic characteristics (FD 2.0 Mbit/s)						
t_{DOUT}	TXD dominant state timeout	0.8	—	5.0	ms	
t_{DOM}	Bus dominant clamping detection	0.8	—	5.0	ms	
t_{LOOP}	Propagation loop delay TXD to RXD • R_{LOAD} = 120 Ω, C between CANH and CANL = 100 pF, C at RXD < 15 pF	—	—	255	ns	
t_{1PWU}	First pulse wake-up time	0.5	—	3.5	µs	
t_{3PWU}	Second and third pulse wake-up time	0.5	—	1.0	µs	
t_{3PTO1}	Multiple pulse wake-up timeout (short)	100	120	—	µs	
t_{3PTO2}	Multiple pulse wake-up timeout (long)	2400	2800	—	µs	
t_{CAN_READY}	Delay to enable CAN by SPI command (NCS rising edge) to CAN to transmit (device in normal mode and CAN interface in TX/RX mode)	—	—	100	µs	[3]
$t_{BIT(BUS)}$	Transmitted recessive bit width at 2.0 Mbit/s	435	—	530	ns	
$t_{BIT(RXD)}$	Received recessive bit width at 2.0 Mbit/s	400	—	550	ns	
t_{REC}	Receiver timing symmetry at 2.0 Mbit/s	–65	—	40	ns	
LIN dynamic characteristics (when 7.0 V < V_{SUP}1, 2, 3 < 18 V, unless otherwise specified)						
t_{RX_PD}	Receiver propagation delay (T_{RX_PD} = MAX (t_{REC_PDR}, t_{REC_PDF}))	—	—	6.0	µs	
t_{RX_SYM}	Symmetry of receiver propagation delay (T_{RX_SYM} = t_{REC_PDF} – t_{REC_PDR})	–2.0	—	2.0	µs	
t_{BUS_WU}	BUS wake-up filter time	—	—	250	µs	
t_{XD_DOM}	TXD_L permanent dominant state detection	—	5.0	—	ms	
$t_{LIN_SHORT_GND}$	LIN Short-circuit to GND deglitcher	—	15	—	ms	
BD_{FAST}	Fast baud rate	—	—	100	KB/s	
D1	Duty cycle D1 TH_{REC}(max) = 0.744 x V_{SUP}, TH_{DOM}(max) = 0.581 x V_{SUP} V_{SUP} 7.0 V to 18 V, t_{BIT} = 50 µs, D1 = t_{BUS}–rec(min)/($2t_{BIT}$)	0.396	—	—	%	[4]
D2	Duty cycle D2 TH_{REC}(min) = 0.422 x V_{SUP}, TH_{DOM}(min) = 0.284 x V_{SUP} V_{SUP} 7.6 V to 18 V, t_{BIT} = 50 µs, D2 = t_{BUS}–rec(max)/($2t_{BIT}$)	—	—	0.581	%	35[4]
D3	Duty cycle D3 TH_{REC}(max) = 0.778 x V_{SUP}, TH_{DOM}(max) = 0.616 x V_{SUP} V_{SUP} 7.0 V to 18 V, t_{BIT} = 96 µs, D3 = t_{BUS}–rec(min)/($2t_{BIT}$)	0.417	—	—	%	35[4]
D4	Duty cycle D4 TH_{REC}(min) = 0.389 x V_{SUP}, TH_{DOM}(min) = 0.251 x V_{SUP} V_{SUP} 7.6 V to 18 V, t_{BIT} = 96 µs, D4 = t_{BUS}–rec(max)/($2t_{BIT}$)	—	—	0.590	%	35[4]

[1] This timing is not guaranteed in case of fault during startup phase (after power-on reset of from LPOFF).
[2] Guaranteed by characterization.
[3] For proper CAN operation, TXD must be set to high level before CAN enable by the SPI, and must remain high for at least T_{CAN_READY}.
[4] LIN Driver, bus load conditions (CBUS, RBUS): 1.0 nF; 1.0 kΩ / 6.8 nF; 660 Ω / 10 nF; 500 Ω.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

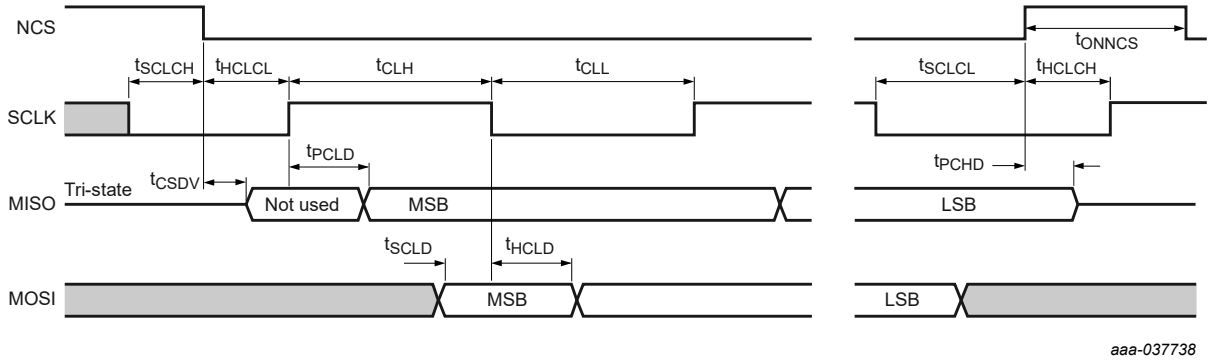


Figure 9. SPI timing diagram

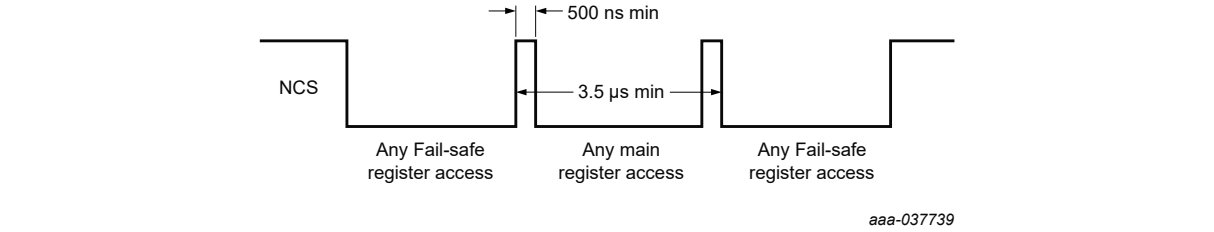


Figure 10. Register access restriction

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

11 Functional pin description

11.1 Introduction

The FS6500/FS4500 is the fourth generation of the system basis chip, combining:

- High efficiency switching voltage regulator for MCU, and linear voltage regulators for integrated CAN FD and LIN interfaces.
- External ICs such as sensors, accurate reference voltage for A to D converters, and keep alive memory supply in low-power mode for MCU static RAM.
- Built-in CAN flexible data interface at 2.0 Mbit/s (ISO 11898-2[(12)] and -5[(13)]), and LIN interface (LIN up to Rev. 2.2[(22)], [(23)]/SAEJ2602-2[(24)]), with local and bus failure diagnostic, protection, and fail-safe operation mode.
- Low-power mode, with ultra low-current consumption.
- Various wake-up capabilities.
- Long duration timer available in normal and low-power mode.
- Enhanced safety features with multiple fail-safe outputs and a scheme to support ASIL D applications.

11.2 Power supplies (VSUP1, VSUP2, VSUP3)

VSUP1 and VSUP2 are the input pins for the internal supply dedicated to the SMPS regulators. VSUP3 is the input pin for internal voltage reference. VSUP1, 2, and 3 are robust against ISO 7637[(14)] pulses. VSUP1, 2, and 3 must be connected to the same supply (Figure 73).

11.3 V_{SENSE} input (VSENSE)

This pin must be connected to the battery line (before the reverse battery protection diode), via a serial resistor. It incorporates a threshold detector to sense the battery voltage, and provide a battery early warning. It also includes a resistor divider to measure VSENSE voltage via the MUX-OUT pin. The VSENSE pin is robust against ISO 7637[(14)] pulses.

11.4 Pre-regulator (VPRE)

A highly flexible SMPS pre-regulator is implemented in the FS6500/FS4500. It can be configured as a 'non-inverting buck-boost converter' (Figure 34) or 'standard buck converter' (Figure 33), depending on the external configuration (connection of pin GATE_LS). The configuration is detected automatically during start-up sequence.

The SMPS pre-regulator is working in current mode control and the compensation network is fully integrated in the device. The high-side switching MOSFET is also integrated to make the current control easier. The pre-regulator delivers a typical output voltage of 6.5 V, which is used internally. Current limitation, overcurrent, overvoltage, and undervoltage detectors are provided. VPRE is enabled by default.

11.5 VCORE output (from 1.0 V to 5.0 V range)

The VCORE block of the FS6500 series is an SMPS regulator. The voltage regulator is a step down DC–DC converter operating in voltage control mode. The stability of the converter is done externally, by using the COMP_CORE pin. The VCORE block of the FS4500 series is a linear regulator. In this case, BOOT_CORE and COMP_CORE pins must be left open.

The output voltage of FS6500/FS4500 is configurable to any voltage from a 1.0 V to 5.0 V range using an external resistor divider connected between VCORE and the feedback pin (FB_CORE) (as example in Figure 1, or Figure 73). Current limitation, overvoltage, and undervoltage detectors are provided. VCORE can be turned

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

on or off via a SPI command, however it is not recommended to turn off VCORE with the SPI when VCORE is configured safety critical (both overvoltage and undervoltage have an impact on fail-safe outputs). VCORE overvoltage information disables VCORE. Diagnostics are reported in the dedicated register and generate an Interrupt. VCORE is enabled by default. For safety purpose, a second resistor bridge (R3/R4 duplicated) connected to FCRBM should be used to detect an external resistor drift.

11.6 VCCA output, 5.0 V, or 3.3 V selectable

The VCCA voltage regulator is used to provide an accurate voltage output (5.0 V, 3.3 V) selectable through an external resistor connected to the SELECT pin.

The VCCA output voltage regulator can be configured using an internal transistor delivering very good accuracy (±1.0 % for 5.0 V and 3.3 V configuration), with a limited current capability (100 mA) for an analog to digital converter, or with an external PNP transistor, giving higher current capability (up to 300 mA) with lower output voltage accuracy (±3.0 % for 300 mA) when using a local ECU supply.

Current limitation, overvoltage, and undervoltage detectors are provided. VCCA can be turned on or off via a SPI command, however it is not recommended to turn off VCCA with the SPI when VCCA is configured safety critical (both overvoltage and undervoltage have an impact on fail-safe outputs). VCCA overcurrent (with the use of external PNP only) and overvoltage information disables VCCA. Diagnostics are reported in the dedicated register and generate an Interrupt. VCCA is enabled by default.

11.7 VAUX output, 5.0 V, or 3.3 V selectable

The VAUX pin provides an auxiliary output voltage (5.0 V, 3.3 V) selectable through an external resistor connected to SELECT pin. It uses an external PNP ballast transistor for flexibility and power dissipation constraints. The VAUX output voltage regulator can be used as ’auxiliary supply’ (local ECU supply) or ’sensor supply’ (external ECU supply) with the possibility to be configured as a tracking regulator following VCCA.

Current limitation, overvoltage, and undervoltage detectors are provided. VAUX can be turned on or off via a SPI command, however it is not recommended to turn off VAUX with the SPI when VAUX is configured safety critical (both overvoltage and undervoltage have an impact on fail-safe outputs). V_{AUX} overcurrent and overvoltage information disables VAUX, reported in the dedicated register, and generates an Interrupt. VAUX is enabled by default.

11.8 SELECT input pin

11.8.1 VCCA, VAUX voltage configuration

VCCA and VAUX output voltage configurations are set by connecting an external resistor between the SELECT pin and Ground or the SELECT pin and VPRE. According to the value of this resistor, the voltage of VCCA and VAUX are configured after each power-on reset, and after a wake-up event when the device is in LPOFF. Information latches until the next hardware configuration read. Regulator voltage values can be read on the dedicated register via the SPI. See Figure 75.

Table 7. V_{CCA}/V_{AUX} voltage selection

V_{CCA}(V)	V_{AUX}(V)	R select	Recommended value[1]
3.3	3.3	<6.0 kΩ	5.1 kΩ ±5.0 %
5.0	5.0	10.8 << 13.2 kΩ	12 kΩ ±5.0 %
3.3	5.0	21.6 << 26.2 kΩ	24 kΩ ±5.0 %
5.0	3.3	45.9 << 56.1 kΩ	51 kΩ ±5.0 %

[1] If the SELECT pin is detected open, the VCCA and VAUX regulators start at their minimum output voltage 3.3 V.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

11.8.2 Deep fail-safe configuration

Deep fail-safe function is enabled when the SELECT pin is connected to ground and disabled when the SELECT pin is connected to VPRE. The configuration is done after each power-on reset, and after a wake-up event when device is in LPOFF by both the main and the fail-safe logics. The Information is latched until the next hardware configuration read (Figure 11).

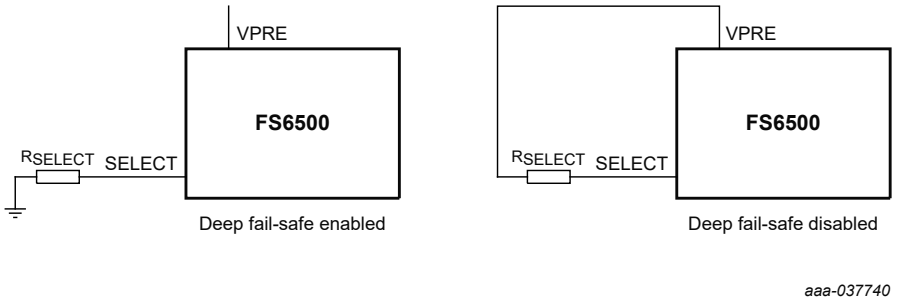


Figure 11. Deep fail-safe enable/disable

11.9 CAN_5V voltage regulator

The CAN_5V voltage regulator is a linear regulator dedicated to the internal CAN FD interface. An external capacitor is required. Current limitation, overvoltage, and undervoltage detectors are provided. If the internal CAN transceiver is not used, the CAN_5V regulator can supply an external load (see Section 12.7.6). CAN_5V is enabled by default.

11.10 Interrupt (INTB)

The INTB output pin generates a low pulse when an Interrupt condition occurs. The INTB behavior as well as the pulse duration are set through the SPI during INIT phase. INTB has an internal pull-up resistor connected to VDDIO.

11.11 CANH, CANL, TXD, RXD

These are the pins of the CAN FD physical interface. The CAN FD transceiver provides the physical interface between the CAN FD protocol controller of an MCU and the physical dual wires CAN-bus. The CAN FD interface is connected to the MCU via the RXD and TXD pins.

11.11.1 TXD

TXD is the device input pin to control the CAN-bus level. TXD is a digital input with an internal pull-up resistor connected to VDDIO. In the application, this pin is connected to the microcontroller transmit pin. In normal mode, when TXD is high or floating, the CANH and CANL drivers are off, setting the bus in a recessive state. When TXD is low, the CANH and CANL drivers are activated and the bus is set to a dominant state. TXD has a built-in timing protection disabling the bus when TXD is dominant for more than t_{DOUT}. In LPOFF mode, VDDIO is off, pulling this pin to GND.

11.11.2 RXD

RXD is the bus output level report pin. In the application, this pin is connected to the microcontroller receive pin. In normal mode, RXD is a push-pull structure. When the bus is in a recessive state, RXD is high. When the bus is dominant, RXD is low. In LPOFF mode, this pin is in the high-impedance state.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

11.11.3 CANH and CANL

These are the CAN-bus pins. CANL is a low-side driver to GND, and CANH is a high-side driver to CAN_5V. In normal mode and TXD high, the CANH and CANL drivers are off, and the voltage at CANH and CANL is approximately 2.5 V, provided by the internal bus biasing circuitry. When TXD is low, CANL is pulled to GND and CANH to CAN_5V, creating a differential voltage on the CAN-bus.

In LPOFF mode, the CANH and CANL drivers are off, and these pins are pulled to GND via the device R_{IN_CHCL} resistors. CANH and CANL have integrated ESD protection and extremely high robustness versus external disturbance, such as EMC and electrical transients. These pins have current limitation and thermal protection.

11.12 LIN, TXDL, RXDL

These are the pins of the LIN physical interface. The LIN transceivers provides the physical interface between the MCU and the physical single wire LIN bus. The LIN interface is connected to the MCU via the RXDL and TXDL pins.

11.12.1 TXDL

The TXDL input pin is the MCU interface to control the state of the LIN output. TXDL is a digital input with an internal pull-up resistor connected to VDDIO. In the application, this pin is connected to the microcontroller transmit pin.

In normal mode, when TXDL is high or floating, the LIN output transistor is OFF, setting the bus in recessive state. When TXDL is low, the LIN output transistor is on and the bus is set to a dominant state. TXDL has a built-in timing protection disabling the bus when TXDL is dominant for more than T_{XD_DOM}. In LPOFF mode, VDDIO is off, pulling this pin to GND.

11.12.2 RXDL

RXDL is the bus output level report pin. In the application, this pin is connected to the microcontroller receive pin. In normal mode, RXD is a push-pull structure. When the bus is in a recessive state, RXD is high. When the bus is dominant, RXD is low. In LPOFF mode, this pin is in the high-impedance state.

11.12.3 LIN

This is the LIN bus pin. The LIN driver is a low-side MOSFET with internal overcurrent thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated so no external pull-up components are required for the application in a responder node. An additional pull-up resistor of 1.0 kΩ must be added when the device is used in the commander node. In normal mode and TXDL high, the LIN transistor is off, and the voltage at LIN is approximately VSUP3, provided by the pull-up resistor with a serial diode structure. When TXD is low, LIN is pulled to GND.

The device has two selectable baud rates: 20 kbit/s for normal baud rate and 10 kbit/s for slow baud rate. An additional fast baud rate (100 kbit/s) is implemented. It can be used to flash the MCU or in the garage for diagnostic. The LIN consortium specification does not specify electrical parameters for this baud rate. The communication only must be guaranteed. In LPOFF mode, the LIN transistor is off, and this pin is pulled up to VSUP3. LIN has integrated ESD protection and extremely high robustness versus external disturbance, such as EMC and electrical transients.

11.13 Multiplexer output MUX_OUT

The MUX_OUT pin (Figure 12) delivers analog voltage to the MCU ADC input. The voltage to be delivered to MUX_OUT is selected via the SPI, from one of the following parameters:

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

- VSENSE
- VIO_0
- VKAM
- Internal 2.5 V reference
- Internal die temperature sensor T(°C) = (V_{AMUX} – V_{AMUX_TP})/$V_{AMUX_TP_CO}$ + 165

Voltage range at MUX_OUT is from GND to VDDIO (3.3 V or 5.0 V)

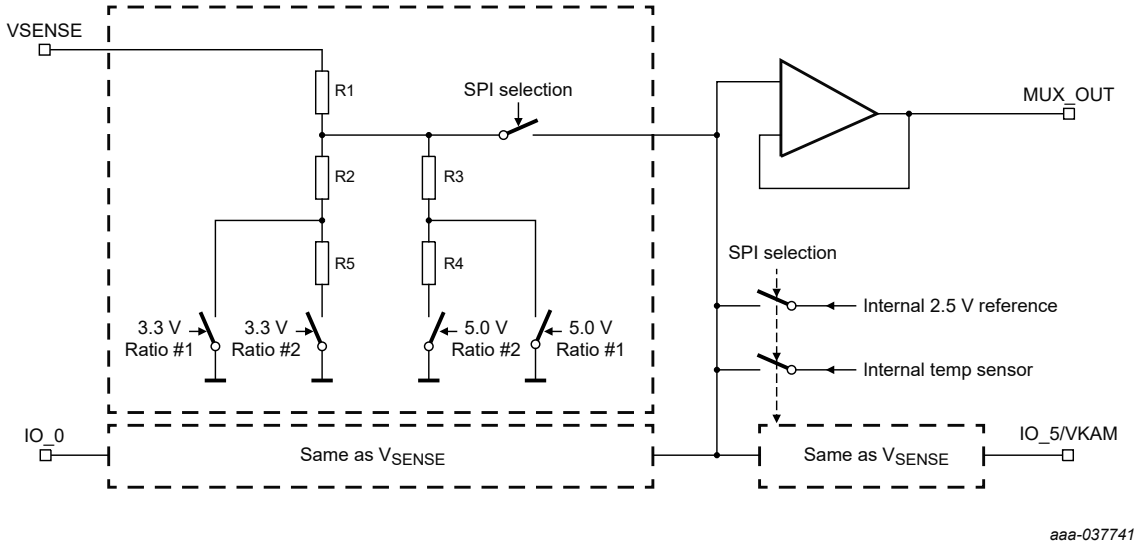


Figure 12. Simplified analog multiplexer block diagram

11.14 I/O pins (I/O_0:I/O_5)

The FS6500/FS4500 includes five multi-purpose I/Os (I/O_0 to I/O_5). I/O_0 and I/O_4 are load dump proof and robust against ISO 7637[(14)] pulses. An external serial resistor must be connected to those pins to limit the current during ISO pulses. I/O_2 and I/O_3 are not load dump proof. I/O_5 requires an external protection (resistor and Zener diode) to be load dump proof and robust against ISO 7637[(14)] pulses.

Table 8. I/Os configuration

I/O number	Digital input wake-up capability	Analog input	Output gate driver	VKAM	FCCU monitoring	Ext. IC monitoring
IO_0	X	X				
IO_2	X				X	
IO_3	X				X	
IO_4	X		X			X
IO_5	X	X		X		X

- IO_0 is selectable as follows:

Analog input (load dump proof) sent to the MCU through the MUX_OUT pin. Wake-up input on the rising or falling edge or based on the previous state. Digital input (logic level) sent to the MCU through the SPI.

Safety purpose: IO_0 is the only wake-up input to resume from deep fail-safe mode.

- IO_2:3 are selectable as follows:

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Digital input (logic level) sent to the MCU through the SPI. Wake-up input on the rising or falling edge or based on the previous state. **Safety purpose**: Digital input (logic level) to monitor MCU error signals (both IO_2 AND IO_3 are used if configured as safety inputs). Only bi-stable protocol is available.

When IO_2:3 are used as safety inputs to monitor FCCU error outputs from the NXP MCU, the monitoring is active only when the fail-safe sate machine is in 'normal WD' state (Figure 17) and all the phases except the 'normal phase' are considered as an error.

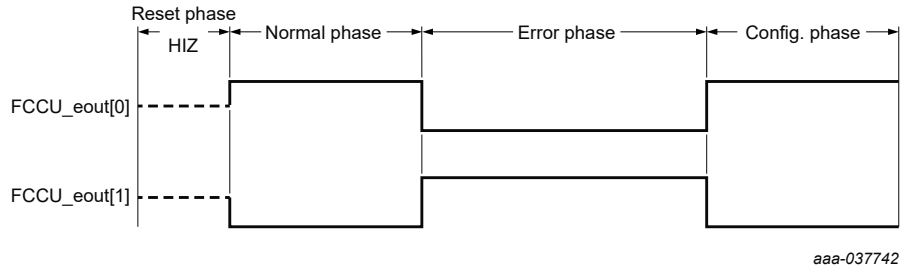


Figure 13. IO_2:3 MCU error monitoring: bi-stable protocol

- IO_4 is selectable as follows:

Digital input (logic level) sent to the MCU through the SPI. Wake-up input (load dump proof) on rising or falling edge or based on previous state. Output gate driver (from V_{PRE}) for low-side logic level MOSFET.

- IO_5 is selectable as follows:

Analog input (20 V max.) sent to the MCU through the MUX_OUT pin. Digital input (logic level) sent to the MCU through the SPI. Wake-up input on rising or falling edge or based on previous state. VKAM output supply.

- IO_4:5 are selectable as follows:

Safety purpose: Digital input (logic level) to perform an IC error monitoring (both IO_4 AND IO_5 are used if configured as safety inputs, see Figure 14).

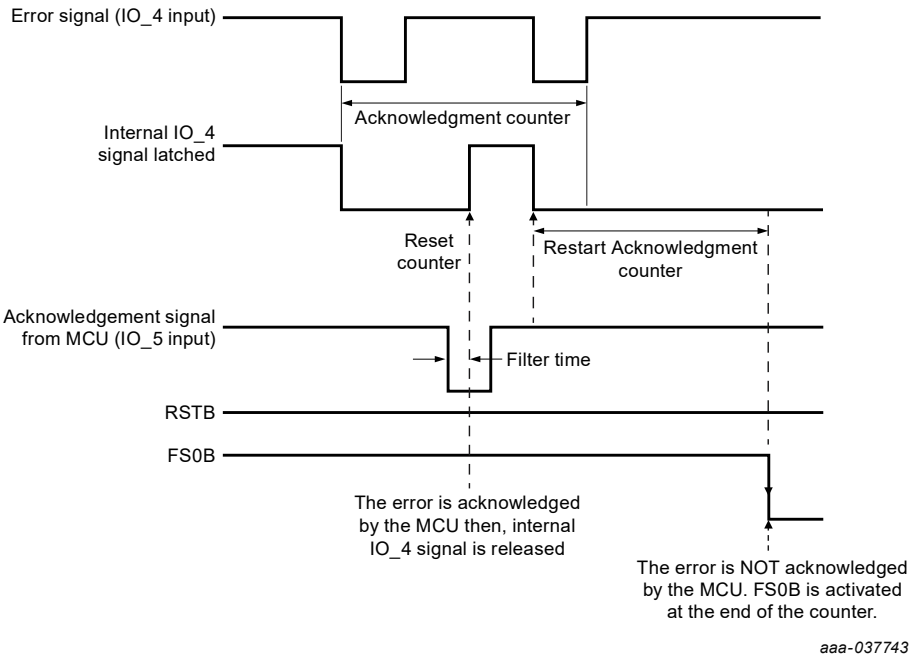


Figure 14. External error signal handling

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

11.15 SAFE output pins (FS0B, FS1B, RSTB)

11.15.1 FS0B pin

FS0B pin is the primary safe output pin. FS0B is asserted low when a fault event occurs (see Section 12.5.5). The objective of this pin is to drive an electrical safe circuitry independent from MCU to deactivate the whole system and set the ECU in a protected and known state.

After each power-on reset or after each wake-up event (LPOFF), the FS0B pin is asserted low. The MCU can decide to release the FS0B pin, when the application is ready to start. An external pull-up circuitry is mandatory connected to VDDIO or VSUP3.

- If the pull-up is connected to VDDIO, the value recommended is 5.0 kΩ, there is no current in LPOFF since VDDIO is off in LPOFF mode.
- If the pull-up is connected to VSUP3, the value must be above 10 kΩ, there is a current in the pull-up resistor to consider at application level in LPOFF mode.

11.15.2 FS1B pin

FS1B pin is the secondary safe output pin. FS1B is asserted low with a configurable delay (t_{DELAY}) or duration (t_{DUR}) when FS0B is asserted low (see Section 12.5.6). This pin can be used to:

- Open the phases of a motor after a configurable delay starting when FS0B is asserted, to demagnetize the motor coils and reduce the inductive effect when the switch is open.
- Disable an external physical layer during a configurable duration starting when FS0B is asserted, to avoid miscommunication when the module is in fail mode.
- Be a redundant safe output pin to FS0B when t_{DELAY} = 0. In this case, FS1B is asserted at the same time than FS0B.
- Any other use case where a second safety pin is needed.

After each power-on reset or after each wake-up event (LPOFF), the FS1B pin is asserted low. Then the MCU can decide to release the FS1B pin, when the application is ready to start. An external pull-up circuitry is mandatory, connected to VPU_FS or VDDIO.

11.15.3 RSTB pin

The RSTB pin must be connected to MCU and is active low. An external pull-up resistor must be connected to VDDIO. In default configuration, the RST delay time has three possible values depending on the mode and product configuration:

- The longest one is used automatically following a power-on reset or when resulting from LPOFF mode (low-power off).
- The two reset durations are then available in the INIT_FSSM register, which are 1.0 ms and 10 ms. The configured duration is finally used in the normal operation when a fault occurs leading to a reset activation. The INIT_FSSM register is available (writing) in the INIT_FS phase.

11.16 VPU_FS (fail-safe pull-up)

This pin is intended to be the pull-up terminal of FS1B, internally attached to V_{PRE} through a reverse diode protection. When FS1B is used in t_{DELAY} configuration, a configurable external RC network provides a minimum backup delay, in case of a loss of the internal fail-safe oscillator or loss of supply. This independent pull-up (compared to FS0B pull-up) avoids common cause failures between the two safe outputs and guarantee FS1B activation with a delay compared to FS0B in all conditions. When FS1B is used with t_{DELAY} = 0 or in t_{DUR} configuration, a pull-up to V_{DDIO} is also possible, taking into account the common cause failure with the same pull-up as FS0B in the safety analysis.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

11.17 DEBUG input (entering in debug mode)

The DEBUG pin allows the product to enter debug mode. To activate the debug mode, voltage applied to the DEBUG pin must be within the V_{DEBUG_IL} and V_{DEBUG_IH} range at start-up. If the voltage applied to DEBUG pin is out of these limits, during the SELECT pin configuration, the device settles into normal mode.

In debug mode, the watchdog window is fully open and no watchdog refresh is required. This allows an easy debug of the hardware and software routines (i.e. SPI commands). However, the whole watchdog functionality is kept on (seed, LFSR, WD refresh counter, WD error counter,...). WD errors are detected and counted with reaction according to WD_IMPACT bit configuration. When the debug mode is activated, the fail-safe outputs (FS0B, FS1B) are asserted low at start-up. The release procedure and the assertion conditions are the same than in normal mode. When the Debug mode is activated, there is no deep fail-safe state.

The CAN transceiver is set to normal operation mode by default allowing CAN communication without SPI configuration (FS1B_CAN_IMP bit = 0). To exit debug mode, the pin must be tied to ground through an external pull-down resistor and a power-on reset or wake-up from LPOFF occurs.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

12 Functional device operation

12.1 Mode and state description of the main state machine

The device has several operation modes. The transition and conditions to enter or leave each mode are illustrated in the functional state diagram (Figure 16). Two state machines work in parallel. The main state machine controls the power management (VPRE, VCORE, VCCA, VAUX,...) and the fail-safe state machine controls all the safety aspects (WD, RSTB, FS0B, FS1B,...).

12.1.1 Buck or buck boost configuration

An external low-side logic level MOSFET (N-type) is required to operate in non-inverting buck-boost converter. The connection of the external MOSFET is detected automatically during the start-up phase (after a power-on reset or from LPOFF).

- If the external low-side MOSFET is **not** connected (GATE_LS pin connected to PGND), the product is configured as a standard buck converter.
- If the external low-side MOSFET is connected (GATE_LS pin connected to external MOSFET gate), the product is configured as a non-inverting buck-boost converter.

The automatic detection is done by pushing 300 µA current on Gate_LS pin and monitoring the corresponding voltage generated. If a voltage >120 mV is detected before the 120 µs timeout, the non-inverting buck-boost configuration is locked. Otherwise, the standard buck configuration is locked. The boost driver has a current capability of ±300 mA.

12.1.2 V_{PRE} on

Pre-regulator is an SMPS regulator. In this phase, the pre-regulator is switched on and a soft start with a specified duration t_{PRE_SOFT} controls the VPRE output capacitor charge.

12.1.3 SELECT pin configuration

This phase detects the required voltage level on VAUX and VCCA, according to the resistor value connected between the SELECT pin and Ground or VPRE, and configures the deep fail-safe function.

12.1.4 V_{CORE}/V_{AUX}/V_{CCA} on

In this stage, the three regulators VCORE, VAUX, VCCA are switched on at the same time with a specified soft start duration. The CAN_5V is also started at this time.

12.1.5 INIT main

This mode is automatically entered after the device is ’powered on’. When RSTB is released, initialization phase starts where the device can be configured via the SPI. During INIT phase, some registers can only be configured in this mode (see Table 19 and Table 20). Other registers can be written in this mode, and also in normal mode.

Once the INIT registers configurations are complete, a last register called ’INIT_INT’ must be configured to switch to normal mode. Writing data in this register (even same default values), automatically locks the INIT registers, and the product switches automatically to normal mode in the main state machine.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

12.1.6 Normal

In this mode, all device functions are available. This mode is entered by a SPI command from the INIT phase by writing in the INIT_INT register. While in normal mode, the device can be set to low-power mode (LPOFF) using secured SPI command.

12.1.7 Low-power mode off

The main state machine has three LPOFF modes with different conditions to enter and exit each LPOFF mode, as described hereafter. After wake-up from LPOFF, all the regulators are enabled by default. In LPOFF, all the regulators are switched off, except VKAM. The register configuration and the ISO pulse requirement are valid for the three LPOFF modes.

12.1.7.1 LPOFF - sleep

Entering in low-power mode LPOFF - sleep is only available if the product is in normal mode by sending a secured SPI command. In this mode, all the regulators are turned off and the MCU connected to the V_{CORE} regulator is unsupplied. Only VKAM is available if VKAM is used (specific part number for VKAM on by default).

Once the FS6500/FS4500 is in LPOFF - sleep, the device monitors external events to wake-up and leave the low-power mode. The wake-up events can occur and depending on the device configuration from:

- Physical layer (CAN or LIN)
- I/O inputs
- Timer

When a wake-up event is detected, the device starts the main state machine again by detecting the VPRE configuration (buck or buck-boost), the wake-up source is reported to the dedicated SPI register, and the fail-safe state machine is also restarted.

12.1.7.2 LPOFF - auto WU

LPOFF - auto WU is entered when the device is in the INIT or normal mode and if the V_{PRE} voltage level is passing the $V_{PRE_UV_4P3}$ threshold (typ 4.3 V). It can be also entered by sending a secured SPI command if the product is in normal mode. It allows a POR and complete restart of the fail-safe state machine. After 1.0 ms, the device attempts to recover by switching on V_{PRE} again.

12.1.7.3 LPOFF - deep FS

LPOFF - deep FS is entered when the device is in deep fail-safe and if the key is off (IO_0 is low). To exit this mode, a transition to high level on IO_0 is required. IO_0 is usually connected to the key on key off signal (see Section 12.3).

12.1.7.4 Register configuration in LPOFF

In LPOFF, the register settings of the main state machine are kept because the internal 2.5 V main digital regulator is available for wake-up operation. However, the register settings of the fail-safe state machine are erased because the 2.5 V fail-safe digital regulator is not available in LPOFF. As a consequence, after a wake-up event, the configuration of the fail-safe registers must be done again during initialization phase (256 ms open window).

12.1.7.5 ISO pulse in LPOFF

If the application has to sustain ISO pulses on V_{BAT} in LPOFF mode, the connection of an external Zener diode and a serial resistor to the ground is mandatory (see Figure 15). During repetitive ISO pulses on V_{BAT}, the

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

capacitors connected on V_{SUP} line are more and more charged and cannot be discharged due to the extremely low-current needed to maintain wake-up capabilities on IOs, CAN, and LIN. As a consequence, if a leakage path is not created artificially with those discrete components, the voltage on V_{SUP} line can exceed the absolute maximum rating supported by this pin.

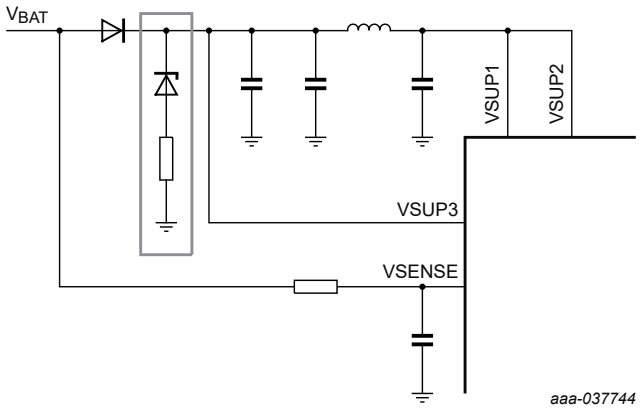


Figure 15. Components involved under ISO pulse in LPOFF

12.2 Mode and state description of fail-safe state machine

12.2.1 LBIST

Included in the fail-safe machine, the logic built-in self-test (LBIST) verifies the correct functionality of the FSSM at start-up. The fail-safe state machine is fully checked. If an issue is reported, the SAFE output pins FS0B and FS1B stays low and a flag is reported, the RSTB pin is released to allow diagnostic by the MCU. LBIST is run at start-up and after each wake-up event when the device is in LPOFF mode.

LBIST fail does not gate the RSTB pin release, but prevents the FS0B and FS1B pins release. It allows the MCU diagnostic keeping the application in a safe sate.

12.2.2 Select pin configuration

This phase detects the required voltage level to apply on VAUX and VCCA according to the resistor value connected between the SELECT pin and Ground or VPRE, and the deep fail-safe configuration. This mode is the equivalent mode seen in the main state machine. In the fail-safe machine this detection is used to internally set the UV/OV threshold on VCCA and VAUX for the voltage supervision, and to enable/disable the deep fail-safe feature.

12.2.3 ABIST

Included in the fail-safe machine, the analog built-in self-test (ABIST) verifies the correct functionality of the analog part of the device like the overvoltage and undervoltage detections of the voltage supervisor and the fail-safe outputs feedback. ABIST fail does not gate the RSTB pin release, but prevents the FS0B and FS1B pins release. It allows the MCU diagnostic, keeping the application in safe sate.

12.2.3.1 ABIST1

The first ABIST1 (Table 9) is always run at start-up and after each wake-up event when device is in LPOFF mode.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 9. Regulators and fail-safe pins checked during ABIST1

Parameters	Overvoltage	Undervoltage	OK/NOK
VPRE	X		
VCORE (including FCRBM)	X	X	
VCCA	X	X	
RSTB			X
FS0B			X

12.2.3.2 ABIST2

The second ABIST2 (Table 10) is run on demand by a SPI command from the MCU. ABIST2 must be executed and pass for FS1B and VAUX, when VAUX is declared safety critical (overvoltage and/or undervoltage have an impact on fail-safe outputs) to release the FS0B pin. Consequently, ABIST2 must be executed at start-up and after each wake-up event when device is in LPOFF mode, to release the fail-safe pin FS0B.

Table 10. Regulators and fail-safe pins checked during ABIST2

Parameters	Overvoltage	Undervoltage	OK/NOK
VAUX	X	X	
FS1B			X

12.2.4 Release RSTB

In this state, the device releases the RSTB pin.

12.2.5 INIT_FS

This mode is automatically entered after the device is 'powered on' and the built-in self-tests (logic LBIST and analog ABIST1) have been executed. This INIT_FS mode starts as soon as RSTB is released.

In this mode, the device can be configured via the SPI within a maximum time of 256 ms, including first watchdog refresh. Some registers can only be configured in this mode and is locked when leaving INIT_FS mode (see Table 19 and Table 20). It is recommended, to configure the device first before sending the first WD refresh. As soon as the first good watchdog refresh is sent by the MCU, the device leaves this mode and goes into normal WD mode.

12.2.6 Normal WD

In this mode, the device waits for a periodic watchdog refresh coming from the MCU, within a specific configured window timing. Configuration of the watchdog window period can be set during INIT_FS phase or in this mode. This mode is exited if a fault occurs leading to an RSTB activation (external reset request included).

12.2.7 Assert RSTB

When the reset pin is asserted low by the device, a delay runs, to release RSTB, if there are no faults present. The reset low duration time is configurable via the SPI in the INIT_ FSSM register, which is accessible for writing only in the INIT_FS phase.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

12.2.8 Assert FSxB and ABIST2

These functions are executed in parallel to INIT_FS or normal WD states of the fail-safe state machine.

12.3 Deep fail-safe state

When the deep fail-safe function is enabled, the fail-safe state machine monitors and counts the number of faults happening, in case of fault detection (see Section 12.5.3). As soon as either the fault error counter reaches its final value or the RESET pin remains asserted low for more than 8.0 s, the device moves to deep fail-safe state in the functional state diagram (Figure 16).

When the device is in deep fail-safe state, all the regulators are off (except VKAM if VKAM was on), RSTB, FS0B, and FS1B are activated. To exit this state, a key off/key on action is needed. IO_0 is usually connected to key signal. Key off (IO_0 low) moves the device to LPOFF-deep FS, and key on (IO_0 high) wakes up the device.

During power up phase, the 8.0 s timer starts when the fail-safe state machine enters in the 'Wait_V_{PRE}' state and stops when the RSTB pin is released. During 'INIT_FS' state, the 8.0 s timer can be disabled in the register INIT_FS_IMPACT. During 'normal WD' state, the 8.0 s timer is activated at each RSTB pin assertion.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

12.4 Functional state diagram

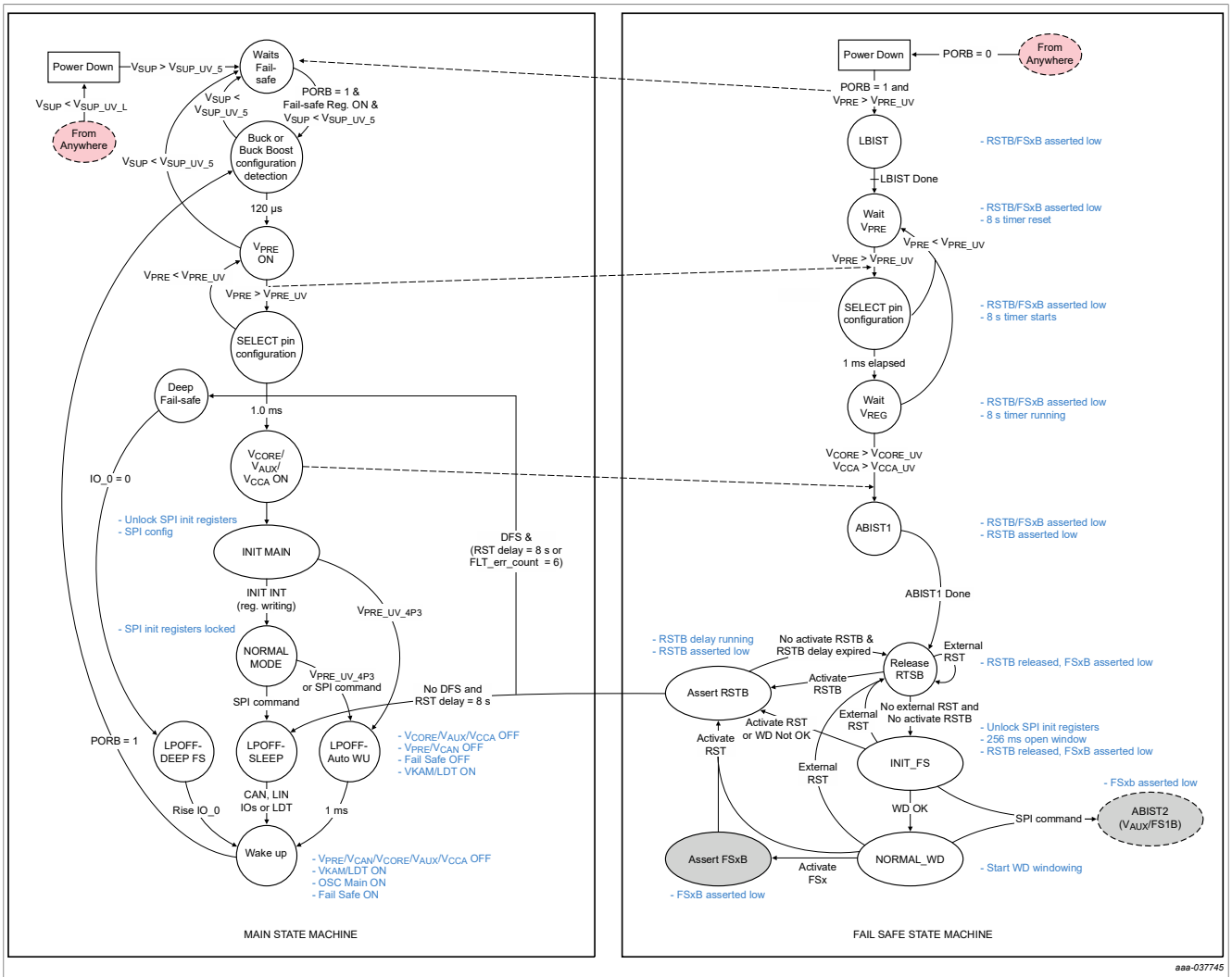


Figure 16. Simplified state diagram

12.5 Fail-safe machine

To fulfill safety critical applications, the FS6500/FS4500 integrates a dedicated fail-safe machine (FSM). The FSM is composed of three main sub-blocks: the voltage supervisor (VS), the fail-safe state machine (FSSM), and the fail-safe output driver (FSO).The FSM is electrically independent from the rest of the circuitry, to avoid common cause failure.

For this reason, the FSM has its own voltage regulators (analog and digital), dedicated band gap, and its own oscillator. Three power supply pins (VSUP 1, 2, and 3) are used to overtake a pin lift issue. The internal voltage regulators are directly connected on VSUP (one bonding wire per pin is used). Additionally, the ground connection is redundant as well to avoid any loss of ground.

All the voltages generated in the device are monitored by the voltage supervisor (under and overvoltage) owing to a dedicated internal voltage reference (different from the one used for the voltage regulators). The result is reported to the MCU through the SPI and delivered to the fail-safe state machine (FSSM) for action, in case of a fault. All the safety relevant signals feed the FSSM, which handles the error handling and controls the fail-safe outputs.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

There are three fail-safe outputs: RSTB (asserted low to reset the MCU), FS0B, and FS1B (asserted low to control any fail-safe circuitry). The fail-safe machine is in charge of bringing and maintaining the application in a fail-safe state.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

12.5.1 Fail-safe machine state diagram

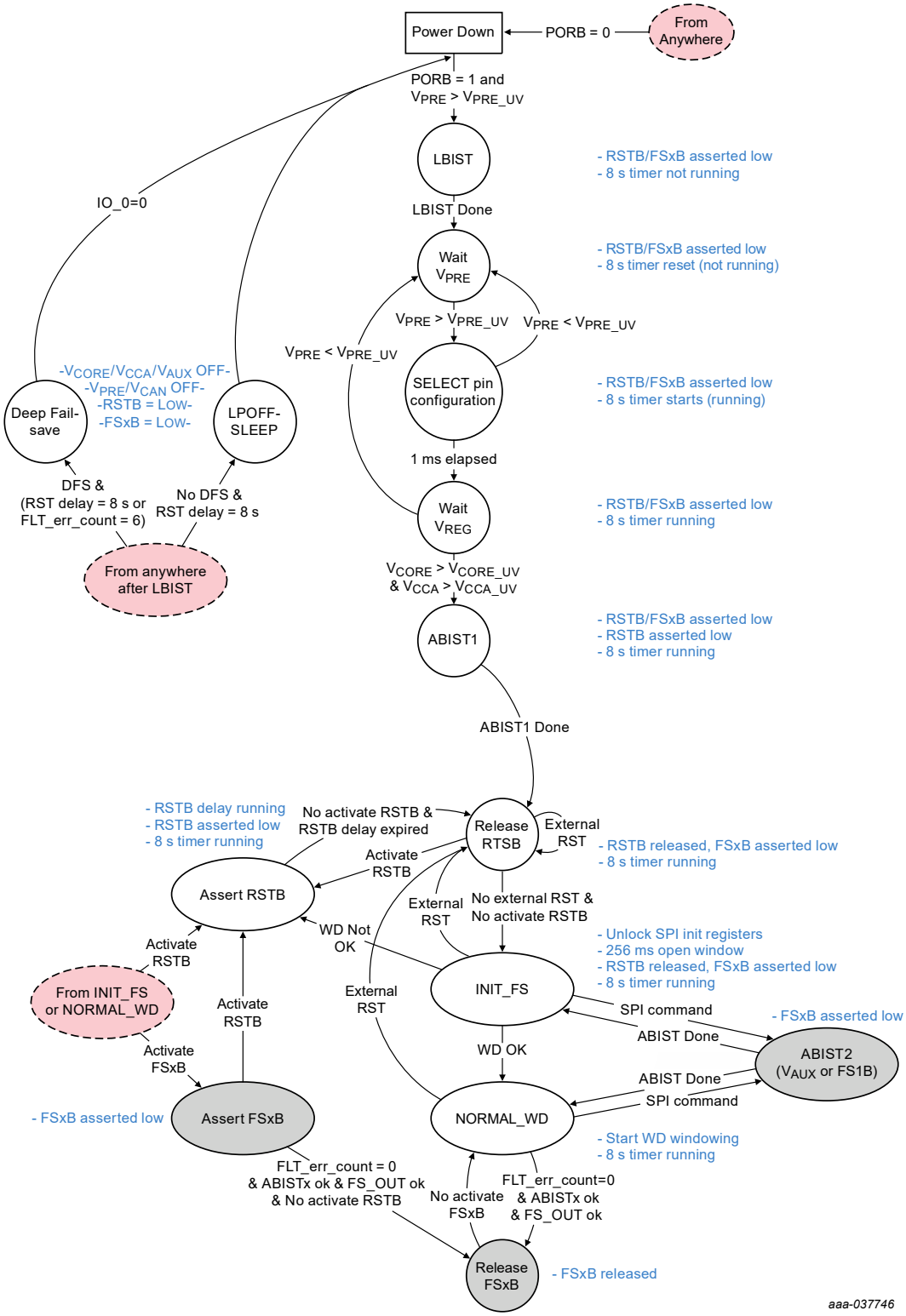


Figure 17. Detailed fail-safe state diagram

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

12.5.2 Watchdog operation

A windowed watchdog is implemented in the FS6500/FS4500 and is based on the "question/answer" principle (challenger). The watchdog must be continuously triggered by the MCU in the open watchdog window, otherwise an error is generated. The error handling and watchdog operations are managed by the fail-safe state machine. For debugging purpose, this functionality can be inhibited by setting the right voltage on the DEBUG pin at start-up.

The watchdog window duration is selectable through the SPI during the INIT_FS phase or in normal mode. The following values are available: 1.0 ms, 2.0 ms, 3.0 ms, 4.0 ms, 6.0 ms, 8.0 ms, 12 ms, 16.0 ms, 24 ms, 32 ms, 64 ms, 128 ms, 256 ms, 512 ms, and 1024 ms. The watchdog can also be inhibited through the SPI register in INIT_FS phase to allow "reprogramming" (i.e. at vehicle level thru CAN).

An 8-bit pseudo-random word is generated by implementing a linear feedback shift register in the FS6500/FS4500. The MCU can send the seed of the LFSR or use the LFSR generated by the FS6500/FS4500 during the INIT phase and performs a pre-defined calculation. The result is sent through the SPI during the "open" watchdog window and verified by the FS6500/FS4500. When the result is right, a new LFSR is generated and the watchdog window is restarted. When the result is wrong, the WD error counter is incremented, the watchdog window is restarted, an INTB is generated, and the LFSR value is not changed. Any access to the WD register during the "closed" watchdog window is considered a wrong WD refresh.

12.5.2.1 Normal operation (first watchdog refresh)

At power up, when the RSTB is released as high (after around 16.5 ms), the INIT phase starts for a maximum duration of 256 ms, and this is considered as a fully open watchdog window. During this initialization phase the MCU sends the seed for the LFSR, or uses the default LFSR value generated by the FS6500/FS4500 (0xB2), available in the WD_LFSR register (Table 90). Using this LFSR, the MCU performs a simple calculation based on this formula. As an example, the result of this calculation based on LFSR default value (0xB2) is 0x4D.

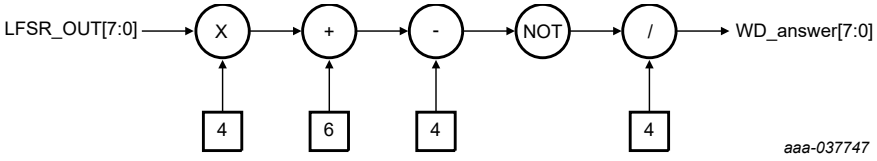


Figure 18. Watchdog answer calculation

The MCU sends the results in the WD_ANSWER register (Table 92). When the watchdog is properly refreshed during the open window, the 256 ms open window is stopped and the initialization phase is finished. A new LFSR is generated and available in the WD_LFSR register (Table 90). If the watchdog refresh is wrong or if the watchdog is not refreshed during this 256 ms open window (INIT_FS phase), the device asserts the RSTB, FS0B, and the fault error counter is incremented by '1'.

After a good watchdog refresh, the device enters the Normal WD refresh mode, where open and closed windows are defined either by the configuration made during initialization phase in the WD_WINDOW register (Table 88), or by the default value already present in this register (3.0 ms).

12.5.2.2 Normal watchdog refresh

The watchdog must be refreshed during every open window of the window period configured in the register WD_ANSWER. Any WD refresh restarts the window. This ensures the synchronization between MCU and FS6500/FS4500.

The duration of the 'window' is selectable through the SPI with no access restriction, meaning the window duration can be changed in the INIT phase or normal mode. Doing the change in normal operation allows the system integrator to configure the watchdog window duration on the fly:

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

- The new WD window duration (except after disable) is taken into account when a write in the WD_ANSWER register occurs (good or bad WD answer) or when the previous WD window is finished without any writing (WD timeout).
- The new WD window duration after disable is taken into account when the SPI command is validated.

The duty cycle of the window is set to 50 % ±10 % and is not modifiable.

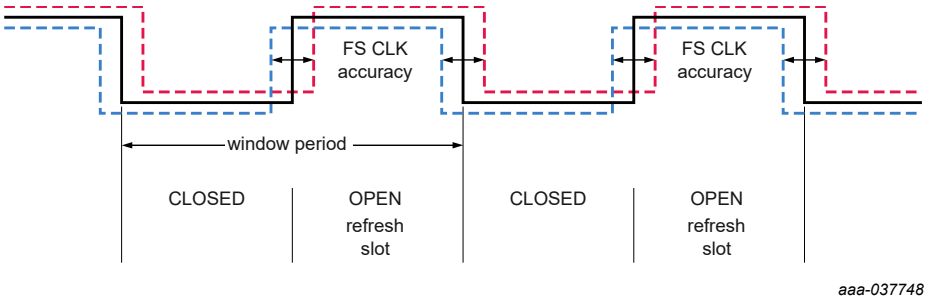


Figure 19. Windowed watchdog with FS clock accuracy

12.5.2.3 Watchdog in debug mode

When the device is in debug mode (entered via the DEBUG pin), the watchdog continues to operate, but does not affect the device operation by asserting a reset of the fail-safe pins. For the user, operation appears without the watchdog. If needed and to debug the watchdog itself, the user can operate as in normal mode and check LFSR values, the watchdog refresh counter, the watchdog error counter, and the reset counter. This allows the user to debug their software and ensure a good watchdog strategy in the application.

12.5.2.4 Wrong watchdog refresh handling

Error counters and strategy are implemented in the device to manage wrong watchdog refreshes from the MCU. According to consecutive numbers of wrong watchdog refreshes, the device can decide to assert the RSTB and/or FS0B pin, depending on the safety configuration set during the INIT_FS phase (WD_IMPACT bit in INIT_SF_IMPACT register, Table 86).

12.5.2.5 Watchdog error counter

The watchdog error counter is implemented in the device to filter the incorrect watchdog refresh. Each time a watchdog failure occurs, the device increments this counter by 2. The WD error counter is decremented by 1 each time the watchdog is properly refreshed. This principle ensures a cyclic 'OK/NOK' behavior converges to a failure detection. To allow flexibility in the application, the maximum value of this counter is configurable in the INIT_WD_CNT register, but only when device is in INIT_FS mode.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

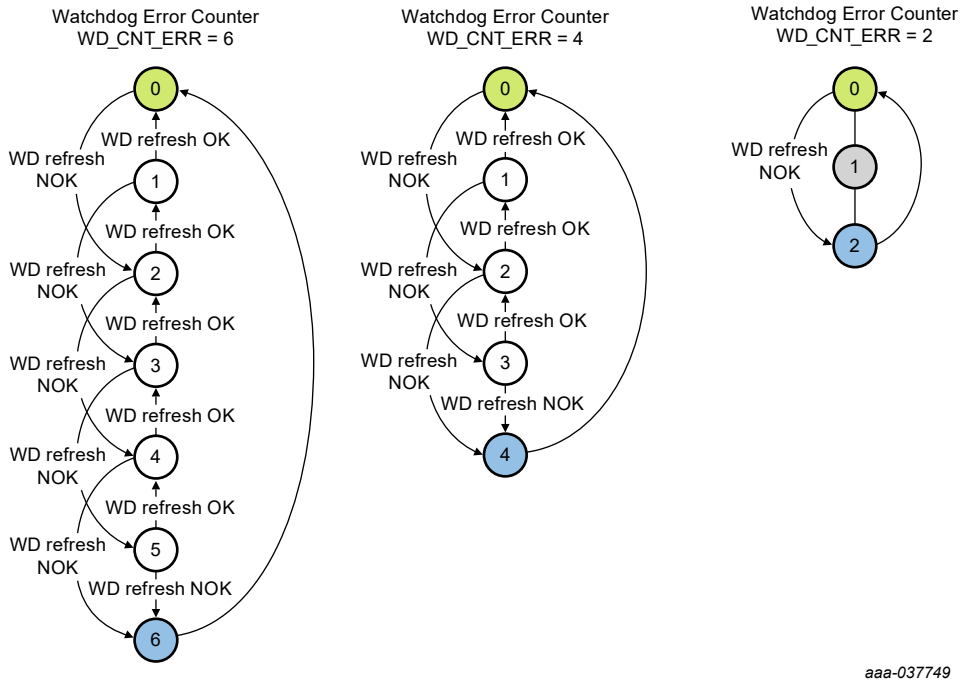


Figure 20. Watchdog error counter configuration (INIT_WD_CNT register, Bits WD_CNT_ERR_1:0)

12.5.2.6 Watchdog refresh counter

The watchdog refresh counter is used to decrement the fault error counter. Each time the watchdog is properly refreshed, the watchdog refresh counter is incremented by ’1’. Each time the watchdog refresh counter reaches ’6’ and if next WD refresh is also good, the fault error counter is decremented by ’1’ (case with WD_CNT_RFR_1:0 configured at 6).

Whatever the position the watchdog refresh counter is in, each time there is a wrong refresh watchdog, the watchdog refresh counter is reset to ’0’. To allow flexibility in the application, the maximum value of this watchdog refresh counter is configurable in the INIT_WD_CNT register, but only when device is in INIT_FS mode.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

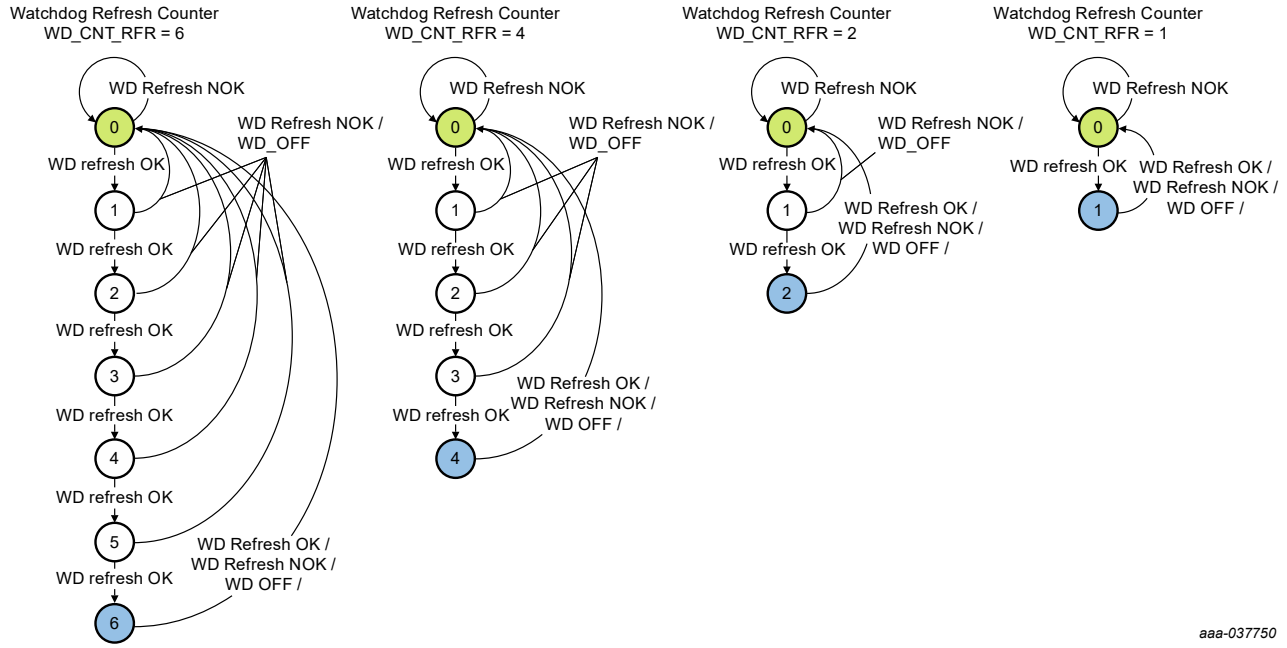


Figure 21. Watchdog refresh counter configuration (INIT_WD_CNT register, WD_CNT_RFR_1:0)

Table 11. Watchdog error table

		Window	
		CLOSED	OPEN
SPI	BAD key	WD_NOK	WD_NOK
	GOOD key	WD_NOK	WD_OK
	None (timeout)	No_issue	WD_NOK

Any access to the watchdog register during the 'closed' watchdog window is considered as a wrong watchdog refresh. Watchdog timeout, meaning no WD refresh during closed or open windows, is considered as a wrong WD refresh.

12.5.3 Fault error counter

The fault error counter manages and counts the number of faults occurring in the application. This counter is incremented not only for the fault linked to consecutive wrong refresh watchdogs, but also for other sources of fault (undervoltage, overvoltage, external reset,...).

The fault error counter is incremented by 1, each time RSTB and/or FS0B pin is asserted. When FS0B is asserted, the fault error counter is incremented by 1, every time the watchdog error counter maximum value is reached. The fault error counter has two output values (intermediate and final).

- The intermediate value can be used to force the FS0B activation or to generate a RSTB pulse depending on the FLT_ERR_IMP_1:0 bit configuration in INIT_FAULT register.
- The final value is used to handle the transition to deep fail-safe when the SELECT pin is connected to Ground. If the SELECT pin is connected to VPRE, the main state machine remains in normal mode and the regulators remain on.

The intermediate value of the fault error counter is configurable to '1' or '3' using the FLT_ERR_FS bit in the INIT_FAULT register (Table 83). The final value of the fault error counter is based on the intermediate configuration. This configuration must be done during INIT_FS phase.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

- FLT_ERR_FS = 0/Intermediate = 3; Final = 6 (Figure 22).
- FLT_ERR_FS = 1/Intermediate = 1; Final = 2 (Figure 23).

In any condition, if the RSTB pin is asserted low for a duration longer than eight seconds, the device goes to:

- Deep fail-safe if the DFS function is enabled (SELECT pin connected to ground)
- LPOFF-sleep if the DFS function is disabled (SELECT pin connected to VPRE)
  The following faults lead to an increment of the fault error counter and can be configured:
- Watchdog error counter = max value (6 by default)
- VCORE, VCCA, VAUX undervoltage
- VCORE, VCCA, VAUX overvoltage
- FCRBM follows VCORE configuration
- IO_45 error detection (external IC error)
  The following faults lead to an increment of the fault error counter and cannot be configured:
- VPRE overvoltage
- Watchdog refresh not OK or watchdog timeout during INIT phase
- SPI DED
- ABIST1, ABIST2 fail
- RSTB short to high (by cascaded effect of FS0B assertion)
- External reset (except reset extension by MCU after reset assertion by the device)
- IO_23 error detection (FCCU)

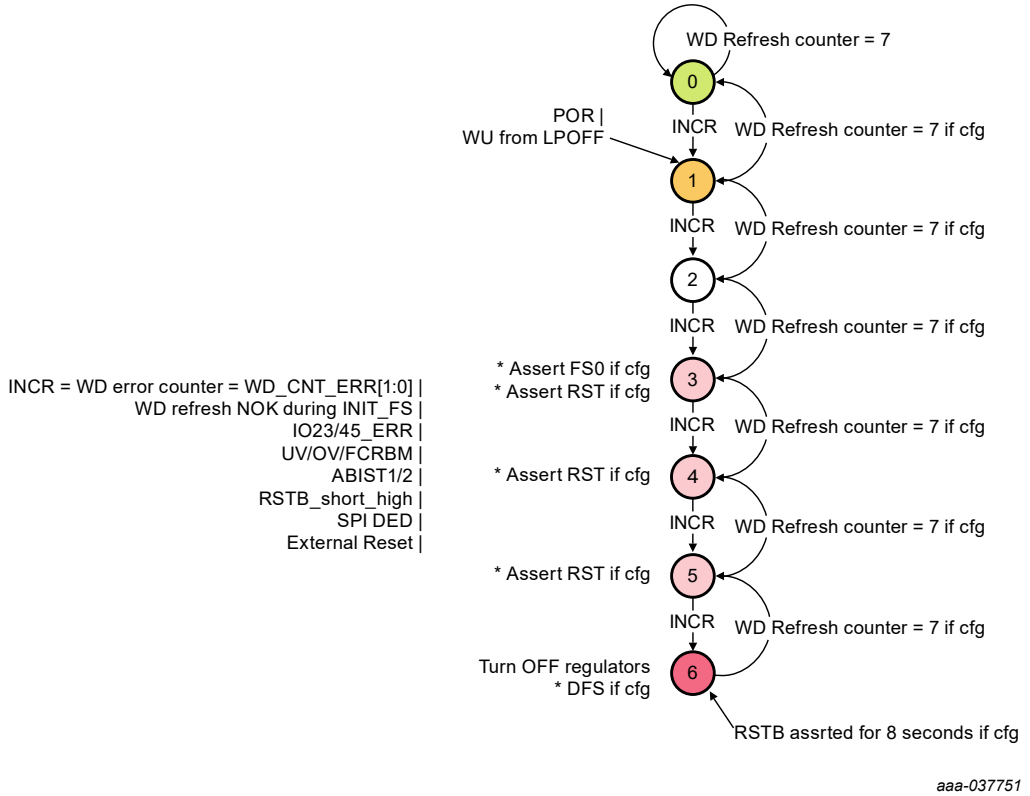


Figure 22. Fault error counter (FLT_ERR_FS = 0, WD_CNT_RFR = 6)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

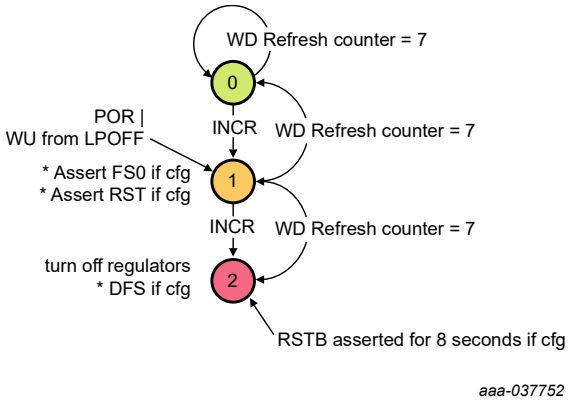


Figure 23. Fault error counter (FLT_ERR_FS = 1, WD_CNT_RFR = 6)

12.5.3.1 Fault error counter intermediate value

Figure 24 illustrates the fault error counter increment when the watchdog error counter maximum value is reached.

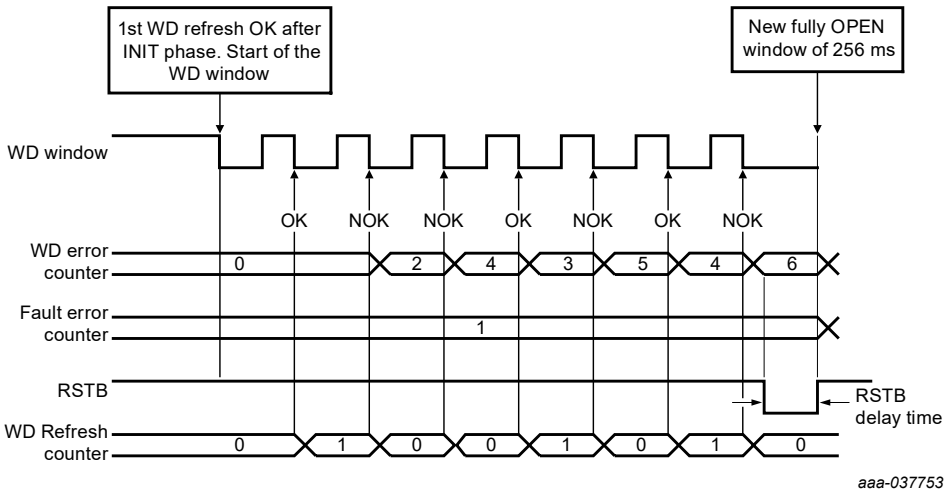


Figure 24. Example of WD operation generating a reset (WD_CNT_ERR = 6)

Figure 25 illustrates the RSTB and FS0B possible behavior at the fault error counter intermediate value depending on WD_IMPACT_1:0 and FLT_ERR_IMP_1:0 bits configurations:

- #1, WD_IMPACT_1:0 = ’01’ and FLT_ERR_IMP_1:0 = ’01’: WD impact on RSTB only and FS0B is asserted low if FLT_ERR_CNT ≥ intermediate value
- #2, WD_IMPACT_1:0 = ’10’ and FLT_ERR_IMP_1:0 = ’10’: WD impact on FS0B only and RSTB is asserted low if FLT_ERR_CNT ≥ intermediate value and WD error counter = WD_CNT_ERR[1:0]

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

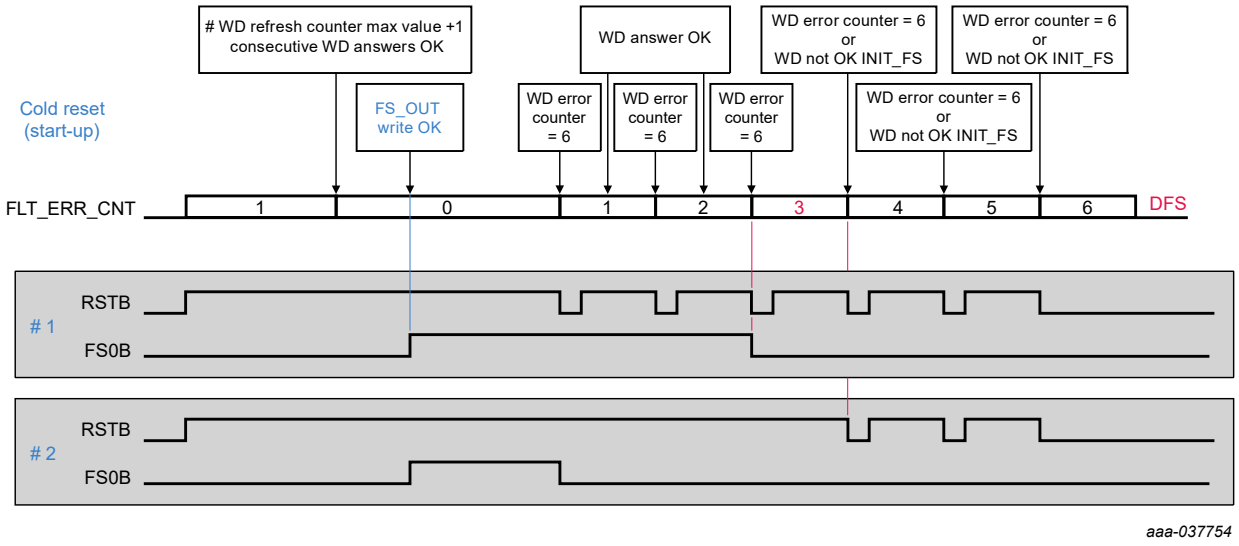


Figure 25. Example of RTSB and FS0B behavior when FLT_ERR_CNT ≥ intermediate value

12.5.3.2 Fault error counter at start-up or resuming from LPOFF mode

At start-up or when resuming from LPOFF mode, the fault error counter starts at level 1 and FS0B is asserted low. To release FS0B, the fault error counter must go back to a '0' value due to several consecutive good watchdog refreshes. The right command is sent to the RELEASE_FSxB register (Figure 27). With the default watchdog refresh counter configuration (WD_RFR_CNT = 6), seven consecutive good watchdog refreshes decrease the fault error counter to 0 (Figure 26).

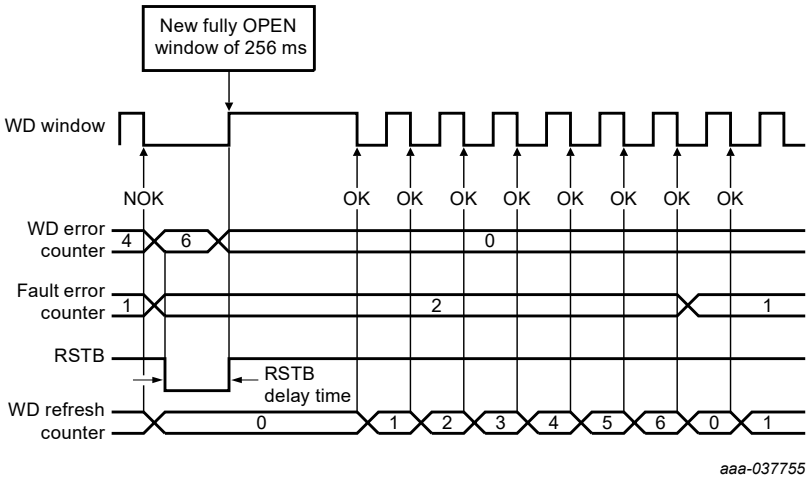


Figure 26. Example of WD operation leading a decrement of the fault error counter (WD_CNT_RFR = 6)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

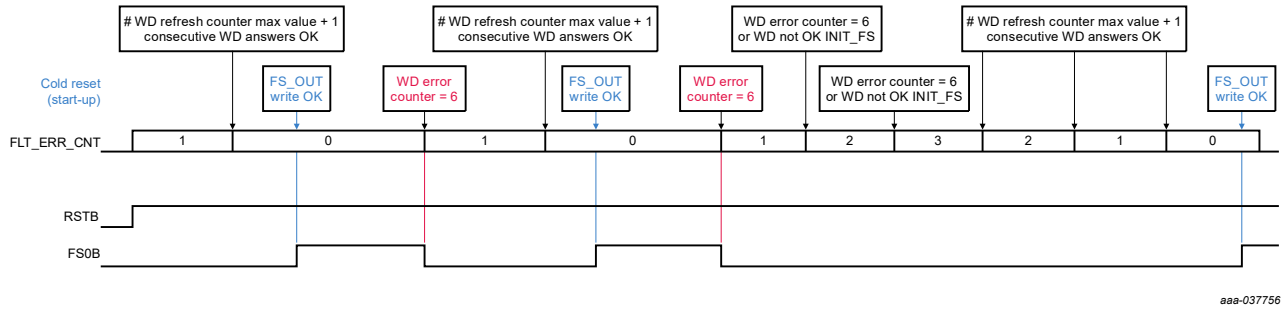


Figure 27. Fault error counter and FS0B deactivation sequence (FLT_ERR_FS = 0 and WD_CNT_ERR = 6)

12.5.4 RESET (RSTB) activation

The activation of RSTB depends on the fail-safe state machine configuration performed during the INIT_FS phase.

The following faults impact on RSTB activation can be configured:

- Watchdog error counter = max value (6 by default)
- VCORE, VCCA, VAUX undervoltage
- VCORE, VCCA, VAUX overvoltage
- FCRBM follows VCORE configuration
- IO_23 error detection (FCCU)
- Fault error counter level

The following faults impact on RSTB activation cannot be configured:

- VPRE overvoltage
- Watchdog refresh not OK or watchdog timeout during INIT phase
- FS0B short to high
- RSTB pulse requested by SPI

12.5.5 Fail-safe output (FS0B) activation

The activation of FS0B depends on the fail-safe state machine configuration performed during the INIT_FS phase.

The following faults impact on FS0B activation can be configured:

- Watchdog error counter = max value (6 by default)
- VCORE, VCCA, VAUX undervoltage
- VCORE, VCCA, VAUX overvoltage
- FCRBM follows VCORE configuration
- IO_23 error detection (FCCU)
- IO_45 error detection (external IC error)
- Fault error counter level

The following faults impact on FS0B activation cannot be configured:

- VPRE overvoltage
- Watchdog refresh not OK or watchdog timeout during INIT phase
- LBIST, ABIST1/2 fail
- RSTB, FS1B short to high
- FS0B low requested by SPI

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

- SPI DED

12.5.6 Fail-safe output (FS1B) activation

The activation of FS1B follows the activation of FS0B with a configurable delay (t_{DELAY}) or for a configurable duration (t_{DUR}).

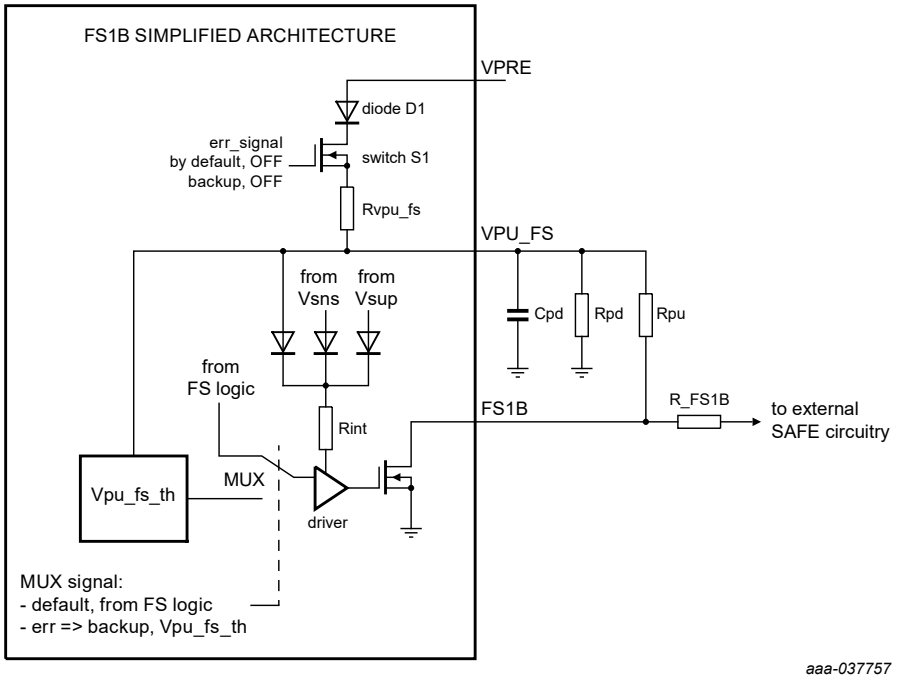


Figure 28. FS1B simplified architecture

VPU_FS is internally connected to VPRE with a reverse diode protection and protected against short-circuit by R_{VPU_FS}. The R_FS1B resistor is needed to be robust against ISO 7637[(14)] pulses.

12.5.6.1 t_{DELAY} operation

In t_{DELAY} configuration, FS1B is asserted low with a delay after FS0B is activated, and remains asserted until it is released by the SPI.

The delay between FS0B and FS1B activation is configurable via the SPI from 0 ms to 3150 ms with the combination of FS1B_TIME_3:0 and FS1B_TIME_RANGE bits. This digital delay is generated by the fail-safe logic with an accuracy of ±10 %. FS1B can be activated at the same time as FS0B if t_{DELAY} = 0 or after a programmable delay if t_{DELAY} > 0 (Figure 29).

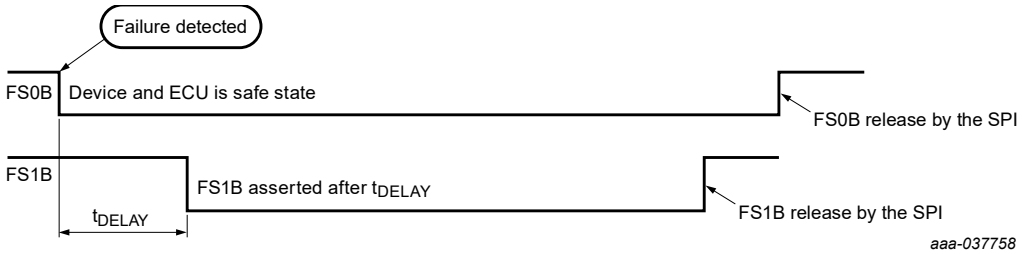


Figure 29. t_{DELAY} operation

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

To ensure the FS1B delay is guaranteed in all system failure cases,VPU_FS pin must be used as a FS1B pull-up (Figure 28).

The R_{PD}/C_{PD} components at VPU_FS provide a configurable backup delay under system failure (loss of internal fail-safe oscillator or loss of power supply). VPU_FS circuit consumption is negligible (~1.0 µA). Consequently, the external components R_{PD}/C_{PD} can be easily calculated for the desired backup delay (Figure 30).

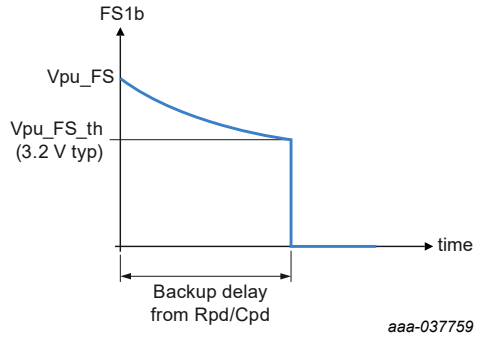


Figure 30. Backup delay operation

R_{PD}/C_{PD} calculation:

- $R_{TOT} = R_{INT} // R_{PD}$ with R_{INT} = 1.0 M ±50 %
- $V_{PU_FS} = [(V_{PRE} - V_{DIODE}) \times R_{TOT}/(R_{TOT} + R_{VPU_FS})]$
- $V_{PU_FS_TH} = V_{PU_FS} \times e(-t_{DELAY}/R_{TOT}C_{PD})$
- $t_{DELAY} = -R_{TOT}C_{PD} \times Ln (V_{PU_FS_TH}/V_{PU_FS})$

R_{PD}/C_{PD} typical use case:

- t_{DELAY} = 33 ms, $V_{PU_FS_TH}$ = 3.2 V, V_{PU_FS} = 5.5 V
- R_{PD} = 16 KΩ, C_{PD} = 3.3 µF

The switch S1 is opened by default and must be closed by a SPI command, due to the FS1B_DLY_REQ bit in the SF_OUTPUT_REQUEST register, before releasing the FS1B pin. V_{PU_FS} rise time is limited by the time constant of $R_{VPU_FS} \times C_{PD}$. 95 % of V_{PU_FS} is reached after 3 x $R_{VPU_FS} \times C_{PD}$ = 15 ms. It is recommended to select high R_{PD} resistor value to be negligible versus R_{VPU_FS} and low C_{PD} capacitor value to reduce V_{PU_FS} rising time.

The external R_{PD}/C_{PD} components connected to VPU_FS are used to generate an FS1B backup delay. This backup delay can be verified at the application level to cover latent faults on these components, by opening the internal switch connecting VPRE to VPU_FS with the FS1B_DLY_REQ bit in the SF_OUPUT_REQ register (FS0B must be asserted first). The backup delay accuracy depends only on external component accuracy.

12.5.6.2 $t_{DURATION}$ operation

In $t_{DURATION}$ configuration, FS1B is asserted low at the same time as FS0B for a configurable duration, and is automatically released after $t_{DURATION}$ timing (Figure 31). The FS1B activation duration is configurable via the SPI from 0 ms to 3150 ms with the combination of the FS1B_TIME_3:0 and FS1B_TIME_RANGE bits. This digital duration is generated by the fail-safe logic with an accuracy of ±10 %.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

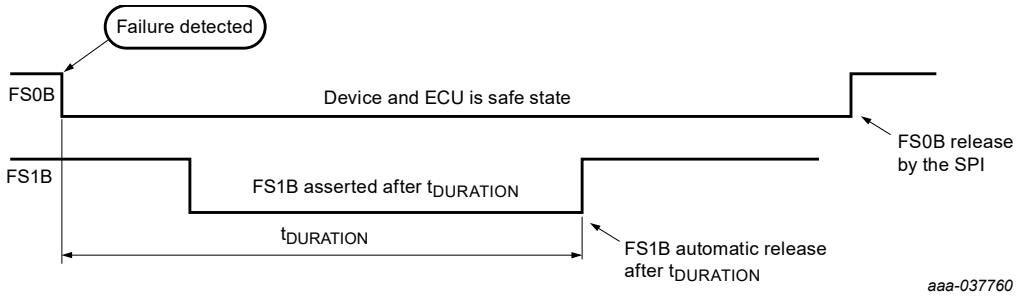


Figure 31. $t_{DURATION}$ operation

12.5.7 Fail-safe outputs (FS0B and FS1B) release

When the fail-safe outputs FS0B and consequently FS1B are asserted low by the device due to a fault, some conditions must be validated before allowing these pins to be released by the device. These conditions are:

- ABIST2_FS1B_OK=1 if part number with FS1B
- ABIST2_VAUX_OK=1 except if VAUX_FS_OV_1:0=VAUX_FS_UV_1:0="00"
- Fault is removed
- Fault error counter must be at ’0’
- Close the S1 switch if FS1B backup delay was engaged (FS1B_DLY_DRV bit = 1)
- RELEASE_FSxB register must be filled with the right value

12.5.7.1 RELEASE_FSxB register

When a fault is removed and the fault error counter changes back to level ’0’, a right word must be filled in the RELEASE_FSxB register. The value depends on the current WD_LFSR. LSB, MSB must be swapped, and a negative operation per bit must be applied.

FS0B and FS1B can be released independently or at the same time, depending on the configuration of the first three bits of the RELEASE_FSxB register (Table 12).The RELEASE_FSxB write command should be done after a WD_LFSR read command. If FS0B and FS1B are released sequentially, the procedure must be done a first time for FS0B, and a second time for FS1B.

Table 12. RELEASE_FSxB register based on LFSR value

	WD_LFSR_7:0	b7	b6	b5	b4	b3	b2	b1	b0
Release FS0B	RELEASE_FSxB_7:0	0	1	1	$\overline{b0}$	$\overline{b1}$	$\overline{b2}$	$\overline{b3}$	$\overline{b4}$
Release FS1B	RELEASE_FSxB_7:0	1	1	0	$\overline{b3}$	$\overline{b4}$	$\overline{b5}$	$\overline{b6}$	$\overline{b7}$
Release FS0B and FS1B	RELEASE_FSxB_7:0	1	0	1	$\overline{b0}$	$\overline{b1}$	$\overline{b2}$	$\overline{b6}$	$\overline{b7}$

12.5.8 SPI DED

Some SPI registers affect some safety critical aspects of the fail-safe functions, and therefore are required to be protected against SEU (single event upset). Only fail-safe registers are concerned. During INIT_FS mode, access to fail-safe registers for product configuration is open. Once the INIT_FS phase is over, the Hamming circuitry is activated to protect registers content.

At this stage, if there is one single bit flip, the detection is made due to Hamming code, the error is corrected automatically (fully transparent for the user), and a flag is sent. If there are two errors (DED - dual error detection), the detection is made due to Hamming code but detected errors cannot be corrected. The flag is sent and FS0B is activated.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

12.6 Input voltage range

Due to the flexibility of the pre-regulator, the device can cover a wide battery input voltage range. However, a more standard voltage range can still be covered using only the buck configuration.

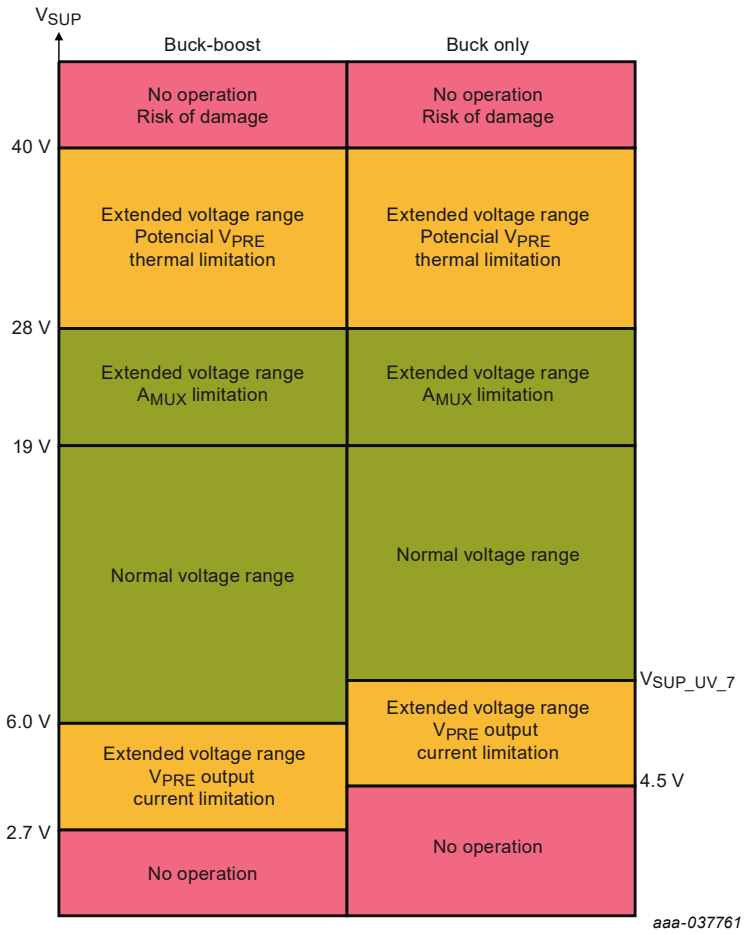


Figure 32. Input voltage range

- V_{SUP} > 28 V: Potential V_{PRE} thermal limitation

$R_{DS(on)}$, Current limitation and overcurrent detection are specified for V_{SUP} < 28 V.

- V_{SUP} > 19 V: MUX_OUT limitation

V_{SENSE} and IO_0 maximum analog input voltage range is 19 V. Internal 2.5 V reference voltage accuracy degraded.

- Buck only, V_{SUP} < $V_{SUP_UV_7}$:

CAN communication is guaranteed for V_{SUP} > 6.0 V. LIN communication stopped when V_{SUP} < 7.0 V if LIN_J2602_DIS bit is not set. For V_{CCA} and V_{AUX} 5.0 V configuration, undervoltage triggers at low V_{SUP} (See Section 9, $V_{CCA_UV_5}$ and $V_{AUX_UV_5}$).

12.7 Power management operation

A thermal sensor is implemented as close as possible to the pass transistor of each regulator (V_{PRE}, V_{CORE}, V_{CCA}, V_{CAN}) and an associated individual thermal shutdown (T_{SD}) protects these regulators independently. When the T_{SD} threshold of a specific regulator is reached, this regulator only is switched off and the information

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

is reported in the main state machine. The regulator restarts automatically when the junction temperature of the pass transistor decrease below the T_{SD} threshold.

12.7.1 VPRE voltage pre-regulator

A highly flexible SMPS pre-regulator is implemented in the FS6500/FS4500. Depending on the input voltage requirement, the device can be configured as 'non-inverting buck-boost converter' (Figure 34) or 'standard buck converter' (Figure 33). An external logic level MOSFET (N-type) is required to operate in 'non-inverting buck-boost converter'. The connection of the external MOSFET is detected automatically during the start-up phase.

The converter operates in current control mode in any configuration. The high-side switching MOSFET is integrated to make the current control easier. The PWM frequency is fixed at a typical 440 kHz. The compensation network is fully integrated. The V_{PRE} output voltage is regulated between 6.0 V and 7.0 V.

If the full current capability is not used for VCORE, VCCA, VAUX, and CAN_5V, an additional external LDO can be connected to VPRE to fulfill application needs, while the current load remains below the maximum current capability in all conditions.

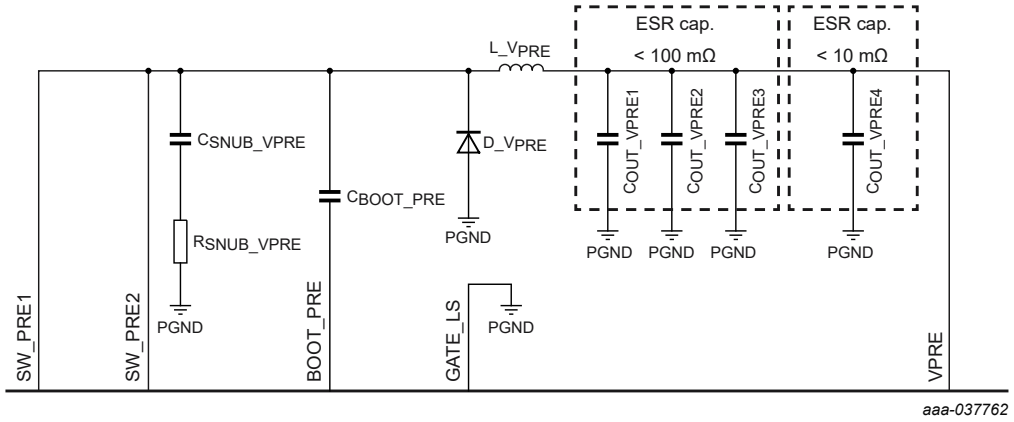


Figure 33. Pre-regulator: buck configuration

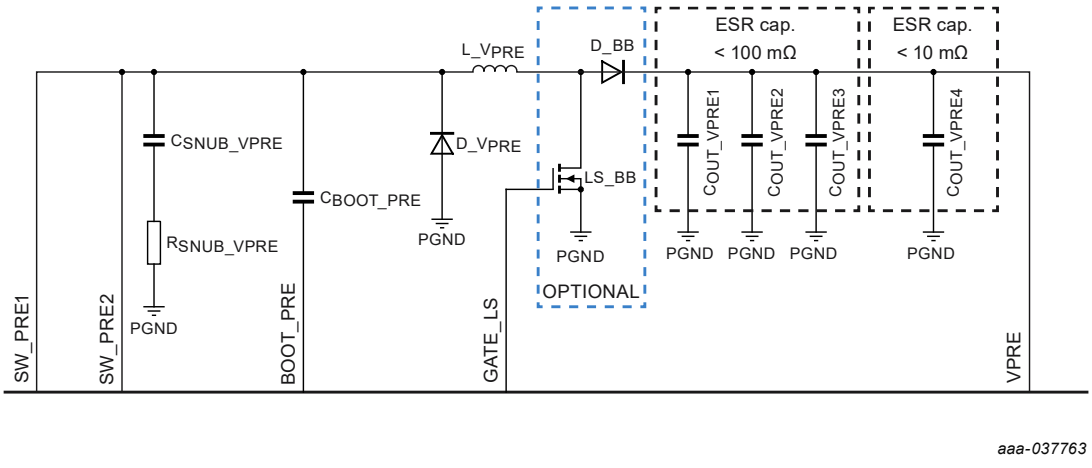


Figure 34. Pre-regulator: buck boost configuration

When the converter is set up to work in boost mode at low V_{SUP}, the transition between buck and boost mode is automatically handled by the device at the $V_{SUP_UV_7}$ threshold. Transition between buck mode and boost mode is based on hysteresis (Figure 35).

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

- When VSUP > $V_{SUP_UV_7}$, the converter works in buck mode and the VPRE output is regulated at 6.5 V typ.
- When VSUP < $V_{SUP_UV_7}$, the converter works in boost mode and the VPRE output is regulated at 6.3 V typ.

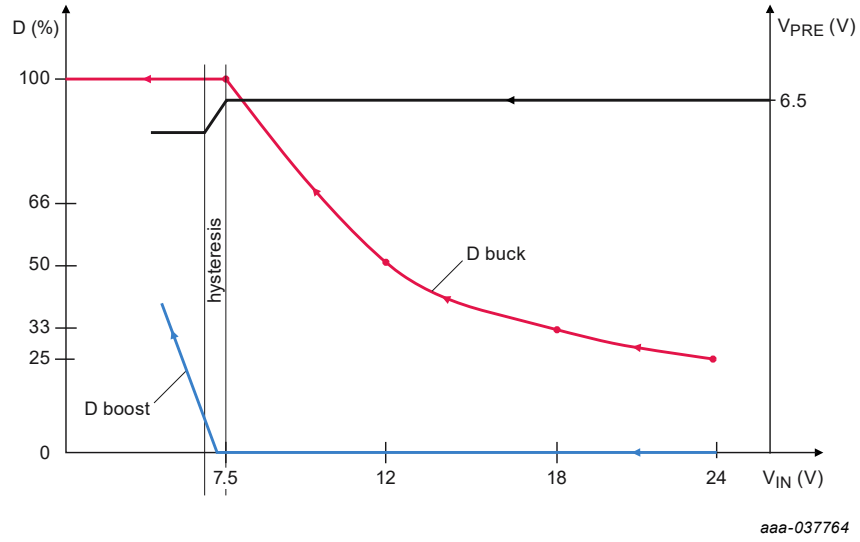


Figure 35. Transition between buck and boost

12.7.1.1 Power up and power down sequence

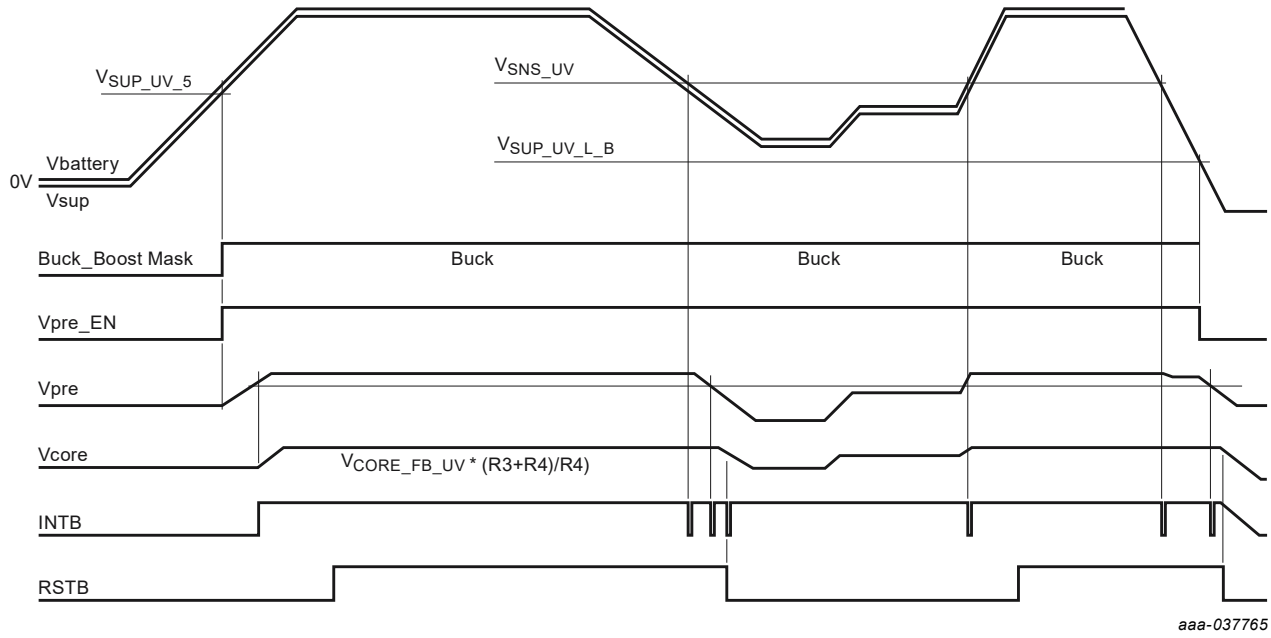


Figure 36. Buck configuration power up and power down

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

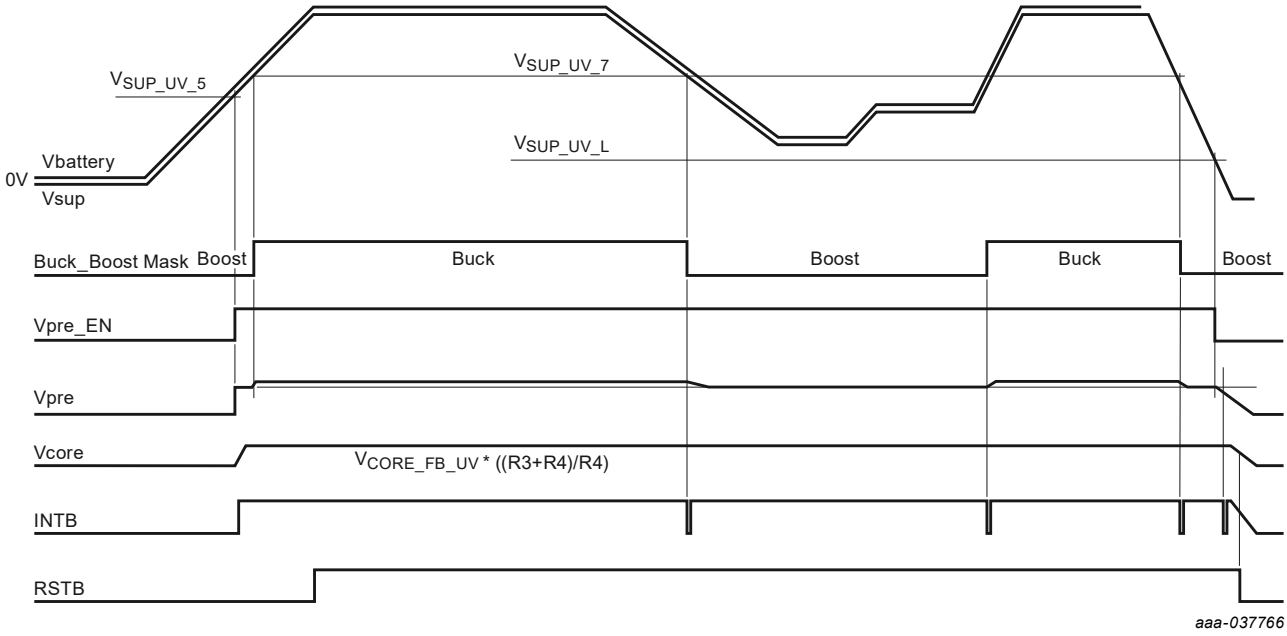


Figure 37. Buck boost configuration power up and power down

12.7.1.2 Cranking management

When VPRE is set up to work in buck only mode, the application can work down to VSUP = $V_{SUP_UV_L_B}$ = 4.5 V with a minimum of 500 mA current guaranteed on VPRE.

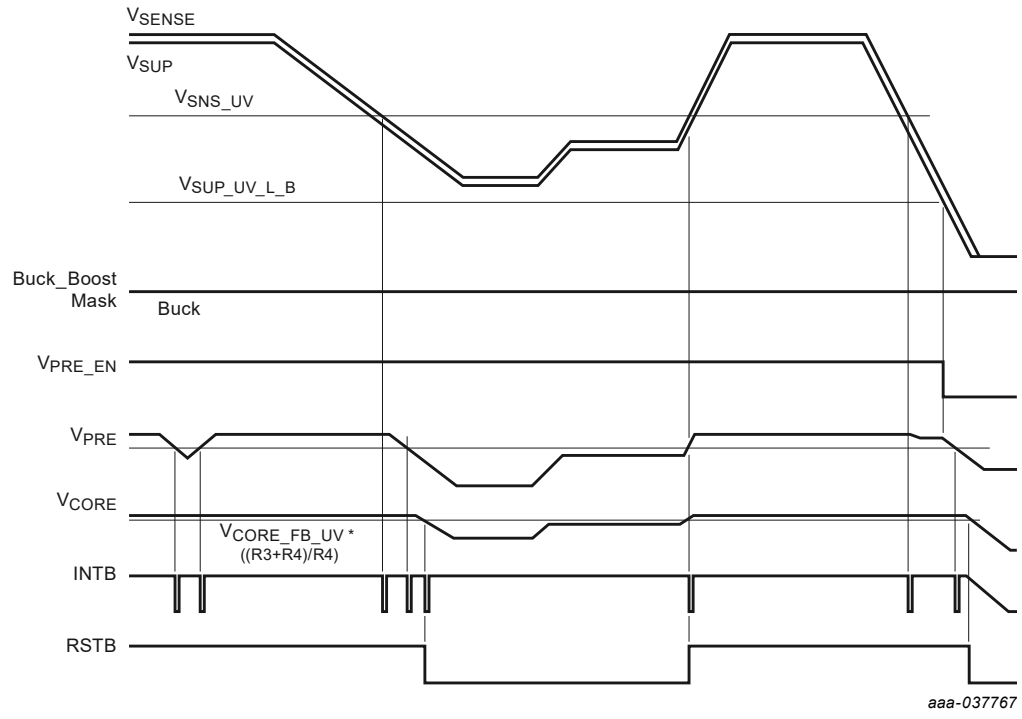


Figure 38. Behavior during cranking (buck configuration)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

When VPRE is set up to work in buck-boost mode, the application can work down to VSUP = $V_{SUP_UV_L}$ = 2.7 V with a minimum of 300 mA current guaranteed on VPRE. The buck-boost configuration helps to pass the LV124 specification requiring a minimum of 3.2 V on V_{BAT} supply during cold cranking conditions.

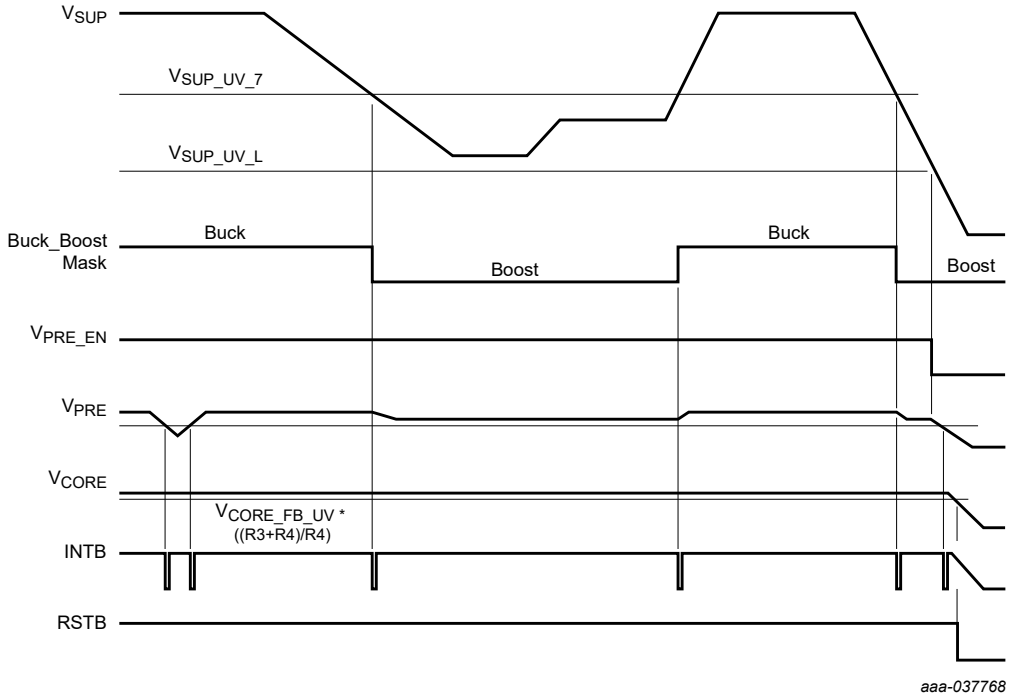


Figure 39. Behavior during cranking (buck boost configuration)

12.7.1.3 Light load condition

To improve the converter efficiency and avoid any unwanted output voltage increase, the VPRE voltage regulator operates in pulse skipping mode during light load conditions.

The transition between normal mode and pulse skipping mode is based on the comparison between the error amplifier output (EA_out) and pre-defined thresholds $V_{PRE_LL_H}$ and $V_{PRE_LL_L}$. When the error amplifier output reaches $V_{PRE_LL_L}$, the VPRE high-side transistor is switched off. When the error amplifier output reaches $V_{PRE_LL_H}$, the VPRE high-side transistor is switched on again for the next switching period (Figure 40).

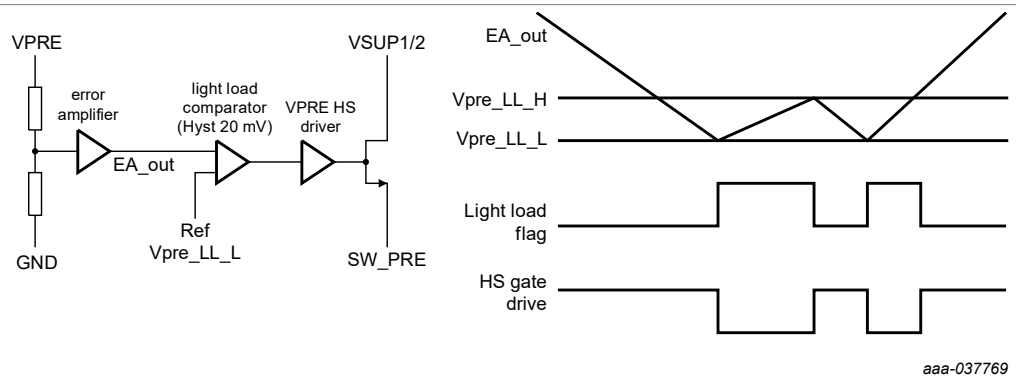


Figure 40. Description of light load conditions

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

12.7.1.4 Input power feed forward condition

To improve the converter efficiency during high input power conditions, the VPRE switching frequency is reduced from 440 kHz to 220 kHz, when VSUP > V_{SUP_IPFF}, to decrease the switching losses. The transition between the two frequencies is transparent for the application.

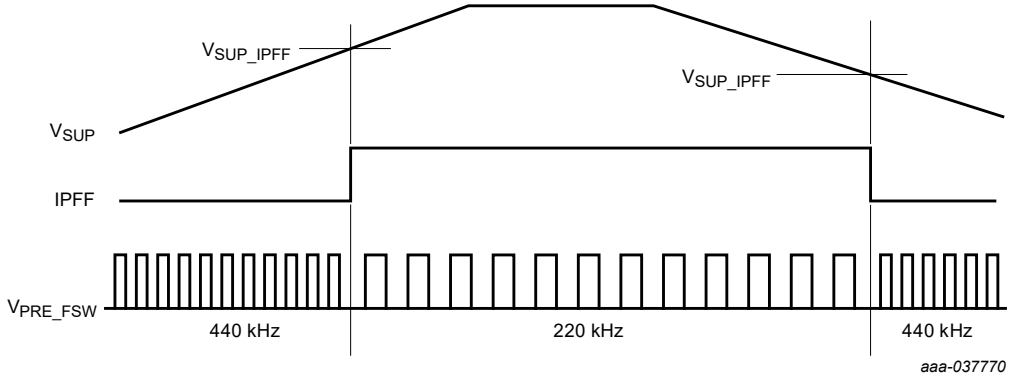


Figure 41. Input power feed forward principle

12.7.1.5 Overcurrent detection and current limitation

12.7.1.5.1 Overcurrent protection:

To ensure the integrity of the high-side MOSFET, an overcurrent detection is implemented. The regulator is switched off by the main state machine when the I_{PRE_OC} overcurrent detection threshold is reached three consecutive times. The overcurrent detection is blanked when the pass transistor is switched on during t_{PRE_OC} to avoid parasitic switch off of the high-side gate driver.

The VPRE output voltage decrease causes an undervoltage condition on one of the cascaded regulators (VCORE, VCCA, VAUX) and brings the device into fail-safe state. The overcurrent protects the regulator in case the SW_PRE pin is shorted to GND. The overcurrent works in buck mode only.

12.7.1.5.2 Current limitation:

A current limitation is also implemented to avoid uncontrolled power dissipation inside the device (duty cycle control) and limits the current. VPRE current limitation is automatically set based on the buck or buck-boost configuration. In buck only mode, the lowest current limitation I_{PRE_LIM2} is applied while in buck-boost mode, the highest current limitation I_{PRE_LIM1} is applied. The current limitation is blanked when the pass transistor is switched on during $t_{PRE_BLK_LIM}$ to allow short-circuit detection on the SW_PRE pin.

When I_{PRE_LIM} threshold is reached during buck mode, the high-side integrated MOSFET is switched off. When the I_{PRE_LIM} threshold is reached during boost mode, the external low-side MOSFET is switched off. In both cases, the MOSFET is not switched on again before the next rising edge of the switching clock.

The current limitation induces a duty cycle reduction and leads to the VPRE output voltage gradually dropping, which may cause an undervoltage condition on one of the cascaded regulators (VCORE, VCCA, VAUX) and bring the device to the fail-safe state. The current limitation does not switch off the regulator. The current limitation protects the regulator when the VPRE pin is shorted to GND.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

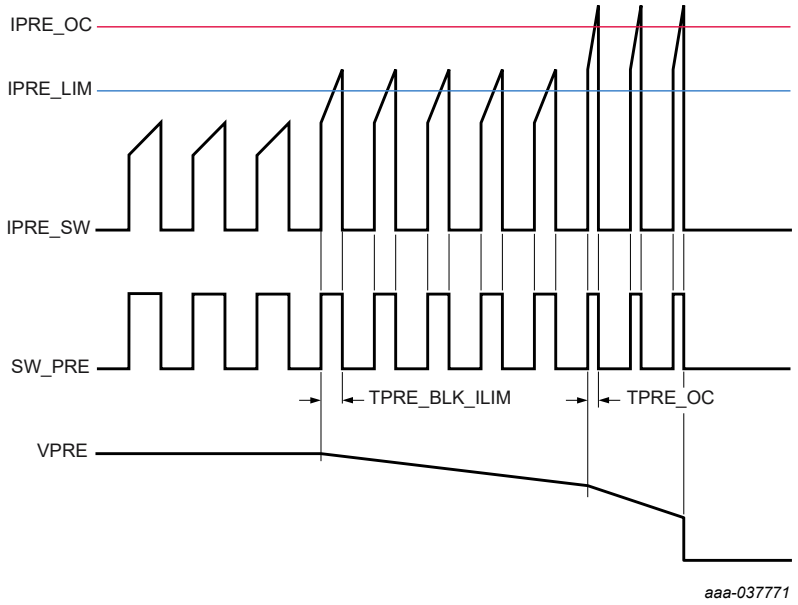


Figure 42. Overcurrent and current limitation scheme

12.7.1.6 VPRE voltage monitoring

The overvoltage detection switches off the regulator. The undervoltage detector is disabled when the regulator is switched off, reporting an undervoltage. Diagnostic is reported in the dedicated register and generates an Interrupt. The undervoltage detection does not switch off the regulator. However, V_{PRE} decrease may induce an undervoltage on a regulator attached to V_{PRE} (VCORE, VCCA, VAUX, or CAN_5V), and bring the application in fail-safe state depending on the supervisor configuration (registers INIT_VCORE_OVUV_IMPACT, INIT_VCCA_OVUV_IMPACT, INIT_VAUX_OVUV_IMPACT).

12.7.1.7 VPRE efficiency

VPRE efficiency versus current load is given for information based on typical external component criteria described in Figure 43, close to the graph and at typical automotive V_{SUP} voltage(14 V). The efficiency is valid in buck mode only and above a 200 mA load on VPRE, to be in continuous mode on the 22 µH inductor. The efficiency is calculated and has to be verified by measurement at the application level.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

EXT. DEVICES	
C_{OUT_VPRE}	57 µF
ESR C_{OUT_VPRE}	100 mΩ
L coil	22 µH
DCR coil	60 mΩ
V_{DIODE}	0.35 V

MOSFET switch	
$R_{DS(on)}$	200 mΩ
C_G	600 pF
t_{SW_ON}	30 ns
t_{SW_OFF}	30 ns
Overdrive	10 V

Converter	
V_{PRE}	6.50 V
Freq	440 kHz

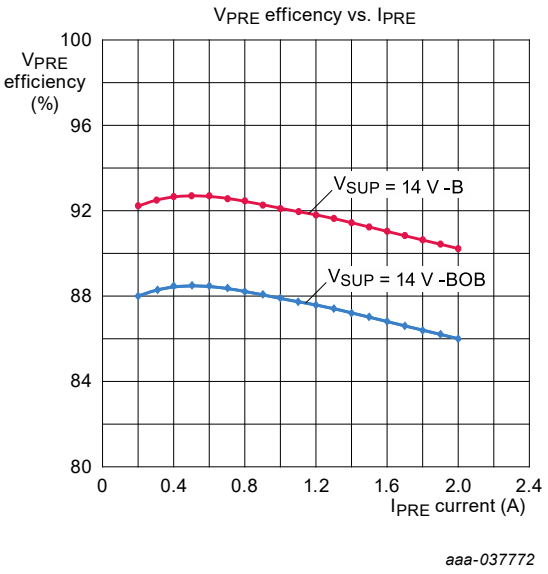


Figure 43. V_{PRE} efficiency

12.7.2 VCORE voltage regulator

This voltage regulator is a step-down DC–DC converter in the FS6500 series and a linear regulator in the FS4500 series.

12.7.2.1 VCORE DC–DC converter

The FS6500 voltage regulator is a step-down DC–DC converter operating in voltage control mode. The high-side switching MOSFET, connected to VPRE, is integrated in the device, and the PWM frequency is fixed at 2.4 MHz typical. The output voltage is configurable from a 1.0 V to 5.0 V range, and adjustable around these voltages with an external resistor divider (R3/R4) connected between VCORE and the feedback pin (FB_CORE) (Figure 44). $V_{CORE} = V_{CORE_FB}$ x ((R3 + R4)/R4).

The voltage accuracy is ±2.0 % (without the external resistor bridge R3/R4 accuracy) and the max output current is 2.2 A. The stability of the overall converter is done by an external compensation network (R1/C1/R2/C2) connected to the pin COMP_CORE. It is recommended to use 1.0 % accuracy resistors and set R4 = 8.06 kΩ and adjust R3 to obtain the final V_{CORE} voltage needed for the MCU core supply.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

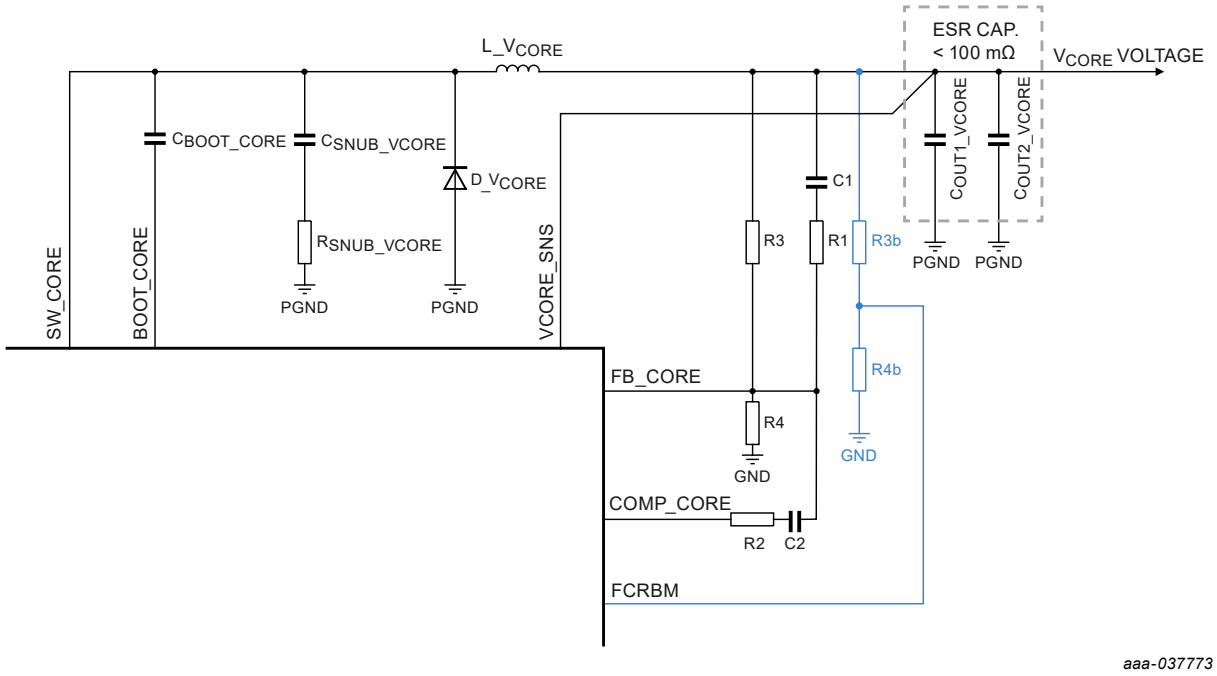


Figure 44. VCORE buck regulator

12.7.2.2 Light load condition

To improve the converter efficiency and avoid any unwanted output voltage increase, the VCORE voltage regulator operates in pulse skipping mode during light load conditions. The principle is the same as the VPRE implementation described in detail in Section 12.7.1.3.

12.7.2.3 Current limitation

A current limitation is implemented to avoid uncontrolled power dissipation inside the device (duty cycle control) and limits the current below I_{CORE_LIM}. The current limitation is banked when the pass transistor is switched on during $t_{CORE_BLK_LIM}$ to avoid parasite detection. When the I_{CORE_LIM} threshold is reached, the high-side integrated MOSFET is switched off. The MOSFET is not switched on again before the next rising edge of the switching clock.

The current limitation induces a duty cycle reduction and leads to the VCORE output voltage to fall gradually and may cause an undervoltage condition, bringing the device into a fail-safe state. The current limitation does not switch off the regulator.

12.7.2.4 Voltage monitoring

The overvoltage detection switches off the regulator. The regulator remains on during an undervoltage detection. Diagnostic is reported in the dedicated register, generates an interrupt, and may bring the application into the fail-safe state, depending on the supervisor configuration (register INIT_VCORE_OVUV_IMPACT).

For safety purposes, the FCRBM pin monitors the external resistor bridge (R3/R4) used to set up the final V_{CORE} voltage through a second resistor bridge (R3b/R4b) to detect an external resistor drift or disconnection. The monitoring compares the FB_CORE and FCRBM pins (Figure 45) and triggers when FB_CORE – FCRBM > ±150 mV max.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

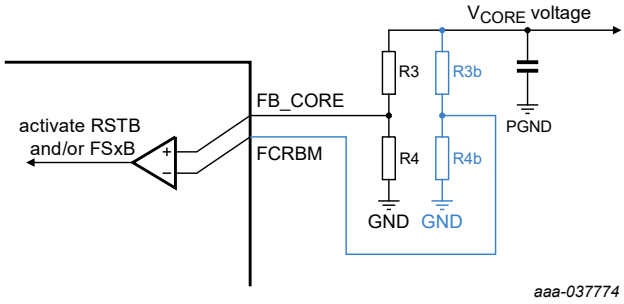


Figure 45. Feedback core resistor bridge monitoring (FCRBM)

If the second resistor bridge (R3b/R4b) is not mounted, FCRBM must be connected directly to FB_CORE to satisfy FB_CORE = FCRBM in all conditions.

12.7.2.5 V_{CORE} efficiency

V_{CORE} efficiency versus current load is given for information based on typical external component criteria described in Figure 46, close to the graph and at three typical V_{CORE} voltages (5.0 V, 3.3 V, and 1.2 V), covering most of the MCU supply ranges. The efficiency is valid above a 200 mA load on V_{CORE} to be in continuous mode in the 2.2 µH inductor. The efficiency is calculated and has to be verified by measurement at the application level. One major contributor degrading the efficiency at V_{CORE} = 1.2 V is the external diode during the recirculation phase. The lower the diode forward voltage (V_F) is, the better the efficiency.

EXT. Devices	
C_{OUT_VCORE}	20 µF
ESR C_{OUT_VCORE}	5.0 mΩ
L coil	2.2 µH
DCR coil	20 mΩ
V_{DIODE}	0.35 V
MOSFET switch	
$R_{DS(on)}$	200 mΩ
C_G	300 pF
t_{SW_ON}	12 ns
t_{SW_OFF}	12 ns
Overdrive	10.0 V
Converter	
V_{CORE}	1.2 V, 3.3 V, 5.0 V
Freq	2400 kHz

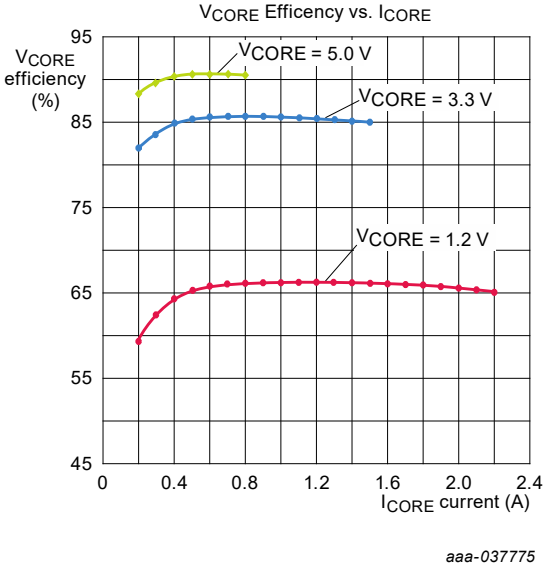


Figure 46. V_{CORE} efficiency

12.7.2.6 VCORE linear regulator

The FS4500 voltage regulator is a linear regulator. The pass device, connected to VPRE, is integrated. The output voltage range is configurable from 1.0 V to 5.0 V, and adjustable around these voltages with an external resistor divider (R3/R4) connected between V_{CORE} and the feedback pin (FB_CORE) (see Figure 47). V_{CORE} = V_{CORE_FB} x ((R3 + R4)/R4).

The voltage accuracy is ±2.0 % (without the external resistor bridge R3/R4 accuracy) and the max. output current is 0.5 A. In this case, the BOOT_CORE and COMP_CORE pins (used in buck converter mode only)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

must be left open. It is recommended to use 1.0 % accuracy resistors and set R4 = 8.06 kΩ and adjust R3 to obtain the final V_{CORE} voltage needed for the MCU core supply. When VCORE is used in linear mode, the power dissipation must be taken into account at low-voltage.

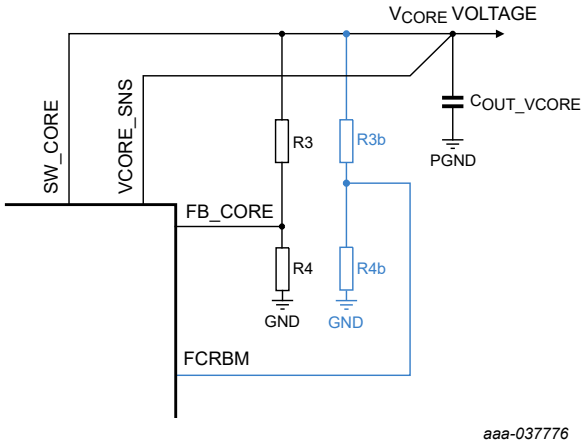


Figure 47. VCORE linear regulator

12.7.2.7 Current limitation

Similar to the buck converter mode, a current limitation is implemented to avoid uncontrolled power dissipation inside the device (see Section 12.7.2.3).

12.7.2.8 Voltage monitoring

The linear regulator has the same voltage monitoring than the DC–DC buck converter (see Section 12.7.2.4).

12.7.3 Charge pump and bootstrap

Both switching MOSFETs of VPRE and VCORE SMPS are driven by external bootstrap capacitors. Additionally, a charge pump is implemented to ensure 100 % duty cycle for both converters. Each converter uses a 100 nF external capacitor minimum to operate properly.

12.7.4 VCCA voltage regulator

VCCA is a linear voltage regulator mainly dedicated to supply the MCU I/Os, especially the ADC. The output voltage is selectable at 5.0 V, or 3.3 V. Since this output voltage can be used to supply MCU I/Os, the output voltage selection is done using an external resistor connected to the SELECT pin and ground or VPRE. When VCCA is used with the internal MOS transistor, the VCCA_E pin must be connected to VPRE. The voltage accuracy is ±1.0 % for 5.0 V and 3.3 V configuration with an output current capability at 100 mA.

When VCCA is used with an external PNP transistor to boost the current capability up to 300 mA, the connection is detected automatically during the start-up sequence of the FS6500/FS4500. In such condition, the internal pass transistor is switched off and all the current is driven through the external PNP to reduce the internal power dissipation. The output voltage accuracy with an external PNP is reduced to ±3.0 % at 300 mA current load. The VCCA output voltage is used as a reference for the auxiliary voltage supply (V_{AUX}) when VAUX is configured as a tracking regulator.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

12.7.4.1 Current limitation

A current limitation is implemented to avoid uncontrolled power dissipation of the internal MOSFET or external PNP transistor. By default, the current limitation threshold is selected based on the auto detection of the external PNP during start-up phase.

- When the internal MOSFET transistor is used, the current is limited to $I_{CCA_LIM_INT}$ and the regulator is kept on
- When the external PNP transistor is used, the current is limited to $I_{CCA_LIM_OUT}$ and the regulator is switch off after a dedicated duration $t_{CCA_LIM_OFF}$ under current limitation. A SPI command is needed to restart the regulator.

In case of an external PNP configuration only, the lowest current limitation threshold can be selected by the SPI in the register INIT_VREG instead of the highest one. A current limitation foldback scheme is implemented to reduce the current limitation to $I_{CCA_LIM_FB}$ when VCCA is below $V_{CCA_LIM_FB}$, limiting the power dissipation in the external PNP transistor during a short-circuit to GND of the VCCA pin.

12.7.4.2 Voltage monitoring

The overvoltage detection switches off the regulator. The regulator remains on if an undervoltage is detected. A diagnostic is reported in the dedicated register, generating an Interrupt and may bring the application into fail-safe state, depending on the supervisor configuration (register INIT_VCCA_OVUV_IMPACT).

12.7.5 VAUX voltage regulator

VAUX is a highly flexible linear voltage regulator, which can be used either as an auxiliary supply dedicated to additional device in the ECU or as a sensor supply (i.e. outside the ECU). An external PNP transistor must be used (no internal current capability).

If VAUX is not used in the application, the VAUX, VAUX_E, and VAUX_B pins must be left open. It is recommended to turn the V_{AUX} driver off and disable the V_{AUX} safety impact by the SPI (VAUX_EN=0 in REG_MODE register and all bits of INIT_VAUX_OVUV_IMPACT register at 0).

If VAUX is used as an auxiliary supply, the output voltage is selectable between 5.0 V and 3.3 V. Since this voltage rail can be used to supply MCU IOs, the selection is done with an external resistor connected between the SELECT pin and ground or VPRE. In such case, the voltage accuracy is ±3.0 %, with a maximum output current capability of 400 mA.

If VAUX is used as a sensor supply rail, the output voltage is selectable between 5.0 V and 3.3 V. VCCA can be used as reference for the sensor supply used as tracker. In this case, the V_{AUX} voltage must match V_{CCA}, limiting the resistor configuration at the SELECT pin to 5.1 kΩ (V_{AUX} = V_{CCA} = 3.3 V) and 12 kΩ (V_{AUX} = V_{CCA} = 5.0 V). The tracker mode selection is done during the INIT phase and secured (bit VAUX_TRK_EN in the INIT_VREG register). The tracking accuracy is ±15 mV.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

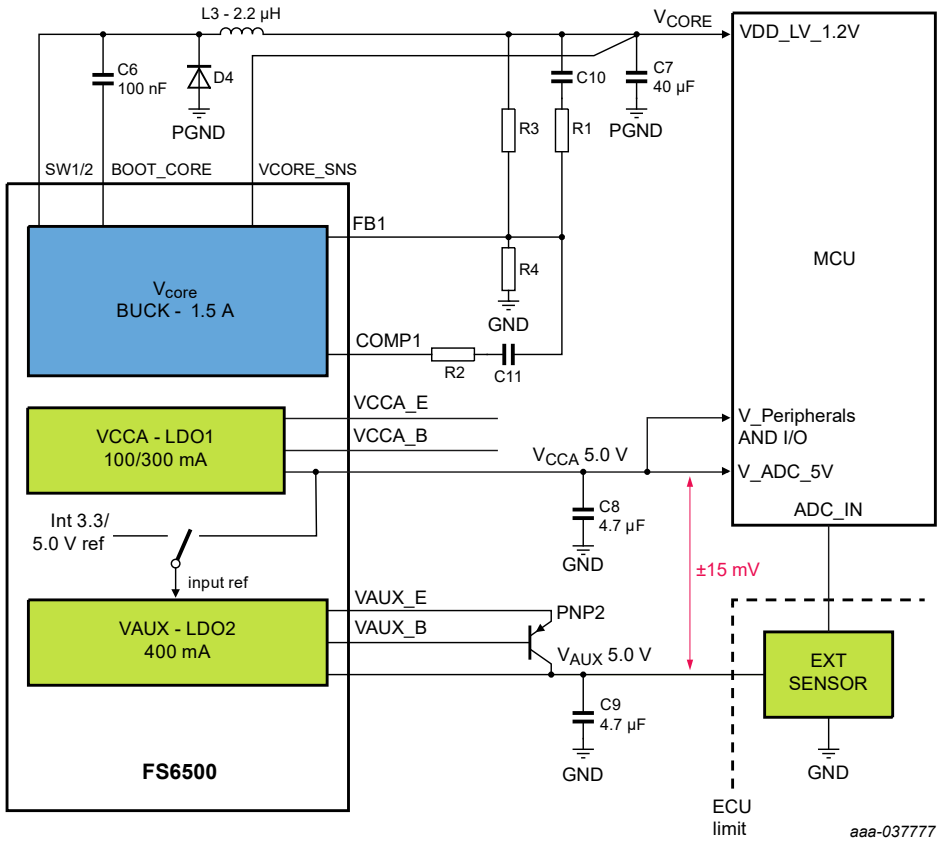


Figure 48. Example of V_{AUX} used in tracker mode

12.7.5.1 Current limitation

A current limitation is implemented to avoid uncontrolled power dissipation of the external PNP transistor. The current is limited to I_{AUX_LIM} and the regulator is switch off after a dedicated duration $t_{AUX_LIM_OFF}$ under current limitation. A SPI command is needed to restart the regulator. A current limitation foldback scheme is implemented to reduce the current limitation to $I_{AUX_LIM_FB}$ when V_{AUX} is below $V_{AUX_LIM_FB}$, limiting the power dissipation in the external PNP transistor during a short-circuit to GND of the VAUX pin.

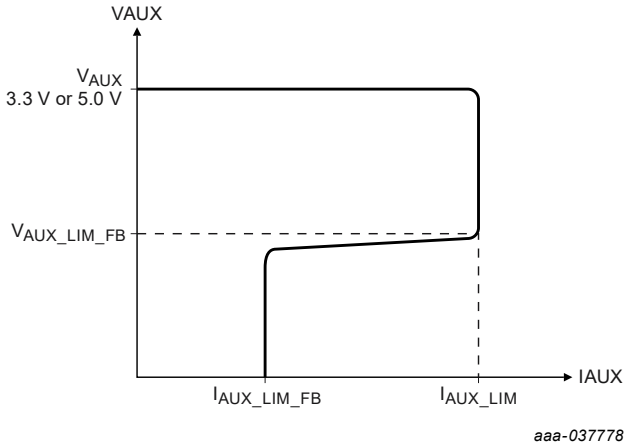


Figure 49. V_{AUX} current limitation scheme with foldback mechanism

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

12.7.5.2 Voltage monitoring

The overvoltage detection switches off the regulator. The regulator remains on if an undervoltage is detected. A diagnostic is reported in the dedicated register, generating an interrupt and may bring the application into the fail-safe state, depending on the supervisor configuration (register INIT_VAUX_OVUV_Impact).

12.7.6 CAN_5V voltage regulator

The CAN_5V voltage regulator is a linear regulator fully dedicated to the internal CAN interface. By default, the CAN_5V regulator and the undervoltage detector are enabled and the overvoltage detector is disabled. The overvoltage detector can be enabled by the SPI during INIT_MAIN state.

If the overvoltage detector is enabled, the CAN_5V regulator switches off when an overvoltage is detected. The undervoltage detector is disabled when the regulator is switched off reporting an undervoltage. A diagnostic is reported in the dedicated register, generating an Interrupt. The CAN_5V regulator is not a safety regulator. Consequently, the CAN_5V voltage monitoring (overvoltage, undervoltage) never asserts the RSTB or FS0B fail-safe pins.

If the FS6500/FS4500 internal CAN FD transceiver is not used in the application, the CAN_5V regulator can be used to supply an external standalone CAN or FLEX–RAY transceiver, provided the current load remains below the maximum current capability in all conditions. In this case, the internal CAN FD transceiver must be put into sleep mode without wake-up capability.

12.7.7 VKAM

The keep alive memory supply is shared with IO_ 5 pin. When VKAM is used, IO_5 is not available and vice versa. Depending on the part number selection (Section 5.2), VKAM can be on or off by default.

- If VKAM is on by default, VKAM starts as soon as VSUP3 is > 4.5 V. VKAM can still be turned off/on by the SPI.
- If VKAM is off by default, VKAM is turned on/off by the SPI.

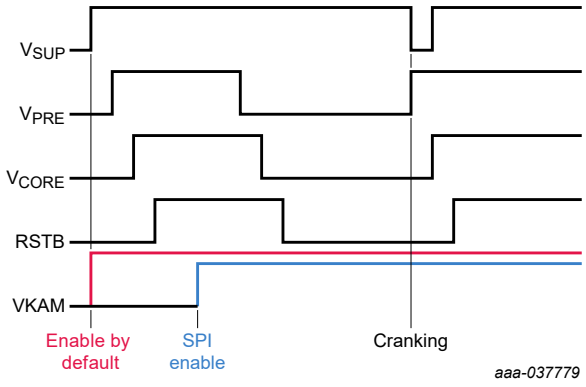


Figure 50. VKAM start-up strategy

VKAM is the only supply available in low-power mode (LPOFF). VKAM can be used to supply the MCU static RAM or any other external IC which does not exceed the current capability. A current limitation is implemented. Neither voltage monitoring, nor thermal shutdown are implemented. VKAM can be selected at the MUX_OUT pin to be monitored by the MCU ADC. The VKAM supply is available down to V_{SUP} = $V_{SUP_UV_L}$ = 2.7 V when the device is in normal mode, and down to V_{SUP} = 4.5 V when the device is in low-power mode off.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

12.7.8 Power dissipation

The FS6500/FS4500 provides high performance SMPS and linear regulators to supply high end MCUs in automotive applications. Each regulator can deliver:

- V_{PRE} (6.5 V) up to 2.0 A
- V_{CORE} (from 1.0 V to 5.0 V range) up to 2.2 A
- V_{CCA} (3.3 V or 5.0 V) up to 100 mA (with internal MOS) or up to 300 mA (with external PNP)
- V_{AUX} (3.3 V or 5.0 V) up to 400 mA (with external PNP)
- V_{CAN} (5.0 V) up to 100 mA

A thermal dissipation analysis has to be performed based on the application use case to ensure the maximum silicon junction temperature does not exceed 150 °C.

Two use cases covering the two main V_{CORE} voltage configurations are provided in Figure 51.

- use case 1: V_{CORE} = 3.3 V, I_{CORE} = 0.7 A, V_{CCA} with int. MOS
- use case 2: V_{CORE} = 1.2 V, I_{CORE} = 1.4 A, V_{CCA} with ext. PNP

Both use cases have a total internal power dissipation below 0.9 W. A junction to ambient thermal resistivity of 30 °C/W allows the application to work up to an ambient temperature of 125 °C. A good soldering of the package expose pad is highly recommended to achieve such thermal performance.

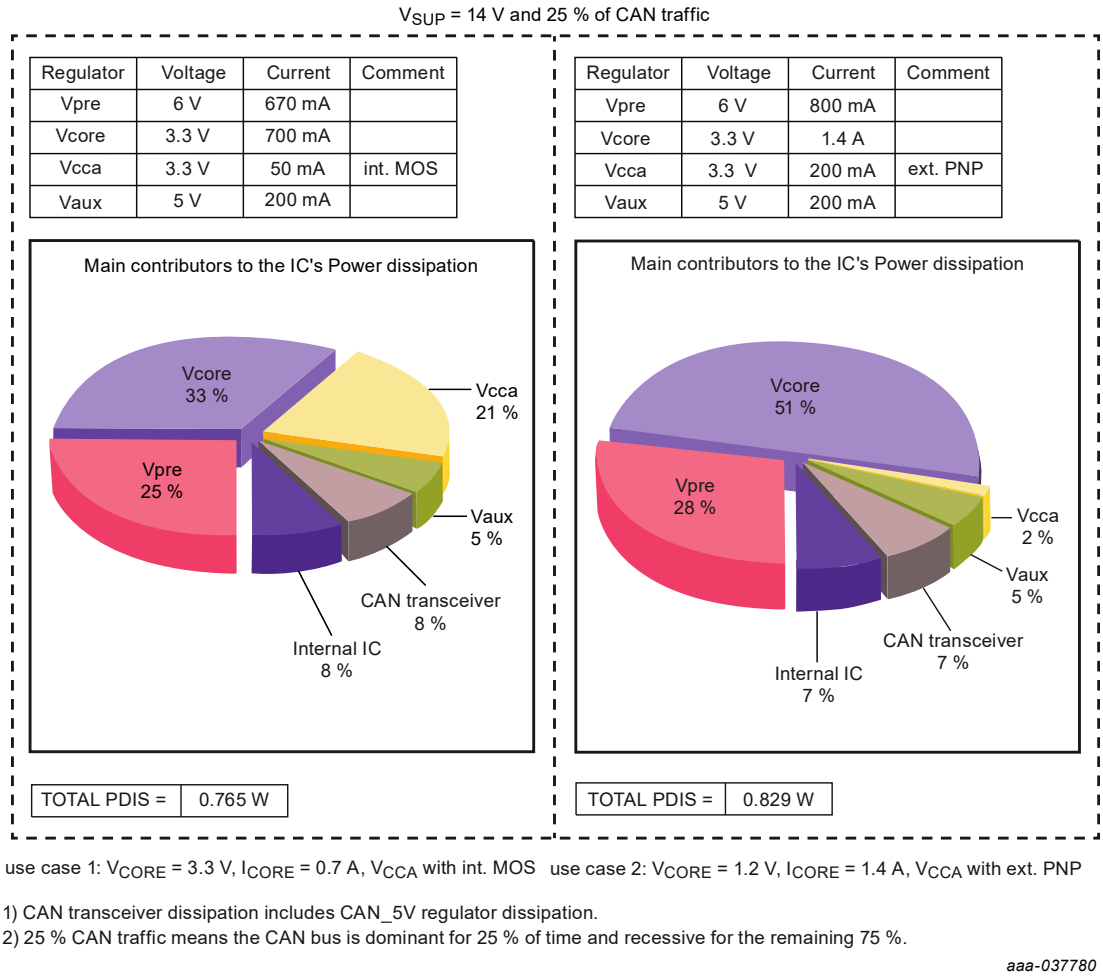


Figure 51. Power dissipation use case

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

The main contributors to the device power dissipation are the V_{PRE}, V_{CORE}, and V_{CCA} (when used with an internal PMOS) regulators. In comparison, the power dissipation from the Internal IC, VAUX, and CAN transceiver are negligible. VPRE power dissipation is mainly induced by the loading of the regulators it is supplying, mainly V_{CORE}, V_{CCA}, and V_{AUX} which are application dependent. The total device power dissipation, depending on the variation of these three regulators, is detailed in Figure 52 with the environmental conditions in the associated table.

	P_{dis} vs. I_{CORE}	P_{dis} vs. I_{CCA}	P_{dis} vs. I_{PRE}
V_{PRE}	6.5 V	6.5 V	6.5 V
I_{PRE}	I_{CORE} + I_{CCA} + I_{AUX} + I_{CAN}	I_{CORE} + I_{CCA} + I_{AUX} + I_{CAN}	from 0.5 to 2A
V_{CORE}	3.3 V and 1.2 V	3.3 V	3.3 V
I_{CORE}	from 0.25 to 1.5 A	0.7 A	0.3 A
V_{CCA}	3.3 V	3.3 V and 5 V	3.3 V
I_{CCA}	50 mA	20 to 100 mA	50 mA
V_{AUX}	3.3 V	3.3 V	3.3 V
I_{AUX}	200 mA	200 mA	200 mA
CAN_5 V	5 V	5 V	5 V
I_{CAN}	33 mA	33 mA	33 mA

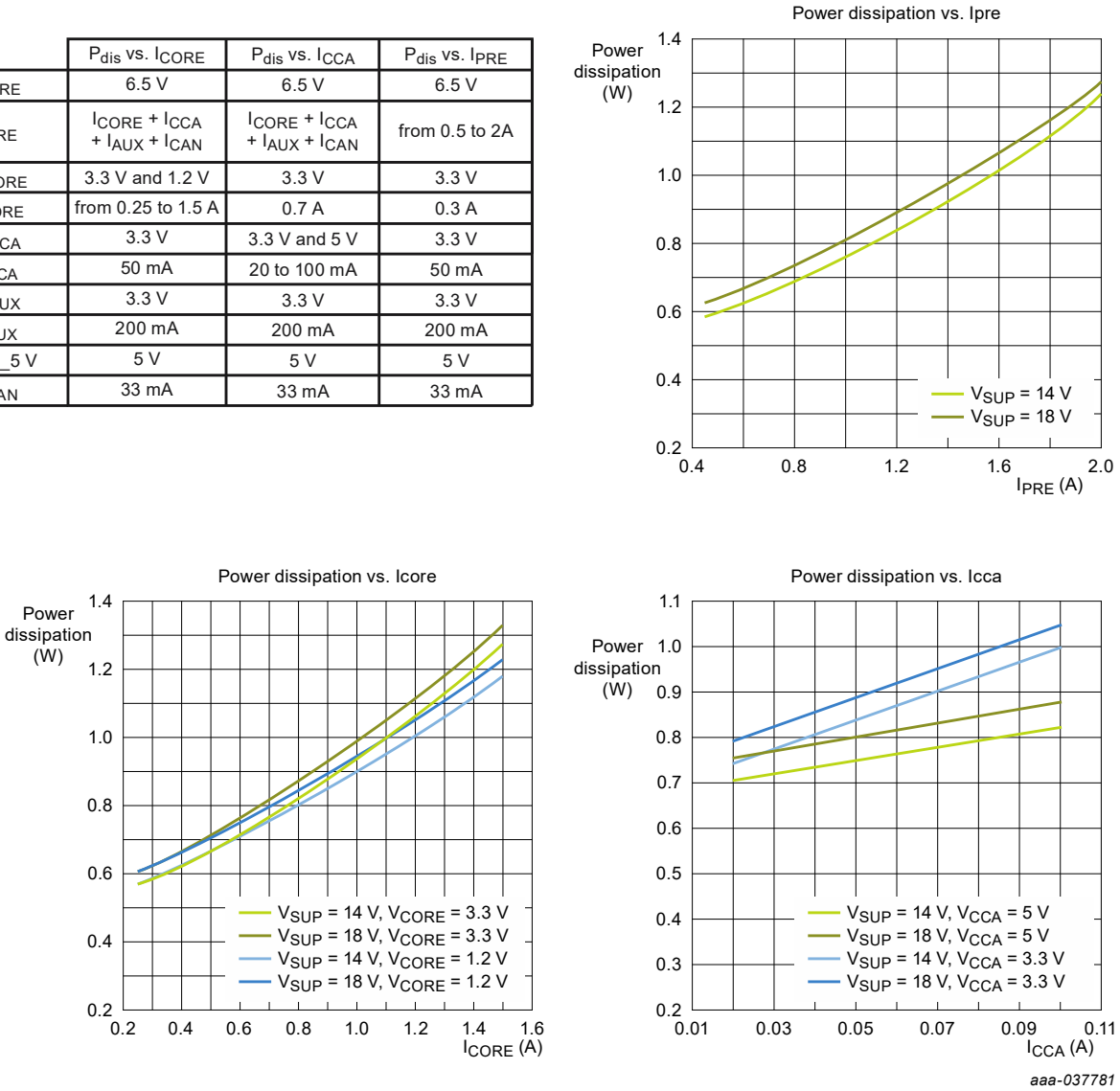


Figure 52. Power dissipation versus I_{CORE}, I_{CCA}, or I_{PRE}

12.7.9 Start-up sequence

To provide a safe and well known start-up sequence, the FS6500/FS4500 includes an undervoltage lockout. This $V_{SUP_UV_5}$ undervoltage lockout applies when the device is under a power-on reset condition or released from LPOFF. All the different voltage rails start automatically as described in Figure 53.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

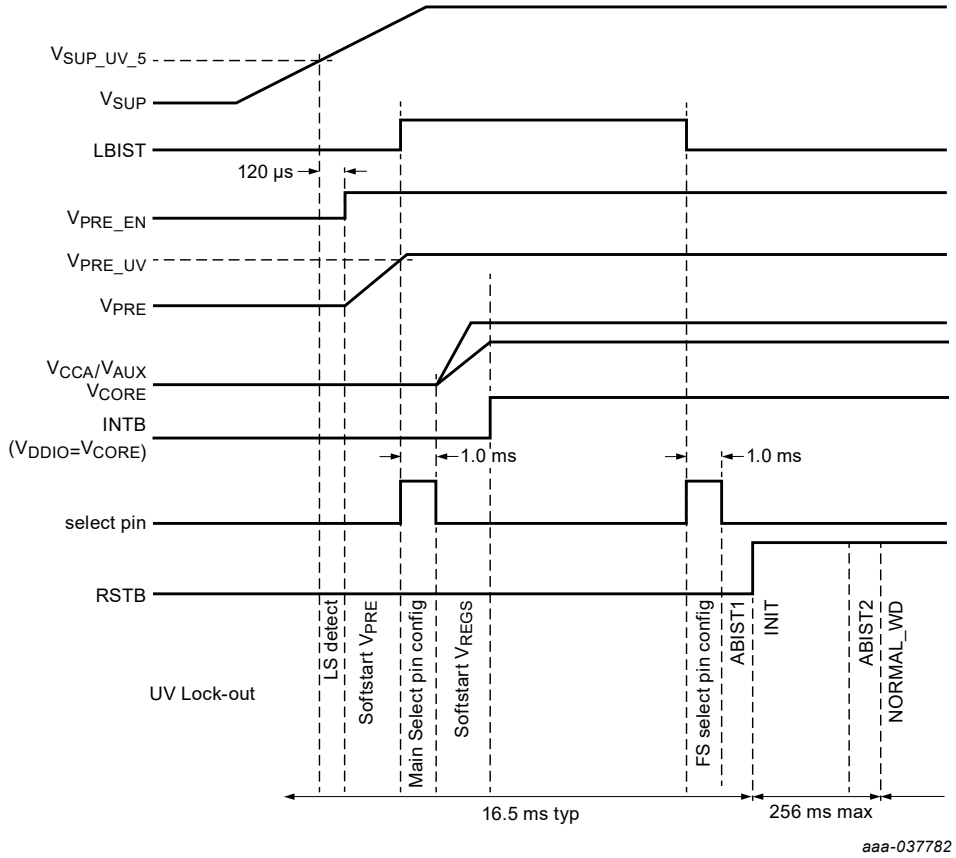


Figure 53. Start-up scheme

The final value of V_{AUX} and V_{CCA} depends on the hardware configuration (resistor values at the SELECT pin). The typical start-up sequence takes around 16.5 ms to release RSTB. RSTB can be pulled low after those 16.5 ms by the MCU, if it is not ready to run after power up. See Section 12.7.7 for the VKAM start-up sequence.

12.8 Long duration timer

The device includes a long duration timer, with an integrated oscillator. The timer is configurable by the SPI and can operate in normal mode and low-power mode. It provides several functions and offers a large range of counting periods, as well as a calibration mechanism, for internal oscillator compensation.

The timer is not part of the safety circuitry, and is not covered by LBIST (logic built in self-test). However it can be activated in normal mode, and all prescaler options can be selected, to allow timer circuitry verification. The timer is based on a 24-bit counter, with a 32768 Hz oscillator, allowing a 1.0 s timebase.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

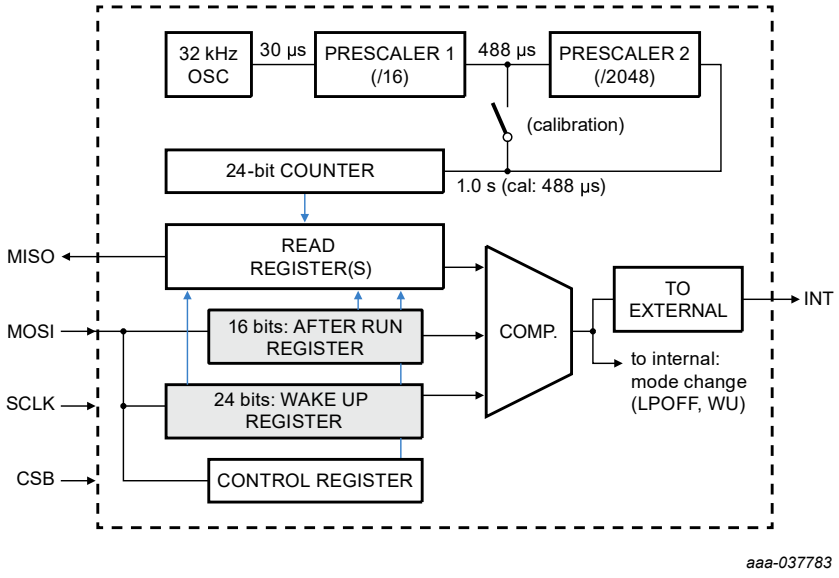


Figure 54. Long duration timer block diagram

12.8.1 Timer characteristics

In normal operation, the timer can count up to 194 days, with 1 second resolution. In calibration mode, the prescaler 2 is bypassed and the timer can count up to 2.28 hours, with 488 µs resolution. The calibration principle consists in activation of the counter for a dedicated and accurate duration, due to the MCU accurate clock and timing. The MCU then reads back the timer count, compares the count versus the accurate time of activation, then calculates a time offset. It is recommended to perform the calibration between -20 °C and +85 °C.

Table 13. Long duration timer characteristics

	Osc freq	Osc period	Prescaler	Counter resolution	Max count	
Operation	32768 Hz	30.52 µs	16 x 2048	1 s	4660 Hrs	194 days
Calibration	32768 Hz	30.52 µs	16	488 µs	8192 s	2.28 Hrs

12.8.2 Calibration procedure

The calibration procedure consists of activating the counter for a specific duration and comparing the result with the MCU's accurate clock and timing. Once the timer expires, the MCU reads back its final value to compare with its own accurate time of activation and to calculate a time offset. NXP recommends performing the calibration between -20 °C and 85 °C.

Calibration example:

- Select the timer function 1 and set the after run value to 65535 (~32 s).
- Start the counter.
- Read the counter when the MCU RTC reaches 20 s (must be less than 30 s with ±5.0 % oscillator accuracy).
- If the oscillator period is at exact typical value (absolutely no deviation error), expected reading is 40960.
- The exact reading calculates the error correction factor ECF = exact_reading/expected_reading.
- ECF < 1 if the oscillator is faster than the exact typical value.
- ECF > 1 if the oscillator is slower than the exact typical value.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

- After calibration, the new after run or wake-up values to set the counter are "after run x ECF" and "wake-up x ECF".

12.8.3 Timer functions

- **Function 1:** In normal mode, count and generate a flag or an Interrupt when the counter reaches the after run value.
- **Function 2:** In normal mode, count until the counter reaches the after run value and enters into low-power mode.
- **Function 3:** In normal mode, count until the counter reaches the after run value and enters into low-power mode. Once in low-power mode, count until the counter reaches the wake-up value and wakes up.
- **Function 4:** In low-power mode, count until the counter reaches the wake-up value and wakes up.
- **Function 5:** In low-power mode, count and do not wake-up unless the counter overflow occurs, or if the device wakes up by another source (CAN, LIN, IO).

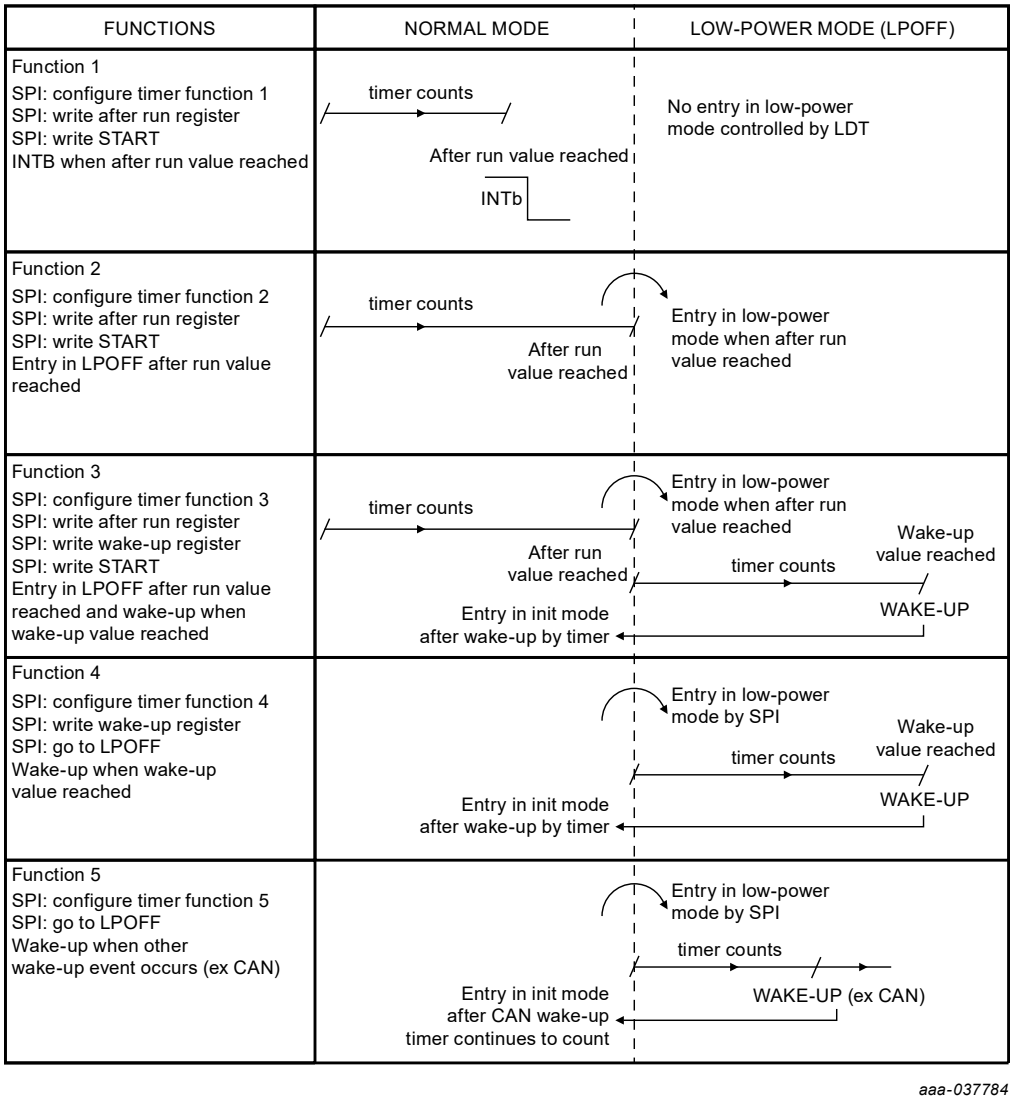


Figure 55. Long duration timer functions

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

12.8.4 Timer operation

The timer is configured and operates with the LONG_DURATION_TIMER register. The 16-bit after-run value and the 24-bit wake-up value are configured and read in the corresponding registers.

Figure 56 describes the independent state machine of long duration timer (LDT). After a POR of the device, the LDT is in idle mode waiting for configuration. The after-run timer function starts when the LDT_ENABLE bit is set by SPI. The wake-up timer function starts when the device enters in LPOFF mode.

- When function 1 is selected and the counter reaches the after run value (EOT), an interrupt is generated and the counter is stopped. The counter must be disabled (~ENABLE) before reading its value and enabled again.
- When function 2 is selected and the counter reaches the after run value (EOT), the device goes to LPOFF mode and the counter is stopped. The counter must be disabled (~ENABLE) before reading its value and enabled again.
- When function 3 is selected and the counter reaches the after run value (EOT), the device goes to LPOFF mode. The counter is reset and restart to count. When the counter reaches the wake-up value (EOT), the device wakes up and the counter is stopped. The counter must be disabled (~ENABLE) before reading its value and enabled again.
- When function 4 is selected and the counter reaches the wake-up value (EOT), the device wakes up and the counter is stopped. The counter must be disabled (~ENABLE) before reading its value and enabled again.
- When function 5 is selected and the counter overflows (OVRFLW), the device wakes up and the counter is stopped. The counter must be disabled (~ENABLE) before reading its value and enabled again. Overflow means counter max value is reached (all 24 bits at logic 1).
- When function 5 is selected and the devices wakes up by CAN, LIN, or IO, the counter is running. The counter must be disabled (~ENABLE) before reading its value and enabled again.

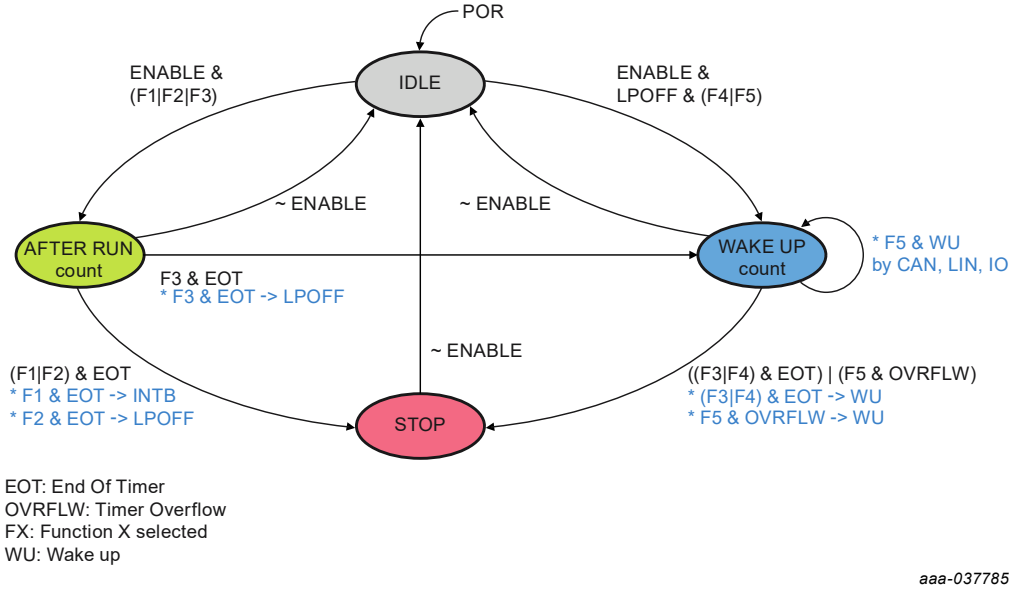


Figure 56. Long duration timer state machine

12.9 CAN transceiver

The CAN (controller area network) transceiver provides the physical interface between the CAN protocol controller of an MCU and the physical dual wires CAN-bus. The FS6500/FS4500 integrated CAN interface is compliant with flexible data standard at 2.0 Mbit/s. It offers excellent EMC and ESD performance, and meets the ISO 11898-2[(12)] and ISO 11898-5[(13)] standards.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

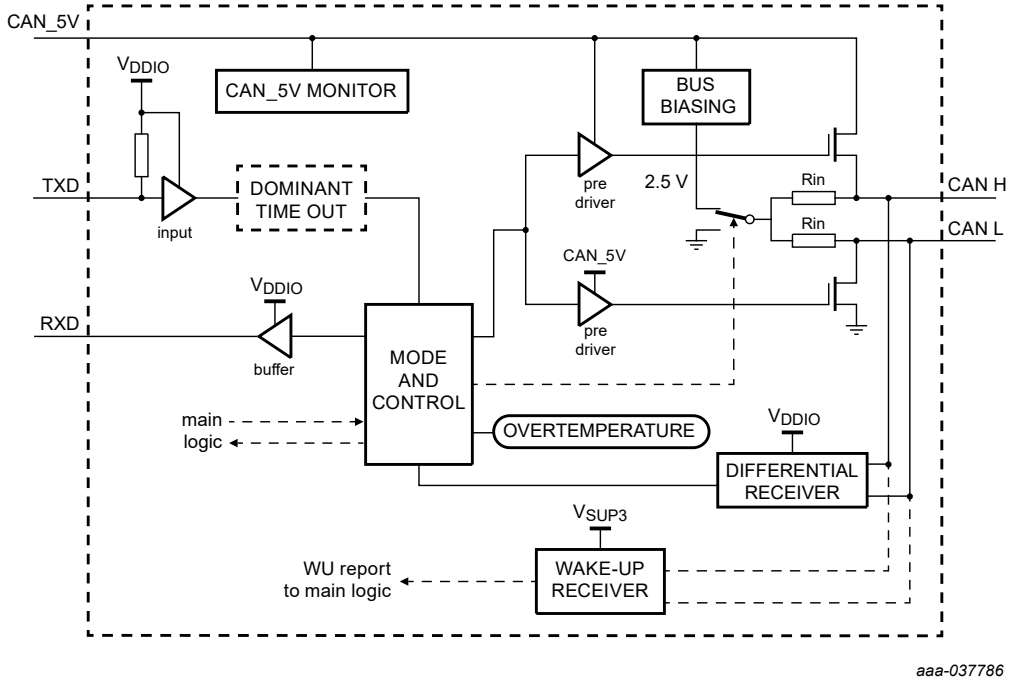


Figure 57. CAN simplified block diagram

12.9.1 Operating modes

12.9.1.1 Normal mode

When the CAN mode bit configuration is ’11’ (CAN in normal operation), the device is able to transmit information from TXD to the bus and report the bus level to the RXD pin. When TXD is high, CANH and CANL drivers are off and the bus is in the recessive state (unless it is in an application where another device drives the bus to the dominant state). When TXD is low, the CANH and CANL drivers are on and the bus is in the dominant state. When the CAN mode bit configuration is ’01’ (CAN in listen only), the device is only able to report the bus level to the RXD pin. The TXD driver is off and the device is not able to transmit information from TXD to the bus. TXD is maintained high by an internal pull-up resistor $TXD_{PULL-UP}$ connected to VDDIO.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

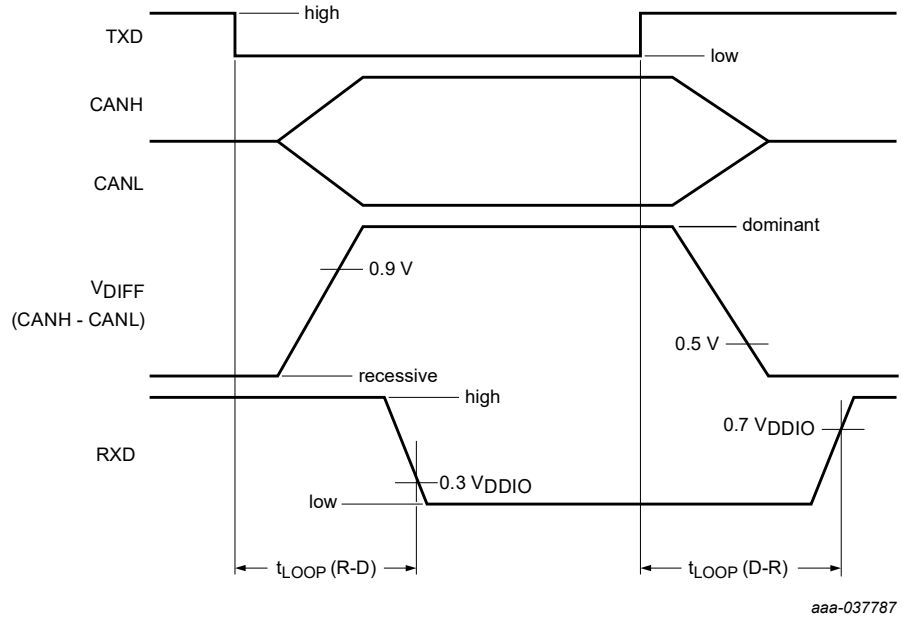


Figure 58. CAN timing diagram

12.9.1.2 Sleep mode

When the device is in LPOFF mode, the CAN transceiver is automatically set in sleep mode with or without wake-up capability, depending on the CAN mode bit configuration. In this case, the CANH and CANL pins are pulled down to GND via the internal R_{IN} resistor, the TXD and RXD pins are pulled to GND, and both driver and receiver are off. The CAN mode is automatically changed to sleep with wake-up capability if not configured to sleep without wake-up capability when the device enters is LPOFF. After LPOFF, the initial CAN mode prior to enter LPOFF is restored (Figure 59).

CAN state before entering LPOFF		CAN state after LPOFF		CAN state after entering LPOFF	
CAN_mode [1:0]	CAN state	CAN_mode [1:0]	CAN state	CAN_mode [1:0]	CAN state
00	Sleep, no wake-up capability	00	Sleep, no wake-up capability	00	Sleep, no wake-up capability
01	Listen only	10	Sleep, wake-up capability	01	Listen only
10	Sleep, wake-up capability			10	Sleep, wake-up capability
11	Normal			11	Normal

aaa-037788

Figure 59. CAN transition when device goes to LPOFF

12.9.2 Fault detection

12.9.2.1 TXD permanent dominant (timeout)

If TXD is set low for a time longer than t_{DOUT}, the CAN drivers are disabled and the CAN-bus returns to the recessive state. The CAN receiver continues to operate. This prevents the bus to be set in the dominant state permanently in case a failure sets the TXD input to a permanent low level.

The CAN_MODE MSB bit is set to 0 and the flag TXD_dominant is reported in the DIAG_CAN_1 register. The device recovers from this error detection after setting the CAN_MODE to normal operation and when a high level is detected on TXD. The TXD failure detection is operating when the CAN transceiver is in normal mode and listen only mode.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

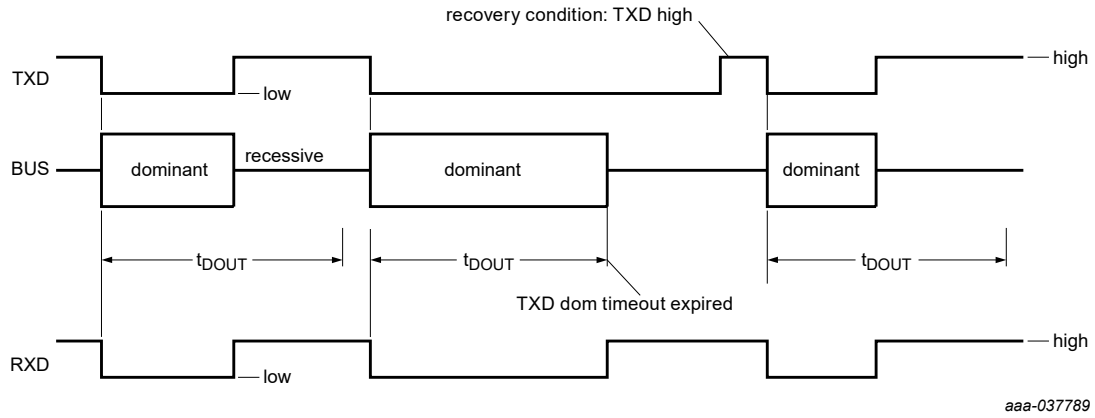


Figure 60. TXD dominant timeout detection

12.9.2.2 RXD permanent recessive

If RXD is detected high for seven consecutive receive/dominant cycles, the CAN drivers and receiver are disabled and the CAN-bus returns to the recessive state. This prevents a CAN protocol controller from starting a CAN message on the TXD pin, while RXD is shorted to a recessive level and seen from a CAN controller as a bus idle state.

The CAN_MODE MSB bit is set to 0 and the flag RXD_REC is reported in the DIAG_CAN_1 register. The device recovers from this error detection after setting the CAN_MODE to normal operation. The RXD failure detection is operating when the CAN transceiver is in normal mode and listen only mode.

12.9.2.3 CAN-bus short-circuits

CANL/CANH short to GND and CANL/CANH short to the battery are detected and reported to the device main logic. The CAN driver and receiver are not disabled. They are detected and reported to the device main logic.

CANL short to GND is detected when CANL is < 0.5 V, 500 ns after TXD is activated low, and five consecutive times, as illustrated for CANL short to GND on Figure 61. CANH short to the battery is detected when CANH is > 5.2 V, 500 ns after TXD is activated low, and five consecutive times. CANL short to the battery and CANH short to GND are detected when I_{CANL} or I_{CANH} > 75 mA (typ), 500 ns after TXD is activated low, and five consecutive times.

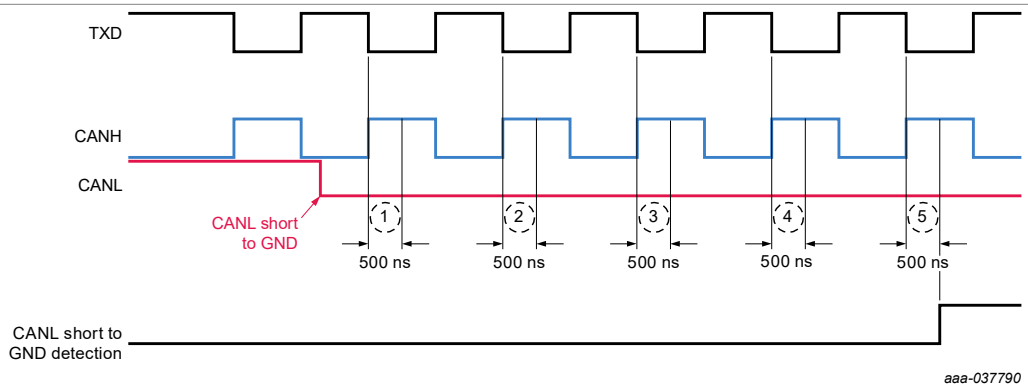


Figure 61. Illustration of CANL short to GND detection mechanism

If the CAN-bus is dominant for a time longer than t_{DOM}, due for instance to an external short-circuit from another CAN node, the flag CAN_DOM is reported in the DIAG_CAN_1 register. This failure does not disable the bus

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

driver. The CAN-bus dominant failure detection is operating when the CAN transceiver is in normal mode and listen only mode.

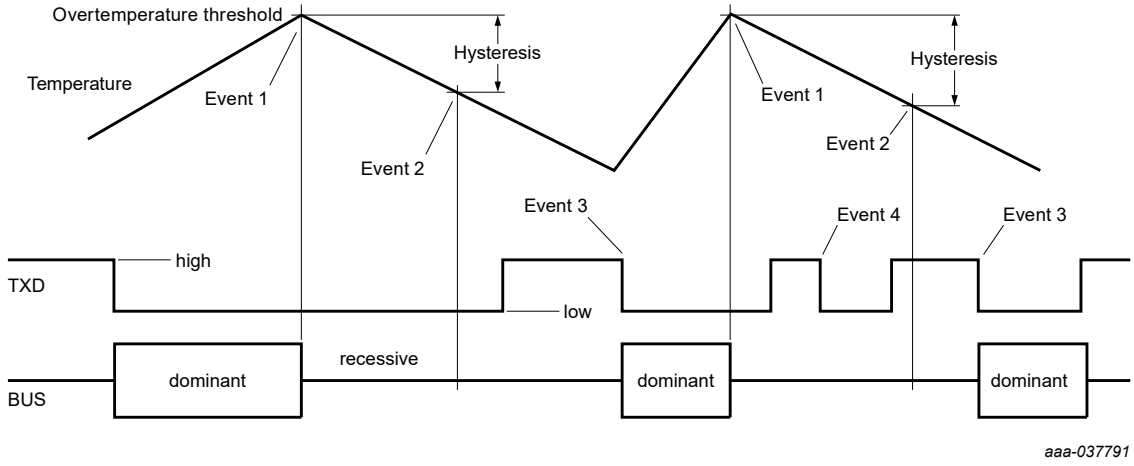
12.9.2.4 CAN current limitation

The current flowing in and out of the CANH and CANL driver is limited to 100 mA, in case of a short-circuit (parameters $I_{CANL-SK}$ and $I_{CANH-SC}$).

12.9.2.5 CAN overtemperature

If the driver temperature exceeds the TSD (T_{OT}), the CAN drivers are disabled and the CAN-bus returns to the recessive state. The CAN receiver continues to operate. The CAN_MODE MSB bit is set to 0 and the flag CAN_OT is reported in the DIAG_CAN_LIN register.

A hysteresis is implemented in this protection feature. The device overtemperature and recovery conditions are shown in Figure 62. The CAN drivers remain disabled until the temperature has fallen below the OT threshold minus hysteresis. The device recovers from this error detection after setting the CAN_MODE to normal operation and when a high level is detected on TXD.



Event 1: overtemperature detection. CAN driver disable.

Event 2: temperature falls below 'overtemp. threshold minus hysteresis' => CAN driver remains disable.

Event 3: temperature below 'overtemp. threshold minus hysteresis' and TXD high to low transition ≥ CAN driver enable.

Event 4: temperature above 'overtemp. threshold minus hysteresis' and TXD high to low transition ≥ CAN driver remains disable.

Figure 62. Overtemperature behavior

12.9.2.6 Distinguish CAN diagnostics and CAN errors

The CAN errors can generate an interruption while the CAN diagnostics are reported in the digital for information only. The interruption generated by the CAN errors can be inhibited setting the INT_INH_CAN bit in the INIT_INH_INT register. The list of CAN diagnostic and CAN error bits is provided in Table 14.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 14. CAN diagnostic and CAN error bits

Register	Bit	Flag type	Effect
DIAG_CAN_FD	CANH_BATT	Diagnostic	No impact on CAN transceiver
	CANH_GND	Diagnostic	No impact on CAN transceiver
	CANL_BATT	Diagnostic	No impact on CAN transceiver
	CANL_GND	Diagnostic	No impact on CAN transceiver
	CAN_DOM	Error	Turn off CAN transceiver
	RXD_REC	Error	Turn off CAN transceiver
	TXD_DOM	Error	Turn off CAN transceiver
DIAG_CAN_LIN	CAN_OT	Error	Turn off CAN transceiver
	CAN_OC	Diagnostic	No impact on CAN transceiver

12.9.3 Wake-up mechanism

The device includes bus monitoring circuitry to detect and report bus wake-ups when the device is in LPOFF and when CAN mode configuration is different from sleep/no wake-up capability. Multiple dominant pulse wake-up detection is implemented. The event must occur within the t_{3PTOX} timeout. t_{3PTOX} = t_{3PTO1} or t_{3PTO2}, depending on the SPI selection. The wake-up events are reported in the WU_SOURCE register.

12.9.3.1 Multiple pulse detection

To activate wake-up report, three events must occur on the CAN-bus:

- event 1: a dominant level longer than t_{1PWU} followed by

- event 2: a dominant level longer than t_{3PWU} followed by

- event 3: a dominant level longer than t_{3PWU}.

The three events and the timeout function avoiding a permanent dominant state on the bus generates permanent wake-up situation which would prevent system to enter in low-power mode.

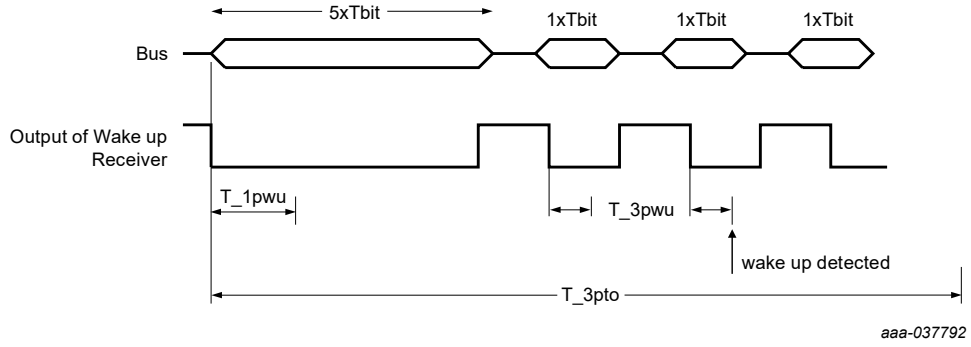


Figure 63. Multiple pulse wake-up pattern illustration

12.10 LIN transceiver

The local interconnect network (LIN) is a serial communication protocol, designed to support automotive networks in conjunction with a controller area network (CAN). The LIN transceiver is operational from a V_{SUP} of 7.0 V to 18 V DC, and compatible with LIN protocol specification 2.0, 2.1[(22)], 2.2[(23)], and SAEJ2602-2[(24)].

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

12.10.1 Simplified block diagram

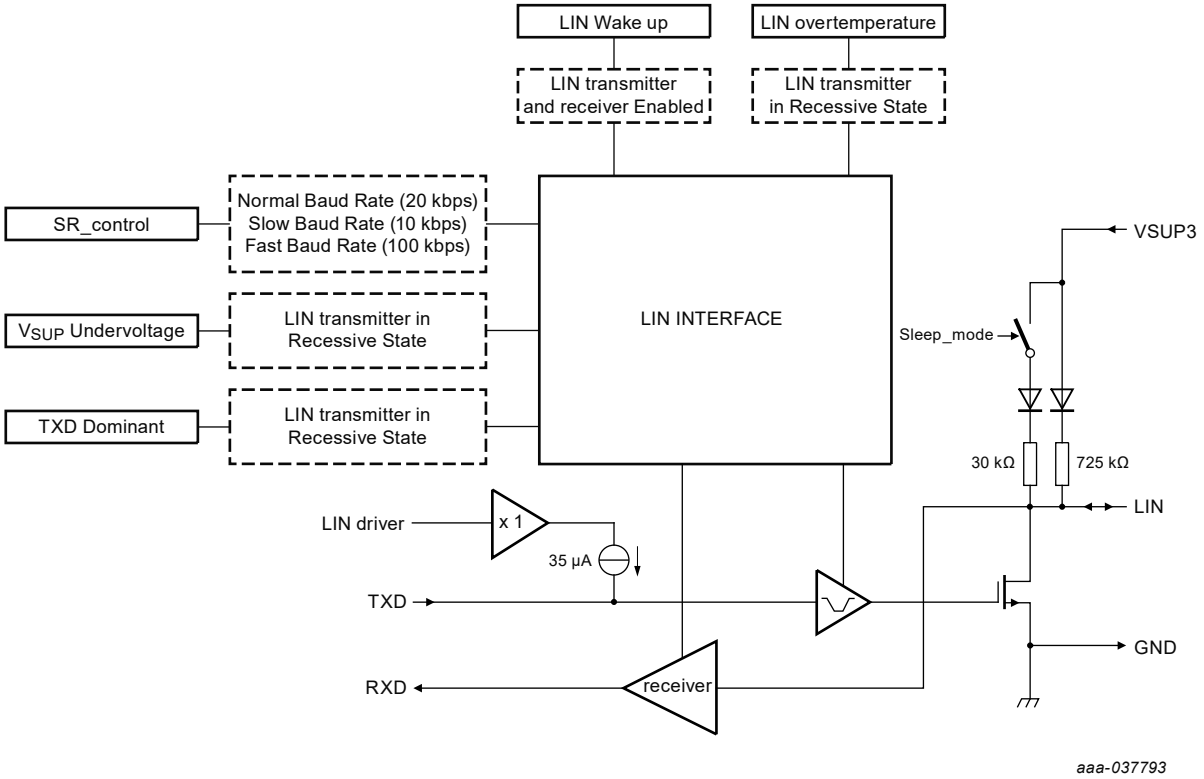


Figure 64. LIN simplified block diagram

12.10.2 Operating modes

12.10.2.1 Normal mode

When the LIN mode bit configuration is ’11’ (LIN in normal operation), the device is able to transmit information from TXDL to the bus and report the bus level to the RXDL pin. When TXDL is high, the LIN driver is off and the bus is in the recessive state (unless it is in an application where another device drives the bus to the dominant state). When TXDL is low, the LIN driver is on and the bus is in the dominant state.

When the LIN mode bit configuration is ’01’ (LIN in listen only), the device is only able to report the bus level to the RXDL pin. The TXDL driver is off and the device is not able to transmit information from TXDL to the bus. TXDL is maintained high by the internal pull-up resistor $TXDL_{PULL-UP}$ connected to VDDIO.

12.10.2.2 Sleep mode

When the device is in LPOFF mode, the LIN transceiver is automatically set into sleep mode with or without wake-up capability, depending on the LIN mode bit configuration. In this case, the LIN pin is pulled up to V_{SUP} via the internal resistor and diode structure, the TXDL and RXDL pins are driven to GND.

12.10.3 Baud rate selection

The device has two selectable baud rates: 20 kB/s for normal baud rate and 10 kB/s for slow baud rate. An additional fast baud rate (100 kB/s) can be used to flash the MCU, or in the garage for diagnostic. The LIN consortium specification does not specify electrical parameters for this baud rate. The communication only

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

is guaranteed. The baud rate selection is done by the SPI setting during the INIT phase of the main logic. Depending on the baud rate setting, the corresponding LIN slope control is automatically selected.

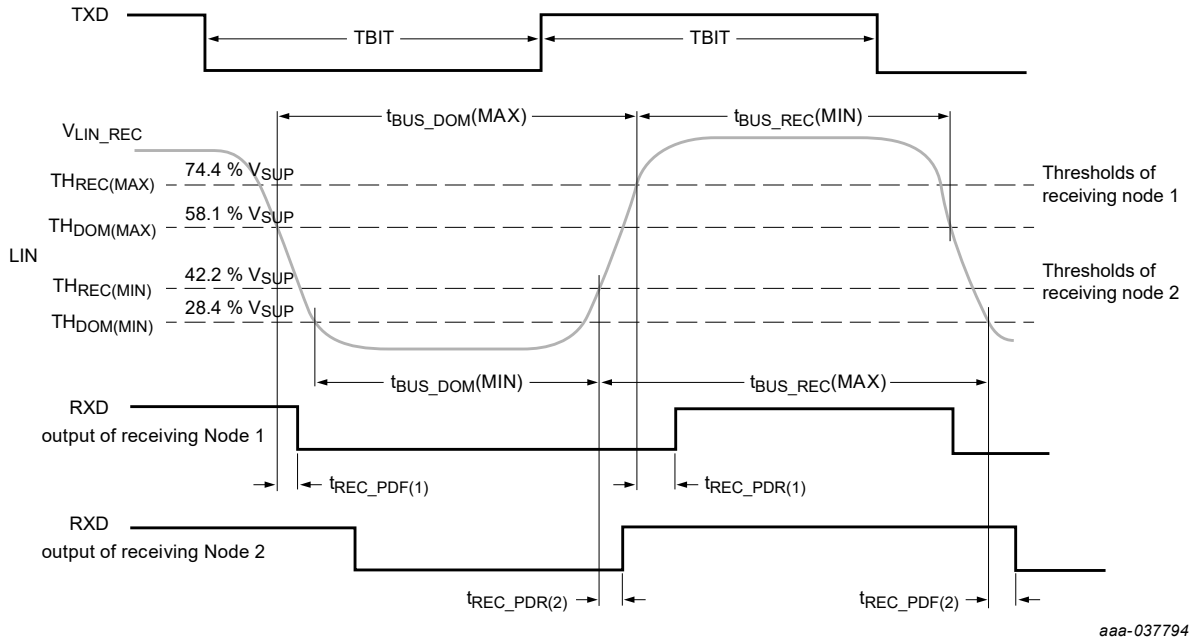


Figure 65. LIN timings for normal baud rate (20 kB/s)

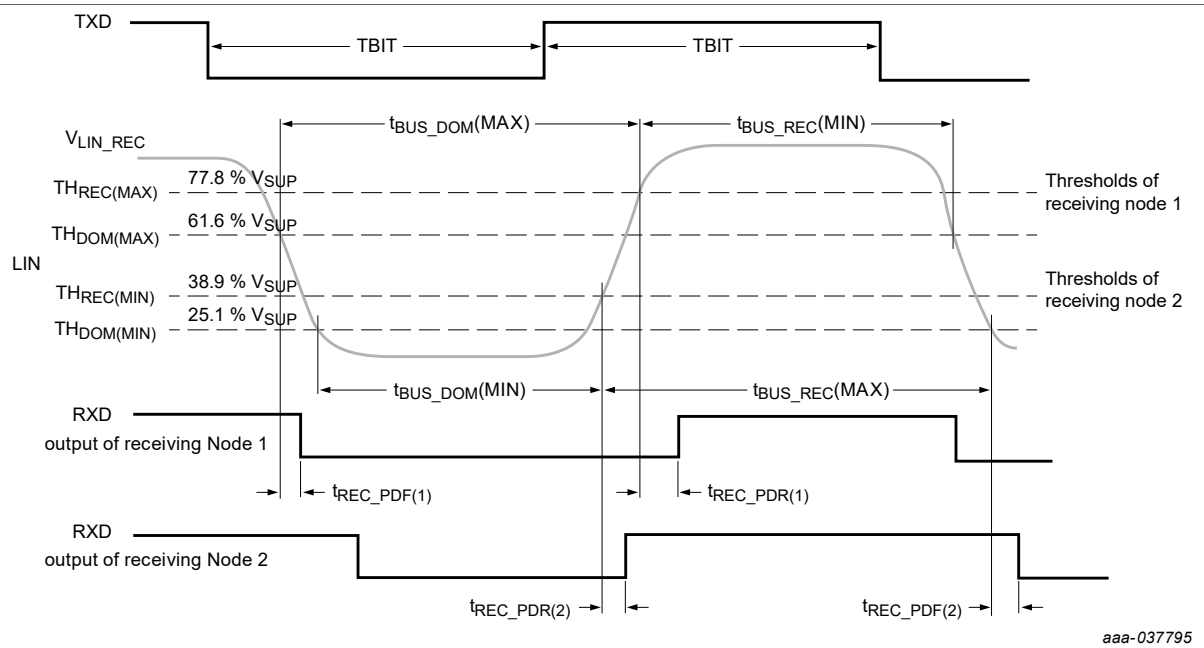


Figure 66. LIN timings for slow baud rate (10 kB/s)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

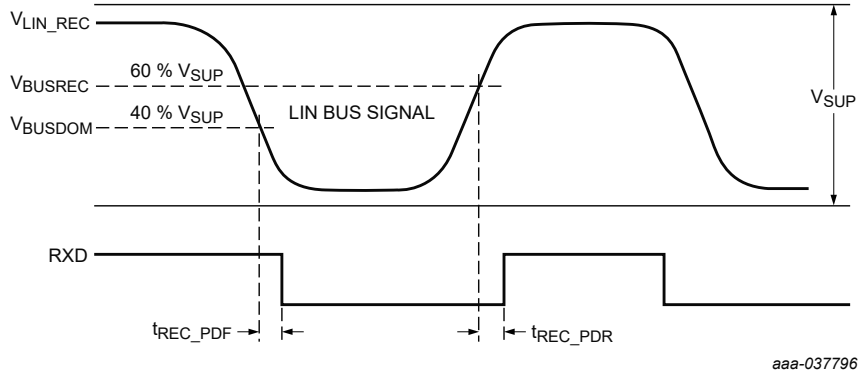


Figure 67. LIN receiver timings

12.10.4 Fault detection

12.10.4.1 VSUP undervoltage

A V_{SUP} undervoltage (V_{LIN_UV}) detection is implemented to be compliant with SAEJ2602-2[(24)] standard. At low V_{SUP} voltage (V_{SUP}<V_{LIN_UV}), the LIN bus goes into recessive state to avoid wrong communication.

12.10.4.2 TXDL permanent dominant (timeout)

If TXDL is set low for a time longer than the t_{XD_DOM} parameter, the LIN driver is disabled and the LIN bus returns to the recessive state. This prevents the bus from being set in dominant state permanently, in case a failure sets the TXDL input permanently to a low level.

The LIN receiver continues to operate. The LIN_mode MSB bit is set to 0 and the TXDL_DOM flag is reported in the DIAG_CAN_LIN register. The device recovers from this error detection after setting the LIN_mode to normal operation, and when a high level is detected on TXDL. The TXDL failure detection is operating when the LIN transceiver is in normal mode and listen only mode.

12.10.4.3 RXDL permanent recessive

If RXDL is detected high for seven consecutive receive/dominant cycles, the LIN driver and receiver are disabled and the LIN bus returns to the recessive state. The LIN_mode MSB bit is set to 0 and the RXDL_REC flag is reported in the DIAG_CAN_LIN register. The device recovers from this error detection after setting the LIN_mode to normal operation, and after a LIN dominant transition. The RXDL failure detection is operating when the LIN transceiver is in normal mode and listen only mode.

12.10.4.4 LIN bus short-circuit

If the LIN bus is dominant for a time longer than $t_{LIN_SHORT_GND}$, due for instance to an external short-circuit to GND, the detection is reported to the device main logic. The BUS bus failure detection is operating when the LIN transceiver is in normal mode and listen only mode.

12.10.4.5 LIN current limitation

In case of a LIN short-circuit to the battery, the current flowing out of the LIN driver is limited to 200 mA (I_{BUS_LIM}), and the LIN driver is not shutdown. The LIN bus goes into the recessive state when the current limitation occurs and returns in the same functional mode as before the failure when the current fell below the current limitation value.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

12.10.4.6 LIN overtemperature

If the driver temperature exceeds TSD (t_{LIN_SD}), the LIN driver is disabled and the LIN bus returns to the recessive state. The LIN receiver continues to operate. The LIN_mode MSB bit is set to 0 and the LIN_OT flag is reported in the DIAG_CAN_LIN register. A hysteresis is implemented in this protection feature. The LIN driver remains disabled until the temperature has fallen below the OT threshold minus hysteresis. The device recovers from this error detection after setting the LIN_mode to normal operation, and when a high level is detected on TXDL.

12.10.4.7 LIN errors

The interruption generated by the LIN errors can be inhibited setting INT_INH_LIN bit in INIT_INH_INT register. The list of LIN error bits is provided in Table 15.

Table 15. LIN error bits

Register	Bit	Flag type	Effect
DIAG_CAN_LIN	LIN_DOM	Error	No impact on LIN transceiver
	RXDL_REC	Error	Turn off LIN transceiver
	TXDL_DOM	Error	Turn off LIN transceiver
	LIN_OT	Error	Turn off LIN transceiver

12.10.5 Wake-up mechanism

The device can wake-up by a LIN dominant pulse longer than t_{BUS_WU}. Dominant pulse means: a recessive to dominant transition, wait for $t > t_{BUS_WU}$, then a dominant to recessive transition.

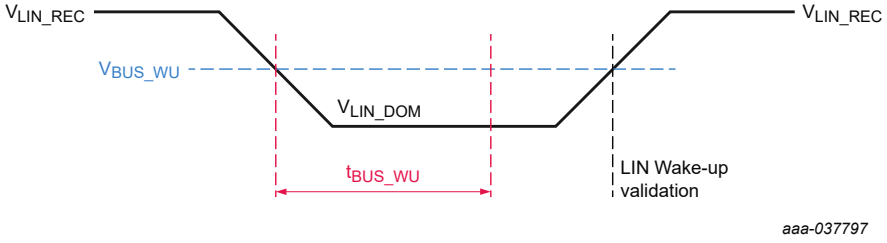


Figure 68. LIN wake-up pattern illustration

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

13 Serial peripheral interface

13.1 High-level overview

13.1.1 SPI

The device uses a 16-bit SPI, with the following arrangement:

MOSI, primary out, secondary in bits:

- Bit 15 read/write
- Bit 14 main or fail-safe register target
- bit 13 to 9 (A4 to A0) to select the register address. Bit 8 is a parity bit in write mode, next bit (=0) in read mode.
- bit7 to 0 (D7 to D0): control bits

MISO, primary in, secondary out bits:

- bits 15 to 8 (S15 to S8) are device status bits
- bits 7 to 0 (Do7 to Do0) are either extended device status bits, device internal control register content or device flags.

Figure 69 is an overview of the SPI implementation.

13.1.2 Parity bit 8 calculation

The parity bit 8 is used in write mode only (bit 15 = 1). It is calculated based on the number of logic ones contained in the bit 15–9, 7–0 sequence (this is the whole 16-bits of the write command except bit 8). In read mode, the parity bit should be set to 0.

Bit 8 must be set to 0 if the number of ones is odd.

Bit 8 must be set to 1 if the number of ones is even.

13.1.3 Device status on MISO

When a write operation is performed to store data or a control bit in the device, the MISO pin reports a 16-bit fixed device status composed of two bytes: device fixed status (bits 15 to 8) + extended device status (bits 7 to 0). In a read operation, MISO reports the fixed device status (bits 15 to 8), and the next eight bits are content of the selected register. A standard serial peripheral interface (SPI) is integrated to allow bidirectional communication between the FS6500/FS4500 and the MCU. The SPI is used for configuration and diagnostic purposes.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

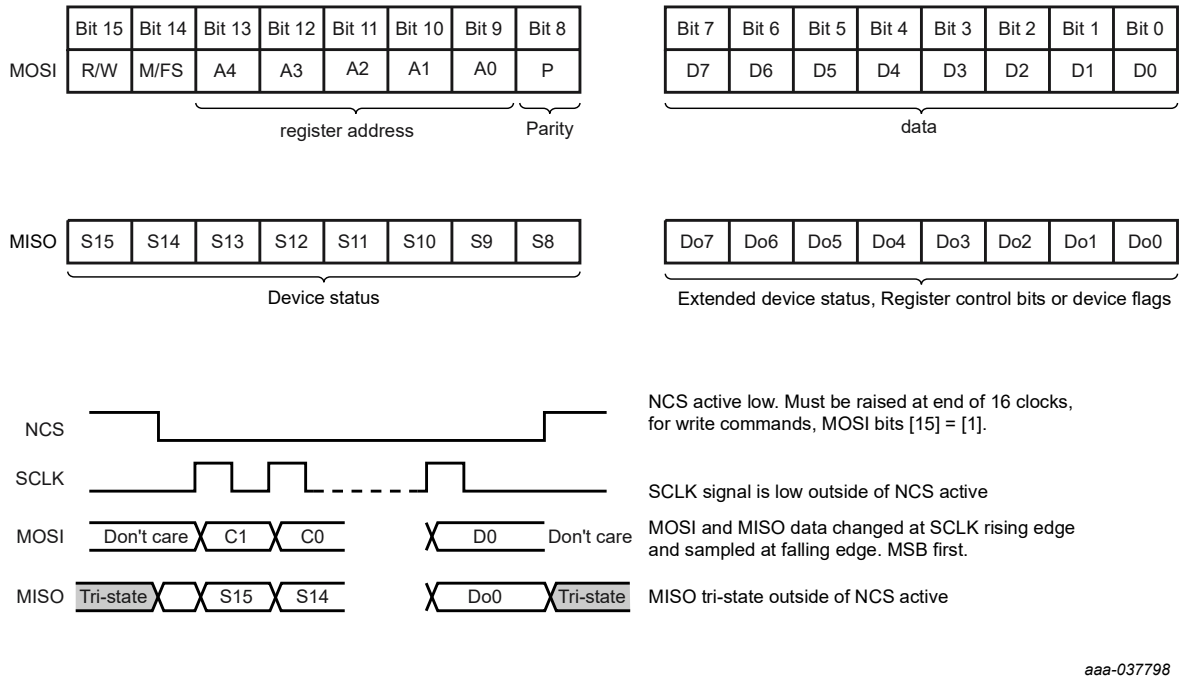


Figure 69. SPI overview: SPI waveform and signals polarity

The device contains several registers. Their address is coded on 7 bits (bits 15 to 9). Each register controls or reports part of the device function. Data can be written to the register, to control the device operation or set default value or behavior. Every register can also be read back to ensure its content (default setting or value previously written) is correct.

13.1.4 Register description

Although the minimum time between two NCS low sequences is defined by t_{ONNCS} (Figure 9), two consecutive accesses to the fail-safe registers must be done with a 3.5 µs minimum NCS high time in between. Although the minimum time between two fail-safe registers accesses is 3.5 µs, some SPI accesses to the main registers can be done in between (Figure 10).

13.2 Detailed operation

13.2.1 SPI command organization

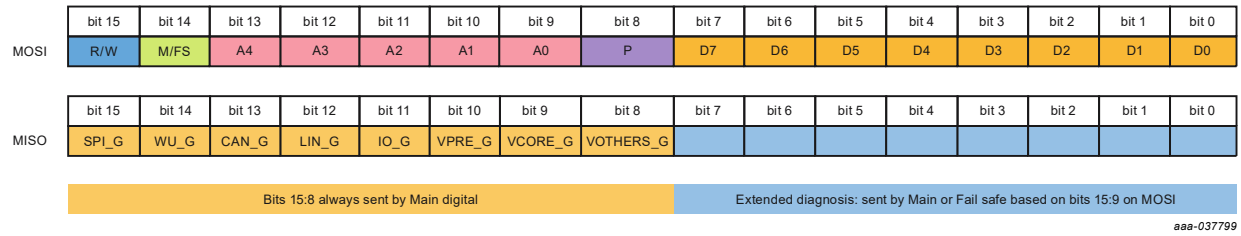


Figure 70. MOSI /MISO SPI command organization

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 16. MOSI bits description

R/W	Description	Set if it is a read or write command
	0	Read
	1	Write
M/FS	Description	Split the addresses between fail-safe state machine and main logic
	0	Main
	1	Fail-safe
A4:0	Description	Set the address to read or write
	0	See register mapping
	1	
P	Description	Parity bit (only use in write mode). Set to 0 in read mode
	0	Number of '1' (bit 15:9 and bit 7:0) is odd
	1	Number of '1' (bit 15:9 and bit 7:0) is even
D7:0	Description	Data in write mode. Must be set to 00h in read mode
	0	See register details
	1	

13.2.2 Main logic general diagnostic

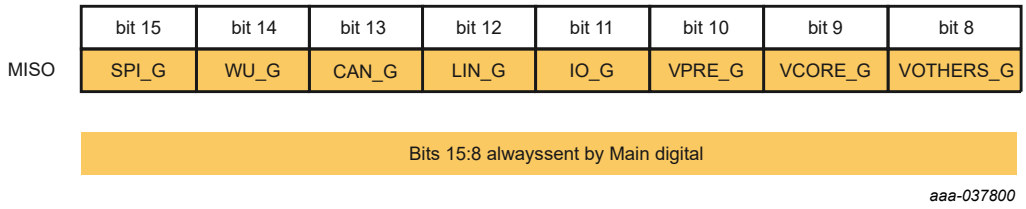


Figure 71. MISO SPI bits 15:8

Table 17. MISO bits description

SPI_G[1]	Description	Report an error in the SPI communication
	0	No failure
	1	Failure
	Reset condition	Power on reset/read
WU_G[2]	Description	Report a wake-up event. Logical OR of all wake-up sources
	0	No WU_G event
	1	WU_G event
	Reset condition	Power on reset/when initial event cleared on read
CAN_G[3]	Description	Report a CAN event (diagnostic)
	0	No event
	1	CAN event
	Reset Condition	Power on reset/when initial event cleared on read

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 17. MISO bits description...*continued*

LIN_G[4]	Description	Report a LIN event (diagnostic)
	0	No event
	1	LIN event
	Reset condition	Power on reset/when initial event cleared on read
IO_G[5]	Description	Report a change in IOs state
	0	No IO transition
	1	IO transition
	Reset condition	Power on reset/when initial event cleared on read
VPRE_G[6]	Description	Report an event from $V_{PRE-REGULATOR}$ and battery monitoring (status change or failure)
	0	No event
	1	Event occurred
	Reset condition	Power on reset/when initial event cleared on read
VCORE_G[7]	Description	Report an event from V_{CORE} regulator (status change or failure)
	0	No event
	1	Event occurred
	Reset condition	Power on reset/when initial event cleared on read
VOTHERS_G[8]	Description	Report an event from V_{CCA}, V_{AUX}, or V_{CAN} regulators (status change or failure)
	0	No event
	1	Event occurred
	Reset condition	Power on reset/when initial event cleared on read

[1] **SPI_G** = SPI_ERR or SPI_CLK or SPI_REQ or SPI_PARITY or SPI_FS_ERR or SPI_FS_CLK or SPI_FS_REQ or SPI_FS_PARITY
[2] **WU_G** = IO_5_WU or IO_4_WU or IO_3_WU or IO_2_WU or IO_0_WU or PHY_WU
[3] **CAN_G** = CANH_BATT or CANH_GND or CANL_BATT or CANL_GND or CAN_DOM or RXD_REC or TXD_DOM or CAN_OT or CAN_OC
[4] **LIN_G** = LIN_OT or RXDL_REC or TXDL_DOM or LIN_DOM
[5] **IO_G** = IO_5 or IO_4 or IO_3 or IO_2 or IO_0
[6] **VPRE_G** = VSNS_UV or VSUP_UV_7 or IPFF or ILIM_PRE or TWARN_PRE or BOB or !VPRE_STATE or VPRE_OV or VPRE_UV
[7] **VCORE_G** = TWARN_CORE or !VCORE_STATE or VCORE_OV or VCORE_UV
[8] **VOTHERS_G** = ILIM_CCA or TWARN_CCA or TSD_CCA or ILIM_CCA_OFF or VCCA_UV or VCCA_OV or ILIM_AUX or TSD_AUX or ILIM_AUX_OFF or VAUX_OV or VAUX_UV or ILIM_CAN or VCAN_UV or VCAN_OV or TSD_CAN

13.2.3 Fail-safe logic general diagnostic

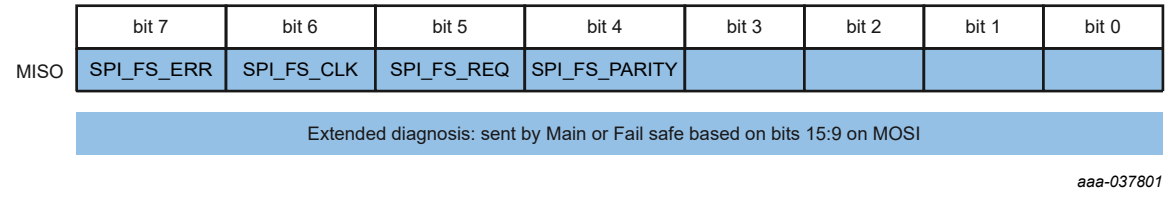


Figure 72. MISO SPI bits 7:4

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 18. MISO bits description

SPI_FS_ERR	Description	Secured SPI communication check, concerns fail-safe logic only.
	0	**No error**
	1	Error detected in the secured bits
	Reset condition	Power on reset
SPI_FS_CLK	Description	SCLK error detection, concerns internal error in fail-safe logic only and external errors (at pin level) for both main and fail-safe logics. Other errors flagged by SPI_CLK_ bit
	0	**16 clock cycles during NCS low**
	1	Wrong number of clock cycles (<16 or >16)
	Reset condition	Power on reset
SPI_FS_REQ	Description	Invalid SPI access (wrong write or read, write to INIT registers in normal mode, wrong address), concerns fail-safe Logic only
	0	**No error**
	1	SPI violation
	Reset condition	Power on reset
SPI_FS_PARITY	Description	SPI parity bit error detection, concerns fail-safe logic only
	0	**Parity bit OK**
	1	Parity bit error
	Reset condition	Power on reset

13.2.4 Main logic register address table

Table 19 is a list of device registers and addresses coded in bits 13 to 9 in MOSI for main logic.

Table 19. Register mapping of main logic

Register	Address							Write description	Table ref.
	FS/M	A4	A3	A2	A1	A0	Hex		
INIT_VREG	0	0	0	0	0	1	#1(01h)	Write during INIT phase then read only	Table 22
INIT_WU1	0	0	0	0	1	0	#2(02h)	Write during INIT phase then read only	Table 24
INIT_WU2	0	0	0	0	1	1	#3(03h)	Write during INIT phase then read only	Table 26
INIT_INT	0	0	0	1	0	0	#4(04h)	Write during INIT phase then read only	Table 28
INIT_INH_INT	0	0	0	1	0	1	#5(05h)	Write during INIT phase then read only	Table 30
LONG_DURATION_TIMER	0	0	0	1	1	0	#6(06h)	Write during normal and read	Table 32
NOT USED	0	0	0	1	1	1	#7(07h)	N/A	N/A
HW_CONFIG	0	0	1	0	0	0	#8(08h)	Read only	Table 34
WU_SOURCE	0	0	1	0	0	1	#9(09h)	Read only	Table 36
DEVICE_ID	0	0	1	0	1	0	#10(0Ah)	Read only	Table 38
IO_INPUT	0	0	1	0	1	1	#11(0Bh)	Read only	Table 40
DIAG_VPRE	0	0	1	1	0	0	#12(0Ch)	Read only	Table 42
DIAG_VCORE	0	0	1	1	0	1	#13(0Dh)	Read only	Table 44
DIAG_VCCA	0	0	1	1	1	0	#14(0Eh)	Read only	Table 46
DIAG_VAUX	0	0	1	1	1	1	#15(0Fh)	Read only	Table 48
DIAG_VSUP_VCAN	0	1	0	0	0	0	#16(10h)	Read only	Table 50
DIAG_CAN_FD	0	1	0	0	0	1	#17(11h)	Read only	Table 52

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 19. Register mapping of main logic *...continued*

Register	Address							Write description	Table ref.
	FS/M	A4	A3	A2	A1	A0	Hex		
DIAG_CAN_LIN	0	1	0	0	1	0	#18(12h)	Read only	Table 54
DIAG_SPI	0	1	0	0	1	1	#19(13h)	Read only	Table 56
NOT USED	0	1	0	1	0	0	#20(14h)	N/A	N/A
MODE	0	1	0	1	0	1	#21(15h)	Write during normal and read	Table 58
REG_MODE	0	1	0	1	1	0	#22(16h)	Write during normal and read	Table 60
IO_OUT_AMUX	0	1	0	1	1	1	#23(17h)	Write during normal and read	Table 62
CAN_LIN_MODE	0	1	1	0	0	0	#24(18h)	Write during normal and read	Table 64
NOT USED	0	1	1	0	0	1	#25(19h)	N/A	N/A
LDT_AFTER_RUN_1	0	1	1	0	1	0	#26(1Ah)	Write during normal and read	Table 66
LDT_AFTER_RUN_2	0	1	1	0	1	1	#27(1Bh)	Write during normal and read	Table 68
LDT_WAKE_UP_1	0	1	1	1	0	0	#28(1Ch)	Write during normal and read	Table 70
LDT_WAKE_UP_2	0	1	1	1	0	1	#29(1Dh)	Write during normal and read	Table 72
LDT_WAKE_UP_3	0	1	1	1	1	0	#30(1Eh)	Write during normal and read	Table 74

13.2.5 Fail-safe logic register address table

Table 20 is a list of device registers and addresses coded in bits 13 to 9 in MOSI for fail-safe logic

Table 20. Register mapping of fail-safe logic

Register	Address							Write description	Table ref.
	FS/M	A4	A3	A2	A1	A0	Hex		
INIT_FS1B_TIMING	1	0	0	0	0	1	#33(21h)	Write during INIT phase then read only	Table 76
BIST	1	0	0	0	1	0	#34(22h)	Write (No restriction) and read	Table 78
INIT_SUPERVISOR	1	0	0	0	1	1	#35(23h)	Write during INIT phase then read only	Table 80
INIT_FAULT	1	0	0	1	0	0	#36(24h)	Write during INIT phase then read only	Table 82
INIT_FSSM	1	0	0	1	0	1	#37(25h)	Write during INIT phase then read only	Table 84
INIT_SF_IMPACT	1	0	0	1	1	0	#38(26h)	Write during INIT phase then read only	Table 86
WD_WINDOW	1	0	0	1	1	1	#39(27h)	Write (no restriction) and read	Table 88
WD_LFSR	1	0	1	0	0	0	#40(28h)	Write (no restriction) and read	Table 90
WD_ANSWER	1	0	1	0	0	1	#41(29h)	Write (no restriction) and read	Table 92
RELEASE_FSxB	1	0	1	0	1	0	#42(2Ah)	Write (no restriction) and read	Table 94
SF_OUTPUT_REQUEST	1	0	1	0	1	1	#43(2Bh)	Write (no restriction) and read	Table 96
INIT_WD_CNT	1	0	1	1	0	0	#44(2Ch)	Write during INIT phase then read only	Table 98
DIAG_SF_IOs	1	0	1	1	0	1	#45(2Dh)	Read only	Table 100
WD_COUNTER	1	0	1	1	1	0	#46(2Eh)	Read only	Table 102
DIAG_SF_ERR	1	0	1	1	1	1	#47(2Fh)	Read only	Table 104
NOT USED	1	1	0	0	0	0	#48(30h)	N/A	N/A
INIT_VCORE_OVUV_IMPACT	1	1	0	0	0	1	#49(31h)	Write during INIT phase then read only	Table 106
INIT_VCCA_OVUV_IMPACT	1	1	0	0	1	0	#50(32h)	Write during INIT phase then read only	Table 108
INIT_VAUX_OVUV_IMPACT	1	1	0	0	1	1	#51(33h)	Write during INIT phase then read only	Table 110
DEVICE_ID_FS	1	1	0	1	0	0	#52(34h)	Read only	Table 112

13.2.6 Secured SPI command

Some SPI commands must be secured to avoid unwanted change of the critical bits. The secured bits in the fail-safe machine and the main state machine are calculated from the data bits sent as follows:

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 21. Secured SPI

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data 3	Data 2	Data 1	Data 0	Secure 3	Secure2	Secure 1	Secure 0

- Secure 3 = NOT(Bit5)
- Secure 2 = NOT(Bit4)
- Secure 1 = Bit7
- Secure 0 = Bit6

13.3 Detail of main logic register mapping

13.3.1 INIT_VREG

Table 22. INIT_VREG register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	0	0	0	0	1	P	ICCA_LIM	TCCA_ LIM_OFF	IPFF_DIS	VCAN_ OV_MON	0	TAUX_ LIM_OFF	VAUX_ TRK_EN	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE _G	VCORE _G	VOTHERS_ G	ICCA_LIM	TCCA_ LIM_OFF	IPFF_DIS	VCAN_ OV_MON	RES ERVED	TAUX_ LIM_OFF	VAUX_ TRK_EN	BAT_FAIL

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE _G	VCORE _G	VOTHERS_ G	ICCA_LIM	TCCA_ LIM_OFF	IPFF_DIS	VCAN_ OV_MON	RES ERVED	TAUX_ LIM_OFF	VAUX_ TRK_EN	BAT_FAIL

Table 23. INIT_VREG description and configuration of the bits (default value in bold)

ICCA_LIM	Description	Configure the current limitation threshold for VCCA. Only available for external PNP.
	0	**ICCA_LIM_OUT**
	1	ICCA_LIM_INT
	Reset condition	Power on reset
TCCA_LIM_OFF	Description	Configure the current limitation duration before VCCA is switched off. Only available for external PNP.
	0	10 ms
	1	**50 ms**
	Reset condition	Power on reset
IPFF_DIS	Description	DISABLE the input power feed forward (IPFF) function of V_{PRE}
	0	**Enabled**
	1	Disabled
	Reset condition	Power on reset

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 23. INIT_VREG description and configuration of the bits (default value in bold) *...continued*

VCAN_OV_MON	Description	CAN_5V overvoltage monitoring
	0	**Off. $V_{CAN\ OV}$** is not monitored. Flag is ignored.
	1	On. $V_{CAN\ OV}$ is monitored. If OV the CAN_5V regulator is switched off.
	Reset condition	Power on reset
TAUX_LIM_OFF	Description	Configure the current limitation duration before VAUX is switched off.
	0	10 ms
	1	**50 ms**
	Reset condition	Power on reset
VAUX_TRK_EN	Description	Configure VAUX regulator as a tracker of VCCA
	0	**NO tracking.**
	1	Tracking mode enabled and latched
	Reset condition	Power on reset
BAT_FAIL[1]	Description	Report a battery disconnection (POR of the main logic)
	0	NO POR
	1	**POR occurred**
	Reset condition	Power on reset
	Clear condition	Read

[1] **BAT_FAIL** = POR_M or $V_{SUP_UV_L}$ or BG_OK (reset sources of main logic). BAT_FAIL bit is cleared by a SPI read.

13.3.2 INIT_WU1

Table 24. INIT_WU1 register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	0	0	0	1	0	P	WU_IO0_1	WU_IO0_0	WU_IO2_1	WU_IO2_0	WU_IO3_1	WU_IO3_0	WU_IO4_1	WU_IO4_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	WU_IO0_1	WU_IO0_0	WU_IO2_1	WU_IO2_0	WU_IO3_1	WU_IO3_0	WU_IO4_1	WU_IO4_0

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	WU_IO0_1	WU_IO0_0	WU_IO2_1	WU_IO2_0	WU_IO3_1	WU_IO3_0	WU_IO4_1	WU_IO4_0

Table 25. INIT_WU1 description and configuration of the bits (default value in bold)

WU_IO0_1:0	Description	IO_0 wake-up configuration
	00	NO wake-up capability
	01	**Wake-up on rising edge - or high level**
	10	Wake-up on falling edge - or low level
	11	Wake-up on any edge
	Reset condition	Power on reset

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 25. INIT_WU1 description and configuration of the bits (default value in bold)*...continued*

WU_IO2_1:0	Description	IO_2 wake-up configuration
	00	**NO wake-up capability**
	01	Wake-up on rising edge - or high level
	10	Wake-up on falling edge - or low level
	11	Wake-up on any edge
	Reset condition	Power on reset
WU_IO3_1:0	Description	IO_3 wake-up configuration
	00	**NO wake-up capability**
	01	Wake-up on rising edge - or high level
	10	Wake-up on falling edge - or low level
	11	Wake-up on any edge
	Reset condition	Power on reset
WU_IO4_1:0	Description	IO_4 wake-up configuration
	00	**NO wake-up capability**
	01	Wake-up on rising edge - or high level
	10	Wake-up on falling edge - or low level
	11	Wake-up on any edge
	Reset condition	Power on reset

13.3.3 INIT_WU2

Table 26. INIT_WU2 register description

Write																
	bit15	**bit14**	**bit13**	**bit12**	**bit11**	**bit10**	**bit9**	**bit8**	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
MOSI	1	0	0	0	0	1	1	P	WU_IO5_1	WU_IO5_0	CAN_DIS_CFG	CAN_WU_TO	0	LIN_J2602_DIS	LIN_SR_1	LIN_SR_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	WU_IO5_1	WU_IO5_0	CAN_DIS_CFG	CAN_WU_TO	RESERVED	LIN_J2602_DIS	LIN_SR_1	LIN_SR_0

Read																
	bit15	**bit14**	**bit13**	**bit12**	**bit11**	**bit10**	**bit9**	**bit8**	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
MOSI	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	WU_IO5_1	WU_IO5_0	CAN_DIS_CFG	CAN_WU_TO	RESERVED	LIN_J2602_DIS	LIN_SR_1	LIN_SR_0

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 27. INIT_WU2 description and configuration of the bits (default value in bold)

WU_IO5_1:0	Description	IO_5 wake-up configuration
	00	**NO wake-up capability**
	01	Wake-up on rising edge - or high level
	10	Wake-up on falling edge - or low level
	11	Wake-up on any edge
	Reset condition	Power on reset
CAN_DIS_CFG	Description	Define CAN behavior when FS1B is asserted low
	0	**CAN in RX only mode (when FS1B_CAN_ IMPACT = 1 in INIT_FAULT register)**
	1	CAN in sleep mode (when FS1B_CAN_ IMPACT = 1 in INIT_FAULT register)
	Reset condition	Power on reset
CAN_WU_TO	Description	Define the CAN wake-up timeout
	0	**120 µs**
	1	2.8 ms
	Reset condition	Power on reset
LIN_J2602_dis	Description	To comply with J2602 standard. Recessive mode when VSUP < 7.0 V
	0	**Compliant with J2602 standard**
	1	Not compliant with J2602 standard
	Reset condition	Power on reset
LIN_SR_1:0	Description	Configure the LIN slew rate
	00	**20 kbit/s**
	01	10 kbit/s
	1X	Fast baud rate (Max: 100 kbit/s)
	Reset condition	Power on reset

13.3.4 INIT_INT

Table 28. INIT_INT register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	0	0	1	0	0	P	INT_ DURATION	INT_INH_ LIN	INT_INH_ ALL	INT_INH_ VSNS	INT_INH_ VPRE	INT_INH_ VCORE	INT_INH_ VOTHER	INT_INH_ CAN
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE _G	VCORE _G	VOTHERS_ G	INT_ DURATION	INT_INH_ LIN	INT_INH_ ALL	INT_INH_ VSNS	INT_INH_ VPRE	INT_INH_ VCORE	INT_INH_ VOTHER	INT_INH_ CAN

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE _G	VCORE _G	VOTHERS_ G	INT_ DURATION	INT_INH_ LIN	INT_INH_ ALL	INT_INH_ VSNS	INT_INH_ VPRE	INT_INH_ VCORE	INT_INH_ VOTHER	INT_INH_ CAN

Table 29. INIT_INT description and configuration of the bits (default value in bold)

INT_DURATION	Description	Define the duration of the interrupt pulse
	0	**100 µs**
	1	25 µs
	Reset condition	Power on reset
INT_INH_LIN	Description	Inhibit the interrupt for LIN error bits
	0	**All INT sources**
	1	LIN error bits change INHIBITED
	Reset condition	Power on reset
INT_INH_ALL	Description	Inhibit ALL the interrupt
	0	**All INT sources**
	1	All INT inhibited
	Reset condition	Power on reset
INT_INH_VSNS	Description	Inhibit the interrupt for V_{SNS_UV}
	0	**All INT sources**
	1	V_{SNS_UV} INT inhibited
	Reset condition	Power on reset
INT_INH_VPRE	Description	Inhibit the interrupt for V_{PRE} status event
	0	**All INT sources**
	1	V_{PRE} status change inhibited
	Reset condition	Power on reset
INT_INH_VCORE	Description	Inhibit the interrupt for V_{CORE} status event
	0	**All INT sources**
	1	V_{CORE} status change inhibited
	Reset condition	Power on reset
INT_INH_VOTHER	Description	Inhibit the interrupt for V_{CCA}/V_{AUX} and V_{CAN} status event
	0	**All INT sources**
	1	V_{CCA}/V_{AUX}/V_{CAN} status change inhibited
	Reset condition	Power on reset
INT_INH_CAN	Description	Inhibit the interrupt for CAN error bits
	0	**All INT sources**
	1	CAN error bits change inhibited
	Reset condition	Power on reset

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

13.3.5 INIT_INH_INT

Table 30. INIT_INH_INT register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	0	0	1	0	1	P	0	0	0	INT_INH_5	INT_INH_4	INT_INH_3	INT_INH_2	INT_INH_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	RESERVED	RESERVED	RESERVED	INT_INH_5	INT_INH_4	INT_INH_3	INT_INH_2	INT_INH_0

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	RESERVED	RESERVED	RESERVED	INT_INH_5	INT_INH_4	INT_INH_3	INT_INH_2	INT_INH_0

Table 31. INIT IO_WU2 description and configuration of the bits (default value in bold)

INT_INH_5	Description	Inhibit the interrupt pulse for IO_5 (masked in IO_G)
	0	**INT not masked**
	1	INT masked
	Reset condition	Power on reset
INT_INH_4	Description	Inhibit the interrupt pulse for IO_4 (masked in IO_G)
	0	**INT not masked**
	1	INT masked
	Reset condition	Power on reset
INT_INH_3	Description	Inhibit the interrupt pulse for IO_3 (masked in IO_G)
	0	INT not masked
	1	**INT masked**
	Reset condition	Power on reset
INT_INH_2	Description	Inhibit the interrupt pulse for IO_2 (masked in IO_G)
	0	INT not masked
	1	**INT masked**
	Reset condition	Power on reset
INT_INH_0	Description	Inhibit the interrupt pulse for IO_0 (masked in IO_G)
	0	**INT not masked**
	1	INT masked
	Reset condition	Power on reset

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

13.3.6 LONG_DURATION_TIMER

Table 32. LONG_DURATION_TIMER register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	0	0	1	1	0	P	F2	F1	F0	REG_SE	0	MODE	LDT_ ENABLE	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE _G	VCORE _G	VOTHERS_ G	F2	F1	F0	REG_SE	LDT_ RUNNING	MODE	LDT_ ENABLE	LDT_INT

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE _G	VCORE _G	VOTHERS_ G	F2	F1	F0	REG_SE	LDT_ RUNNING	MODE	LDT_ ENABLE	LDT_INT

Table 33. LONG_DURATION_TIMER description and configuration of the bits (default value in bold)

F2:F0	Description	Select timer operating function
	000	**Function 1: in normal mode count and generate flag or INT when counter reaches the after run value.**
	001	Function 2: in normal mode count until after run value is reached, then enters in LPOFF.
	010	Function 3: in normal mode count until after run value is reached, then enters in LPOFF. Once in LPOFF, count until wake-up value is reached and wake-up.
	011	Function 4: in LPOFF, count until wake-up value is reached and wake-up.
	100	Function 5: in LPOFF, count and do not wake-up. Counter value is stored in wake-up register.
	101... 111	N/A
	Reset condition	Power on reset
REG_SE	Description	Counter register selection
	0	**Read programmed wake-up register**
	1	Read real time counter into wake-up register (after counter is stopped with LDT_ENABLE bit)
	Reset condition	Power on reset
MODE	Description	Operating mode selection
	0	Calibration mode (488 µs resolution)
	1	**Normal mode (1 s resolution)**
	Reset condition	Power on reset
LDT_ENABLE	Description	LDT counter control
	0	**LDT counter stop**
	1	LDT counter start
	Reset condition	Power on reset

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 33. LONG_DURATION_TIMER description and configuration of the bits (default value in bold)*...continued*

LDT_RUNNING	Description	Counter status
	0	**Counter not running**
	1	Counter running
	Reset condition	Power on reset
LDT_INT	Description	Counter interrupt generation when function 1 is selected
	0	**No INT generated**
	1	INT generated when counter reach after run value
	Reset condition	Power on reset/read

13.3.7 HW_CONFIG

Table 34. HW_CONFIG register description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	LS_DETECT	RESERVED	VCCA_PNP_DET	VCCA_HW	VAUX_HW	1	DFS_HW1	DBG_HW

Table 35. HW_CONFIG description and configuration of the bits (default value in bold)

LS_DETECT	Description	Report the hardware configuration of V_{PRE}
	0	Buck-boost
	1	Buck only
	Reset condition	Power on reset/refresh after LPOFF
VCCA_PNP_DET	Description	Report the connection of an external PNP on V_{CCA}
	0	External PNP connected
	1	Internal MOSFET
	Reset condition	Power on reset/refresh after LPOFF
VCCA_HW	Description	Report the hardware configuration for V_{CCA}
	0	3.3 V
	1	5.0 V
	Reset condition	Power on reset/refresh after LPOFF
VAUX_HW	Description	Report the hardware configuration for V_{AUX}
	0	5.0 V
	1	3.3 V
	Reset condition	Power on reset/refresh after LPOFF
DFS_HW1	Description	Report the deep fail-safe hardware configuration (main logic)
	0	Deep fail-safe disable
	1	Deep fail-safe enable
	Reset condition	Power on reset/refresh after LPOFF

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 35. HW_CONFIG description and configuration of the bits (default value in bold)*...continued*

DBG_HW	Description	Report the configuration of the DEBUG mode
	0	Normal operation
	1	Debug mode selected
	Reset condition	Power on reset/refresh after LPOFF

13.3.8 WU_SOURCE

Table 36. WU_SOURCE register description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	IO_5_WU	IO_4_WU	IO_3_WU	IO_2_WU	IO_0_WU	AUTO_WU	LDT_WU	PHY_WU

Table 37. WU_SOURCE description and configuration of the bits (default value in bold)

IO_5_WU	Description	Report a wake-up event from IO_5
	0	**No wake-up**
	1	Wake-up event detected
	Reset condition	Power on reset/read
IO_4_WU	Description	Report a wake-up event from IO_4
	0	**No wake-up**
	1	Wake-up event detected
	Reset condition	Power on reset/read
IO_3_WU	Description	Report a wake-up event from IO_3
	0	**No wake-up**
	1	Wake-up event detected
	Reset condition	Power on reset/read
IO_2_WU	Description	Report a wake-up event from IO_2
	0	**No wake-up**
	1	Wake-up event detected
	Reset condition	Power on reset/read
IO_0_WU	Description	Report a wake-up event from IO_0
	0	**No wake-up**
	1	Wake-up event detected
	Reset condition	Power on reset/read
AUTO_WU	Description	Report an automatic wake-up event
	0	**No wake-up**
	1	Wake-up event detected
	Reset condition	Power on reset/read

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 37. WU_SOURCE description and configuration of the bits (default value in bold) *...continued*

LDT_WU	Description	Report a wake-up event from long duration timer
	0	**No wake-up**
	1	Wake-up event detected
	Reset condition	Power on reset/read
PHY_WU	Description	Report a wake-up event from CAN or LIN
	0	**No wake-up**
	1	Wake-up event detected
	Reset condition	Power on reset/read CAN_WU or/and LIN_WU

13.3.9 DEVICE _ID

Table 38. DEVICE_ID register description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE _G	VCORE _G	VOTHERS_ G	VCORE_1	VCORE_0	PHY_1	PHY_0	VKAM	DEV_ REV_2	DEV_ REV_1	DEV_ REV_0

Table 39. DEVICE_ID description and configuration of the bits (default value in bold)

VCORE_1:0	Description	VCORE current capability
	00	1.5 A
	01	0.8 A
	10	0.5 A
	11	2.2 A
	Reset condition	Power on reset
PHY_1:0	Description	CAN or LIN physical layer
	00	No CAN/no LIN
	01	CAN only
	10	LIN only
	11	CAN and LIN
	Reset condition	Power on reset
VKAM	Description	VKAM supply
	0	VKAM off by default
	1	VKAM on by default
	Reset condition	Power on reset

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 39. DEVICE_ID description and configuration of the bits (default value in bold)*...continued*

DEV_REV_2:0	Description	Device silicon revision
	000	Silicon Rev. xxx - For ASIL D devices, DEV_REV_2:0 = 010 - For ASIL B devices, DEV_REV_2:0 = 111;
	...	
	111	
	Reset condition	Power on reset

13.3.10 IO_INPUT

Table 40. IO_INPUT register description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	IO_5	IO_4	0	IO_3	IO_2	0	0	IO_0

Table 41. IO_INPUT description and configuration of the bits

IO_5	Description	Report IO_5 digital state in normal mode. No update in LPOFF mode since wake-up features available
	0	Low
	1	High
	Reset condition	Power on reset/read
IO_4	Description	Report IO_4 digital state in normal mode. No update in LPOFF mode since wake-up features available
	0	Low
	1	High
	Reset condition	Power on reset/read
IO_3	Description	Report IO_3 digital state in normal mode. No update in LPOFF mode since wake-up features available
	0	Low
	1	High
	Reset condition	Power on reset/read
IO_2	Description	Report IO_2 digital state in normal mode. No update in LPOFF mode since wake-up features available
	0	Low
	1	High
	Reset condition	Power on reset/read
IO_0	Description	Report IO_0 digital state in normal mode. No update in LPOFF mode since wake-up features available
	0	Low
	1	High
	Reset condition	Power on reset/read

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

13.3.11 DIAG_VPRE

Table 42. DIAG_VPRE register description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERSG	BoB	VPRE_STATE	TWARN_PRE	TSD_PRE	VPRE_OV	VPRE_UV	ILIM_PRE	0

Table 43. DIAG_VPRE description and configuration of the bits (default value in bold)

BoB	Description	Report a running mode of V_{PRE}
	0	**Buck**
	1	Boost
	Reset condition	Power on reset
VPRE_STATE	Description	Report the activation state of V_{PRE} SMPS
	0	SMPS off
	1	**SMPS on**
	Reset condition	Power on reset
TWARN_PRE	Description	Report a thermal warning from V_{PRE}
	0	**No thermal warning ($T_J < T_{WARN_PRE}$)**
	1	Thermal warning ($T_J > T_{WARN_PRE}$)
	Reset condition	Power on reset/read
TSD_PRE	Description	Thermal shutdown of V_{PRE}
	0	**No TSD ($T_J < T_{SD_PRE}$)**
	1	TSD occurred ($T_J > T_{SD_PRE}$)
	Reset condition	Power on reset/read
VPRE_OV	Description	V_{PRE} overvoltage detection
	0	**No overvoltage ($V_{PRE} < V_{PRE_OV}$)**
	1	Overvoltage detected ($V_{PRE} > V_{PRE_OV}$)
	Reset condition	Power on reset/read
VPRE_UV	Description	V_{PRE} undervoltage detection
	0	No undervoltage ($V_{PRE} > V_{PRE_UV}$)
	1	**Undervoltage detected ($V_{PRE} < V_{PRE_UV}$)**
	Reset condition	Power on reset/read
ILIM_PRE	Description	Report a current limitation condition on V_{PRE}
	0	**No current limitation ($I_{PRE_PK} < I_{PRE_LIM}$)**
	1	Current limitation ($I_{PRE_PK} > I_{PRE_LIM}$)
	Reset condition	Power on reset/read

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

13.3.12 DIAG_VCORE

Table 44. DIAG_VCORE register description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE _G	VCORE _G	VOTHERS_ G	0	VCORE_ STATE	TWARN_ CORE	TSD_ CORE	VCORE_ FB_OV	VCORE_ FB_UV	0	0

Table 45. DIAG_VCORE description and configuration of the bits (default value in bold)

VCORE_STATE	Description	Report the activation state of V_{CORE} SMPS
	0	SMPS off
	1	**SMPS on**
	Reset condition	Power on reset
TWARN_CORE	Description	Report a thermal warning from V_{CORE}
	0	**No thermal warning ($T_J < T_{WARN_CORE}$)**
	1	Thermal warning ($T_J > T_{WARN_CORE}$)
	Reset condition	Power on reset/read
TSD_CORE	Description	Thermal shutdown of V_{CORE}
	0	**No TSD ($T_J < T_{SD_CORE}$)**
	1	TSD occurred ($T_J > T_{SD_CORE}$)
	Reset condition	Power on reset/read
VCORE_FB_OV	Description	V_{CORE} overvoltage detection
	0	**No overvoltage ($V_{CORE_FB} < V_{CORE_FB_OV}$)**
	1	Overvoltage detected ($V_{CORE_FB} > V_{CORE_FB_OV}$)
	Reset condition	Power on reset/read
VCORE_FB_UV	Description	V_{CORE} undervoltage detection
	0	No undervoltage ($V_{CORE_FB} > V_{CORE_FB_UV}$)
	1	**Undervoltage ($V_{CORE_FB} < V_{CORE_FB_UV}$)**
	Reset condition	Power on reset/read

13.3.13 DIAG_VCCA

Table 46. DIAG_VCCA register description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE _G	VCORE _G	VOTHERS_ G	0	0	TWARN_ CCA	TSD_CCA	VCCA_OV	VCCA_UV	ILIM_CCA	ILIM_CCA_ OFF

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 47. DIAG_VCCA description and configuration of the bits (default value in bold)

TWARN_CCA	Description	Report a thermal warning from V_{CCA}. Available only for internal pass MOSFET
	0	**No thermal warning (T_J < T_{WARN_CCA})**
	1	Thermal warning (T_J > T_{WARN_CCA})
	Reset condition	Power on reset/read
TSD_CCA	Description	Thermal shutdown of V_{CCA}
	0	**NO TSD (T_J < T_{SD_CCA})**
	1	TSD occurred (T_J > T_{SD_CCA})
	Reset condition	Power on reset/read
VCCA_OV	Description	V_{CCA} overvoltage detection
	0	**No overvoltage (V_{CCA} < V_{CCA_OV})**
	1	Overvoltage detected (V_{CCA} > V_{CCA_OV})
	Reset condition	Power on reset/read
VCCA_UV	Description	V_{CCA} undervoltage detection
	0	No undervoltage (V_{CCA} > V_{CCA_UV})
	1	**Undervoltage detected (V_{CCA} < V_{CCA_UV})**
	Reset condition	Power on reset/read
ILIM_CCA	Description	Report a current limitation condition on V_{CCA}
	0	**No current limitation (I_{CCA} < I_{CCA_LIM})**
	1	Current limitation (I_{CCA} > I_{CCA_LIM})
	Reset condition	Power on reset/read
ILIM_CCA_OFF	Description	Maximum current limitation duration. Available only when an external PNP is connected
	0	**$T_{_LIMITATION}$ < $T_{CCA_LIM_OFF}$**
	1	$T_{_LIMITATION}$ >$T_{CCA_LIM_OFF}$
	Reset condition	Power on reset/read

13.3.14 DIAG_VAUX

Table 48. DIAG_VAUX register description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE _G	VCORE _G	VOTHERS_ G	0	0	0	TSD_AUX	VAUX_OV	VAUX_UV	ILIM_AUX	ILIM_AUX_ OFF

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 49. DIAG_VAUX description and configuration of the bits (default value in bold)

TSD_AUX	Description	Thermal shutdown of V_{AUX}
	0	**No TSD ($T_J < T_{SD_AUX}$)**
	1	TSD occurred ($T_J > T_{SD_AUX}$)
	Reset condition	Power on reset/read
VAUX_OV	Description	V_{AUX} overvoltage detection
	0	**No overvoltage ($V_{AUX} < V_{AUX_OV}$)**
	1	Overvoltage detected ($V_{AUX} > V_{AUX_OV}$)
	Reset condition	Power on reset/read
VAUX_UV	Description	V_{AUX} undervoltage detection
	0	No undervoltage ($V_{AUX} > V_{AUX_UV}$)
	1	**Undervoltage detected ($V_{AUX} < V_{AUX_UV}$)**
	Reset condition	Power on reset/read
ILIM_AUX	Description	Report a current limitation condition on V_{AUX}
	0	**No current limitation ($I_{AUX} < I_{AUX_LIM}$)**
	1	Current limitation ($I_{AUX} > I_{AUX_LIM}$)
	Reset condition	Power on reset/read
ILIM_AUX_OFF	Description	Maximum current limitation duration
	0	**$T_{_LIMITATION} < T_{AUX_LIM_OFF}$**
	1	$T_{_LIMITATION} > T_{AUX_LIM_OFF}$
	Reset condition	Power on reset/read

13.3.15 DIAG_VSUP_VCAN

Table 50. DIAG_VSUP_VCAN register description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	VSNS_UV	VSUP_UV_7	IPFF	TSD_CAN	VCAN_OV	VCAN_UV	ILIM_CAN	0

Table 51. DIAG_VSUP_VCAN description and configuration of the bits (default value in bold)

VSNS_UV	Description	Detection of battery voltage below V_{SNS_UV}
	0	$V_{BAT} > V_{SNS_UV}$
	1	**$V_{BAT} < V_{SNS_UV}$**
	Reset condition	Power on reset/read
VSUP_UV_7	Description	Detection of V_{SUP} below $V_{SUP_UV_7}$
	0	$V_{SUP} > V_{SUP_UV_7}$
	1	**$V_{SUP} < V_{SUP_UV_7}$**
	Reset condition	Power on reset/read

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 51. DIAG_VSUP_VCAN description and configuration of the bits (default value in bold)*...continued*

IPFF	Description	Input power feed forward (IPFF)
	0	**Normal operation**
	1	IPFF mode activated
	Reset condition	Power on reset/read
TSD_CAN	Description	Thermal shutdown of V_{CAN}
	0	**NO TSD ($T_J < T_{SD_CAN}$)**
	1	TSD occurred ($T_J > T_{SD_CAN}$)
	Reset condition	Power on reset/read
VCAN_OV	Description	V_{CAN} overvoltage detection
	0	**No overvoltage ($V_{CAN} < V_{CAN_OV}$)**
	1	Overvoltage detected ($V_{CAN} > V_{CAN_OV}$)
	Reset condition	Power on reset/read
VCAN_UV	Description	V_{CAN} undervoltage detection
	0	No undervoltage ($V_{CAN} > V_{CAN_UV}$)
	1	**Undervoltage detected ($V_{CAN} < V_{CAN_UV}$)**
	Reset condition	Power on reset/read
ILIM_CAN	Description	Report a current limitation condition on V_{CAN}
	0	**No current limitation ($I_{CAN} < I_{CAN_LIM}$)**
	1	Current limitation ($I_{CAN} > I_{CAN_LIM}$)
	Reset condition	Power on reset/read

13.3.16 DIAG_CAN_FD

Table 52. DIAG_CAN_FD register description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	CANH_BATT	CANH_GND	CANL_BATT	CANL_GND	CAN_DOM	0	RXD_REC	TXD_DOM

Table 53. DIAG_CAN_FD description and configuration of the bits (default value in bold)

CANH_BATT	Description	CANH short-circuit to battery detection
	0	**No failure**
	1	Failure detected
	Reset condition	Power on reset/read
CANH_GND	Description	CANH short-circuit to GND detection
	0	**No failure**
	1	Failure detected
	Reset condition	Power on reset/read

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 53. DIAG_CAN_FD description and configuration of the bits (default value in bold)*...continued*

CANL_BATT	Description	CANL short-circuit to battery detection
	0	**No failure**
	1	Failure detected
	Reset condition	Power on reset/read
CANL_GND	Description	CANL short-circuit to GND detection
	0	**No failure**
	1	Failure detected
	Reset condition	Power on reset/read
CAN_DOM	Description	CAN-bus dominant clamping detection
	0	**No failure**
	1	Failure detected
	Reset condition	Power on reset/read
RXD_REC	Description	RXD recessive clamping detection (short-circuit to 5.0 V)
	0	**No failure**
	1	Failure detected
	Reset condition	Power on reset/read
TXD_DOM	Description	TXD dominant clamping detection (short-circuit to GND)
	0	**No failure**
	1	Failure detected
	Reset condition	Power on reset/read

13.3.17 DIAG_CAN_LIN

Table 54. DIAG_CAN_LIN register description

Read																
	bit15	**bit14**	**bit13**	**bit12**	**bit11**	**bit10**	**bit9**	**bit8**	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
MOSI	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	LIN_DOM	TXDL_DOM	0	RXDL_REC	LIN_OT	0	CAN_OT	CAN_OC

Table 55. DIAG_CAN_LIN description and configuration of the bits (default value in bold)

LIN_DOM	Description	LIN bus dominant clamping detection
	0	**No failure**
	1	Failure detected
	Reset condition	Power on reset/read
TDXL_DOM	Description	LIN TXD dominant clamping detection (short-circuit to GND)
	0	**No failure**
	1	Failure detected
	Reset condition	Power on reset/read

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 55. DIAG_CAN_LIN description and configuration of the bits (default value in bold)*...continued*

RXDL_REC	Description	LIN RXD recessive clamping detection (short-circuit to 5.0 V)
	0	**No failure**
	1	Failure detected
	Reset condition	Power on reset/read
LIN_OT	Description	LIN overtemperature detection
	0	**No failure**
	1	Failure detected
	Reset condition	Power on reset/read
CAN_OT	Description	CAN overtemperature detection
	0	**No failure**
	1	Failure detected
	Reset condition	Power on reset/read
CAN_OC	Description	CAN overcurrent detection
	0	**No failure**
	1	Failure detected
	Reset condition	Power on reset/read

13.3.18 DIAG_SPI

Table 56. DIAG_SPI register description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_ERR	0	SPI_CLK	0	SPI_REQ	0	SPI_PARITY	0

Table 57. DIAG_SPI description and configuration of the bits (default value in blue)

SPI_ERR	Description	Secured SPI communication check
	0	**No error**
	1	Error detected in the secured bits
	Reset condition	Power on reset/read
SPI_CLK	Description	SCLK error detection
	0	**16 clock cycles during NCS low**
	1	Wrong number of clock cycles (<16 or > 16)
	Reset condition	Power on reset/read
SPI_REQ	Description	Invalid SPI access (wrong write or read, write to INIT registers in normal mode, wrong address)
	0	**No error**
	1	SPI violation
	Reset condition	Power on reset/read

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 57. DIAG_SPI description and configuration of the bits (default value in blue)*...continued*

SPI_PARITY	Description	SPI parity bit error detection
	0	**Parity bit OK**
	1	Parity bit error
	Reset condition	Power on reset/read

13.3.19 Mode

Table 58. Mode register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	0	1	0	1	P	VKAM_EN	LPOFF_ AUTO_WU	GO_ LPOFF	INT_REQ	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE _G	VCORE _G	VOTHERS_ G	VKAM_EN	RESERVED	RES ERVED	RES ERVED	INIT	NORMAL	DFS	LPOFF

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE _G	VCORE _G	VOTHERS_ G	VKAM_EN	RESERVED	RES ERVED	RES ERVED	INIT	NORMAL	DFS	LPOFF

Table 59. Mode description and configuration of the bits (default value in bold)

VKAM_EN	Description	V_{KAM} control (default state depends on part number)
	0	DISABLED
	1	ENABLED
	Reset condition	Power on reset
LPOFF_AUTO_WU	Description	Configure the device in LPOFF_AUTO_WU
	0	**No action**
	1	Go to LPOFF mode and wake-up automatically after 1.0 ms
	Reset condition	Power on reset/refresh after LPOFF
GO_LPOFF	Description	Configure the device in LPOFF–SLEEP
	0	**No action**
	1	Go to LPOFF mode and wait for wake-up event
	Reset condition	Power on reset/refresh after LPOFF
INT_REQ	Description	Request for an INT pulse
	0	**No Request**
	1	Request for an INT pulse
	Reset condition	Power on reset
INIT	Description	Report if INIT mode of the main logic state machine is entered
	0	Not in INIT mode
	1	**INIT mode**
	Reset condition	Power on reset

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 59. Mode description and configuration of the bits (default value in bold)*...continued*

NORMAL	Description	Report if normal mode of the main logic state machine is entered
	0	**Not in normal mode**
	1	Normal mode
	Reset condition	Power on reset
DFS	Description	Report if the device resumes from deep fail-safe mode
	0	**Not in deep fail-safe**
	1	Resume from deep fail-safe
	Reset condition	Power on reset/read
LPOFF	Description	Report if the device resumes from LPOFF-sleep or LPOFF_AUTO_WU mode
	0	**Not in LPOFF**
	1	Resume from LPOFF
	Reset condition	Power on reset/read
Secure 3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6

13.3.20 REG_MODE

Table 60. REG_MODE register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	0	1	1	0	P	VCORE_EN	VCCA_EN	VAUX_EN	VCAN_EN	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	RESERVED	RESERVED	RESERVED	RESERVED	VCORE_EN	VCCA_EN	VAUX_EN	VCAN_EN

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	RESERVED	RESERVED	RESERVED	RESERVED	VCORE_EN	VCCA_EN	VAUX_EN	VCAN_EN

Table 61. REG_MODE description and configuration of the bits (default value in bold)

VCORE_EN	Description	V_{CORE} control (switch off not recommended if V_{CORE} is safety critical)
	0	Disabled
	1	**Enabled**
	Reset condition	Power on reset
VCCA_EN	Description	V_{CCA} control (switch off not recommended if V_{CCA} is safety critical)
	0	Disabled
	1	**Enabled**
	Reset condition	Power on reset

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 61. REG_MODE description and configuration of the bits (default value in bold)*...continued*

VAUX_EN	Description	V_{AUX} control (switch off not recommended if V_{AUX} is safety critical)
	0	Disabled
	1	**Enabled**
	Reset condition	Power on reset
VCAN_EN	Description	V_{CAN} control
	0	Disabled
	1	**Enabled**
	Reset condition	Power on reset
Secure 3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6

13.3.21 IO_OUT_AMUX

Table 62. IO_OUT_AMUX register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	0	1	1	1	P	IO_OUT_4_EN	IO_OUT_4	0	0	0	AMUX_2	AMUX_1	AMUX_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	IO_OUT_4_EN	IO_OUT_4	RESERVED	RESERVED	RESERVED	AMUX_2	AMUX_1	AMUX_0

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	IO_OUT_4_EN	IO_OUT_4	RESERVED	RESERVED	RESERVED	AMUX_2	AMUX_1	AMUX_0

Table 63. IO_OUT_AMUX description and configuration of the bits (default value in bold)

IO_OUT_4_EN	Description	Enable the output gate driver capability for IO_4
	0	**High-impedance (IO_4 configured as input)**
	1	Enabled (IO_4 configured as output gate driver)
	Reset condition	Power on reset
IO_OUT_4	Description	Configure IO_4 output gate driver state
	0	**Low**
	1	High
	Reset condition	Power on reset

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 63. IO_OUT_AMUX description and configuration of the bits (default value in bold)*...continued*

AMUX_2:0	Description	Select AMUX output
	000	**V_{REF}**
	001	V_{SNS} wide range
	010	IO_0 wide range
	011	IO_5 wide range
	100	V_{SNS} tight range
	101	IO_0 tight range
	110	IO_5 tight range/VKAM
	111	Die Temperature Sensor
	Reset condition	Power on reset

13.3.22 CAN_LIN_MODE

Table 64. CAN_LIN_MODE register description

Write																
	bit15	**bit14**	**bit13**	**bit12**	**bit11**	**bit10**	**bit9**	**bit8**	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
MOSI	1	0	1	1	0	0	0	P	CAN_ MODE_1	CAN_ MODE_0	CAN_ AUTO_ DIS	LIN_ MODE_1	LIN_ MODE_0	LIN_ AUTO_ DIS	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE _G	VCORE _G	VOTHERS_ G	CAN_ MODE_1	CAN_ MODE_0	CAN_ AUTO_ DIS	LIN_ MODE_1	LIN_ MODE_0	LIN_ AUTO_ DIS	CAN_WU	LIN_WU

Read																
	bit15	**bit14**	**bit13**	**bit12**	**bit11**	**bit10**	**bit9**	**bit8**	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
MOSI	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE _G	VCORE _G	VOTHERS_ G	CAN_ MODE_1	CAN_ MODE_0	CAN_ AUTO_ DIS	LIN_ MODE_1	LIN_ MODE_0	LIN_ AUTO_ DIS	CAN_WU	LIN_WU

Table 65. CAN_LIN_MODE description and configuration of the bits (default value in bold)

CAN_MODE_1:0[1]	Description	Configure the CAN mode
	00	Sleep/no wake-up capability
	01	Listen only
	10	**Sleep/wake-up capability**
	11	Normal operation mode
	Reset condition	Power on reset
CAN_AUTO_DIS	Description	Automatic CAN TX disable
	0	NO auto disable
	1	**Reset CAN_MODE from ’11’ to ’01’ on CAN_OT or TXD_DOM or RXD_REC event**
	Reset condition	Power on reset

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 65. CAN_LIN_MODE description and configuration of the bits (default value in bold)*...continued*

LIN_MODE_1:0	Description	Configure the LIN mode
	00	Sleep/no wake-up capability
	01	Listen only
	10	**Sleep/wake-up capability**
	11	Normal operation mode
	Reset condition	Power on reset
LIN_AUTO_DIS	Description	Automatic LIN mode disable
	0	No auto disable
	1	**Reset LIN_mode from '11' to '01' on LIN_OT or TXDL_DOM or RXDL_REC event**
	Reset condition	Power on reset
CAN_WU	Description	Report a wake-up event from the CAN
	0	**No wake-up**
	1	Wake-up detected
	Reset condition	Power on reset/read
LIN_WU	Description	Report a wake-up event from the LIN
	0	**No wake-up**
	1	Wake-up detected
	Reset condition	Power on reset/read

[1] CAN mode is automatically configured to 'sleep + wake-up capability[10]' if CAN mode was different than 'sleep + no wake-up capability [00]' before the device enters in LPOFF. After LPOFF, the initial CAN mode prior to enter LPOFF is restored.

13.3.23 LDT_AFTER_RUN_1

Table 66. LDT_AFTER_RUN_1 register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	1	0	1	0	P	B15	B14	B13	B12	B11	B10	B9	B8
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	B15	B14	B13	B12	B11	B10	B9	B8

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	B15	B14	B13	B12	B11	B10	B9	B8

Table 67. LDT_AFTER_RUN_1 description and configuration of the bits (default value in bold)

B15:8	Description	Long duration timer - after run value
	00 to FF	After run value (8 most significant bits)
	Reset condition	Power on reset

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

13.3.24 LDT_AFTER_RUN_2

Table 68. LDT_AFTER_RUN_2 register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	1	0	1	1	P	B7	B6	B5	B4	B3	B2	B1	B0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	B7	B6	B5	B4	B3	B2	B1	B0

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	B7	B6	B5	B4	B3	B2	B1	B0

Table 69. LDT_AFTER_RUN_2 description and configuration of the bits (default value in bold)

B7:0	Description	Long duration timer - after run value
	00 to FF	After run value (8 least significant bits)
	Reset condition	Power on reset

13.3.25 LDT_WAKE_UP_1

Table 70. LDT_WAKE_UP_1 register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	1	1	0	0	P	B23	B22	B21	B20	B19	B18	B17	B16
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	B23	B22	B21	B20	B19	B18	B17	B16

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	B23	B22	B21	B20	B19	B18	B17	B16

Table 71. LDT_WAKE_UP_1 description and configuration of the bits (default value in bold)

B23:16	Description	Long duration timer – wake-up value
	00 to FF	Wake-up value (8 most significant bits)
	Reset condition	Power on reset

13.3.26 LDT_WAKE_UP_2

Table 72. LDT_WAKE_UP_2 register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	1	1	0	1	P	B15	B14	B13	B12	B11	B10	B9	B8
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	B15	B14	B13	B12	B11	B10	B9	B8

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	B15	B14	B13	B12	B11	B10	B9	B8

Table 73. LDT_WAKE_UP_2 description and configuration of the bits (default value in bold)

B15:8	Description	Long duration timer – wake-up value
	00 to FF	Wake-up value (8 intermediate bits)
	Reset condition	Power on reset

13.3.27 LDT_WAKE_UP_3

Table 74. LDT_WAKE_UP_3 register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	1	1	1	0	P	B7	B6	B5	B4	B3	B2	B1	B0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	B7	B6	B5	B4	B3	B2	B1	B0

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	B7	B6	B5	B4	B3	B2	B1	B0

Table 75. LDT_WAKE_UP_3 description and configuration of the bits (default value in bold)

B7:0	Description	Long duration timer – wake-up value
	00 to FF	Wake-up value (8 least significant bits)
	Reset condition	Power on reset

13.4 Detail of fail-safe logic register mapping

13.4.1 INIT_FS1B_TIMING

Table 76. INIT_FS1B_TIMING register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	0	0	1	p	FS1B_TIME_3	FS1B_TIME_2	FS1B_TIME_1	FS1B_TIME_0	SECURE_3	SECURE_2	SECURE_1	SECURE_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	FS1B_TIME_3	FS1B_TIME_2	FS1B_TIME_1	FS1B_TIME_0

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	FS1B_TIME_3	FS1B_TIME_2	FS1B_TIME_1	FS1B_TIME_0

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 77. INIT_FS1B_TIMING. Description and configuration of the bits (Default value in bold)

FS1B_TIME_3:0 (timing made with fail-safe oscillator)	Description	FS1B timing range factor x1 (FS1B_TIME_RANGE bit = 0)	FS1B timing range factor x8 (FS1B_TIME_RANGE bit = 1)
	0000	0	0
	0001	10 ms	80 ms
	0010	13 ms	104 ms
	0011	17 ms	135 ms
	0100	22 ms	176 ms
	0101	29 ms	228 ms
	0110	**37 ms**	297 ms
	0111	48 ms	386 ms
	1000	63 ms	502 ms
	1001	82 ms	653 ms
	1010	106 ms	848 ms
	1011	138 ms	1103 ms
	1100	179 ms	1434 ms
	1101	233 ms	1864 ms
	1110	303 ms	2423 ms
	1111	394 ms	3150 ms
	Reset condition	Power on reset	
Secure3:0	Description	Secured bits based on write bits	
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6	

13.4.2 BIST

Table 78. BIST register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	0	1	0	P	0	ABIST2_ FS1B	ABIST2_ VAUX	0	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE _G	VCORE _G	VOTHERS_ G	SPI_FS_ ERR	SPI_FS_ CLK	SPI_FS_ REQ	SPI_FS_ PARITY	LBIST_ OK	ABIST2_ FS1B_OK	ABIST2_ VAUX_OK	ABIST1_ OK

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE _G	VCORE _G	VOTHERS_ G	SPI_FS_ ERR	SPI_FS_ CLK	SPI_FS_ REQ	SPI_FS_ PARITY	LBIST_ OK	ABIST2_ FS1B_OK	ABIST2_ VAUX_OK	ABIST1_ OK

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 79. BIST description and configuration of the bits (default value in bold)

ABIST2_FS1B	Description	Request ABIST execution on FS1B
	0	**No action**
	1	Launch ABIST on FS1B
	Reset condition	Fail-safe power-on-reset
ABIST2_VAUX	Description	Request ABIST execution on VAUX
	0	**No action**
	1	Launch ABIST on VAUX
	Reset condition	Fail-safe power-on-reset
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6
LBIST_OK	Description	Diagnostic of fail-safe logic BIST (automatically executed)
	0	LBIST fail
	1	**LBIST pass**
	Reset condition	Fail-safe power-on-reset
ABIST2_FS1B_OK	Description	Diagnostic of FS1B Analog BIST2 (executed on demand)
	0	**FS1B ABIST fail or not executed**
	1	FS1B ABIST pass
	Reset condition	Fail-safe power-on-reset
ABIST2_VAUX_OK	Description	Diagnostic of VAUX Analog BIST2 (executed on demand)
	0	**VAUX ABIST fail or not executed**
	1	VAUX ABIST pass
	Reset condition	Fail-safe power-on-reset
ABIST1_OK	Description	Diagnostic of analog BIST1 (automatically executed)
	0	ABIST1 fail
	1	**ABIST1 pass**
	Reset condition	Fail-safe power-on-reset

13.4.3 INIT_SUPERVISOR

Table 80. INIT_SUPERVISOR register description

Write																
	bit15	**bit14**	**bit13**	**bit12**	**bit11**	**bit10**	**bit9**	**bit8**	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
MOSI	1	1	0	0	0	1	1	P	VCORE_5D	VCCA_5D	VAUX_5D	FS1B_TIME_RANGE	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	VCORE_5D	VCCA_5D	VAUX_5D	FS1B_TIME_RANGE

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	VCORE_5D	VCCA_5D	VAUX_5D	FS1B_TIME_RANGE

Table 81. INIT_SUPERVISOR description and configuration of the bits (default value in bold)

VCORE_5D	Description	Configure the V_{CORE} undervoltage in degraded mode. Only valid for 5.0 V
	0	**Normal 5.0 V undervoltage detection threshold ($V_{CORE_FB_UV}$)**
	1	Degraded mode, lower undervoltage detection threshold applied ($V_{CORE_FB_UV_D}$)
	Reset condition	Power on reset
VCCA_5D	Description	Configure the V_{CCA} undervoltage in degraded mode. Only valid for 5.0 V
	0	**Normal 5.0 V undervoltage detection threshold ($V_{CCA_UV_5}$)**
	1	Degraded mode, lower undervoltage detection threshold applied ($V_{CCA_UV_D}$)
	Reset condition	Power on reset
VAUX_5D	Description	Configure the V_{AUX} undervoltage in degraded mode. Only valid for 5.0 V
	0	**Normal 5.0 V undervoltage detection threshold ($V_{AUX_UV_5}$)**
	1	Degraded mode; lower undervoltage detection threshold applied ($V_{AUX_UV_5D}$)
	Reset condition	Power on reset
FS1B_TIME_RANGE	Description	Configure the FS1B timing range factor x1 or x8
	0	**x1 timing range factor**
	1	x8 timing range factor
	Reset condition	Power on reset
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2= NOT(bit4) Secured_1=bit7 Secured_0=bit6

13.4.4 INIT_FAULT

Table 82. INIT_FAULT register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	1	0	0	P	FLT_ERR_FS	FS1B_CAN_IMPACT	FLT_ERR_IMP_1	FLT_ERR_IMP_0	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	FLT_ERR_FS	FS1B_CAN_IMPACT	FLT_ERR_IMP_1	FLT_ERR_IMP_0

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	FLT_ERR_FS	FS1B_CAN_IMPACT	FLT_ERR_IMP_1	FLT_ERR_IMP_0

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 83. INIT_FAULT description and configuration of the bits (default value in bold)

FLT_ERR_FS	Description	Configure the values of the fault error counter
	0	**intermediate = 3; final = 6**
	1	intermediate = 1; final = 2
	Reset condition	Power on reset
FS1B_CAN_IMPACT	Description	Configure CAN behavior when FS1B is asserted low
	0	No effect
	1	**CAN in RX only or sleep mode when FS1B is asserted (depends on CAN_DIS_CFG bit in INIT_WU2 register)**
	Reset condition	Power on reset
FLT_ERR_IMP_1:0	Description	Configure RSTB and FS0B behavior when fault error counter ≥ intermediate value
	00	No effect on RSTB and FS0B
	01	**FS0B is asserted low if FLT_ERR_CNT** ≥ intermediate value
	10	RSTB is asserted low if FLT_ERR_CNT ≥ intermediate value and WD error counter = WD_CNT_ERR[1:0]
	11	FS0B is asserted low if FLT_ERR_CNT ≥ intermediate value RSTB is asserted low if FLT_ERR_CNT ≥ intermediate value and WD error counter = WD_CNT_ERR[1:0]
	Reset condition	Power on reset
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6

13.4.5 INIT_FSSM

Table 84. INIT_FSSM register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	1	0	1	P	IO_45_FS	IO_23_FS	PS	RSTB_ DURATION	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE _G	VCORE _G	VOTHERS_ G	SPI_FS_ ERR	SPI_FS_ CLK	SPI_FS_ REQ	SPI_FS_ PARITY	IO_45_FS	IO_23_FS	PS	RSTB_ DURATION

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE _G	VCORE _G	VOTHERS_ G	SPI_FS_ ERR	SPI_FS_ CLK	SPI_FS_ REQ	SPI_FS_ PARITY	IO_45_FS	IO_23_FS	PS	RSTB_ DURATION

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 85. INIT_FSSM description and configuration of the bits (default value in bold)

IO_45_FS	Description	Configure the couple of IO_4:5 as safety inputs for external IC error monitoring
	0	**Not safety**
	1	Safety critical
	Reset condition	Power on reset
IO_23_FS	Description	Configure the couple of IO_3:2 as safety inputs for FCCU monitoring
	0	Not safety
	1	**Safety critical**
	Reset condition	Power on reset
PS	Description	Configure the F_{CCU} polarity
	0	**Fccu_eaout_1:0 active high**
	1	Fccu_eaout_1:0 active low
	Reset condition	Power on reset
RSTB_DURATION	Description	Configure the RSTB low duration time
	0	**10 ms**
	1	1.0 ms
	Reset condition	Power on reset
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6

13.4.6 INIT_SF_IMPACT

Table 86. INIT_SF_IMPACT register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	1	1	0	P	TDLY_ TDUR	DIS_8S	WD_ IMPACT_1	WD_ IMPACT_0	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE _G	VCORE _G	VOTHERS_ G	SPI_FS_ ERR	SPI_FS_ CLK	SPI_FS_ REQ	SPI_FS_ PARITY	TDLY_ TDUR	DIS_8S	WD_ IMPACT_1	WD_ IMPACT_0

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE _G	VCORE _G	VOTHERS_ G	SPI_FS_ ERR	SPI_FS_ CLK	SPI_FS_ REQ	SPI_FS_ PARITY	TDLY_ TDUR	DIS_8S	WD_ IMPACT_1	WD_ IMPACT_0

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 87. INIT_SF_IMPACT description and configuration of the bits (default value in bold)

TDLY_TDUR	Description	FS1B delay or FS1B duration mode selection
	0	**FS1B t_{DELAY} mode**
	1	FS1B $t_{DURATION}$ mode
	Reset condition	Power on reset
DIS_8S	Description	Disable the 8.0 s timer used to enter deep fail-safe mode
	0	**Enabled**
	1	Disabled
	Reset condition	Power on reset
WD_IMPACT_1:0	Description	Watchdog impact on RSTB and/or FS0B assertion
	00	No effect on RSTB and FS0B if WD error counter = WD_CNT_ERR[1:0]
	01	**RSTB only is asserted low if WD error counter = WD_CNT_ERR[1:0]**
	10	FS0B only is asserted low if WD error counter = WD_CNT_ERR[1:0]
	11	RSTB and FS0B are asserted low if WD error counter = WD_CNT_ERR[1:0]
	Reset condition	Power on reset
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6

13.4.7 WD_WINDOW

Table 88. WD_WINDOW register description

Write[1]																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	1	1	1	P	WD_WINDOW_3	WD_WINDOW_2	WD_WINDOW_1	WD_WINDOW_0	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	WD_WINDOW_3	WD_WINDOW_2	WD_WINDOW_1	WD_WINDOW_0

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	WD_WINDOW_3	WD_WINDOW_2	WD_WINDOW_1	WD_WINDOW_0

[1] Any write command to the WD_WINDOW register in the normal mode should be followed by a read command to verify the correct change of the WD window duration.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 89. WD_WINDOW description and configuration of the bits (default value in bold)

WD_WINDOW_3:0	Description	Configure the watchdog window duration. Duty cycle if set to 50 %
	0000	Disable (in INIT phase only)
	0001	1.0 ms
	0010	2.0 ms
	0011	**3.0 ms**
	0100	4.0 ms
	0101	6.0 ms
	0110	8.0 ms
	0111	12 ms
	1000	16 ms
	1001	24 ms
	1010	32 ms
	1011	64 ms
	1100	128 ms
	1101	256 ms
	1110	512 ms
	1111	1024 ms
	Reset condition	Power on reset
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6

13.4.8 WD_LFSR

Table 90. WD_LFSR register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	1	0	0	0	P	WD_LFSR_7	WD_LFSR_6	WD_LFSR_5	WD_LFSR_4	WD_LFSR_3	WD_LFSR_2	WD_LFSR_1	WD_LFSR_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	WD_LFSR_7	WD_LFSR_6	WD_LFSR_5	WD_LFSR_4	WD_LFSR_3	WD_FSR_2	WD_LFSR_1	WD_LFSR_0

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	WD_LFSR_7	WD_LFSR_6	WD_LFSR_5	WD_LFSR_4	WD_LFSR_3	WD_LFSR_2	WD_LFSR_1	WD_LFSR_0

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 91. WD_LFSR description and configuration of the bits (default value in bold)

WD_LFSR_7:0	Description	WD 8 bits LFSR value. Used to write the seed at any time
	0...	bit7:bit0: 10110010 default value at start-up or after a power-on-reset: 0xB2[1], [2]
	1...	
	Reset condition	Power on reset

[1] Value Bit7:Bit0: 1111 1111 is prohibited.
[2] During a write command, MISO reports the previous register content.

13.4.9 WD_ANSWER

Table 92. WD_ANSWER register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	1	0	0	1	P	WD_ANSWER_7	WD_ANSWER_6	WD_ANSWER_5	WD_ANSWER_4	WD_ANSWER_3	WD_ANSWER_2	WD_ANSWER_1	WD_ANSWER_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	RSTB	FSxB	WD_BAD_DATA	FSO_G	IO_FS_G	WD_BAD_TIMING	ERR_INT_HW	ERR_INT_SW

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	RSTB	FSxB	WD_BAD_DATA	FSO_G	IO_FS_G	WD_BAD_TIMING	ER_INT_HW	ER_INT_SW

Table 93. WD_ANSWER description and configuration of the bits (default value in bold)

WD_ANSWER_7:0	Description	WD answer from the MCU
	0...	Answer = (NOT(((LFSR x 4)+6)–4))/4
	1...	
	Reset condition	Power on reset/RSTB low
RSTB	Description	Report a reset event
	0	**No reset**
	1	Reset occurred
	Reset condition	Power on reset/read
FSxB	Description	Report a fail-safe event
	0	No fail-safe
	1	**Fail-safe event occurred (default state at power up and after LPOFF as FS0B/FS1B are asserted low)**
	Reset condition	Power on reset/read
WD_BAD_DATA	Description	Report a watchdog data refresh error
	0	**WD data refresh OK**
	1	Wrong WD data refresh
	Reset condition	Power on reset/read

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 93. WD_ANSWER description and configuration of the bits (default value in bold) *...continued*

FSO_G[1]	Description	Report a fail-safe output failure
	0	**No failure**
	1	Failure
	Reset condition	Power on reset/read
IO_FS_G[2]	Description	Report an IO monitoring error
	0	**No error**
	1	Error detected
	Reset condition	Power on reset/read
WD_BAD_TIMING	Description	Report a watchdog timing refresh error
	0	**WD timing refresh OK**
	1	Wrong WD timing refresh
	Reset condition	Power on reset/read
ERR_INT_HW	Description	Report an error from an internal redundant structure of the fail-safe state machine
	0	**No error**
	1	Error detected
	Reset condition	Power on reset/read
ERR_INT_SW	Description	Report an error from the EDC of the fail-safe state machine (error detection correction)
	0	**No error**
	1	Error detected
	Reset condition	Power on reset/read

[1] **FSO_G** = RSTB_short_high or FS0B_short_high or FS0B_short_low or FS1B_short_high or FS1B_short_low
[2] **IO_FS_G** = IO_23_fail or IO_45_fail

Values of the two registers WD_COUNTER and DIAG_SF_ERR are updated at the end of any SPI access to one of the three registers WD_ANSWER, WD_COUNTER, and DIAG_SF_ERR. To always get up to date values, it is recommended to make two consecutive SPI accesses to WD_COUNTER and DIAG_SF_ERR registers or access (read or write) WD_ANSWER register first.

Example1: read or write WD_ANSWER to update the registers, read WD_COUNTER and DIAG_SF_ERR to report the latest information

Example2: read WD_COUNTER to update the register, read again WD_COUNTER to report the latest information

13.4.10 RELEASE_FSxB

Table 94. RELEASE_FSxB register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	1	0	1	0	P	RELEASE_FSxB_7	RELEASE_FSxB_6	RELEASE_FSxB_5	RELEASE_FSxB_4	RELEASE_FSxB_3	RELEASE_FSxB_2	RELEASE_FSxB_1	RELEASE_FSxB_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	RESERVED	FS1B_SNS	FS0B_SNS	RSTB_SNS

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	RESERVED	FS1B_SNS	FS0B_SNS	RSTB_SNS

Table 95. RELEASE_FSxB description and configuration of the bits (default value in bold)

RELEASE_FSxB_7:0	Description	Secured 8 bits word to release the FS0B and FS1B pins
	0...	Depends on LFSR_out value and calculation
	1...	
	Reset condition	Power on reset -> default = 00h
FS1B_SNS	Description	Sense of FS1B pad
	0	**FS1B pad sense low**
	1	FS1B pad sense high
	Reset condition	Power on reset
FS0B_SNS	Description	Sense of FS0B pad
	0	**FS0B pad sense low**
	1	FS0B pad sense high
	Reset condition	Power on reset
RSTB_SNS	Description	Sense of RSTB pad
	0	RSTB pad sense low
	1	**RSTB pad sense high**
	Reset condition	Power on reset

13.4.11 SF_OUTPUT_REQUEST

Table 96. SF_OUTPUT_REQUEST register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	1	0	1	1	P	FS1B_REQ	FS1B_DLY_REQ	FS0B_REQ	RSTB_REQ	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	FS1B_DRV	FS1B_DLY_DRV	FS0B_DRV	RSTB_DRV

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	FS1B_DRV	FS1B_DLY_DRV	FS0B_DRV	RSTB_DRV

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 97. SF_OUTPUT_REQUEST description and configuration of the bits (default value in bold)

FS1B_REQ	Description	Request FS1B to be asserted low
	0	**No request**
	1	Request FS1B assertion with immediate assertion, no delay
	Reset condition	Power on reset
FS1B_DLY_REQ	Description	Request activation of FS1B internal pull-up (open/close switch S1)
	0	Close S1
	1	**Open S1**
	Reset condition	Power on reset
FS0B_REQ	Description	Request FS0B to be asserted low
	0	**No request**
	1	Request FS0B assertion
	Reset condition	Power On reset
RSTB_REQ	Description	Request a RSTB low pulse
	0	**No request**
	1	Request a RSTB low pulse
	Reset condition	Power on reset
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6
FS1B_DRV	Description	Sense of FS1B driver command from fail-safe logic (digital)
	0	**FS1B digital driver sense low**
	1	FS1B digital driver sense high
	Reset condition	Power on reset
FS1B_DLY_DRV	Description	Sense of FS1B driver command from internal pull-up (analog)
	0	FS1B analog driver sense low
	1	FS1B analog driver sense high
	Reset condition	Power on reset
FS0B_DRV	Description	Sense of FS0B driver command from fail-safe logic
	0	**FS0B driver sense low**
	1	FS0B driver sense high
	Reset condition	Power on reset
RSTB_DRV	Description	Sense of RSTB driver command from fail-safe logic
	0	RSTB driver sense low
	1	**RSTB driver sense high**
	Reset condition	Power on reset

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

13.4.12 INIT_WD_CNT

Table 98. INIT_WD_CNT register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	1	1	0	0	P	WD_CNT_ERR_1	WD_CNT_ERR_0	WD_CNT_RFR_1	WD_CNT_RFR_0	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	WD_CNT_ERR_1	WD_CNT_ERR_0	WD_CNT_RFR_1	WD_CNT_RFR_0

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	WD_CNT_ERR_1	WD_CNT_ERR_0	WD_CNT_RFR_1	WD_CNT_RFR_0

Table 99. INIT_WD_CNT description and configuration of the bits (default value in bold)

WD_CNT_ERR_1:0	Description	Configure the maximum value of the WD error counter
	00	**6**
	01	6
	10	4
	11	2
	Reset condition	Power on reset
WD_CNT_RFR_1:0	Description	Configure the maximum value of the WD refresh counter
	00	**6**
	01	4
	10	2
	11	1
	Reset condition	Power on reset
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6

13.4.13 DIAG_SF_IOs

Table 100. DIAG_SF_IOs register description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	RSTB_EXT	RSTB_DIAG	FS0B_DIAG_1	FS0B_DIAG_0	FS1B_DIAG_1	FS1B_DIAG_0	IO_23_FAIL	Io_45_FAIL

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 101. DIAG_SF_IOs description and configuration of the bits (default value in bold)

RSTB_EXT	Description	Report an external RSTB
	0	**No external RSTB**
	1	External RSTB
	Reset condition	Power on reset/read
RSTB_DIAG	Description	Report a RSTB short-circuit to high
	0	**No Failure**
	1	Short-circuit high
	Reset condition	Power on reset/read
FS0B_DIAG_1:0	Description	Report a failure on FS0B
	00	**No Failure**
	01	Short-circuit low/open load
	1X	Short-circuit high
	Reset condition	Power on reset/read
FS1B_DIAG_1:0	Description	Report a failure on FS1B
	00	**No Failure**
	01	Short-circuit low/open load
	1X	Short-circuit high
	Reset condition	Power on reset/read
IO_23_FAIL	Description	Report an error in the FCCU protocol
	0	**No error**
	1	Error detected
	Reset condition	Power on reset/read
IO_45_FAIL	Description	Report an error in the IO_45 protocol
	0	**No error**
	1	Error detected
	Reset condition	Power on reset/read

13.4.14 WD_COUNTER

Table 102. WD_COUNTER register description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	WD_ERR_2	WD_ERR_1	WD_ERR_0	RESERVED	WD_RFR_2	WD_RFR_1	WD_RFR_0	RESERVED

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 103. WD_COUNTER description and configuration of the bits (default value in bold)

WD_ERR_2:0	Description	Report the value of the watchdog error counter
	000	From 0 to 5 (6 generate an increase of the FLT_ERR_CNT and this counter is reset to 0)
	to 110	
	Reset condition	Power on reset
WD_RFR_2:0	Description	Report the value of the watchdog refresh counter
	000	From 0 to 6 (7 generate a decrease of the FLT_ERR_CNT and this counter is reset to 0)
	to 111	
	Reset condition	Power on reset

13.4.15 DIAG_SF_ERR

Table 104. DIAG_SF_ERR register description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	FLT_ERR_2	FLT_ERR_1	FLT_ERR_0	RESERVED	V2P5_M_A_OV	V2P5_M_D_OV	FCRBM_OV	FCRBM_UV

Table 105. DIAG_SF_ERR description and configuration of the bits (default value in bold)

FLT_ERR_2:0	Description	Report the value of the fault error counter
	000 001 … 110	Error counter is set to 1 by default
	Reset condition	Power on reset
V2P5_M_A_OV	Description	Report an overvoltage on V2P5 main analog regulator
	0	**No overvoltage ($V_{2P5_M_A} < V_{2P5_M_A_OV}$)**
	1	Overvoltage detected ($V_{2P5_M_A} > V_{2P5_M_A_OV}$)
	Reset condition	Power on reset/read
V2P5_M_D_OV	Description	Report an overvoltage on V2P5 main digital regulator
	0	**No overvoltage ($V_{2P5_M_D} < V_{2P5_M_D_OV}$)**
	1	Overvoltage detected ($V_{2P5_M_D} > V_{2P5_M_D_OV}$)
	Reset condition	Power on reset/read
FCRBM_OV	Description	Report an overvoltage on FCRBM
	0	**No overvoltage (FB_Core – FCRBM < 150 mV)**
	1	Overvoltage detected (FB_Core – FCRBM > 150 mV)
	Reset condition	Power on reset/read

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 105. DIAG_SF_ERR description and configuration of the bits (default value in bold)*...continued*

FCRBM_UV	Description	Report an undervoltage on FCRBM
	0	**No undervoltage (FB_Core – FCRBM > –150 mV)**
	1	Undervoltage detected (FB_Core – FCRBM < –150 mV)
	Reset condition	Power on reset/read

13.4.16 INIT_VCORE_OVUV_IMPACT

Table 106. INIT_VCORE_OVUV_IMPACT register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	1	0	0	0	1	P	VCORE_ FS_OV_1	VCORE_ FS_OV_0	VCORE_ FS_UV_1	VCORE_ FS_UV_0	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE _G	VCORE _G	VOTHERS_ G	SPI_FS_ ERR	SPI_FS_ CLK	SPI_FS_ REQ	SPI_FS_ PARITY	VCORE_ FS_OV_1	VCORE_ FS_OV_0	VCORE_ FS_UV_1	VCORE_ FS_UV_0

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE _G	VCORE _G	VOTHERS_ G	SPI_FS_ ERR	SPI_FS_ CLK	SPI_FS_ REQ	SPI_FS_ PARITY	VCORE_ FS_OV_1	VCORE_ FS_OV_0	VCORE_ FS_UV_1	VCORE_ FS_UV_0

Table 107. INIT_VCORE_OVUV_IMPACT description and configuration of the bits (default value in bold)

VCORE_FS_OV_1:0	Description	V_{CORE_FB} overvoltage safety impact
	00	No effect of $V_{CORE_FB_OV}$ on RSTB and FS0B
	01	$V_{CORE_FB_OV}$ does have an impact on RSTB only
	10	$V_{CORE_FB_OV}$ does have an impact on FS0B only
	11	**V**$_{CORE_FB_OV}$ does have an impact on RSTB and FS0B
	Reset condition	Power on reset
VCORE_FS_UV_1:0	Description	V_{CORE_FB} undervoltage safety impact
	00	No effect of $V_{CORE_FB_UV}$ on RSTB and FS0B
	01	$V_{CORE_FB_UV}$ does have an impact on RSTB only
	10	**V**$_{CORE_FB_UV}$ does have an impact on FS0B only
	11	$V_{CORE_FB_UV}$ does have an impact on RSTB and FS0B
	Reset condition	Power on reset
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

13.4.17 INIT_VCCA_OVUV_IMPACT

Table 108. INIT_VCCA_OVUV_IMPACT register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	1	0	0	1	0	P	VCCA_FS_OV_1	VCCA_FS_OV_0	VCCA_FS_UV_1	VCCA_FS_UV_0	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	VCCA_FS_OV_1	VCCA_FS_OV_0	VCCA_FS_UV_1	VCCA_FS_UV_0

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	VCCA_FS_OV_1	VCCA_FS_OV_0	VCCA_FS_UV_1	VCCA_FS_UV_0

Table 109. INIT_VCCA_OVUV_IMPACT description and configuration of the bits (default value in bold)

VCCA_FS_OV_1:0	Description	V_{CCA} overvoltage safety impact
	00	No effect of V_{CCA_OV} on RSTB and FS0B
	01	V_{CCA_OV} does have an impact on RSTB only
	10	V_{CCA_OV} does have an impact on FS0B only
	11	**V_{CCA_OV}** does have an impact on RSTB and FS0B
	Reset Condition	Power on reset
VCCA_FS_UV_1:0	Description	V_{CCA} undervoltage safety impact
	00	No effect of V_{CCA_UV} on RSTB and FS0B
	01	V_{CCA_UV} does have an impact on RSTB only
	10	**V_{CCA_UV}** does have an impact on FS0B only
	11	V_{CCA_UV} does have an impact on RSTB and FS0B
	Reset Condition	Power on reset
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6

13.4.18 INIT_VAUX_OVUV_IMPACT

Table 110. INIT_VAUX_OVUV_IMPACT register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	1	0	0	1	1	P	VAUX_FS_OV_1	VAUX_FS_OV_0	VAUX_FS_UV_1	VAUX_FS_UV_0	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	VAUX_FS_OV_1	VAUX_FS_OV_0	VAUX_FS_UV_1	VAUX_FS_UV_0

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERSG	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	VAUX_FS_OV_1	VAUX_FS_OV_0	VAUX_FS_UV_1	VAUX_FS_UV_0

Table 111. INIT_VAUX_OVUV_IMPACT description and configuration of the bits (default value in bold)

VAUX_FS_OV_1:0	Description	V_{AUX} overvoltage safety impact
	00	No effect of V_{AUX_OV} on RSTB and FS0B
	01	V_{AUX_OV} does have an impact on RSTB only
	10	V_{AUX_OV} does have an impact on FS0B only
	11	**V**$_{AUX_OV}$ does have an impact on RSTB and FS0B
	Reset condition	Power on reset
VAUX_FS_UV_1:0	Description	V_{AUX} undervoltage safety impact
	00	No effect of V_{AUX_UV} on RSTB and FS0B
	01	V_{AUX_UV} does have an impact on RSTB only
	10	**V**$_{AUX_UV}$ does have an impact on FS0B only
	11	V_{AUX_UV} does have an impact on RSTB and FS0B
	Reset condition	Power on reset
Secure3:0	Description	Secured bits based on write bits
		Secured_3 = NOT(bit5) Secured_2 = NOT(bit4) Secured_1 = bit7 Secured_0 = bit6

13.4.19 DEVICE_ID_FS

Table 112. DEVICE_ID_FS register description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERSG	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	DFS_HW2	FS1

Table 113. DEVICE_ID_FS description and configuration of the bits (default value in bold)

DFS_HW2	Description	Report the deep fail-safe hardware configuration (fail-safe logic)
	0	Deep fail-safe disable
	1	Deep fail-safe enable
	Reset condition	Power on reset

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 113. DEVICE_ID_FS description and configuration of the bits (default value in bold)*...continued*

FS1	Description	Report the FS1B function availability (depends on part number)
	0	Disabled
	1	Enabled
	Reset condition	Power on reset

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

14 List of interruptions and description

The INTB output pin generates a low pulse when an Interrupt condition occurs. The INTB behavior as well as the pulse duration are set through the SPI during INIT phase. It is possible to mask some Interruption source (see Section 13.3).

Table 114. Interruptions list

Event	Description
V_{SNS_UV}	Detection of $V_{BATTERY}$ below 8.5 V
$V_{SUP_UV_7}$	Detection of V_{SUP} below 7.0 V (after reverse current protection diode)
I_{PFF}	Input power feed forward. Based on V_{SUP} and I_{PRE_PEAK}
I_{LIM_PRE}	Pre-regulator current limitation
T_{WARN_PRE}	Temperature warning on the pass transistor
BoB	Return the running state of V_{PRE} converter (buck or boost mode)
V_{PRE_STATE} ($V_{PRE_SMPS_EN}$)	Return the activation state of V_{PRE} DC-DC converter
V_{PRE} OV	Report a V_{PRE} overvoltage detection
V_{PRE} UV	Report a V_{PRE} undervoltage detection
T_{WARN_CORE}	Temperature warning on the pass transistor
V_{CORE_STATE} ($V_{CORE_SMPS_EN}$)	Return the activation state of V_{CORE} DC-DC converter
V_{CORE} OV	Report a V_{CORE} overvoltage detection
V_{CORE} UV	Report a V_{CORE} undervoltage detection
I_{LIM_CCA}	V_{CCA} current limitation
$I_{LIM_CCA_OFF}$	Current limitation maximum duration expiration. Only used when external PNP connected.
T_{WARN_CCA}	Temperature warning on the pass transistor (internal pass transistor only)
TSD_{VCCA}	Temperature shutdown of the VCCA
V_{CCA} OV	Report a V_{CCA} overvoltage detection
V_{CCA} UV	Report a V_{CCA} undervoltage detection
I_{LIM_AUX}	V_{AUX} current limitation
$I_{LIM_AUX_OFF}$	Current limitation maximum duration expiration. Only used when external PNP connected.
TSD_{VAUX}	Temperature shutdown of the VAUX
V_{AUX} OV	Report a V_{AUX} overvoltage detection
V_{AUX} UV	Report a V_{AUX} undervoltage detection
I_{LIM_CAN}	V_{CAN} current limitation
V_{CAN} OV	Report a V_{CAN} overvoltage detection
TSD_{CAN}	Temperature shutdown on the pass transistor. Auto restart when $T_J < (TSD_{CAN} - TSD_{CAN_HYST})$.
V_{CAN} UV	Report a V_{CAN} undervoltage detection
IO_0	Report IO_0 digital state change
IO_2	Report IO_2 digital state change

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 114. Interruptions list*...continued*

Event	Description
IO_3	Report IO_3 digital state change
IO_4	Report IO_4 digital state change
IO_5	Report IO_5 digital state change
IO_0_WU	Report IO_0 wake-up event
IO_2_WU	Report IO_2 wake-up event
IO_3_WU	Report IO_3 wake-up event
IO_4_WU	Report IO_4 wake-up event
IO_5_WU	Report IO_5 wake-up event
CAN_WU	Report a CAN wake-up event
CAN_OT	CAN overtemperature detection
RXD_REC	CAN RXD recessive clamping detection (short-circuit to 5.0 V)
TXD_DOM	CAN TXD dominant clamping detection (short-circuit to GND)
CAN_DOM	CAN-bus dominant clamping detection
LIN_WU	Report a LIN wake-up event
LIN_OT	LIN overtemperature detection
RXDL_REC	LIN RXDL recessive clamping detection (short to high)
TXDL_DOM	LIN TXDL dominant clamping detection (short to GND)
LIN_DOM	LIN bus dominant clamping detection
INT_REQ	MCU request for an interrupt pulse
LDT_F1	Long duration timer configured in function 1 and after run value is reach
SPI_ERR	Secured SPI communication check
SPI_CLK	Report a wrong number of CLK pulse different than 16 during the NCS low pulse in main state machine
SPI_REQ	Invalid SPI access (wrong write or read, write to INIT registers in normal mode, wrong address)
SPI_PARITY	Report a parity error in main state machine

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

15 Typical applications

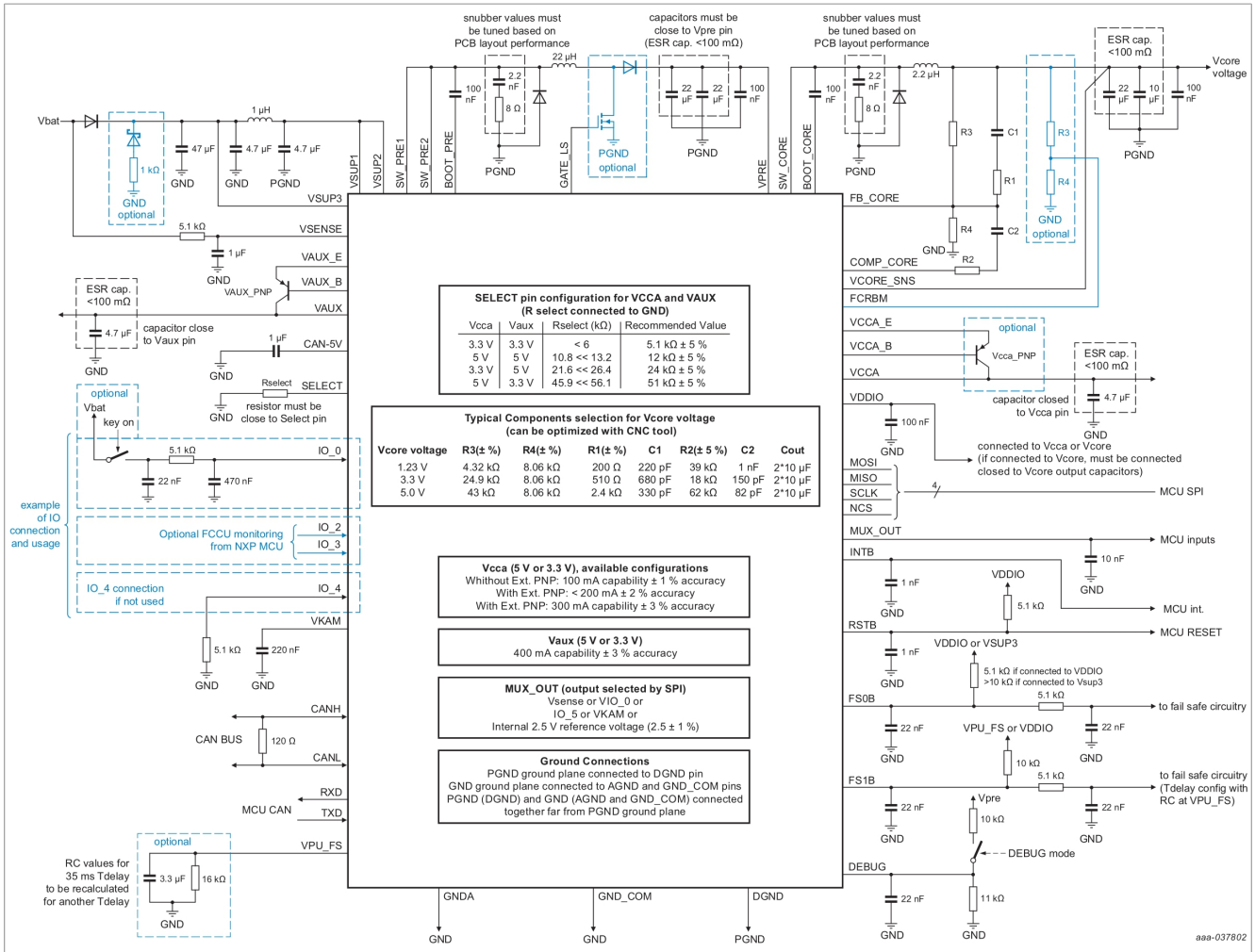


Figure 73. FS6500 simplified application schematic with CAN, FS1B, VKAM, buck/boost V_{PRE} configuration

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

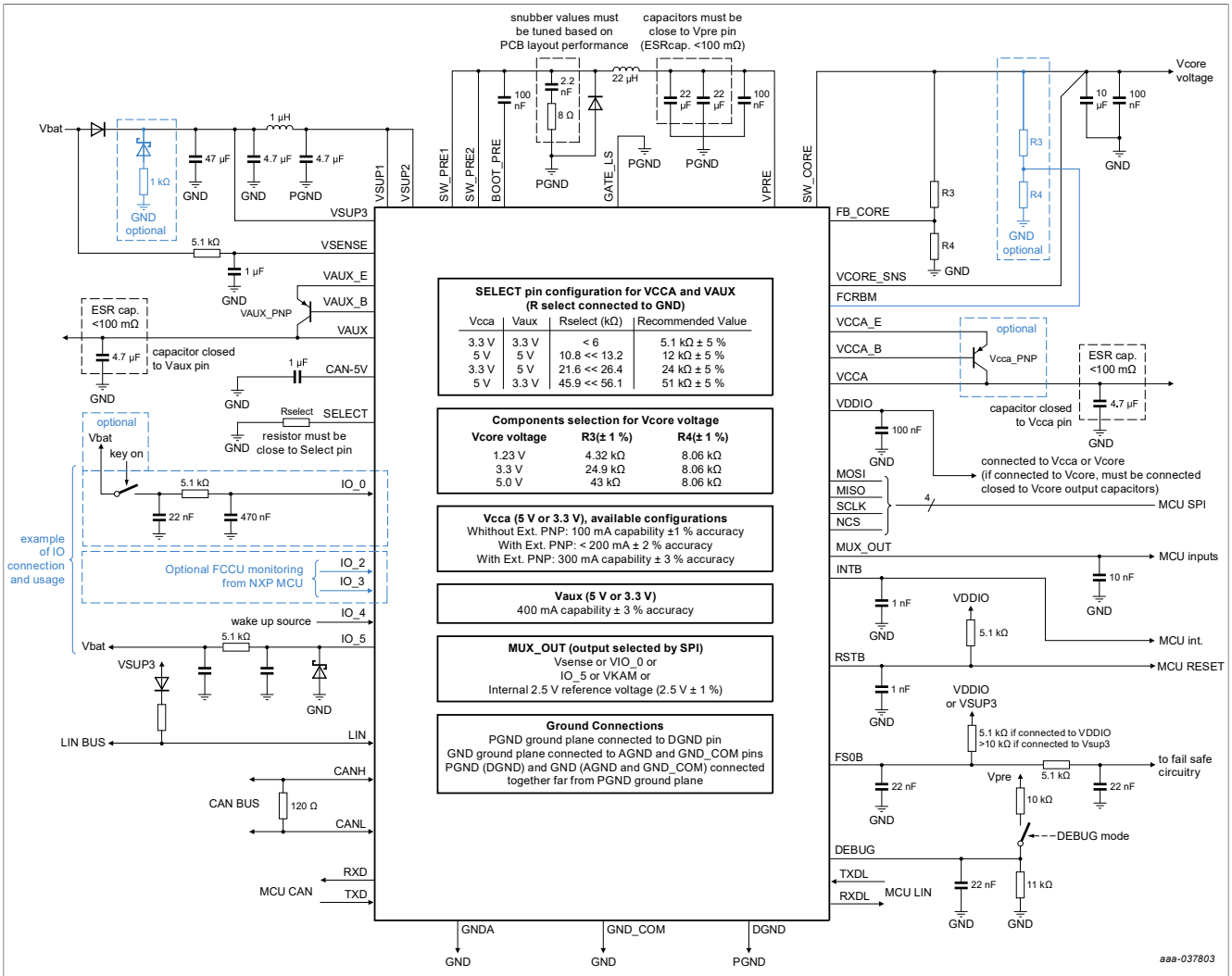


Figure 74. F4500 simplified application schematic with CAN, LIN, IO_5, buck only V_{PRE} configuration

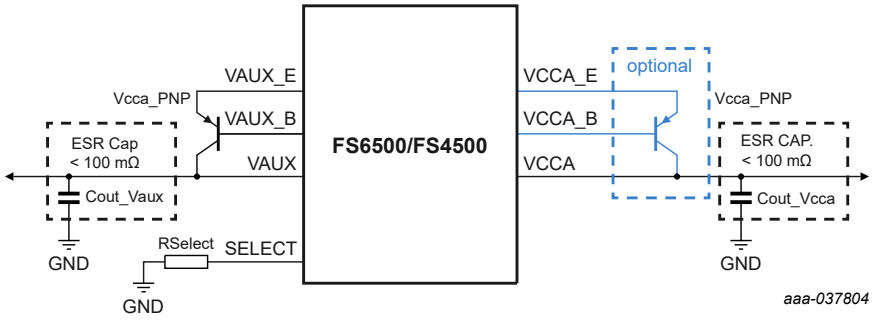


Figure 75. V_{AUX}/V_{CCA} connection, deep fail-safe enabled

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

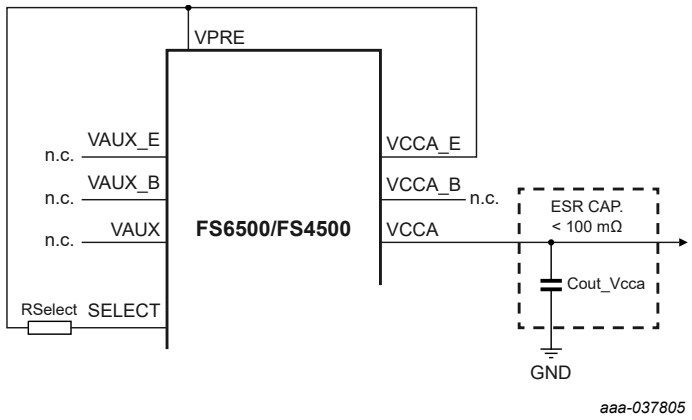


Figure 76. V_{AUX} not used, V_{CCA} configuration up to 100 mA, deep fail-safe disabled

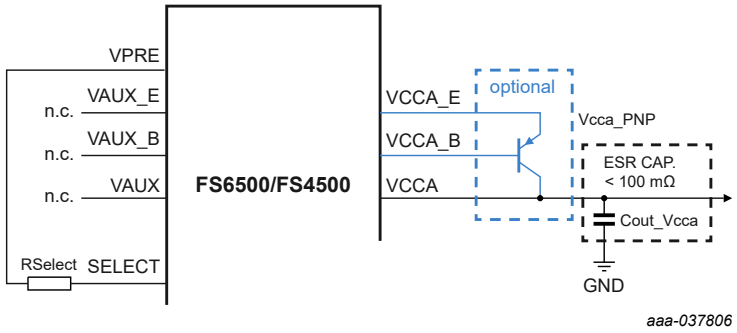


Figure 77. V_{CCA} connection, V_{AUX} not used, deep fail-safe disabled

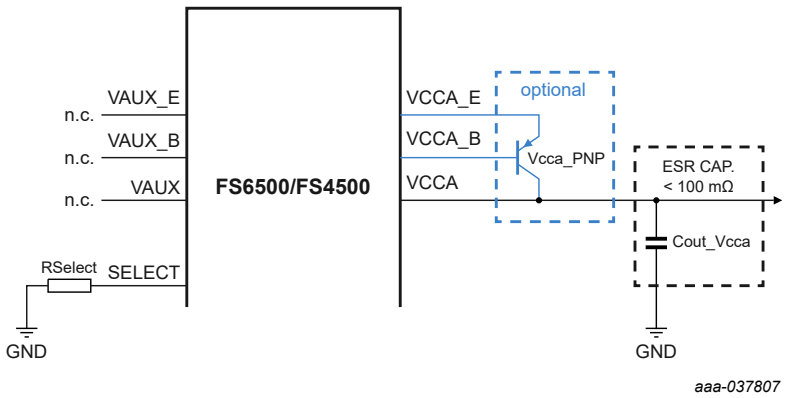


Figure 78. V_{CCA} connection, V_{AUX} not used, deep fail-safe enabled

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

16 Packaging

16.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

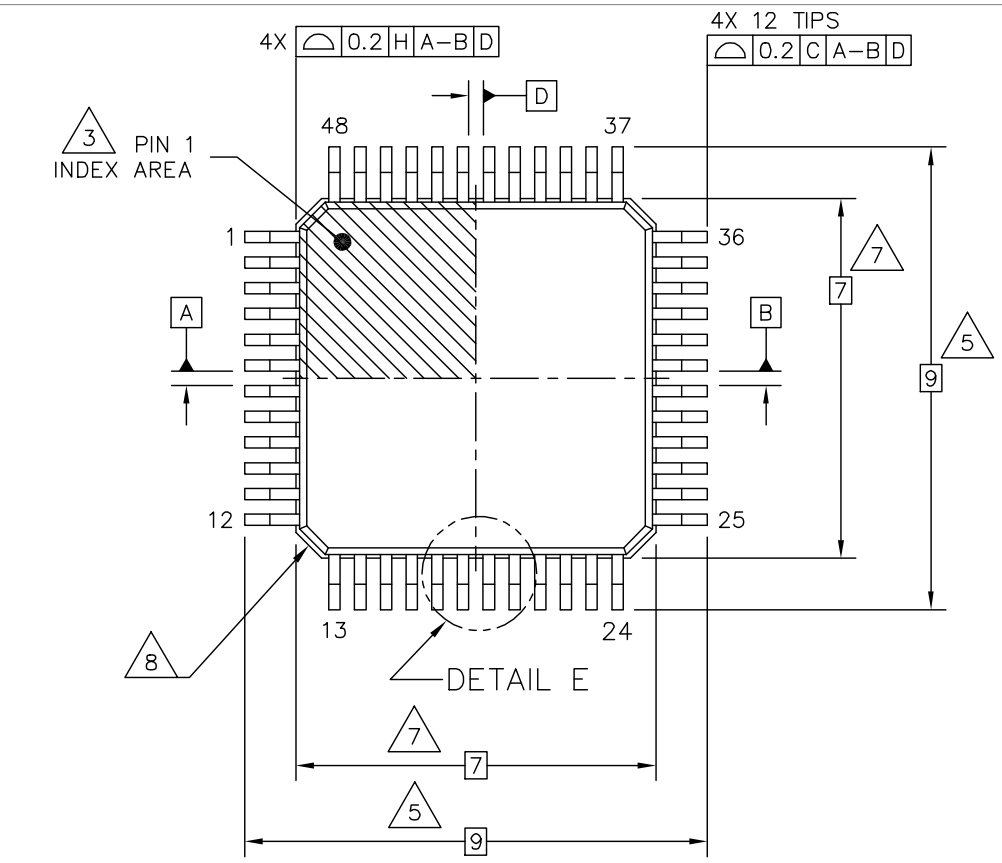
Table 115. Package mechanical dimensions

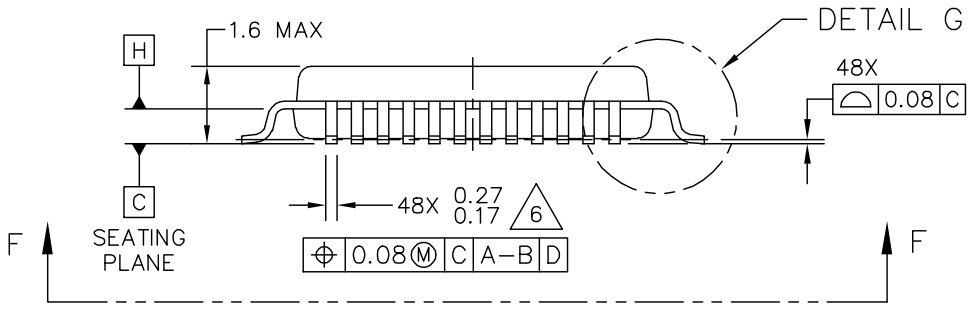
Package	Suffix	Package outline drawing number
7.0 × 7.0, 48–Pin LQFP exposed pad, with 0.5 mm pitch, and a 4.5 × 4.5 exposed pad	AE	98ASA00173D

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

16.2 Package outline





© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED

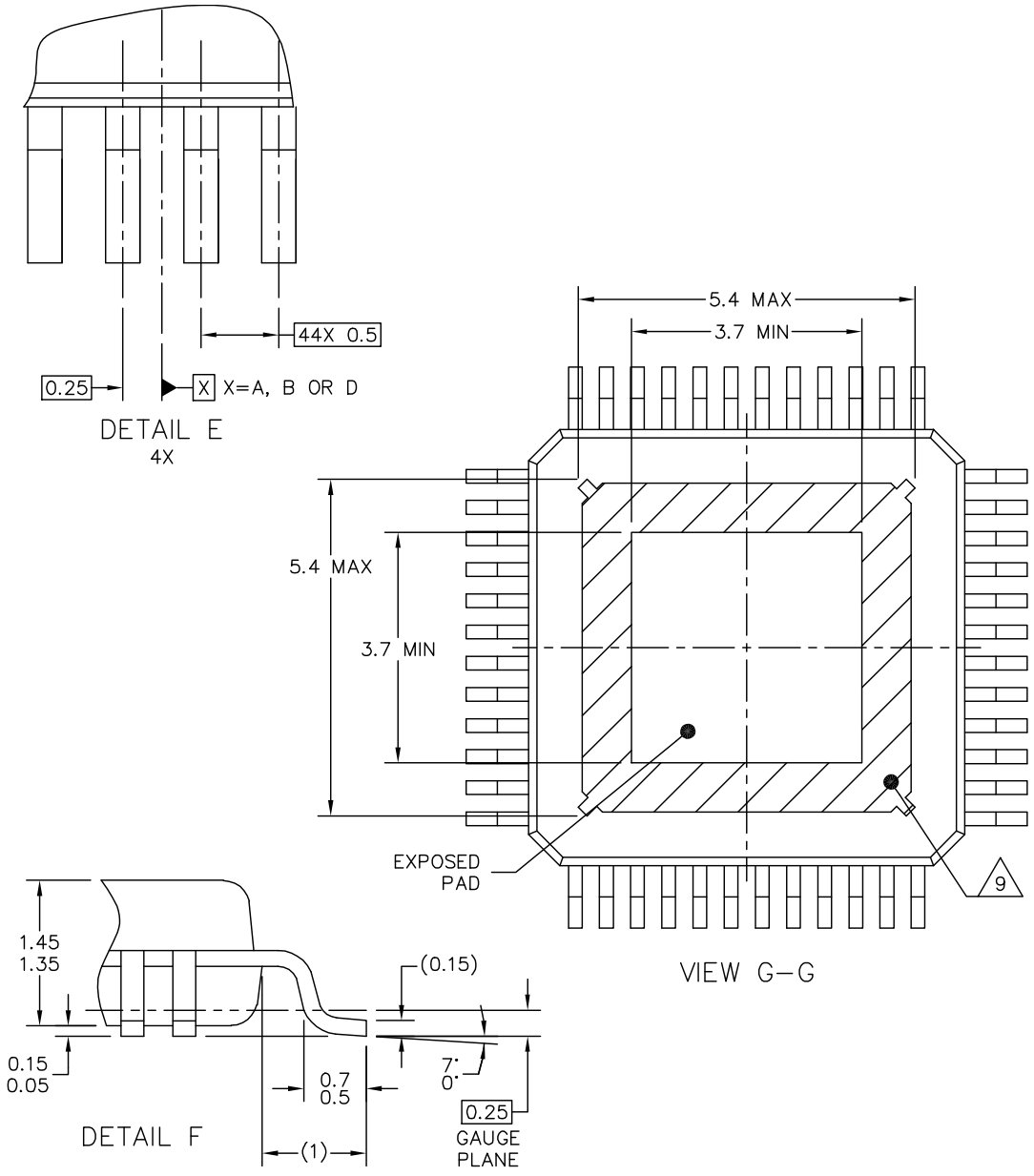
DATE: 14 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: JEDEC MS–026 BBC	DRAWING NUMBER: SOT1571–1	REVISION: F	

Figure 79. SOT1571-1 Rev F

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.



© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED DATE: 14 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: JEDEC MS–026 BBC	DRAWING NUMBER: SOT1571–1	REVISION: F	

Figure 80. SOT1571-1 Rev. F Detail View

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

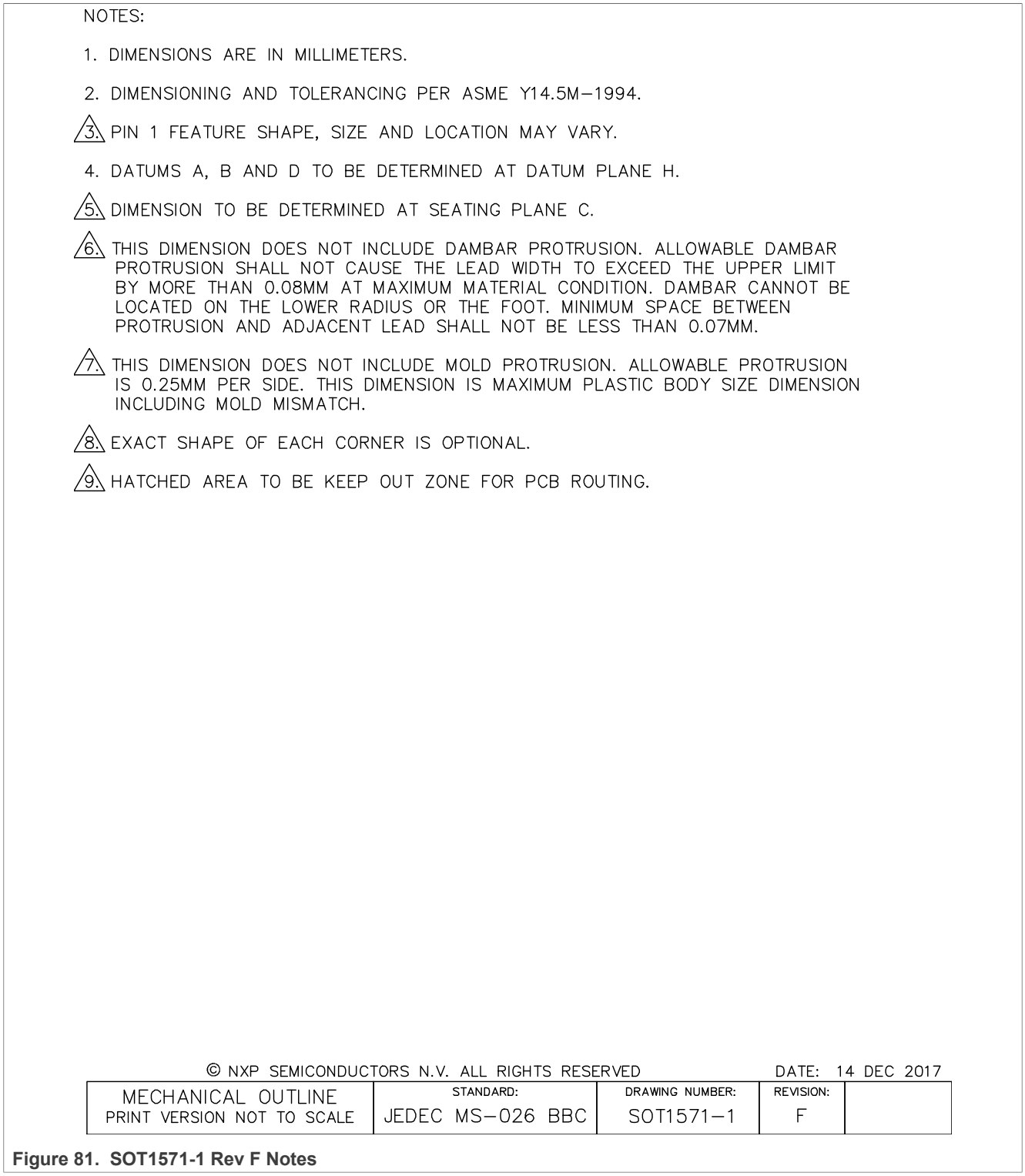
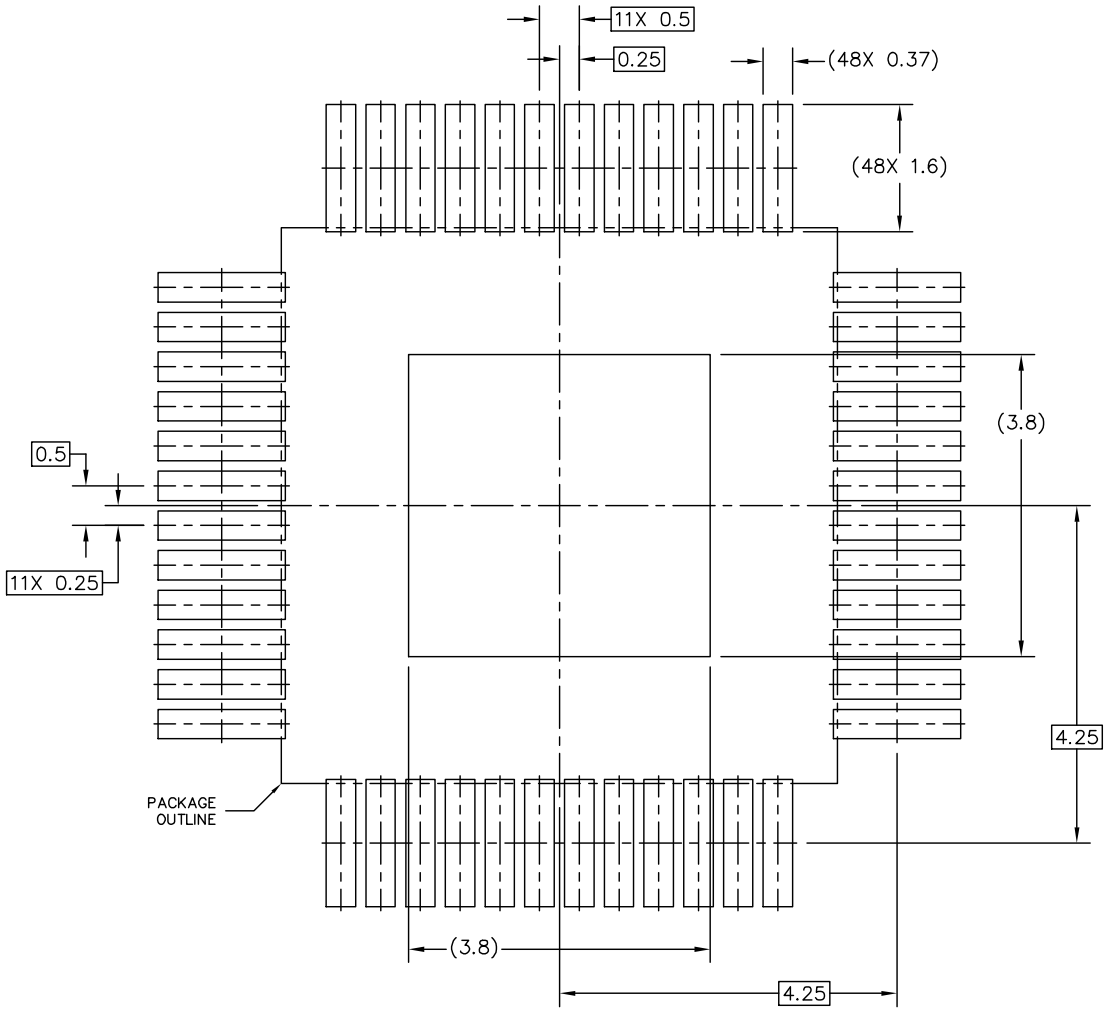


Figure 81. SOT1571-1 Rev F Notes

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

17 Soldering



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

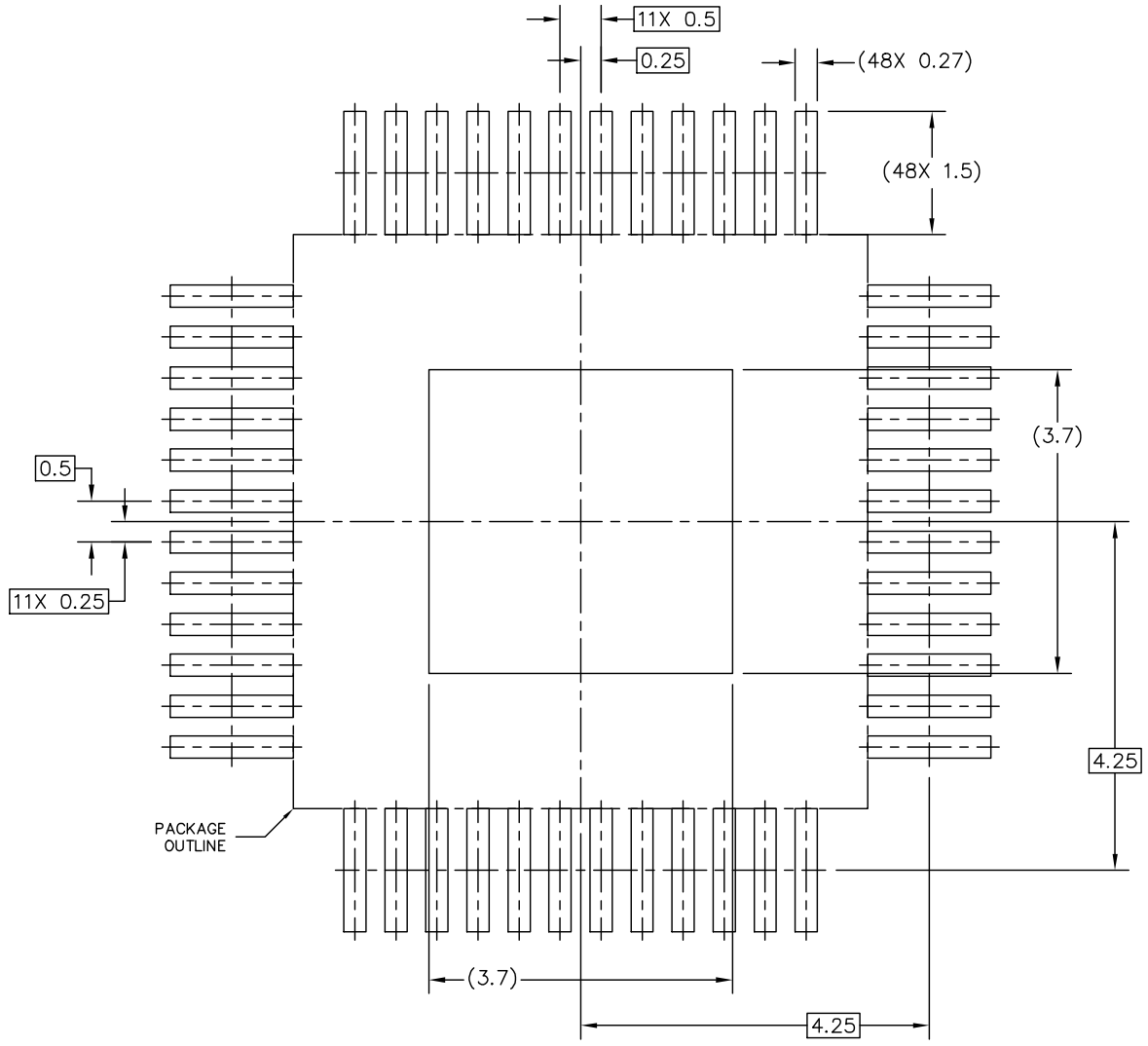
© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED DATE: 14 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: JEDEC MS–026 BBC	DRAWING NUMBER: SOT1571–1	REVISION: F	

Figure 82. SOT1571-1 Rev. F - PCB design guidelines - solder mask opening pattern

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

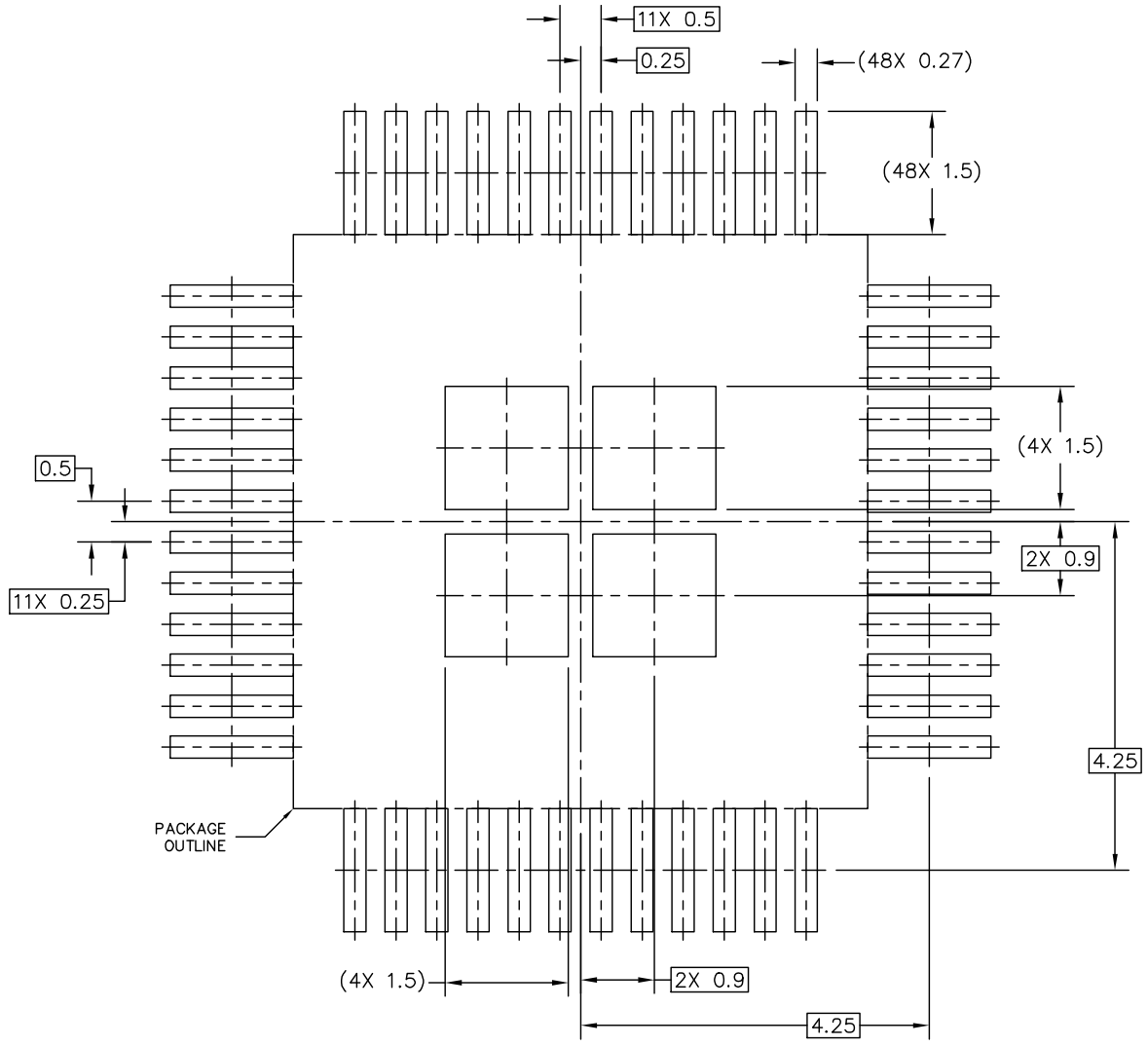
© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED DATE: 14 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: JEDEC MS–026 BBC	DRAWING NUMBER: SOT1571–1	REVISION: F	

Figure 83. SOT1571-1 Rev. F - PCB design guidelines - I/O pads and solderable area

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.



STENCIL THICKNESS 0.125 OR 0.150

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED DATE: 14 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: JEDEC MS–026 BBC	DRAWING NUMBER: SOT1571–1	REVISION: F	

Figure 84. SOT1571-1 Rev. F - PCB design guidelines - solder paste stencil

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

18 References

Obtain additional information on related NXP products and application solutions through the documents and URLs listed below.

(1) **AN5238** - FS6500 and FS4500 Safe System Basis Chip Hardware Design and Product Guidelines - Application Note
https://www.nxp.com/AN5238-DOWNLOAD

(2) **AN4388** - Quad Flat Package (QFP)
Requires NXP login

(3) **FS6500-FS4500PDTCALC** - Power dissipation tool (Excel File)
Requires NXP login

(4) **V_{CORE} compensation network simulation tool (CNC)**[1]

(5) **FMEDA** - FS6500/FS4500 FMEDA[1]

(6) **FS6500-FS4500SMUG** - FS6500/FS4500 Safety manual – user guide
https://www.docstore.nxp.com/products/product-hierarchy?query=Sm5509

(7) **KITFS6507LAEEVM** - FS6507, System Basis Chip, ASIL B, DC-DC 0.8 A Vcore, LDT, CAN, LIN
https://www.nxp.com/KITFS6507LAEEVM

(8) **KITFS4508CAEEVM** - FS4508, System Basis Chip, ASIL B, Linear 0.5 A Vcore, FS1b, LDT, CAN
https://www.nxp.com/KITFS4508CAEEVM

(9) **FS6500 product summary page** -
https://www.nxp.com/FS6500

(10) **FS4500 product summary page** -
https://www.nxp.com/FS4500

(11) **Analog power management homepage** -
https://www.nxp.com/products/power-management

(12) **ISO 11898-2:2003** - Road vehicles — Controller area network (CAN) — Part 2: High-speed medium access unit
https://www.iso.org/standard/33423.html

(13) **ISO 11898-5:2007** - Road vehicles — Controller area network (CAN) — Part 5: High-speed medium access unit with low-power mode
https://www.iso.org/contents/data/standard/04/12/41284.html

(14) **ISO 7637-2:2011** - Road vehicles — Electrical disturbances from conduction and coupling — Part 2: Electrical transient conduction along supply lines only
https://www.iso.org/standard/50925.html

(15) **ISO 10605:2008** - Road vehicles — Test methods for electrical disturbances from electrostatic discharge
https://www.iso.org/standard/41937.html

(16) **IEC 61000-4-2:2008** - Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test
https://webstore.iec.ch/publication/4189

(17) **JESD51- 6** - INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - FORCED CON VECTION (MOVING AIR)

(18) **JESD51-7** - HIGH EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD FOR LEADED SURFACE MOUNT PAC KAGES

(19) **JESD22-A114F** - ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING HUMAN BODY MODEL (HBM)

(20) **JESD22-C101F** - FIELD-INDUCED CHARGED-DEVICE MODEL TEST METHOD FOR ELECTROSTATIC DIS CHARGE WITHSTAND THRESHOLDS OF MICROELECTRONIC COMPONENTS

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

(21) **MIL-STD-883-1, Method 1012.1** - TEST METHOD STANDARD MICROCIRCUITS

(22) **LIN Specification Package Revision 2.1:2006**
https://www.lin-cia.org/fileadmin/microsites/lin-cia.org/resources/documents/LIN-Spec_Pac2_1.pdf

(23) **LIN Specification Package Revision 2.2A:2010**
https://www.lin-cia.org/fileadmin/microsites/lin-cia.org/resources/documents/LIN_2.2A.pdf

(24) **SAE J2602-2:201211 - LIN Network for Vehicle Applications Conformance Test**
https://www.sae.org/standards/content/j2602/2_201211/

[1] Available upon request.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

19 Revision history

Table 117. Revision history

Document ID	Release date	Description
FS6500-FS4500-ASILD v. 9.0	15 July 2026	• CIN# 202605006I • Product data sheet • Revised Section 5.1 *Part number definition*, to capture the different part number strategies for backend manufacturing flows: China (AE suffix) or Malaysia (KE suffix). • Revised Table 2 • Revised Section 18 • Updated Legal information
FS6500-FS4500-ASILD v.8	05 August 2024	• Product data sheet • CIN 202407025I • Supercedes FS6500-FS4500 v.7.0 • Updated status from confidential to public • Updated document title from "FS6500, FS4500" to "FS6500-FS4500-ASILD" • Updated Revision history to reflect new NXP standard • Section 11.6: changed "(±1.0 % for 5.0 V configuration and ±1.5 % for 3.3 V configuration)," to (±1.0 % for 5.0 V and 3.3 V configuration)," in the second paragraph. • Section 12.7.4: changed last sentence of first paragraph from "The voltage accuracy is ±1.0 % for 5.0 V configuration and ±1.5 % for 3.3 V configuration ..." to "The voltage accuracy is ±1.0 % for 5.0 V and 3.3 V configuration ..." • Changed "master" to "primary" and "slave" to "secondary" throughout, except for LIN topics Section 9 and Section 11.12.3, where "master" was changed to "commander" and "slave" to "responder" • Revised Figure 4 • In Section 12.1.7.2, revised parameter name • In Section 12.5.2.5, changed INIT_WD to INIT_WD_CNT • Revised Section 12.5.3 • Added Section 12.8.2 • Updated Figure 16 • Revised Figure 17 • Revised Figure 64 • Revised Section 13.1.2 • In Section 13.1.4, • Corrected Figure 72 • Updated description of bit field DEV_REV_2:0 in Table 39 • Revised Figure 73 • Updated Legal information

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 117. Revision history...*continued*

Document ID	Release date	Description
FS6500-FS4500 v.7.0	11 November 2020	• Product data sheet • Updated as per CIN 202011012I • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors, N.V. Legal texts have been adapted to the new company name where appropriate. • Changed product status from "Advance information" to "Product data sheet". • Global: Performed minor grammar, punctuation, and typographical changes throughout the document. • Revised all images in Figures 1 through 78. • Section 1, added new paragraph beginning with "High temperature capability.…" • Section 8, Table 4, added footnote on $V_{ESD_HB!1}$, "Compared to AGND." • Section 9, Table 5, revised as follows: – V_{DRIVER_DOM}, V_{BUS_DOM} and V_{HYST}: added multiplication operand between the coefficient and V_{SUP} in the Max column. – V_{BUS_REC}: added multiplication operand between the coefficient and V_{SUP} in the Min column. – V_{BUS_WU} V_{BUS_CNT}: added multiplication operand between the coefficient and V_{SUP} in the Min and Max columns. • Section 12.5.7.1, revised the second paragraph • Section 12.8.1, Added table title "Long duration timer characteristics" to Table 13. • Section 16.2, updated the package outline images and created separate figures for each drawing in Figure 79, Figure 80, and Figure 81 • Section 17, added new Soldering section and Figure 82, Figure 83, and Figure 84. • Section 18, Updated reference to FS6500-FS4500SMUG - FS6500/FS4500 Safety Manual – user guide and added industry standard documents referenced in the narrative.
FS6500-FS4500 v.6.0	October 2017	• Advance Information • Updated as per CIN 201709027I • Updated pinout diagrams (Figure 5, Figure 6, Figure 7, and Figure 8) • Reduced max. value for $V_{CCA_OV_5}$ from 5.6 V to 5.5 V and $V_{CCA_OV_33}$ from 3.7 V to 3.6 V in Table 5 • Reduced max. value for $V_{AUX_OV_5}$ from 5.6 V to 5.5 V and $V_{AUX_OV_33}$ from 3.7 V to 3.6 V in Table 5 • Reduced max. value for t_{1PWU} from 5.0 µs to 3.5 µs in Table 6 • Updated Section 12.5.8 • Updated Section 12.10.4.3 • Updated the effect for LIN_DOM bit in Table 15 • Updated package drawings
FS6500-FS4500 v.5.0	January 2017	• Advance Information • Added C_{IN_CM} and C_{IN_DIFF} parameters in Table 5 • Reduced $I_{BUS_NO_BAT}$ high limit from 100 µA to 30 µA in Table 5 • Added Figure 77 • Applies for silicon revision DEV_REV_2:0 = "010" in DEVICE_ID register
FS6500-FS4500 v.4.0	January 2017	• Advance Information • Corrected $R_{\theta JCTOP}$ value in Table 4 • Updated Section 12.5.7 • Updated Figure 22 and Figure 23 • Corrected typos • Applies for silicon revision DEV_REV_2:0 = "010" in DEVICE_ID register
FS6500-FS4500 v.3.0	June 2016	• Advance Information

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 117. Revision history...*continued*

Document ID	Release date	Description
		• Corrected LIN parameters (V_{BUS_CNT}, D2, D3) in Table 5 and Table 6 to be compliant with LIN standard • Applies for silicon revision DEV_REV_2:0 = "010" in DEVICE_ID register
FS6500-FS4500 v.2.0	June 2016	• Advance Information • PPAP release • Applies for silicon revision DEV_REV_2:0 = "010" in DEVICE_ID register
FS6500-FS4500 v.1.0	September 2015	• Product preview • Initial release • Applies for silicon revision DEV_REV_2:0 = "001" in DEVICE_ID register

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

Suitability for use in automotive applications (functional safety) — This NXP product has been qualified for use in automotive applications. It has been developed in accordance with ISO 26262, and has been ASIL classified accordingly. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as "Critical Applications"), then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys' fees) that NXP may incur related to customer's incorporation of any product in a Critical Application.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Tables

Tab. 1. Part number breakdown 6
Tab. 2. Orderable part variations 6
Tab. 3. FS6500/FS4500 pin definition 12
Tab. 4. Maximum ratings 15
Tab. 5. Static electrical characteristics 17
Tab. 6. Dynamic electrical characteristics 26
Tab. 7. VCCA/VAUX voltage selection 32
Tab. 8. I/Os configuration 35
Tab. 9. Regulators and fail-safe pins checked during ABIST1 42
Tab. 10. Regulators and fail-safe pins checked during ABIST2 42
Tab. 11. Watchdog error table 50
Tab. 12. RELEASE_FSxB register based on LFSR value 57
Tab. 13. Long duration timer characteristics 75
Tab. 14. CAN diagnostic and CAN error bits 82
Tab. 15. LIN error bits 86
Tab. 16. MOSI bits description 89
Tab. 17. MISO bits description 89
Tab. 18. MISO bits description 91
Tab. 19. Register mapping of main logic 91
Tab. 20. Register mapping of fail-safe logic 92
Tab. 21. Secured SPI 93
Tab. 22. INIT_VREG register description 93
Tab. 23. INIT_VREG description and configuration of the bits (default value in bold) 93
Tab. 24. INIT_WU1 register description 94
Tab. 25. INIT_WU1 description and configuration of the bits (default value in bold) 94
Tab. 26. INIT_WU2 register description 95
Tab. 27. INIT_WU2 description and configuration of the bits (default value in bold) 96
Tab. 28. INIT_INT register description 96
Tab. 29. INIT_INT description and configuration of the bits (default value in bold) 97
Tab. 30. INIT_INH_INT register description 98
Tab. 31. INIT IO_WU2 description and configuration of the bits (default value in bold) 98
Tab. 32. LONG_DURATION_TIMER register description 99
Tab. 33. LONG_DURATION_TIMER description and configuration of the bits (default value in bold) 99
Tab. 34. HW_CONFIG register description 100
Tab. 35. HW_CONFIG description and configuration of the bits (default value in bold) 100
Tab. 36. WU_SOURCE register description 101
Tab. 37. WU_SOURCE description and configuration of the bits (default value in bold) 101
Tab. 38. DEVICE_ID register description 102
Tab. 39. DEVICE_ID description and configuration of the bits (default value in bold) 102
Tab. 40. IO_INPUT register description 103
Tab. 41. IO_INPUT description and configuration of the bits 103
Tab. 42. DIAG_VPRE register description 104
Tab. 43. DIAG_VPRE description and configuration of the bits (default value in bold) 104
Tab. 44. DIAG_VCORE register description 105
Tab. 45. DIAG_VCORE description and configuration of the bits (default value in bold) 105
Tab. 46. DIAG_VCCA register description 105
Tab. 47. DIAG_VCCA description and configuration of the bits (default value in bold) 106
Tab. 48. DIAG_VAUX register description 106
Tab. 49. DIAG_VAUX description and configuration of the bits (default value in bold) 107
Tab. 50. DIAG_VSUP_VCAN register description 107
Tab. 51. DIAG_VSUP_VCAN description and configuration of the bits (default value in bold) 107
Tab. 52. DIAG_CAN_FD register description 108
Tab. 53. DIAG_CAN_FD description and configuration of the bits (default value in bold) 108
Tab. 54. DIAG_CAN_LIN register description 109
Tab. 55. DIAG_CAN_LIN description and configuration of the bits (default value in bold) 109
Tab. 56. DIAG_SPI register description 110
Tab. 57. DIAG_SPI description and configuration of the bits (default value in blue) 110
Tab. 58. Mode register description 111
Tab. 59. Mode description and configuration of the bits (default value in bold) 111
Tab. 60. REG_MODE register description 112
Tab. 61. REG_MODE description and configuration of the bits (default value in bold) 112
Tab. 62. IO_OUT_AMUX register description 113
Tab. 63. IO_OUT_AMUX description and configuration of the bits (default value in bold) 113
Tab. 64. CAN_LIN_MODE register description 114
Tab. 65. CAN_LIN_MODE description and configuration of the bits (default value in bold) 114
Tab. 66. LDT_AFTER_RUN_1 register description 115
Tab. 67. LDT_AFTER_RUN_1 description and configuration of the bits (default value in bold) 115
Tab. 68. LDT_AFTER_RUN_2 register description 116
Tab. 69. LDT_AFTER_RUN_2 description and configuration of the bits (default value in bold) 116
Tab. 70. LDT_WAKE_UP_1 register description 116
Tab. 71. LDT_WAKE_UP_1 description and configuration of the bits (default value in bold) 116

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Tab. 72. LDT_WAKE_UP_2 register description 116
Tab. 73. LDT_WAKE_UP_2 description and configuration of the bits (default value in bold) 117
Tab. 74. LDT_WAKE_UP_3 register description 117
Tab. 75. LDT_WAKE_UP_3 description and configuration of the bits (default value in bold) 117
Tab. 76. INIT_FS1B_TIMING register description 117
Tab. 77. INIT_FS1B_TIMING. Description and configuration of the bits (Default value in bold) 118
Tab. 78. BIST register description 118
Tab. 79. BIST description and configuration of the bits (default value in bold) 119
Tab. 80. INIT_SUPERVISOR register description 119
Tab. 81. INIT_SUPERVISOR description and configuration of the bits (default value in bold) 120
Tab. 82. INIT_FAULT register description 120
Tab. 83. INIT_FAULT description and configuration of the bits (default value in bold) 121
Tab. 84. INIT_FSSM register description 121
Tab. 85. INIT_FSSM description and configuration of the bits (default value in bold) 122
Tab. 86. INIT_SF_IMPACT register description 122
Tab. 87. INIT_SF_IMPACT description and configuration of the bits (default value in bold) 123
Tab. 88. WD_WINDOW register description 123
Tab. 89. WD_WINDOW description and configuration of the bits (default value in bold) 124
Tab. 90. WD_LFSR register description 124
Tab. 91. WD_LFSR description and configuration of the bits (default value in bold) 125
Tab. 92. WD_ANSWER register description 125
Tab. 93. WD_ANSWER description and configuration of the bits (default value in bold) 125
Tab. 94. RELEASE_FSxB register description 126
Tab. 95. RELEASE_FSxB description and configuration of the bits (default value in bold) 127
Tab. 96. SF_OUTPUT_REQUEST register description 127
Tab. 97. SF_OUTPUT_REQUEST description and configuration of the bits (default value in bold) 128
Tab. 98. INIT_WD_CNT register description 129
Tab. 99. INIT_WD_CNT description and configuration of the bits (default value in bold) 129
Tab. 100. DIAG_SF_IOs register description 129
Tab. 101. DIAG_SF_IOs description and configuration of the bits (default value in bold) 130
Tab. 102. WD_COUNTER register description 130
Tab. 103. WD_COUNTER description and configuration of the bits (default value in bold) 131
Tab. 104. DIAG_SF_ERR register description 131
Tab. 105. DIAG_SF_ERR description and configuration of the bits (default value in bold) 131
Tab. 106. INIT_VCORE_OVUV_IMPACT register description 132
Tab. 107. INIT_VCORE_OVUV_IMPACT description and configuration of the bits (default value in bold) 132
Tab. 108. INIT_VCCA_OVUV_IMPACT register description 133
Tab. 109. INIT_VCCA_OVUV_IMPACT description and configuration of the bits (default value in bold) 133
Tab. 110. INIT_VAUX_OVUV_IMPACT register description 133
Tab. 111. INIT_VAUX_OVUV_IMPACT description and configuration of the bits (default value in bold) 134
Tab. 112. DEVICE_ID_FS register description 134
Tab. 113. DEVICE_ID_FS description and configuration of the bits (default value in bold) 134
Tab. 114. Interruptions list 136
Tab. 115. Package mechanical dimensions 141
Tab. 116. Revision history 150
Tab. 117. Revision history 150

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Figures

Fig. 1. FS6500C simplified application diagram - buck boost configuration - FS1B 4
Fig. 2. FS6500L simplified application diagram - buck configuration - LIN - VCCA = 100 mA 4
Fig. 3. FS4500C simplified application diagram - buck boost configuration - FS1B 5
Fig. 4. FS6500/FS4500 with CAN and LIN simplified internal block diagram 9
Fig. 5. FS6500 pinout with CAN and FS1B 10
Fig. 6. FS6500 pinout with CAN and LIN 10
Fig. 7. FS6500 pinout without CAN, without LIN 11
Fig. 8. FS4500 pinout with CAN and FS1B 11
Fig. 9. SPI timing diagram 30
Fig. 10. Register access restriction 30
Fig. 11. Deep fail-safe enable/disable 33
Fig. 12. Simplified analog multiplexer block diagram 35
Fig. 13. IO_2:3 MCU error monitoring: bi-stable protocol 36
Fig. 14. External error signal handling 36
Fig. 15. Components involved under ISO pulse in LPOFF 41
Fig. 16. Simplified state diagram 44
Fig. 17. Detailed fail-safe state diagram 46
Fig. 18. Watchdog answer calculation 47
Fig. 19. Windowed watchdog with FS clock accuracy 48
Fig. 20. Watchdog error counter configuration (INIT_WD_CNT register, Bits WD_CNT_ERR_1:0) 49
Fig. 21. Watchdog refresh counter configuration (INIT_WD_CNT register, WD_CNT_RFR_1:0) 50
Fig. 22. Fault error counter (FLT_ERR_FS = 0, WD_CNT_RFR = 6) 51
Fig. 23. Fault error counter (FLT_ERR_FS = 1, WD_CNT_RFR = 6) 52
Fig. 24. Example of WD operation generating a reset (WD_CNT_ERR = 6) 52
Fig. 25. Example of RTSB and FS0B behavior when FLT_ERR_CNT ≥ intermediate value 53
Fig. 26. Example of WD operation leading a decrement of the fault error counter (WD_CNT_RFR = 6) 53
Fig. 27. Fault error counter and FS0B deactivation sequence (FLT_ERR_FS = 0 and WD_CNT_ERR = 6) 54
Fig. 28. FS1B simplified architecture 55
Fig. 29. tDELAY operation 55
Fig. 30. Backup delay operation 56
Fig. 31. tDURATION operation 57
Fig. 32. Input voltage range 58
Fig. 33. Pre-regulator: buck configuration 59
Fig. 34. Pre-regulator: buck boost configuration 59
Fig. 35. Transition between buck and boost 60
Fig. 36. Buck configuration power up and power down 60
Fig. 37. Buck boost configuration power up and power down 61
Fig. 38. Behavior during cranking (buck configuration) 61
Fig. 39. Behavior during cranking (buck boost configuration) 62
Fig. 40. Description of light load conditions 62
Fig. 41. Input power feed forward principle 63
Fig. 42. Overcurrent and current limitation scheme 64
Fig. 43. VPRE efficiency 65
Fig. 44. VCORE buck regulator 66
Fig. 45. Feedback core resistor bridge monitoring (FCRBM) 67
Fig. 46. VCORE efficiency 67
Fig. 47. VCORE linear regulator 68
Fig. 48. Example of VAUX used in tracker mode 70
Fig. 49. VAUX current limitation scheme with foldback mechanism 70
Fig. 50. VKAM start-up strategy 71
Fig. 51. Power dissipation use case 72
Fig. 52. Power dissipation versus ICORE, ICCA, or IPRE 73
Fig. 53. Start-up scheme 74
Fig. 54. Long duration timer block diagram 75
Fig. 55. Long duration timer functions 76
Fig. 56. Long duration timer state machine 77
Fig. 57. CAN simplified block diagram 78
Fig. 58. CAN timing diagram 79
Fig. 59. CAN transition when device goes to LPOFF 79
Fig. 60. TXD dominant timeout detection 80
Fig. 61. Illustration of CANL short to GND detection mechanism 80
Fig. 62. Overtemperature behavior 81
Fig. 63. Multiple pulse wake-up pattern illustration 82
Fig. 64. LIN simplified block diagram 83
Fig. 65. LIN timings for normal baud rate (20 kB/s) 84
Fig. 66. LIN timings for slow baud rate (10 kB/s) 84
Fig. 67. LIN receiver timings 85
Fig. 68. LIN wake-up pattern illustration 86
Fig. 69. SPI overview: SPI waveform and signals polarity 88
Fig. 70. MOSI /MISO SPI command organization 88
Fig. 71. MISO SPI bits 15:8 89
Fig. 72. MISO SPI bits 7:4 90
Fig. 73. FS6500 simplified application schematic with CAN, FS1B, VKAM, buck/boost VPRE configuration 138
Fig. 74. F4500 simplified application schematic with CAN, LIN, IO_5, buck only VPRE configuration 139
Fig. 75. VAUX/VCCA connection, deep fail-safe enabled 139
Fig. 76. VAUX not used, VCCA configuration up to 100 mA, deep fail-safe disabled 140

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Fig. 77. VCCA connection, VAUX not used, deep fail-safe disabled 140
Fig. 78. VCCA connection, VAUX not used, deep fail-safe enabled 140
Fig. 79. SOT1571-1 Rev F 142
Fig. 80. SOT1571-1 Rev. F Detail View 143
Fig. 81. SOT1571-1 Rev F Notes 144
Fig. 82. SOT1571-1 Rev. F - PCB design guidelines - solder mask opening pattern 145
Fig. 83. SOT1571-1 Rev. F - PCB design guidelines - I/O pads and solderable area 146
Fig. 84. SOT1571-1 Rev. F - PCB design guidelines - solder paste stencil 147

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Contents

1 General description 1
2 Features and benefits 2
3 Applications 3
4 Simplified application diagrams 4
5 Ordering information 6
5.1 Part number definition 6
5.2 Part numbers list 6
6 Block diagram 9
7 Pinning information 10
7.1 Pinning information 10
7.2 Pin description 12
8 Maximum ratings 15
9 Static electrical characteristics 17
10 Dynamic electrical characteristics 26
11 Functional pin description 31
11.1 Introduction 31
11.2 Power supplies (VSUP1, VSUP2, VSUP3) 31
11.3 VSENSE input (VSENSE) 31
11.4 Pre-regulator (VPRE) 31
11.5 VCORE output (from 1.0 V to 5.0 V range) 31
11.6 VCCA output, 5.0 V, or 3.3 V selectable 32
11.7 VAUX output, 5.0 V, or 3.3 V selectable 32
11.8 SELECT input pin 32
11.8.1 VCCA, VAUX voltage configuration 32
11.8.2 Deep fail-safe configuration 33
11.9 CAN_5V voltage regulator 33
11.10 Interrupt (INTB) 33
11.11 CANH, CANL, TXD, RXD 33
11.11.1 TXD 33
11.11.2 RXD 33
11.11.3 CANH and CANL 34
11.12 LIN, TXDL, RXDL 34
11.12.1 TXDL 34
11.12.2 RXDL 34
11.12.3 LIN 34
11.13 Multiplexer output MUX_OUT 34
11.14 I/O pins (I/O_0:I/O_5) 35
11.15 SAFE output pins (FS0B, FS1B, RSTB) 37
11.15.1 FS0B pin 37
11.15.2 FS1B pin 37
11.15.3 RSTB pin 37
11.16 VPU_FS (fail-safe pull-up) 37
11.17 DEBUG input (entering in debug mode) 38
12 Functional device operation 39
12.1 Mode and state description of the main state machine 39
12.1.1 Buck or buck boost configuration 39
12.1.2 VPRE on 39
12.1.3 SELECT pin configuration 39
12.1.4 VCORE/VAUX/VCCA on 39
12.1.5 INIT main 39
12.1.6 Normal 40
12.1.7 Low-power mode off 40
12.1.7.1 LPOFF - sleep 40
12.1.7.2 LPOFF - auto WU 40
12.1.7.3 LPOFF - deep FS 40
12.1.7.4 Register configuration in LPOFF 40
12.1.7.5 ISO pulse in LPOFF 40
12.2 Mode and state description of fail-safe state machine 41
12.2.1 LBIST 41
12.2.2 Select pin configuration 41
12.2.3 ABIST 41
12.2.3.1 ABIST1 41
12.2.3.2 ABIST2 42
12.2.4 Release RSTB 42
12.2.5 INIT_FS 42
12.2.6 Normal WD 42
12.2.7 Assert RSTB 42
12.2.8 Assert FSxB and ABIST2 43
12.3 Deep fail-safe state 43
12.4 Functional state diagram 44
12.5 Fail-safe machine 44
12.5.1 Fail-safe machine state diagram 46
12.5.2 Watchdog operation 47
12.5.2.1 Normal operation (first watchdog refresh) 47
12.5.2.2 Normal watchdog refresh 47
12.5.2.3 Watchdog in debug mode 48
12.5.2.4 Wrong watchdog refresh handling 48
12.5.2.5 Watchdog error counter 48
12.5.2.6 Watchdog refresh counter 49
12.5.3 Fault error counter 50
12.5.3.1 Fault error counter intermediate value 52
12.5.3.2 Fault error counter at start-up or resuming from LPOFF mode 53
12.5.4 RESET (RSTB) activation 54
12.5.5 Fail-safe output (FS0B) activation 54
12.5.6 Fail-safe output (FS1B) activation 55
12.5.6.1 tDELAY operation 55
12.5.6.2 tDURATION operation 56
12.5.7 Fail-safe outputs (FS0B and FS1B) release 57
12.5.7.1 RELEASE_FSxB register 57
12.5.8 SPI DED 57
12.6 Input voltage range 58
12.7 Power management operation 58
12.7.1 VPRE voltage pre-regulator 59
12.7.1.1 Power up and power down sequence 60
12.7.1.2 Cranking management 61
12.7.1.3 Light load condition 62
12.7.1.4 Input power feed forward condition 63
12.7.1.5 Overcurrent detection and current limitation 63
12.7.1.6 VPRE voltage monitoring 64
12.7.1.7 VPRE efficiency 64
12.7.2 VCORE voltage regulator 65
12.7.2.1 VCORE DC–DC converter 65
12.7.2.2 Light load condition 66
12.7.2.3 Current limitation 66
12.7.2.4 Voltage monitoring 66
12.7.2.5 VCORE efficiency 67
12.7.2.6 VCORE linear regulator 67
12.7.2.7 Current limitation 68
12.7.2.8 Voltage monitoring 68

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

12.7.3 Charge pump and bootstrap 68
12.7.4 VCCA voltage regulator 68
12.7.4.1 Current limitation 69
12.7.4.2 Voltage monitoring 69
12.7.5 VAUX voltage regulator 69
12.7.5.1 Current limitation 70
12.7.5.2 Voltage monitoring 71
12.7.6 CAN_5V voltage regulator 71
12.7.7 VKAM 71
12.7.8 Power dissipation 72
12.7.9 Start-up sequence 73
12.8 Long duration timer 74
12.8.1 Timer characteristics 75
12.8.2 Calibration procedure 75
12.8.3 Timer functions 76
12.8.4 Timer operation 77
12.9 CAN transceiver 77
12.9.1 Operating modes 78
12.9.1.1 Normal mode 78
12.9.1.2 Sleep mode 79
12.9.2 Fault detection 79
12.9.2.1 TXD permanent dominant (timeout) 79
12.9.2.2 RXD permanent recessive 80
12.9.2.3 CAN-bus short-circuits 80
12.9.2.4 CAN current limitation 81
12.9.2.5 CAN overtemperature 81
12.9.2.6 Distinguish CAN diagnostics and CAN errors 81
12.9.3 Wake-up mechanism 82
12.9.3.1 Multiple pulse detection 82
12.10 LIN transceiver 82
12.10.1 Simplified block diagram 83
12.10.2 Operating modes 83
12.10.2.1 Normal mode 83
12.10.2.2 Sleep mode 83
12.10.3 Baud rate selection 83
12.10.4 Fault detection 85
12.10.4.1 VSUP undervoltage 85
12.10.4.2 TXDL permanent dominant (timeout) 85
12.10.4.3 RXDL permanent recessive 85
12.10.4.4 LIN bus short-circuit 85
12.10.4.5 LIN current limitation 85
12.10.4.6 LIN overtemperature 86
12.10.4.7 LIN errors 86
12.10.5 Wake-up mechanism 86
13 Serial peripheral interface 87
13.1 High-level overview 87
13.1.1 SPI 87
13.1.2 Parity bit 8 calculation 87
13.1.3 Device status on MISO 87
13.1.4 Register description 88
13.2 Detailed operation 88
13.2.1 SPI command organization 88
13.2.2 Main logic general diagnostic 89
13.2.3 Fail-safe logic general diagnostic 90
13.2.4 Main logic register address table 91
13.2.5 Fail-safe logic register address table 92
13.2.6 Secured SPI command 92
13.3 Detail of main logic register mapping 93
13.3.1 INIT_VREG 93
13.3.2 INIT_WU1 94
13.3.3 INIT_WU2 95
13.3.4 INIT_INT 96
13.3.5 INIT_INH_INT 98
13.3.6 LONG_DURATION_TIMER 99
13.3.7 HW_CONFIG 100
13.3.8 WU_SOURCE 101
13.3.9 DEVICE _ID 102
13.3.10 IO_INPUT 103
13.3.11 DIAG_VPRE 104
13.3.12 DIAG_VCORE 105
13.3.13 DIAG_VCCA 105
13.3.14 DIAG_VAUX 106
13.3.15 DIAG_VSUP_VCAN 107
13.3.16 DIAG_CAN_FD 108
13.3.17 DIAG_CAN_LIN 109
13.3.18 DIAG_SPI 110
13.3.19 Mode 111
13.3.20 REG_MODE 112
13.3.21 IO_OUT_AMUX 113
13.3.22 CAN_LIN_MODE 114
13.3.23 LDT_AFTER_RUN_1 115
13.3.24 LDT_AFTER_RUN_2 116
13.3.25 LDT_WAKE_UP_1 116
13.3.26 LDT_WAKE_UP_2 116
13.3.27 LDT_WAKE_UP_3 117
13.4 Detail of fail-safe logic register mapping 117
13.4.1 INIT_FS1B_TIMING 117
13.4.2 BIST 118
13.4.3 INIT_SUPERVISOR 119
13.4.4 INIT_FAULT 120
13.4.5 INIT_FSSM 121
13.4.6 INIT_SF_IMPACT 122
13.4.7 WD_WINDOW 123
13.4.8 WD_LFSR 124
13.4.9 WD_ANSWER 125
13.4.10 RELEASE_FSxB 126
13.4.11 SF_OUTPUT_REQUEST 127
13.4.12 INIT_WD_CNT 129
13.4.13 DIAG_SF_IOs 129
13.4.14 WD_COUNTER 130
13.4.15 DIAG_SF_ERR 131
13.4.16 INIT_VCORE_OVUV_IMPACT 132
13.4.17 INIT_VCCA_OVUV_IMPACT 133
13.4.18 INIT_VAUX_OVUV_IMPACT 133
13.4.19 DEVICE_ID_FS 134
14 List of interruptions and description 136
15 Typical applications 138
16 Packaging 141
16.1 Package mechanical dimensions 141
16.2 Package outline 142
17 Soldering 145
18 References 148
19 Revision history 150
Legal information 153

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

FS6500-FS4500-ASILD

Safety power system basis chip with CAN FD and LIN transceivers

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© 2026 NXP B.V. All rights reserved.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View MC33FS6528NAE on WIN SOURCE
- NXP / Nexperia Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management