**NXP Semiconductors**
Data Sheet: Technical Data

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# MPC8640 and MPC8640D Integrated Host Processor Hardware Specifications

## 1 Overview

The MPC8640 processor family integrates either one or two Power Architecture™ e600 processor cores with system logic required for networking, storage, wireless infrastructure, and general-purpose embedded applications. The MPC8640 integrates one e600 core while the MPC8640D integrates two cores.

This section provides a high-level overview of the MPC8640 and MPC8640D features. When referring to the MPC8640 throughout the document, the functionality described applies to both the MPC8640 and the MPC8640D. Any differences specific to the MPC8640D are noted.

Figure 1 shows the major functional units within the MPC8640 and MPC8640D. The major difference between the MPC8640 and MPC8640D is that there are two cores on the MPC8640D.

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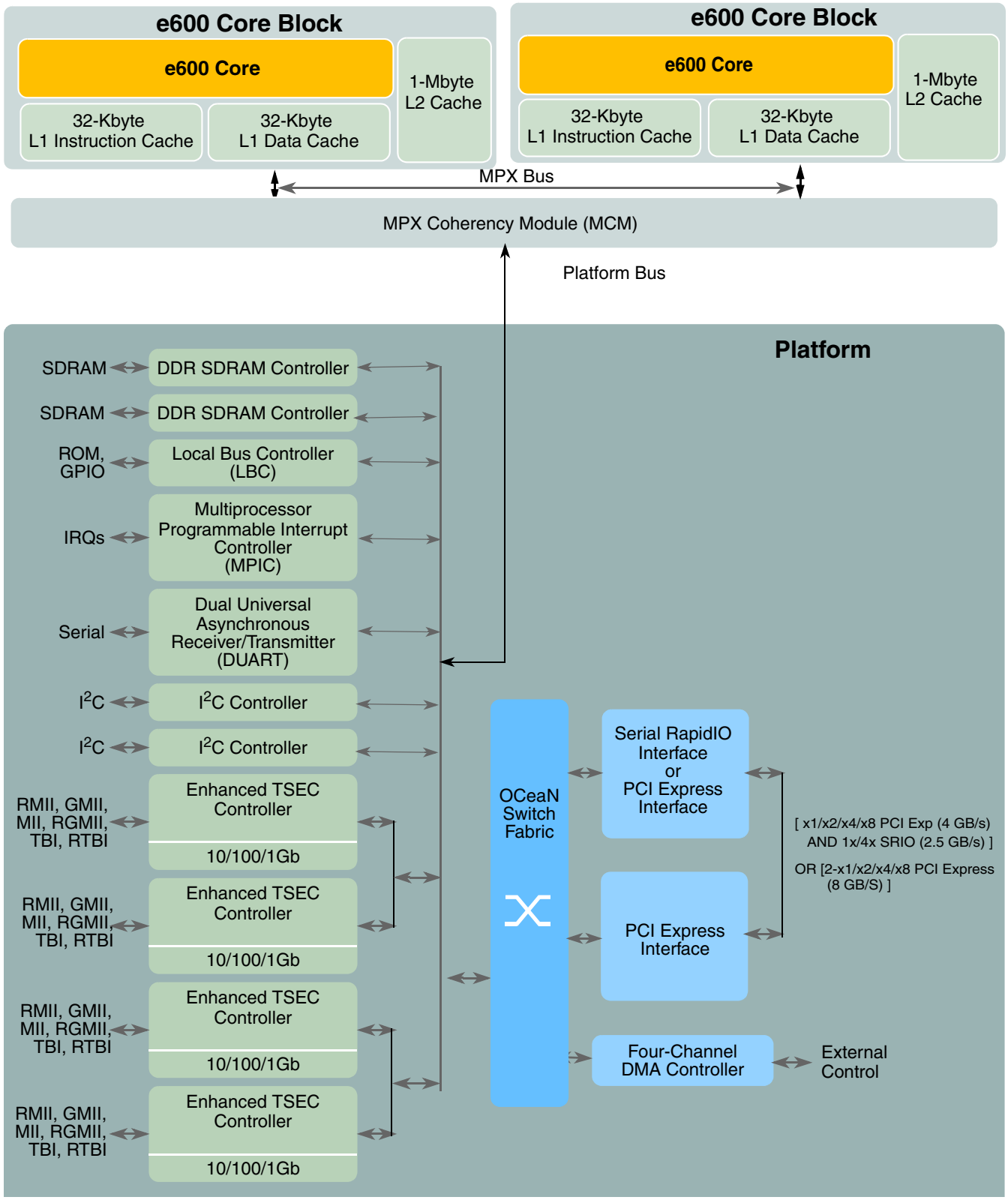



**Figure 1. MPC8640 and MPC8640D**

## 1.1 Key Features

The following lists the MPC8640 key feature set:

- Major features of the e600 core are as follows:
  - High-performance, 32-bit superscalar microprocessor that implements the PowerPC instruction set architecture (ISA)
  - Eleven independent execution units and three register files
    - Branch processing unit (BPU)
    - Four integer units (IUs) that share 32 GPRs for integer operands
    - 64-bit floating-point unit (FPU)
    - Four vector units and a 32-entry vector register file (VRs)
    - Three-stage load/store unit (LSU)
  - Three issue queues, FIQ, VIQ, and GIQ, can accept as many as one, two, and three instructions, respectively, in a cycle.
  - Rename buffers
  - Dispatch unit
  - Completion unit
  - Two separate 32-Kbyte instruction and data level 1 (L1) caches
  - Integrated 1-Mbyte, eight-way set-associative unified instruction and data level 2 (L2) cache with ECC
  - 36-bit real addressing
  - Separate memory management units (MMUs) for instructions and data
  - Multiprocessing support features
  - Power and thermal management
  - Performance monitor
  - In-system testability and debugging features
  - Reliability and serviceability
- MPX coherency module (MCM)
  - Ten local address windows plus two default windows
  - Optional low memory offset mode for core 1 to allow for address disambiguation
- Address translation and mapping units (ATMUs)
  - Eight local access windows define mapping within local 36-bit address space
  - Inbound and outbound ATMUs map to larger external address spaces
  - Three inbound windows plus a configuration window on PCI Express® interface unit
  - Four inbound windows plus a default window on serial RapidIO interface unit
  - Four outbound windows plus default translation for PCI Express interface unit
  - Eight outbound windows plus default translation for serial RapidIO® interface unit with segmentation and subsegmentation support

- DDR memory controllers
  - Dual 64-bit memory controllers (72-bit with ECC)
  - Support of up to a 266 MHz clock rate and a 533 MHz DDR2 SDRAM
  - Support for DDR, DDR2 SDRAM
  - Up to 16 Gbytes per memory controller
  - Cache line and page interleaving between memory controllers.
- Serial RapidIO interface unit
  - Supports *RapidIO Interconnect Specification*, Revision 1.2
  - Both 1× and 4× LP-Serial link interfaces
  - Transmission rates of 1.25-, 2.5-, and 3.125-Gbaud (data rates of 1.0-, 2.0-, and 2.5-Gbps) per lane
  - Message unit compliant with RapidIO specifications
  - RapidIO atomic transactions to the memory controller
- PCI Express interface
  - PCI Express 1.0a compatible
  - Supports ×1, ×2, ×4, and ×8 link widths
  - 2.5 Gbaud, 2.0 Gbps lane
- Four enhanced three-speed Ethernet controllers (eTSECs)
  - Three-speed support (10/100/1000 Mbps)
  - Four controllers that comply with IEEE Std. 802.3®, 802.3u®, 802.3x®, 802.3z®, 802.3ac®, 802.3ab® standards
  - Support for the following physical interfaces: MII, RMII, GMII, RGMII, TBI, and RTBI
  - Support for a full-duplex FIFO mode for high-efficiency ASIC connectivity
  - TCP/IP off-load
  - Header parsing
  - Quality of service support
  - VLAN insertion and deletion
  - MAC address recognition
  - Buffer descriptors are backward compatible with PowerQUICC II and PowerQUICC III programming models
  - RMON statistics support
  - MII management interface for control and status
- Programmable interrupt controller (PIC)
  - Programming model is compliant with the OpenPIC architecture
  - Supports 16 programmable interrupt and processor task priority levels
  - Supports 12 discrete external interrupts and 48 internal interrupts
  - Eight global high resolution timers/counters that can generate interrupts

  - Allows processors to interrupt each other with 32b messages
  - Support for PCI-Express message-shared interrupts (MSIs)
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data operating at up to 125 MHz
  - Eight chip selects support eight external slaves
- Integrated DMA controller
  - Four-channel controller
  - All channels accessible by both the local and the remote masters
  - Supports transfers to or from any local memory or I/O port
  - Ability to start and flow control each DMA channel from external 3-pin interface
- Device performance monitor
  - Supports eight 32-bit counters that count the occurrence of selected events
  - Ability to count up to 512 counter-specific events
  - Supports 64 reference events that can be counted on any of the 8 counters
  - Supports duration and quantity threshold counting
  - Burstiness feature that permits counting of burst events with a programmable time between bursts
  - Triggering and chaining capability
  - Ability to generate an interrupt on overflow
- Dual $I^2C$ controllers
  - Two-wire interface
  - Multiple master support
  - Master or slave $I^2C$ mode support
  - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
  - Optionally loads configuration data from serial ROM at reset via the $I^2C$ interface
  - Can be used to initialize configuration registers and/or memory
  - Supports extended $I^2C$ addressing mode
  - Data integrity checked with preamble signature and CRC
- DUART
  - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
  - Programming model compatible with the original 16450 UART and the PC16550D
- IEEE 1149.1™-compliant, JTAG boundary scan
- Available as 1023 pin Hi-CTE flip chip ceramic ball grid array (FC-CBGA)

# 2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8640. The MPC8640 is currently targeted to these specifications.

## 2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

### 2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

**Table 1. Absolute Maximum Ratings[1]**

| Parameter | Symbol | Absolute Maximum Value | Unit | Notes |
|---|---|---|---|---|
| Cores supply voltages | $V_{DD}$_Core0, $V_{DD}$_Core1 | –0.3 to 1.21 V | V | 2 |
| Cores PLL supply | $AV_{DD}$_Core0, $AV_{DD}$_Core1 | –0.3 to 1.21 V | V | — |
| SerDes Transceiver Supply (Ports 1 and 2) | $SV_{DD}$ | –0.3 to 1.21 V | V | — |
| SerDes Serial I/O Supply Port 1 | $XV_{DD}$_SRDS1 | –0.3 to 1.21 V | V | — |
| SerDes Serial I/O Supply Port 2 | $XV_{DD}$_SRDS2 | –0.3 to 1.21 V | V | — |
| SerDes DLL and PLL supply voltage for Port 1 and Port 2 | $AV_{DD}$_SRDS1, $AV_{DD}$_SRDS2 | –0.3 to 1.21V | V | — |
| Platform Supply voltage | $V_{DD}$_PLAT | –0.3 to 1.21V | V | — |
| Local Bus and Platform PLL supply voltage | $AV_{DD}$_LB, $AV_{DD}$_PLAT | –0.3 to 1.21V | V | — |
| DDR and DDR2 SDRAM I/O supply voltages | D1_$GV_{DD}$, D2_$GV_{DD}$ | –0.3 to 2.75 V | V | 3 |
| | | –0.3 to 1.98 V | V | 3 |
| eTSEC 1 and 2 I/O supply voltage | $LV_{DD}$ | –0.3 to 3.63 V | V | 4 |
| | | –0.3 to 2.75 V | V | 4 |
| eTSEC 3 and 4 I/O supply voltage | $TV_{DD}$ | –0.3 to 3.63 V | V | 4 |
| | | –0.3 to 2.75 V | V | 4 |
| Local Bus, DUART, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, $I^2C$, JTAG and Miscellaneous I/O voltage | $OV_{DD}$ | –0.3 to 3.63V | V | — |

**Table 1. Absolute Maximum Ratings[1] (continued)**

| Parameter | | Symbol | Absolute Maximum Value | Unit | Notes |
|---|---|---|---|---|---|
| Input voltage | DDR and DDR2 SDRAM signals | D*n*_$MV_{IN}$ | –0.3 to (D*n*_$GV_{DD}$ + 0.3) | V | 5 |
| | DDR and DDR2 SDRAM reference | D*n*_$MV_{REF}$ | –0.3 to (D*n*_$GV_{DD}$ ÷ 2 + 0.3) | V | — |
| | Three-speed Ethernet signals | $LV_{IN}$<br>$TV_{IN}$ | GND to ($LV_{DD}$ + 0.3)<br>GND to ($TV_{DD}$ + 0.3) | V | 5 |
| | DUART, Local Bus, DMA, Multiprocessor Interrupts, System Control and Clocking, Debug, Test, Power management, $I^2C$, JTAG and Miscellaneous I/O voltage | $OV_{IN}$ | GND to ($OV_{DD}$ + 0.3) | V | 5 |
| Storage temperature range | | $T_{STG}$ | –55 to 150 | °C | — |

**Notes:**
1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. Core 1 characteristics apply only to MPC8640D. If two separate power supplies are used for $V_{DD}$_Core0 and $V_{DD}$_Core1, they must be kept within 100 mV of each other during normal run time.
3. The –0.3 to 2.75 V range is for DDR and –0.3 to 1.98 V range is for DDR2.
4. The 3.63 V maximum is only supported when the port is configured in GMII, MII, RMII, or TBI modes; otherwise the 2.75 V maximum applies. See Section 8.2, "FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications," for details on the recommended operating conditions per protocol.
5. During run time (M,L,T,O)$V_{IN}$ and D*n*_$MV_{REF}$ may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

## 2.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8640. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed. For details on order information and specific operating conditions for parts, see Section 21, "Ordering Information."

**Table 2. Recommended Operating Conditions**

| Parameter | Symbol | Recommended Value | Unit | Notes |
|---|---|---|---|---|
| Cores supply voltages | $V_{DD}$_Core0, $V_{DD}$_Core1 | 1.05 ± 50 mV | V | 1, 2 |
| | | 0.95 ± 50 mV | | 1, 2, 10 |
| Cores PLL supply | $AV_{DD}$_Core0, $AV_{DD}$_Core1 | 1.05 ± 50 mV | V | 11 |
| | | 0.95 ± 50 mV | | 10, 11 |
| SerDes Transceiver Supply (Ports 1 and 2) | $SV_{DD}$ | 1.05 ± 50 mV | V | 9 |
| SerDes Serial I/O Supply Port 1 | $XV_{DD}$_SRDS1 | 1.05 ± 50 mV | V | — |
| SerDes Serial I/O Supply Port 2 | $XV_{DD}$_SRDS2 | 1.05 ± 50 mV | V | — |
| SerDes DLL and PLL supply voltage for Port 1 and Port 2 | $AV_{DD}$_SRDS1, $AV_{DD}$_SRDS2 | 1.05 ± 50 mV | V | — |

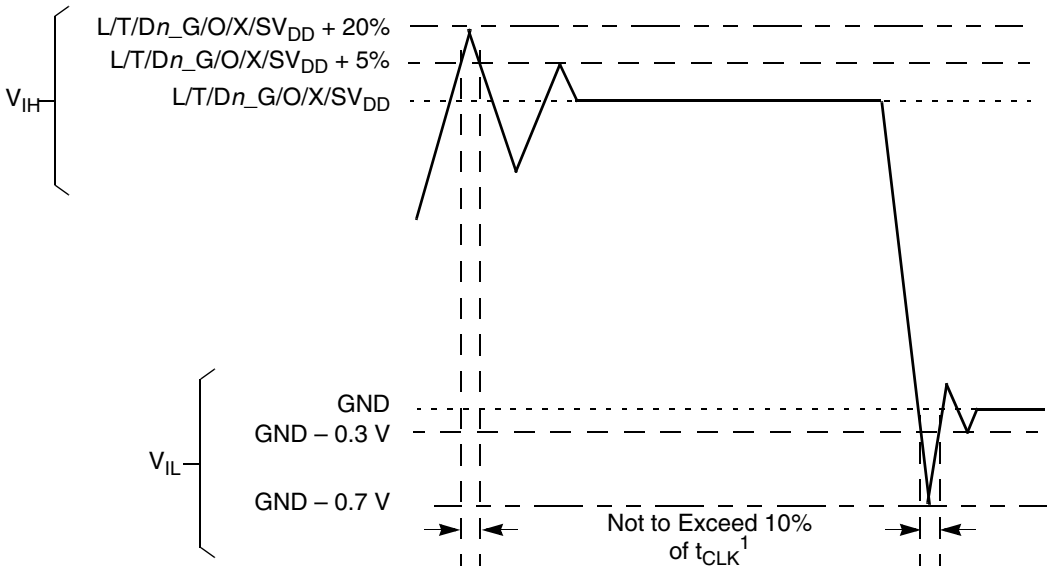
**Table 2. Recommended Operating Conditions (continued)**

| Parameter | | Symbol | Recommended Value | Unit | Notes |
|---|---|---|---|---|---|
| Platform supply voltage | | $V_{DD}$_PLAT | 1.05 ± 50 mV | V | — |
| Local Bus and Platform PLL supply voltage | | $AV_{DD}$_LB, $AV_{DD}$_PLAT | 1.05 ± 50 mV | V | — |
| DDR and DDR2 SDRAM I/O supply voltages | | D1_$GV_{DD}$, D2_$GV_{DD}$ | 2.5 V ± 125 mV | V | 7 |
| | | | 1.8 V ± 90 mV | | 7 |
| eTSEC 1 and 2 I/O supply voltage | | $LV_{DD}$ | 3.3 V ± 165 mV | V | 8 |
| | | | 2.5 V ± 125 mV | V | 8 |
| eTSEC 3 and 4 I/O supply voltage | | $TV_{DD}$ | 3.3 V ± 165 mV | V | 8 |
| | | | 2.5 V ± 125 mV | V | 8 |
| Local Bus, DUART, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, $I^2C$, JTAG and Miscellaneous I/O voltage | | $OV_{DD}$ | 3.3 V ± 165 mV | V | 5 |
| Input voltage | DDR and DDR2 SDRAM signals | D*n*_$MV_{IN}$ | GND to D*n*_$GV_{DD}$ | V | 3, 6 |
| | DDR and DDR2 SDRAM reference | D*n*_$MV_{REF}$ | D*n*_$GV_{DD}$/2 ± 1% | V | — |
| | Three-speed Ethernet signals | $LV_{IN}$ $TV_{IN}$ | GND to $LV_{DD}$ GND to $TV_{DD}$ | V | 4, 6 |
| | DUART, Local Bus, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, $I^2C$, JTAG and Miscellaneous I/O voltage | $OV_{IN}$ | GND to $OV_{DD}$ | V | 5,6 |
| Junction temperature range | | $T_J$ | 0 to 105 | °C | — |
| | | | –40 to 105 | | 12 |

**Notes:**

1. Core 1 characteristics apply only to MPC8640D
2. If two separate power supplies are used for $V_{DD}$_Core0 and $V_{DD}$_Core1, they must be at the same nominal voltage and the individual power supplies must be tracked and kept within 100 mV of each other during normal run time.
3. **Caution:** D*n*_$MV_{IN}$ must meet the overshoot/undershoot requirements for D*n*_$GV_{DD}$ as shown in Figure 2.
4. **Caution:** L/$TV_{IN}$ must meet the overshoot/undershoot requirements for L/$TV_{DD}$ as shown in Figure 2 during regular run time.
5. **Caution:** $OV_{IN}$ must meet the overshoot/undershoot requirements for $OV_{DD}$ as shown in Figure 2 during regular run time.
6. Timing limitations for M,L,T,O)$V_{IN}$ and D*n*_$MV_{REF}$ during regular run time is provided in Figure 2
7. The 2.5 V ± 125 mV range is for DDR and 1.8 V ± 90 mV range is for DDR2.
8. See Section 8.2, "FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications," for details on the recommended operating conditions per protocol.
9. The PCI Express interface of the device is expected to receive signals from 0.175 to 1.2 V. For more information refer to Section 14.4.3, "Differential Receiver (Rx) Input Specifications."
10. Applies to Part Number MC8640wxx1067Nz only. $V_{DD}$_Core*n* = 0.95 V and $V_{DD}$_PLAT = 1.05 V devices. Refer to Table 74 Part Numbering Nomenclature to determine if the device has been marked for $V_{DD}$_Core*n* = 0.95 V.
11. This voltage is the input to the filter discussed in Section 20.2, "Power Supply Design and Sequencing," and not necessarily the voltage at the $AV_{DD}$_Core*n* pin, which may be reduced from $V_{DD}$_Core*n* by the filter.
12. Applies to part number MC8640DTxxyyyyaz. Refer to Table 74 Part Numbering Nomenclature to determine if the device has been marked for extended operating temperature range.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8640.




**Note:**

1. $t_{CLK}$ references clocks for various functional blocks as follows:

DDRn = 10% of Dn_MCK period
eTSECn = 10% of ECn_GTX_CLK125 period
Local Bus = 10% of LCLK[0:2] period
I2C = 10% of SYSCLK
JTAG = 10% of SYSCLK

**Figure 2. Overshoot/Undershoot Voltage for D*n*_M/O/L/TV$_{IN}$**

The MPC8640 core voltage must always be provided at nominal $V_{DD}$_Core*n* (See Table 2 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. $OV_{DD}$ and $L/TV_{DD}$ based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced to each externally supplied D*n*_$MV_{REF}$ signal (nominally set to D*n*_$GV_{DD}$/2) as is appropriate for the (SSTL-18 and SSTL-25) electrical signaling standards.

### 2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

**Table 3. Output Drive Capability**

| Driver Type | Programmable Output Impedance (Ω) | Supply Voltage | Notes |
|---|---|---|---|
| DDR1 signal | 18<br>36 (half strength mode) | D*n*_$GV_{DD}$ = 2.5 V | 4, 9 |
| DDR2 signal | 18<br>36 (half strength mode) | D*n*_$GV_{DD}$ = 1.8 V | 1, 5, 9 |
| Local Bus signals | 45<br>25 | $OV_{DD}$ = 3.3 V | 2, 6 |
| eTSEC/10/100 signals | 45 | $T/LV_{DD}$ = 3.3 V | 6 |
| | 30 | $T/LV_{DD}$ = 2.5 V | 6 |
| DUART, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, JTAG and Miscellaneous I/O voltage | 45 | $OV_{DD}$ = 3.3 V | 6 |
| $I^2C$ | 150 | $OV_{DD}$ = 3.3 V | 7 |
| SRIO, PCI Express | 100 | $SV_{DD}$ = 1.1/1.05 V | 3, 8 |

**Notes:**
1. See the DDR Control Driver registers in the MPC8641D reference manual for more information.
2. Only the following local bus signals have programmable drive strengths: LALE, LAD[0:31], LDP[0:3], LA[27:31], LCKE, LCS[1:2], LWE[0:3], LGPL1, LGPL2, LGPL3, LGPL4, LGPL5, LCLK[0:2]. The other local bus signals have a fixed drive strength of 45 Ω. See the POR Impedance Control register in the MPC8641D reference manual for more information about local bus signals and their drive strength programmability.
3. See Section 17, "Signal Listings," for details on resistor requirements for the calibration of SD*n*_IMP_CAL_TX and SD*n*_IMP_CAL_RX transmit and receive signals.
4. Stub Series Terminated Logic (SSTL-25) type pins.
5. Stub Series Terminated Logic (SSTL-18) type pins.
6. Low Voltage Transistor-Transistor Logic (LVTTL) type pins.
7. Open Drain type pins.
8. Low Voltage Differential Signaling (LVDS) type pins.
9. The drive strength of the DDR interface in half strength mode is at $T_j$ = 105C and at D*n*_$GV_{DD}$ (min).

## 2.2 Power-Up/Down Sequence

The MPC8640 requires its power rails to be applied in a specific sequence to ensure proper device operation.

**NOTE**

The recommended maximum ramp up time for power supplies is 20 milliseconds.

The chronological order of power up is:

1. All power rails other than DDR I/O (D*n*_$GV_{DD}$, and D*n*_$MV_{REF}$).

**NOTE**

There is no required order sequence between the individual rails for this item (# 1). However, $V_{DD}$_PLAT, $AV_{DD}$_PLAT rails must reach 90% of their recommended value before the rail for Dn_$GV_{DD}$, and Dn_$MV_{REF}$ (in next step) reaches 10% of their recommended value. $AV_{DD}$ type supplies must be delayed with respect to their source supplies by the RC time constant of the PLL filter circuit described in Section 20.2.1, "PLL Power Supply Filtering."

2. D*n*_$GV_{DD}$, D*n*_$MV_{REF}$

**NOTE**

It is possible to leave the related power supply (D*n*_$GV_{DD}$, D*n*_$MV_{REF}$) turned off at reset for a DDR port that will not be used. Note that these power supplies can only be powered up again at reset for functionality to occur on the DDR port.

3. 3. SYSCLK

The recommended order of power down is as follows:

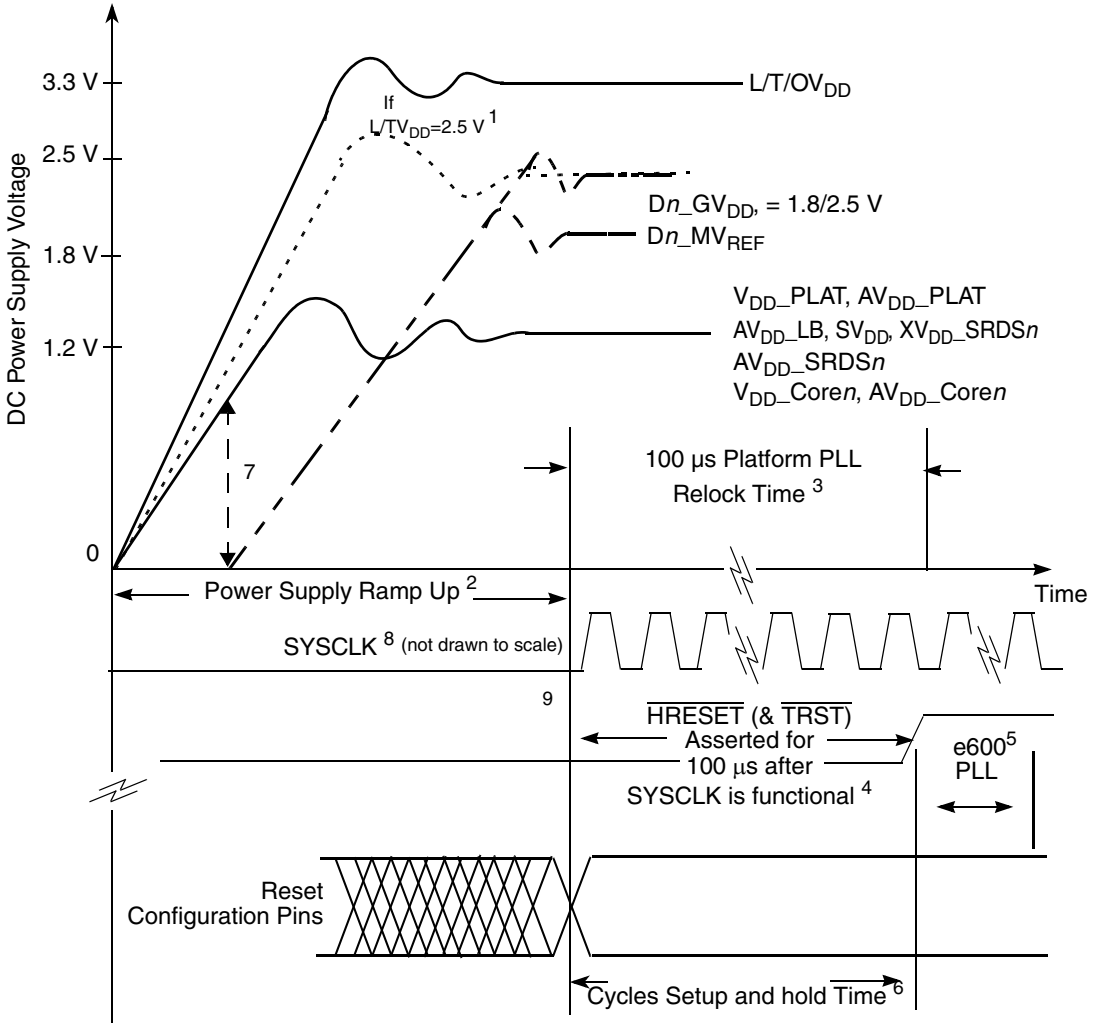
1. D*n*_$GV_{DD}$, D*n*_$MV_{REF}$
2. All power rails other than DDR I/O (D*n*_$GV_{DD}$, D*n*_$MV_{REF}$).

**NOTE**

SYSCLK may be powered down simultaneous to either of item # 1 or # 2 in the power down sequence. Beyond this, the power supplies may power down simultaneously if the preservation of DDR*n* memory is not a concern.

See Figure 3 for more details on the power and reset sequencing details.

Figure 3 illustrates the power up sequence as described above.




**Notes:**

1. Dotted waveforms correspond to optional supply values for a specified power supply. See Table 2.
2. The recommended maximum ramp up time for power supplies is 20 milliseconds.
3. Refer to Section 5, "RESET Initialization," for additional information on PLL relock and reset signal assertion timing requirements.
4. Refer to Table 11 for additional information on reset configuration pin setup timing requirements. In addition see Figure 68 regarding HRESET and JTAG connection details including TRST.
5. e600 PLL relock time is 100 microseconds maximum plus 255 MPX_clk cycles.
6. Stable PLL configuration signals are required as stable SYSCLK is applied. All other POR configuration inputs are required 4 SYSCLK cycles before HRESET negation and are valid at least 2 SYSCLK cycles after HRESET has negated (hold requirement). See Section 5, "RESET Initialization," for more information on setup and hold time of reset configuration signals.
7. V$_{DD}$_PLAT, AV$_{DD}$_PLAT must strictly reach 90% of their recommended voltage before the rail for D$n$_GV$_{DD}$, and D$n$_MV$_{REF}$ reaches 10% of their recommended voltage.
8. SYSCLK must be driven only AFTER the power for the various power supplies is stable.
9. In device sleep mode, the reset configuration signals for DRAM types (TSEC2_TXD[4],TSEC2_TX_ER) must be valid BEFORE HRESET is asserted.

**Figure 3. MPC8640 Power-Up and Reset Sequence**

# 3 Power Characteristics

The power dissipation for the dual core MPC8640D device is shown in Table 4.

**Table 4. MPC8640D Power Dissipation (Dual Core)**

| Power Mode | Core Frequency (MHz) | Platform Frequency (MHz) | $V_{DD}$_Coren, $V_{DD}$_PLAT (Volts) | Junction Temperature | Power (Watts) | Notes |
|---|---|---|---|---|---|---|
| Typical | 1250 MHz | 500 MHz | 1.05 V | 65 °C | 21.7 | 1, 2 |
| Thermal | | | | 105 °C | 27.3 | 1, 3 |
| Maximum | | | | | 31 | 1, 4 |
| Typical | 1000 MHz | 500 MHz | 1.05 V | 65 °C | 18.9 | 1, 2 |
| Thermal | | | | 105 °C | 23.8 | 1, 3 |
| Maximum | | | | | 27 | 1, 4 |
| Typical | 1067 MHz | 533 MHz | 0.95/1.05 V | 65 °C | 15.7 | 1, 2, 5 |
| Thermal | | | | 105 °C | 19.5 | 1, 3, 5 |
| Maximum | | | | | 22 | 1, 4, 5 |

**Notes:**
1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured at the nominal recommended core voltage ($V_{DD}$_Core*n*) and 65 °C junction temperature (see Table 2)while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz with one core at 100% efficiency and the second core at 65% efficiency.
3. Thermal power is the average power measured at nominal core voltage ($V_{DD}$_Core*n*) and maximum operating junction temperature (see Table 2) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz on both cores and a typical workload on platform interfaces.
4. Maximum power is the maximum power measured at nominal core voltage ($V_{DD}$_Core*n*) and maximum operating junction temperature (see Table 2) while running a test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep all the execution units maximally busy on both cores.
5. These power numbers are for Part Number MC8640Dwxx1067Nz and MC8640wxx1067Nz only. $V_{DD}$_Core*n* = 0.95 V and $V_{DD}$_PLAT = 1.05 V.

The power dissipation for individual power supplies of the MPC8640D is shown in Table 5.

**Table 5. MPC8640D Individual Supply Maximum Power Dissipation [1]**

| Component Description | Supply Voltage (Volts) | Power (Watts) | Notes |
|---|---|---|---|
| Per Core voltage Supply | $V_{DD}$_Core0/$V_{DD}$_Core1 = 1.05 V at 1250 MHz | 17.00 | — |
| Per Core PLL voltage supply | $AV_{DD}$_Core0/$AV_{DD}$_Core1 = 1.05 V at 1250 MHz | 0.0125 | — |
| Per Core voltage Supply | $V_{DD}$_Core0/$V_{DD}$_Core1 = 1.05 V at 1000 MHz | 15.00 | — |
| Per Core PLL voltage supply | $AV_{DD}$_Core0/$AV_{DD}$_Core1 = 1.05 V at 1000 MHz | 0.0125 | — |
| Per Core voltage Supply | $V_{DD}$_Core0/$V_{DD}$_Core1 = 0.95 V at 1067 MHz | 11.50 | 5 |
| Per Core PLL voltage supply | $AV_{DD}$_Core0/$AV_{DD}$_Core1 = 0.95 V at 1067 MHz | 0.0125 | 5 |
| DDR Controller I/O voltage supply | D*n*_$GV_{DD}$ = 2.5 V at 400 MHz | 0.80 | 2, 6 |
| | D*n*_$GV_{DD}$ = 1.8 V at 533 MHz | 0.68 | 2, 6 |

**Table 5. MPC8640D Individual Supply Maximum Power Dissipation (continued)[1]**

| Component Description | Supply Voltage (Volts) | Power (Watts) | Notes |
|---|---|---|---|
| 16-bit FIFO @ 200 MHz eTsec 1&2/3&4 Voltage Supply | $L/TV_{DD}$ = 3.3 V | 0.11 | 2, 3, 6 |
| non-FIFO eTsec*n* Voltage Supply | $L/TV_{DD}$ = 3.3 V | 0.08 | 2, 6 |
| x8 SerDes transceiver Supply | $SV_{DD}$ = 1.05 V | 0.70 | 2, 6 |
| x8 SerDes I/O Supply | $XV_{DD}$_SRDS*n* = 1.05 V | 0.66 | 2, 6 |
| SerDes PLL voltage supply Port 1 or 2 | $AV_{DD}$_SRDS1/$AV_{DD}$_SRDS2 = 1.05 V | 0.10 | 2, 6 |
| Platform I/O Supply | $OV_{DD}$ = 3.3 V | 0.45 | 4, 6 |
| Platform source Supply | $V_{DD}$_PLAT = 1.05 V at 533 MHz | 3.5 | — |
| Platform source Supply | $V_{DD}$_PLAT = 1.05 Vn at 500 MHz | 3.5 | 5 |
| Platform, Local Bus PLL voltage Supply | $AV_{DD}$_PLAT, $AV_{DD}$_LB = 1.1 V | 0.0125 | — |

**Notes:**
1. This is a maximum power supply number which is provided for power supply and board design information. The numbers are based on 100% bus utilization for each component. The components listed are not expected to have 100% bus usage simultaneously for all components. Actual numbers may vary based on activity.
2. Number is based on a per port/interface value.
3. This is based on one eTSEC port used. Since 16-bit FIFO mode involves two ports, the number will need to be multiplied by two for the total. The other eTSEC protocols dissipate less than this number per port. Note that the power needs to be multiplied by the number of ports used for the protocol for the total eTSEC port power dissipation.
4. Platform I/O includes local bus, DUART, $I^2C$, DMA, multiprocessor interrupts, system control and clocking, debug, test, power management, JTAG and miscellaneous I/O voltage.
5. Power numbers with $V_{DD}$_Core*n* = 0.95 V and $V_{DD}$_PLAT = 1.05 V are for Part Number MC8640xxx1067Nz only.
6. The maximum power supply number for the I/Os are estimates.

The power dissipation for the MPC8640 single core device is shown in Table 6.

**Table 6. MPC8640 Power Dissipation (Single Core)**

| Power Mode | Core Frequency (MHz) | Platform Frequency (MHz) | $V_{DD}$_Coren, $V_{DD}$_PLAT (Volts) | Junction Temperature | Power (Watts) | Notes |
|---|---|---|---|---|---|---|
| Typical | 1250 MHz | 500 MHz | 1.05 V | 65 °C | 13.3 | 1, 2 |
| Thermal | | | | 105 °C | 16.5 | 1, 3 |
| Maximum | | | | | 19 | 1, 4 |
| Typical | 1000 MHz | 500 MHz | 1.05 V | 65 °C | 11.9 | 1, 2 |
| Thermal | | | | 105 °C | 14.8 | 1, 3 |
| Maximum | | | | | 17 | 1, 4 |

**Table 6. MPC8640 Power Dissipation (Single Core) (continued)**

| Power Mode | Core Frequency (MHz) | Platform Frequency (MHz) | $V_{DD}$_Coren, $V_{DD}$_PLAT (Volts) | Junction Temperature | Power (Watts) | Notes |
|---|---|---|---|---|---|---|
| Typical | 1067 MHz | 533 MHz | 0.95 V, 1.05 V | 65 °C | 10.1 | 1, 2, 5 |
| Thermal | | | | 105 °C | 12.3 | 1, 3, 5 |
| Maximum | | | | | 14 | 1, 4, 5 |

**Notes:**
1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured at the nominal recommended core voltage ($V_{DD}$_Core*n*) and 65 °C junction temperature (see Table 2) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz.
3. Thermal power is the average power measured at nominal core voltage ($V_{DD}$_Core*n*) and maximum operating junction temperature (see Table 2) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz and a typical workload on platform interfaces.
4. Maximum power is the maximum power measured at nominal core voltage ($V_{DD}$_Core*n*) and maximum operating junction temperature (see Table 2) while running a test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep all the execution units maximally busy.
5. These power numbers are for Part Number MC8640Dwxx1067Nz and MC8640wxx1067Nz only. $V_{DD}$_Core*n* = 0.95 V and $V_{DD}$_PLAT = 1.05 V.

# 4 Input Clocks

Table provides the system clock (SYSCLK) DC specifications for the MPC8640.

**Table 7. SYSCLK DC Electrical Characteristics ($OV_{DD}$ = 3.3 V ± 165 mV)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current ($V_{IN}$ [1] = 0 V or $V_{IN}$ = $V_{DD}$) | $I_{IN}$ | — | ±5 | μA |

**Note:**
1. Note that the symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.

## 4.1 System Clock Timing

Table 8 provides the system clock (SYSCLK) AC timing specifications for the MPC8640.

**Table 8. SYSCLK AC Timing Specifications**

At recommended operating conditions (see Table 2) with $OV_{DD}$ = 3.3 V ± 165 mV.

| Parameter | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| SYSCLK frequency | $f_{SYSCLK}$ | 66 | — | 166.66 | MHz | 1 |
| SYSCLK cycle time | $t_{SYSCLK}$ | 6 | — | — | ns | — |

**Table 8. SYSCLK AC Timing Specifications (continued)**

At recommended operating conditions (see Table 2) with $OV_{DD}$ = 3.3 V ± 165 mV.

| Parameter | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| SYSCLK rise and fall time | $t_{KH}$, $t_{KL}$ | 0.6 | 1.0 | 1.2 | ns | 2 |
| SYSCLK duty cycle | $t_{KHK}/t_{SYSCLK}$ | 40 | — | 60 | % | 3 |
| SYSCLK jitter | — | — | — | 150 | ps | 4, 5 |

**Notes:**
1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 18.2, "MPX to SYSCLK PLL Ratio," and Section 18.3, "e600 to MPX clock PLL Ratio," for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.4 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the short term jitter only and is guaranteed by design.
5. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter. Note that the frequency modulation for SYSCLK reduces significantly for the spread spectrum source case. This is to guarantee what is supported based on design.

### 4.1.1 SYSCLK and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter to diffuse the EMI spectral content. The jitter specification given in Table 8 considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet the MPC8640 input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the MPC8640 is compatible with spread spectrum sources if the recommendations listed in Table 9 are observed.

**Table 9. Spread Spectrum Clock Source Recommendations**

At recommended operating conditions. See Table 2.

| Parameter | Min | Max | Unit | Notes |
|---|---|---|---|---|
| Frequency modulation | — | 50 | kHz | 1 |
| Frequency spread | — | 1.0 | % | 1, 2 |

**Notes:**
1. Guaranteed by design.
2. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 8.

It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e600 core frequency should avoid violating the stated limits by using down-spreading only.

SD*n*_REF_CLK and $\overline{\text{SD}n\text{_REF_CLK}}$ were designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30-33 kHz rate is allowed), assuming both ends have same reference clock. For better results, use a source without significant unintended modulation.

## 4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (MPX clock). The output of the sampling latch is then used as an input to the counters of the PIC. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2× the period of the MPX clock. That is, minimum clock high time is $2 \times t_{MPX}$, and minimum clock low time is $2 \times t_{MPX}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

## 4.3 eTSEC Gigabit Reference Clock Timing

Table 10 provides the eTSEC gigabit reference clocks (EC1_GTX_CLK125 and EC2_GTX_CLK125) AC timing specifications for the MPC8640.

**Table 10. EC*n*_GTX_CLK125 AC Timing Specifications**

| Parameter | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| EC*n*_GTX_CLK125 frequency | $f_{G125}$ | — | 125 ± 100 ppm | — | MHz | 3 |
| EC*n*_GTX_CLK125 cycle time | $t_{G125}$ | — | 8 | — | ns | — |
| EC*n*_GTX_CLK125 peak-to-peak jitter | $t_{G125J}$ | — | — | 250 | ps | 1 |
| EC*n*_GTX_CLK125 duty cycle<br>GMII, TBI<br>1000Base-T for RGMII, RTBI | $t_{G125H}/t_{G125}$ | <br>45<br>47 | — | <br>55<br>53 | % | 1, 2 |

**Notes:**
1. Timing is guaranteed by design and characterization.
2. EC*n*_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC*n*_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.6, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.
3. ±100 ppm tolerance on EC*n*_GTX_CLK125 frequency.

**NOTE**

The phase between the output clocks TSEC1_GTX_CLK and TSEC2_GTX_CLK (ports 1 and 2) is no more than 100 ps. The phase between the output clocks TSEC3_GTX_CLK and TSEC4_GTX_CLK (ports 3 and 4) is no more than 100 ps.

## 4.4 Platform Frequency Requirements for PCI-Express and Serial RapidIO

The MPX platform clock frequency must be considered for proper operation of the high-speed PCI Express and Serial RapidIO interfaces as described below.

For proper PCI Express operation, the MPX clock frequency must be greater than or equal to:

$$\frac{527\ \text{MHz} \times (\text{PCI-Express link width})}{16 / (1 + \text{cfg_plat_freq})}$$

Note that at MPX = 400 MHz, cfg_plat_freq = 0 and at MPX > 400 MHz, cfg_plat_freq = 1. Therefore, when operating PCI Express in x8 link width, the MPX platform frequency must be 400 MHz with cfg_plat_freq = 0 or greater than or equal to 527 MHz with cfg_plat_freq = 1.

For proper Serial RapidIO operation, the MPX clock frequency must be greater than or equal to:

$$\frac{2 \times (0.8512) \times (\text{Serial RapidIO interface frequency}) \times (\text{Serial RapidIO link width})}{64}$$

## 4.5 Other Input Clocks

For information on the input clocks of other functional blocks of the platform such as SerDes, and eTSEC, see the specific section of this document.

# 5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the MPC8640. Table 11 provides the RESET initialization AC timing specifications.

**Table 11. RESET Initialization Timing Specifications**

| Parameter | Min | Max | Unit | Notes |
|---|---|---|---|---|
| Required assertion time of $\overline{\text{HRESET}}$ | 100 | — | μs | — |
| Minimum assertion time for $\overline{\text{SRESET_0}}$ & $\overline{\text{SRESET_1}}$ | 3 | — | SYSCLKs | 1 |
| Platform PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation | 100 | — | μs | 2 |
| Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$ | 4 | — | SYSCLKs | 1 |
| Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$ | 2 | — | SYSCLKs | 1 |
| Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$ | — | 5 | SYSCLKs | 1 |

**Notes:**
1. SYSCLK is the primary clock input for the MPC8640.
2 This is related to $\overline{\text{HRESET}}$ assertion time. Stable PLL configuration inputs are required when a stable SYSCLK is applied. See the *MPC8641D Integrated Host Processor Reference Manual* for more details on the power-on reset sequence.

Table 12 provides the PLL lock times.

**Table 12. PLL Lock Times**

| Parameter | Min | Max | Unit | Notes |
|---|---|---|---|---|
| (Platform and E600) PLL lock times | — | 100 | μs | 1 |
| Local bus PLL | — | 50 | μs | — |

**Notes:**
1.The PLL lock time for e600 PLLs require an additional 255 MPX_CLK cycles.

# 6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8640. Note that DDR SDRAM is D*n*_$GV_{DD}$(typ) = 2.5 V and DDR2 SDRAM is D*n*_$GV_{DD}$(typ) = 1.8 V.

## 6.1 DDR SDRAM DC Electrical Characteristics

Table 13 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8640 when D*n*_$GV_{DD}$(typ) = 1.8 V.

**Table 13. DDR2 SDRAM DC Electrical Characteristics for D*n*_$GV_{DD}$(typ) = 1.8 V**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| I/O supply voltage | D*n*_$GV_{DD}$ | 1.71 | 1.89 | V | 1 |
| I/O reference voltage | D*n*_$MV_{REF}$ | 0.49 × D*n*_$GV_{DD}$ | 0.51 × D*n*_$GV_{DD}$ | V | 2 |
| I/O termination voltage | $V_{TT}$ | D*n*_$MV_{REF}$ – 0.04 | D*n*_$MV_{REF}$ + 0.04 | V | 3 |
| Input high voltage | $V_{IH}$ | D*n*_$MV_{REF}$ + 0.125 | D*n*_$GV_{DD}$ + 0.3 | V | — |
| Input low voltage | $V_{IL}$ | –0.3 | D*n*_$MV_{REF}$ – 0.125 | V | — |
| Output leakage current | $I_{OZ}$ | –50 | 50 | μA | 4 |
| Output high current ($V_{OUT}$ = 1.420 V) | $I_{OH}$ | –13.4 | — | mA | — |
| Output low current ($V_{OUT}$ = 0.280 V) | $I_{OL}$ | 13.4 | — | mA | — |

**Notes:**
1. D*n*_$GV_{DD}$ is expected to be within 50 mV of the DRAM D*n*_$GV_{DD}$ at all times.
2. D*n*_$MV_{REF}$ is expected to be equal to 0.5 × D*n*_$GV_{DD}$, and to track D*n*_$GV_{DD}$ DC variations as measured at the receiver. Peak-to-peak noise on D*n*_$MV_{REF}$ may not exceed ±2% of the DC value.
3. $V_{TT}$ is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to D*n*_$MV_{REF}$. This rail should track variations in the DC level of D*n*_$MV_{REF}$.
4. Output leakage is measured with all outputs disabled, 0 V ≤ $V_{OUT}$ ≤ D*n*_$GV_{DD}$.

Table 14 provides the DDR2 capacitance when Dn_$GV_{DD(typ)}$ = 1.8 V.

**Table 14. DDR2 SDRAM Capacitance for D*n*_$GV_{DD}$(typ)=1.8 V**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input/output capacitance: DQ, DQS, $\overline{\text{DQS}}$ | $C_{IO}$ | 6 | 8 | pF | 1 |
| Delta input/output capacitance: DQ, DQS, $\overline{\text{DQS}}$ | $C_{DIO}$ | — | 0.5 | pF | 1 |

**Note:**
1. This parameter is sampled. D*n*_$GV_{DD}$ = 1.8 V ± 0.090 V, f = 1 MHz, $T_A$ = 25°C, $V_{OUT}$ = D*n*_$GV_{DD}$ ÷ 2, $V_{OUT(peak\text{-}to\text{-}peak)}$ = 0.2 V.

Table 15 provides the recommended operating conditions for the DDR SDRAM component(s) when D*n*_$GV_{DD}$(typ) = 2.5 V.

**Table 15. DDR SDRAM DC Electrical Characteristics for D*n*_$GV_{DD}$ (typ) = 2.5 V**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| I/O supply voltage | D*n*_$GV_{DD}$ | 2.375 | 2.625 | V | 1 |
| I/O reference voltage | D*n*_$MV_{REF}$ | 0.49 × D*n*_$GV_{DD}$ | 0.51 × D*n*_$GV_{DD}$ | V | 2 |
| I/O termination voltage | $V_{TT}$ | D*n*_$MV_{REF}$ – 0.04 | D*n*_$MV_{REF}$ + 0.04 | V | 3 |
| Input high voltage | $V_{IH}$ | D*n*_$MV_{REF}$ + 0.15 | D*n*_$GV_{DD}$ + 0.3 | V | — |
| Input low voltage | $V_{IL}$ | –0.3 | D*n*_$MV_{REF}$ – 0.15 | V | — |
| Output leakage current | $I_{OZ}$ | –50 | 50 | μA | 4 |
| Output high current ($V_{OUT}$ = 1.95 V) | $I_{OH}$ | –16.2 | — | mA | — |
| Output low current ($V_{OUT}$ = 0.35 V) | $I_{OL}$ | 16.2 | — | mA | — |

**Notes:**
1. D*n*_$GV_{DD}$ is expected to be within 50 mV of the DRAM D*n*_$GV_{DD}$ at all times.
2. $MV_{REF}$ is expected to be equal to 0.5 × D*n*_$GV_{DD}$, and to track D*n*_$GV_{DD}$ DC variations as measured at the receiver. Peak-to-peak noise on D*n*_$MV_{REF}$ may not exceed ±2% of the DC value.
3. $V_{TT}$ is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to D*n*_$MV_{REF}$. This rail should track variations in the DC level of D*n*_$MV_{REF}$.
4. Output leakage is measured with all outputs disabled, 0 V ≤ $V_{OUT}$ ≤ D*n*_$GV_{DD}$.

Table 16 provides the DDR capacitance when D*n*_$GV_{DD}$ (typ) = 2.5 V.

**Table 16. DDR SDRAM Capacitance for D*n*_$GV_{DD}$ (typ) = 2.5 V**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input/output capacitance: DQ, DQS | $C_{IO}$ | 6 | 8 | pF | 1 |
| Delta input/output capacitance: DQ, DQS | $C_{DIO}$ | — | 0.5 | pF | 1 |

**Note:**
1. This parameter is sampled. D*n*_$GV_{DD}$ = 2.5 V ± 0.125 V, f = 1 MHz, $T_A$ = 25°C, $V_{OUT}$ = D*n*_GVDD/2, $V_{OUT}$ (peak-to-peak) = 0.2 V.

Table 17 provides the current draw characteristics for $MV_{REF}$.

**Table 17. Current Draw Characteristics for $MV_{REF}$**

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Current draw for $MV_{REF}$ | $I_{MVREF}$ | — | 500 | μA | 1 |

1. The voltage regulator for $MV_{REF}$ must be able to supply up to 500 μA current.

## 6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

### 6.2.1 DDR SDRAM Input AC Timing Specifications

Table 18 provides the input AC timing specifications for the DDR2 SDRAM when D*n*_$GV_{DD(typ)}$ = 1.8 V.

**Table 18. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface**

At recommended operating conditions (see Table 2)

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| AC input low voltage | $V_{IL}$ | — | D*n*_$MV_{REF}$ – 0.25 | V | — |
| AC input high voltage | $V_{IH}$ | D*n*_$MV_{REF}$ + 0.25 | — | V | — |

Table 19 provides the input AC timing specifications for the DDR SDRAM when D*n*_$GV_{DD(typ)}$ = 2.5 V.

**Table 19. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface**

At recommended operating conditions (see Table 2)

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| AC input low voltage | $V_{IL}$ | — | D*n*_$MV_{REF}$ – 0.31 | V | — |
| AC input high voltage | $V_{IH}$ | D*n*_$MV_{REF}$ + 0.31 | — | V | — |

Table 20 provides the input AC timing specifications for the DDR SDRAM interface.

**Table 20. DDR SDRAM Input AC Timing Specifications**

At recommended operating conditions (see Table 2)

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Controller Skew for MDQS—MDQ/MECC | $t_{CISKEW}$ | — | — | ps | 1, 2 |
| 533 MHz | — | –300 | 300 | — | 3 |
| 400 MHz | — | –365 | 365 | — | — |

**Note:**

1. $t_{CISKEW}$ represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called $t_{DISKEW}$.This can be determined by the following equation: $t_{DISKEW}$ = ±(T ³ 4 – abs($t_{CISKEW}$)) where T is the clock period and abs($t_{CISKEW}$) is the absolute value of $t_{CISKEW}$.
3. Maximum DDR1 frequency is 400 MHz.

Figure 4 shows the DDR SDRAM input timing for the MDQS to MDQ skew measurement (tDISKEW).

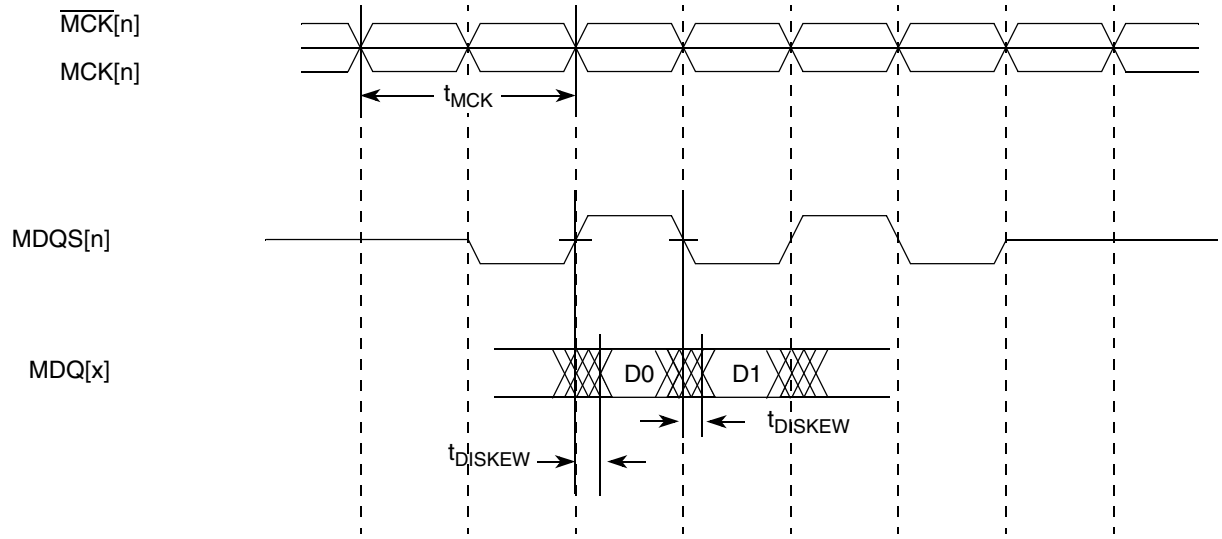



**Figure 4. DDR Input Timing Diagram for tDISKEW**

## 6.2.2 DDR SDRAM Output AC Timing Specifications

**Table 21. DDR SDRAM Output AC Timing Specifications**

At recommended operating conditions (see Table 2).

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| MCK[n] cycle time, MCK[n]/$\overline{\text{MCK}}$[n] crossing | $t_{MCK}$ | 3 | 10 | ns | 2 |
| MCK duty cycle | $t_{MCKH}/t_{MCK}$ | | | % | |
| 533 MHz | | 47 | 53 | | 8 |
| 400 MHz | | 47 | 53 | | 8 |
| ADDR/CMD output setup with respect to MCK | $t_{DDKHAS}$ | | | ns | 3 |
| 533 MHz | | 1.48 | — | | 7 |
| 400 MHz | | 1.95 | — | | |
| ADDR/CMD output hold with respect to MCK | $t_{DDKHAX}$ | | | ns | 3 |
| 533 MHz | | 1.48 | — | | 7 |
| 400 MHz | | 1.95 | — | | |
| $\overline{\text{MCS}}$[n] output setup with respect to MCK | $t_{DDKHCS}$ | | | ns | 3 |
| 533 MHz | | 1.48 | — | | 7 |
| 400 MHz | | 1.95 | — | | |
| $\overline{\text{MCS}}$[n] output hold with respect to MCK | $t_{DDKHCX}$ | | | ns | 3 |
| 533 MHz | | 1.48 | — | | 7 |
| 400 MHz | | 1.95 | — | | |
| MCK to MDQS Skew | $t_{DDKHMH}$ | –0.6 | 0.6 | ns | 4 |

**Table 21. DDR SDRAM Output AC Timing Specifications (continued)**

At recommended operating conditions (see Table 2).

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| MDQ/MECC/MDM output setup with respect to MDQS | $t_{DDKHDS}$, $t_{DDKLDS}$ | | | ps | 5 |
| 533 MHz | | 590 | — | | 7 |
| 400 MHz | | 700 | — | | |
| MDQ/MECC/MDM output hold with respect to MDQS | $t_{DDKHDX}$, $t_{DDKLDX}$ | | | ps | 5 |
| 533 MHz | | 590 | — | | 7 |
| 400 MHz | | 700 | — | | |
| MDQS preamble start | $t_{DDKHMP}$ | $-0.5 \times t_{MCK} - 0.6$ | $-0.5 \times t_{MCK} + 0.6$ | ns | 6 |
| MDQS epilogue end | $t_{DDKHME}$ | –0.6 | 0.6 | ns | 6 |

**Note:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, $t_{DDKHAS}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, $t_{DDKLDX}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that $t_{DDKHMH}$ follows the symbol conventions described in note 1. For example, $t_{DDKHMH}$ describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). $t_{DDKHMH}$ can be modified through control of the DQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8641 Integrated Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that $t_{DDKHMP}$ follows the symbol conventions described in note 1.
7. Maximum DDR1 frequency is 400 MHz
8. Per the JEDEC spec the DDR2 duty cycle at 400 and 533 MHz is the low and high cycle time values.

## NOTE

For the ADDR/CMD setup and hold specifications in Table 21, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.

Figure 5 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement ($t_{DDKHMH}$).

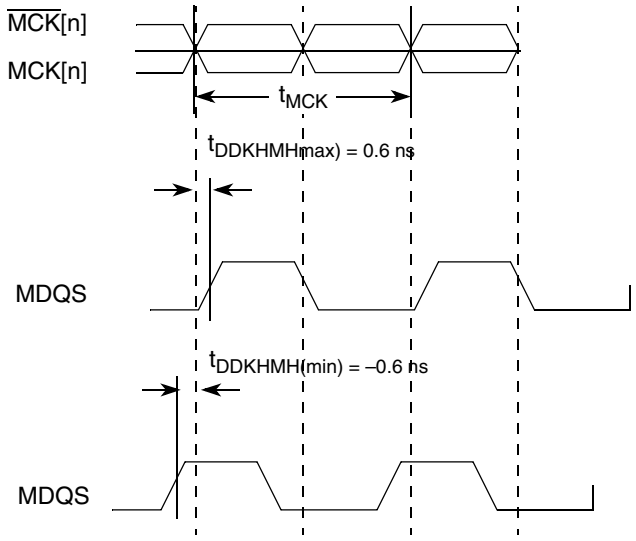



**Figure 5. Timing Diagram for tDDKHMH**

Figure 6 shows the DDR SDRAM output timing diagram.

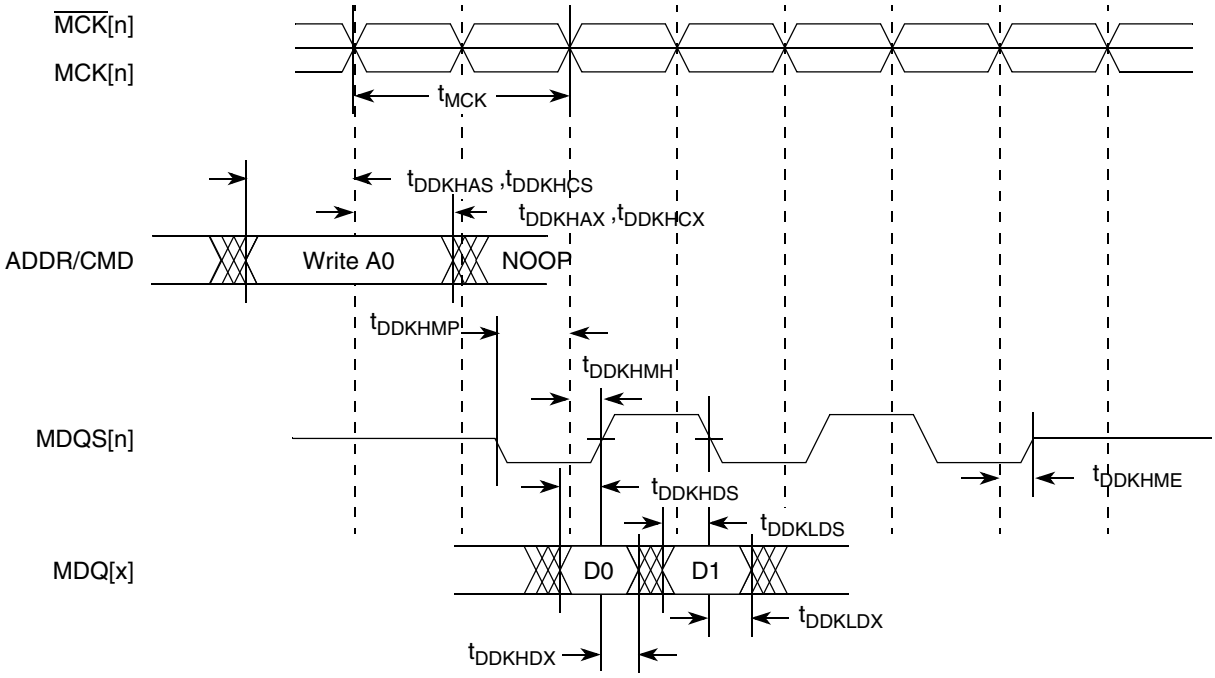



**Figure 6. DDR SDRAM Output Timing Diagram**

Figure 7 provides the AC test load for the DDR bus.

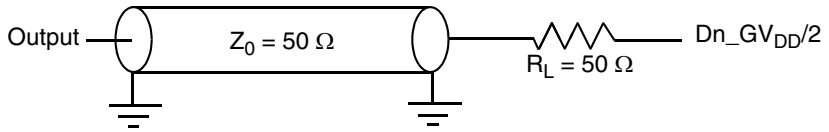



**Figure 7. DDR AC Test Load**

# 7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8640.

## 7.1 DUART DC Electrical Characteristics

Table 22 provides the DC electrical characteristics for the DUART interface.

**Table 22. DUART DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current ($V_{IN}$ [1] = 0 V or $V_{IN}$ = $V_{DD}$) | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage ($OV_{DD}$ = min, $I_{OH}$ = –100 μA) | $V_{OH}$ | $OV_{DD}$ – 0.2 | — | V |
| Low-level output voltage ($OV_{DD}$ = min, $I_{OL}$ = 100 μA) | $V_{OL}$ | — | 0.2 | V |

**Note:**
1. Note that the symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.

## 7.2 DUART AC Electrical Specifications

Table 23 provides the AC timing parameters for the DUART interface.

**Table 23. DUART AC Timing Specifications**

| Parameter | Value | Unit | Notes |
|---|---|---|---|
| Minimum baud rate | MPX clock/1,048,576 | baud | 1,2 |
| Maximum baud rate | MPX clock/16 | baud | 1,3 |
| Oversample rate | 16 | — | 1,4 |

**Notes:**
1. Guaranteed by design.
2. MPX clock refers to the platform clock.
3. Actual attainable baud rate will be limited by the latency of interrupt processing.
4. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

# 8 Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management

This section provides the AC and DC electrical characteristics for enhanced three-speed and MII management.

## 8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII and TBI interfaces can be operated at 3.3 or 2.5 V. Whether the GMII or TBI interface is operated at 3.3 or 2.5 V, the timing is compliant with the IEEE 802.3 standard. The RGMII and RTBI interfaces follow the Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3 (12/10/2000). The RMII interface follows the RMII Consortium RMII Specification Version 1.2 (3/20/1998). The electrical characteristics for MDIO and MDC are specified in Section 9, "Ethernet Management Interface Electrical Characteristics."

### 8.1.1 eTSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RMII and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 24 and Table 25. The potential applied to the input of a GMII, MII, TBI, RGMII, RMII or RTBI receiver may exceed the potential of the receiver's power supply (that is, a GMII driver powered from a 3.6-V supply driving $V_{OH}$ into a GMII receiver powered from a 2.5-V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

**Table 24. GMII, MII, RMII, TBI and FIFO DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Supply voltage 3.3 V | $LV_{DD}$<br>$TV_{DD}$ | 3.135 | 3.465 | V | 1, 2 |
| Output high voltage<br>($LV_{DD}/TV_{DD}$ = Min, $I_{OH}$ = –4.0 mA) | $V_{OH}$ | 2.40 | — | V | — |
| Output low voltage<br>($LV_{DD}/TV_{DD}$ = Min, $I_{OL}$ = 4.0 mA) | $V_{OL}$ | — | 0.50 | V | — |
| Input high voltage | $V_{IH}$ | 2.0 | — | V | — |

**Table 24. GMII, MII, RMII, TBI and FIFO DC Electrical Characteristics (continued)**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input low voltage | $V_{IL}$ | — | 0.90 | V | — |
| Input high current ($V_{IN}$ = $LV_{DD}$, $V_{IN}$ = $TV_{DD}$) | $I_{IH}$ | — | 40 | μA | 1, 2, 3 |
| Input low current ($V_{IN}$ = GND) | $I_{IL}$ | –600 | — | μA | 3 |

**Notes:**
1. $LV_{DD}$ supports eTSECs 1 and 2
2. $TV_{DD}$ supports eTSECs 3 and 4
3. The symbol $V_{IN}$, in this case, represents the $LV_{IN}$ and $TV_{IN}$ symbols referenced in Table 1 and Table 2

**Table 25. GMII, RGMII, RTBI, TBI and FIFO DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Supply voltage 2.5 V | $LV_{DD}$/$TV_{DD}$ | 2.375 | 2.625 | V | 1, 2 |
| Output high voltage ($LV_{DD}$/$TV_{DD}$ = Min, $I_{OH}$ = –1.0 mA) | $V_{OH}$ | 2.00 | — | V | — |
| Output low voltage ($LV_{DD}$/$TV_{DD}$ = Min, $I_{OL}$ = 1.0 mA) | $V_{OL}$ | — | 0.40 | V | — |
| Input high voltage | $V_{IH}$ | 1.70 | — | V | — |
| Input low voltage | $V_{IL}$ | — | 0.90 | V | — |
| Input high current ($V_{IN}$ = $LV_{DD}$, $V_{IN}$ = $TV_{DD}$) | $I_{IH}$ | — | 10 | μA | 1, 2, 3 |
| Input low current ($V_{IN}$ = GND) | $I_{IL}$ | –15 | — | μA | 3 |

**Note:**

1 $LV_{DD}$ supports eTSECs 1 and 2.
2 $TV_{DD}$ supports eTSECs 3 and 4.
3 Note that the symbol $V_{IN}$, in this case, represents the $LV_{IN}$ and $TV_{IN}$ symbols referenced in Table 1 and Table 2.

## 8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII and RTBI are presented in this section.

### 8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications because they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n*'s TSEC*n*_TX_CLK, while the receive clock must be applied to pin TSEC*n*_RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the TSEC*n*_GTX_CLK pin (while transmit data appears on TSEC*n*_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*_GTX_CLK as a source- synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is relationship between the maximum FIFO speed and the platform speed. For more information, see Section 18.4.2, "Platform to FIFO Restrictions."

**NOTE**

The phase between the output clocks TSEC1_GTX_CLK and TSEC2_GTX_CLK (ports 1 and 2) is no more than 100 ps. The phase between the output clocks TSEC3_GTX_CLK and TSEC4_GTX_CLK (ports 3 and 4) is no more than 100 ps.

A summary of the FIFO AC specifications appears in Table 26 and Table 27.

**Table 26. FIFO Mode Transmit AC Timing Specification**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5% and 2.5 V ± 5%.

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TX_CLK, GTX_CLK clock period (GMII mode) | $t_{FIT}$ | 8.4 | 8.0 | 100 | ns |
| TX_CLK, GTX_CLK clock period (Encoded mode) | $t_{FIT}$ | 6.4 | 8.0 | 100 | ns |
| TX_CLK, GTX_CLK duty cycle | $t_{FITH}/t_{FIT}$ | 45 | 50 | 55 | % |
| TX_CLK, GTX_CLK peak-to-peak jitter | $t_{FITJ}$ | — | — | 250 | ps |
| Rise time TX_CLK (20%–80%) | $t_{FITR}$ | — | — | 0.75 | ns |
| Fall time TX_CLK (80%–20%) | $t_{FITF}$ | — | — | 0.75 | ns |
| FIFO data TXD[7:0], TX_ER, TX_EN setup time to GTX_CLK | $t_{FITDV}$ | 2.0 | — | — | ns |
| GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time | $t_{FITDX}$ | 0.5 | — | 3.0 | ns |

**Table 27. FIFO Mode Receive AC Timing Specification**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5% and 2.5 V ± 5%.

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period (GMII mode) | $t_{FIR}$[1] | 8.4 | 8.0 | 100 | ns |
| RX_CLK clock period (Encoded mode) | $t_{FIR}$[1] | 6.4 | 8.0 | 100 | ns |
| RX_CLK duty cycle | $t_{FIRH}/t_{FIR}$ | 45 | 50 | 55 | % |
| RX_CLK peak-to-peak jitter | $t_{FIRJ}$ | — | — | 250 | ps |

**Table 27. FIFO Mode Receive AC Timing Specification (continued)**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5% and 2.5 V ± 5%.

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Rise time RX_CLK (20%–80%) | $t_{FIRR}$ | — | — | 0.75 | ns |
| Fall time RX_CLK (80%–20%) | $t_{FIRF}$ | — | — | 0.75 | ns |
| RXD[7:0], RX_DV, RX_ER setup time to RX_CLK | $t_{FIRDV}$ | 1.5 | — | — | ns |
| RXD[7:0], RX_DV, RX_ER hold time to RX_CLK | $t_{FIRDX}$ | 0.5 | — | — | ns |

[1] ±100 ppm tolerance on RX_CLK frequency

Timing diagrams for FIFO appear in Figure 8 and Figure 9.

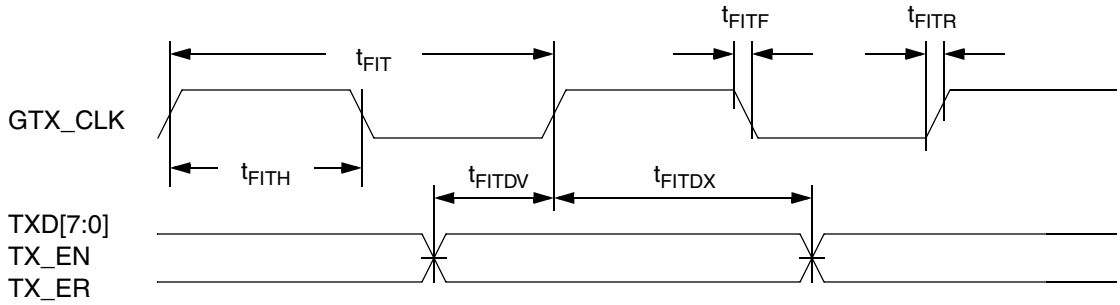



**Figure 8. FIFO Transmit AC Timing Diagram**

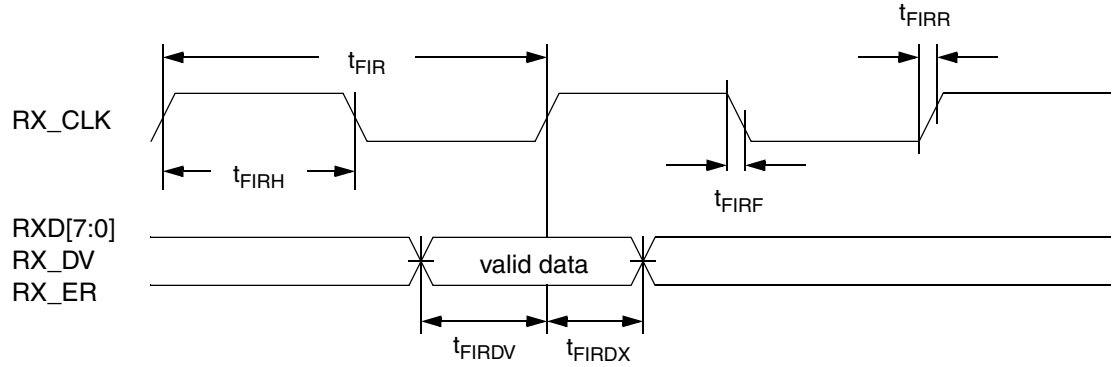



**Figure 9. FIFO Receive AC Timing Diagram**

## 8.2.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

### 8.2.2.1 GMII Transmit AC Timing Specifications

Table 28 provides the GMII transmit AC timing specifications.

**Table 28. GMII Transmit AC Timing Specifications**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5% and 2.5 V ± 5%.

| Parameter | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| GMII data TXD[7:0], TX_ER, TX_EN setup time | $t_{GTKHDV}$ | 2.5 | — | — | ns |
| GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay | $t_{GTKHDX}$ | 0.5 | — | 5.0 | ns |
| GTX_CLK data clock rise time (20%–80%) | $t_{GTXR}$[2] | — | — | 1.0 | ns |
| GTX_CLK data clock fall time (80%–20%) | $t_{GTXF}$[2] | — | — | 1.0 | ns |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{GTKHDV}$ symbolizes GMII transmit timing (GT) with respect to the $t_{GTX}$ clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, $t_{GTKHDX}$ symbolizes GMII transmit timing (GT) with respect to the $t_{GTX}$ clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{GTX}$ represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 10 shows the GMII transmit AC timing diagram.

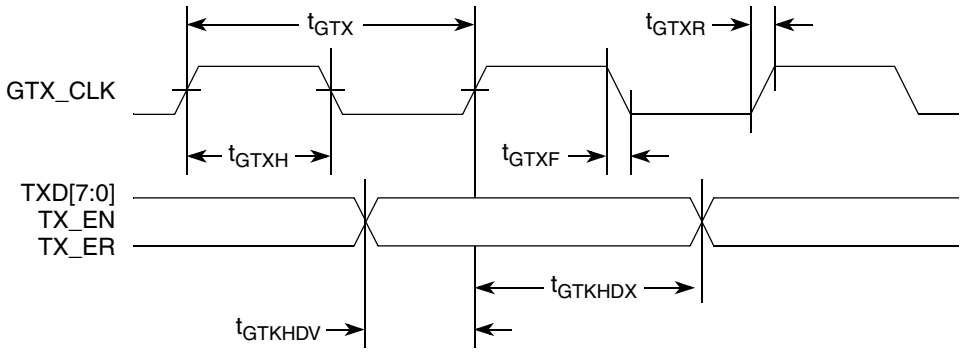



**Figure 10. GMII Transmit AC Timing Diagram**

### 8.2.2.2 GMII Receive AC Timing Specifications

Table 29 provides the GMII receive AC timing specifications.

**Table 29. GMII Receive AC Timing Specifications**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5% and 2.5 V ± 5%.

| Parameter | Symbol[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period | $t_{GRX}$[3] | — | 8.0 | — | ns |
| RX_CLK duty cycle | $t_{GRXH}/t_{GRX}$ | 40 | — | 60 | ns |
| RXD[7:0], RX_DV, RX_ER setup time to RX_CLK | $t_{GRDVKH}$ | 2.0 | — | — | ns |

**Table 29. GMII Receive AC Timing Specifications (continued)**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5% and 2.5 V ± 5%.

| Parameter | Symbol[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RXD[7:0], RX_DV, RX_ER hold time to RX_CLK | $t_{GRDXKH}$ | 0.5 | — | — | ns |
| RX_CLK clock rise time (20%–80%) | $t_{GRXR}$[2] | — | — | 1.0 | ns |
| RX_CLK clock fall time (80%-20%) | $t_{GRXF}$[2] | — | — | 1.0 | ns |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{GRDVKH}$ symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{RX}$ clock reference (K) going to the high state (H) or setup time. Also, $t_{GRDXKL}$ symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{GRX}$ clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{GRX}$ represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.
3. ±100 ppm tolerance on RX_CLK frequency

Figure 11 provides the AC test load for eTSEC.

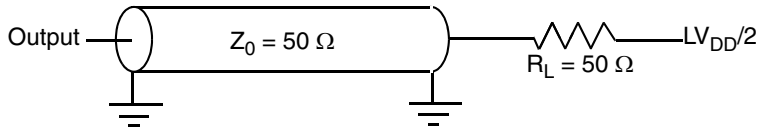



**Figure 11. eTSEC AC Test Load**

Figure 12 shows the GMII receive AC timing diagram.

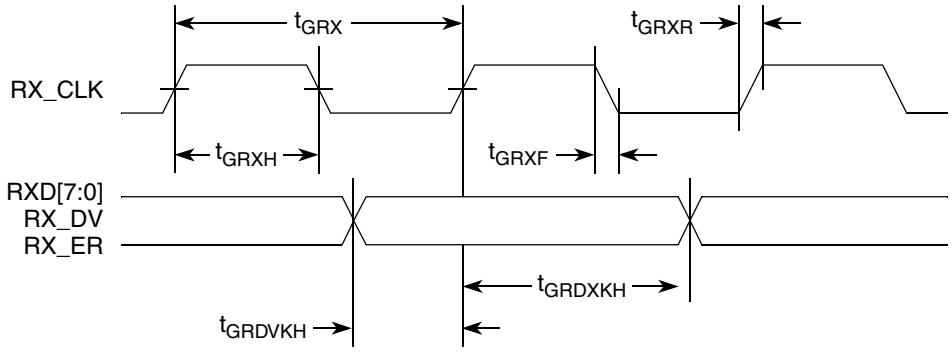



**Figure 12. GMII Receive AC Timing Diagram**

## 8.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

### 8.2.3.1 MII Transmit AC Timing Specifications

Table 30 provides the MII transmit AC timing specifications.

**Table 30. MII Transmit AC Timing Specifications**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5%.

| Parameter | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TX_CLK clock period 10 Mbps | $t_{MTX}$[2] | — | 400 | — | ns |
| TX_CLK clock period 100 Mbps | $t_{MTX}$ | — | 40 | — | ns |
| TX_CLK duty cycle | $t_{MTXH}/t_{MTX}$ | 35 | — | 65 | % |
| TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay | $t_{MTKHDX}$ | 1 | 5 | 15 | ns |
| TX_CLK data clock rise time (20%–80%) | $t_{MTXR}$[2] | 1.0 | — | 4.0 | ns |
| TX_CLK data clock fall time (80%–20%) | $t_{MTXF}$[2] | 1.0 | — | 4.0 | ns |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MTKHDX}$ symbolizes MII transmit timing (MT) for the time $t_{MTX}$ clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of $t_{MTX}$ represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 13 shows the MII transmit AC timing diagram.

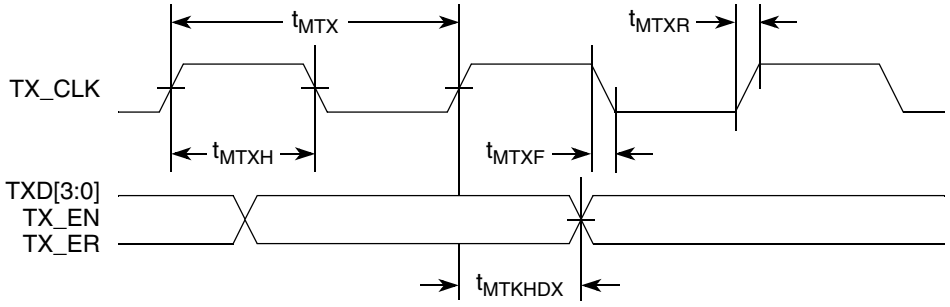



**Figure 13. MII Transmit AC Timing Diagram**

### 8.2.3.2 MII Receive AC Timing Specifications

Table 31 provides the MII receive AC timing specifications.

**Table 31. MII Receive AC Timing Specifications**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5%.

| Parameter | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period 10 Mbps | $t_{MRX}$[2,3] | — | 400 | — | ns |
| RX_CLK clock period 100 Mbps | $t_{MRX}$[3] | — | 40 | — | ns |
| RX_CLK duty cycle | $t_{MRXH}/t_{MRX}$ | 35 | — | 65 | % |
| RXD[3:0], RX_DV, RX_ER setup time to RX_CLK | $t_{MRDVKH}$ | 10.0 | — | — | ns |

**Table 31. MII Receive AC Timing Specifications (continued)**

At recommended operating conditions with $LV_{DD}/TV_{DD}$ of 3.3 V ± 5%.

| Parameter | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RXD[3:0], RX_DV, RX_ER hold time to RX_CLK | $t_{MRDXKH}$ | 10.0 | — | — | ns |
| RX_CLK clock rise time (20%–80%) | $t_{MRXR}$[2] | 1.0 | — | 4.0 | ns |
| RX_CLK clock fall time (80%–20%) | $t_{MRXF}$[2] | 1.0 | — | 4.0 | ns |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MRDVKH}$ symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MRX}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{MRDXKL}$ symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{MRX}$ clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{MRX}$ represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.
3. ±100 ppm tolerance on RX_CLK frequency

Figure 14 provides the AC test load for eTSEC.

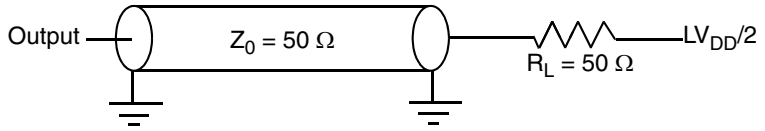



**Figure 14. eTSEC AC Test Load**

Figure 15 shows the MII receive AC timing diagram.

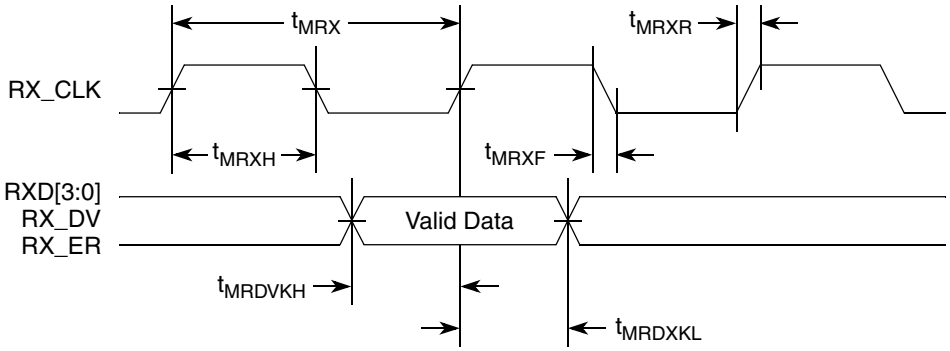



**Figure 15. MII Receive AC Timing Diagram**

## 8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

### 8.2.4.1 TBI Transmit AC Timing Specifications

Table 32 provides the TBI transmit AC timing specifications.

**Table 32. TBI Transmit AC Timing Specifications**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5% and 2.5 V ± 5%.

| Parameter | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TCG[9:0] setup time GTX_CLK going high | $t_{TTKHDV}$ | 2.0 | — | — | ns |
| TCG[9:0] hold time from GTX_CLK going high | $t_{TTKHDX}$ | 1.0 | — | — | ns |
| GTX_CLK rise time (20%–80%) | $t_{TTXR}$[2] | — | — | 1.0 | ns |
| GTX_CLK fall time (80%–20%) | $t_{TTXF}$[2] | — | — | 1.0 | ns |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state )(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{TTKHDV}$ symbolizes the TBI transmit timing (TT) with respect to the time from $t_{TTX}$ (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, $t_{TTKHDX}$ symbolizes the TBI transmit timing (TT) with respect to the time from $t_{TTX}$ (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{TTX}$ represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 16 shows the TBI transmit AC timing diagram.

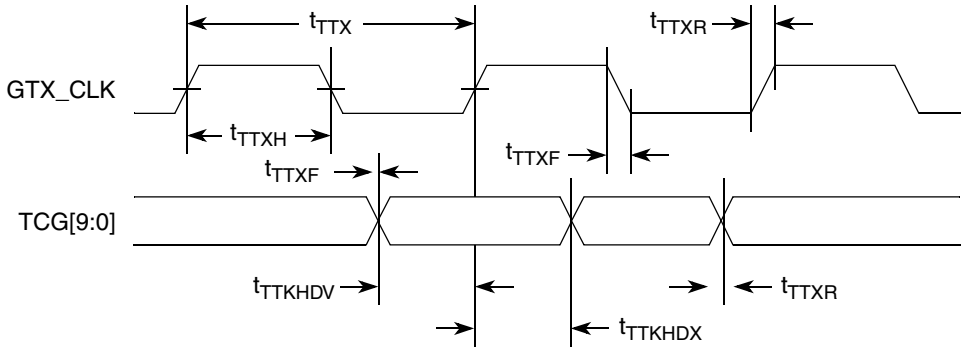



**Figure 16. TBI Transmit AC Timing Diagram**

### 8.2.4.2 TBI Receive AC Timing Specifications

Table 33 provides the TBI receive AC timing specifications.

**Table 33. TBI Receive AC Timing Specifications**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5% and 2.5 V ± 5%.

| Parameter | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| PMA_RX_CLK[0:1] clock period | $t_{TRX}$[3] | — | 16.0 | — | ns |
| PMA_RX_CLK[0:1] skew | $t_{SKTRX}$ | 7.5 | — | 8.5 | ns |
| PMA_RX_CLK[0:1] duty cycle | $t_{TRXH}/t_{TRX}$ | 40 | — | 60 | % |
| RCG[9:0] setup time to rising PMA_RX_CLK | $t_{TRDVKH}$ | 2.5 | — | — | ns |
| RCG[9:0] hold time to rising PMA_RX_CLK | $t_{TRDXKH}$ | 1.5 | — | — | ns |
| PMA_RX_CLK[0:1] clock rise time (20%–80%) | $t_{TRXR}$[2] | 0.7 | — | 2.4 | ns |
| PMA_RX_CLK[0:1] clock fall time (80%–20%) | $t_{TRXF}$[2] | 0.7 | — | 2.4 | ns |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{TRDVKH}$ symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{TRX}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{TRDXKH}$ symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{TRX}$ clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{TRX}$ represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
2. Guaranteed by design.
3. ±100 ppm tolerance on PMA_RX_CLK[0:1] frequency

Figure 17 shows the TBI receive AC timing diagram.

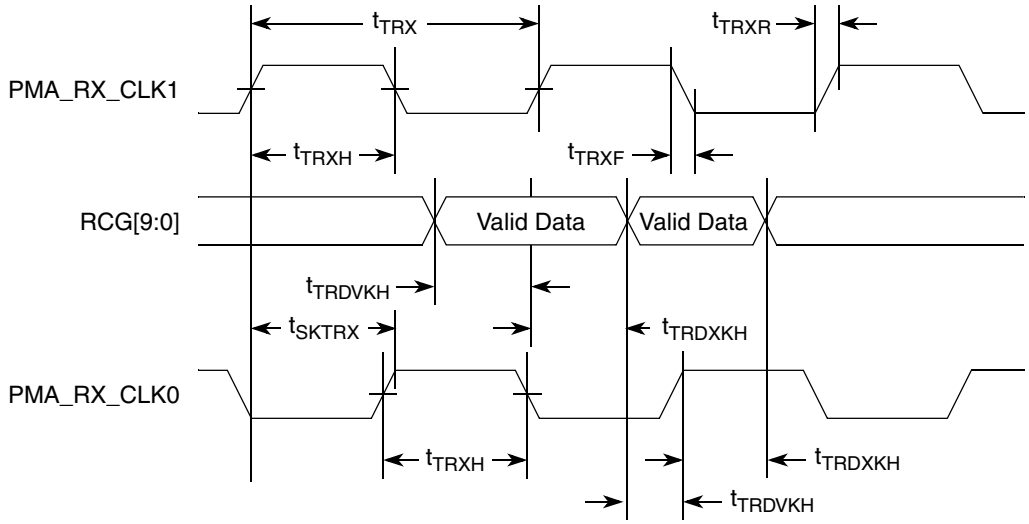



**Figure 17. TBI Receive AC Timing Diagram**

## 8.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when TBICON[CLKSEL] = 1 a 125-MHz TBI receive clock is supplied on TSEC*n*_RX_CLK pin (no receive clock is used on TSEC*n*_TX_CLK in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied on the TSEC_GTX_CLK125 pin in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in Table 34.

**Table 34. TBI single-clock Mode Receive AC Timing Specification**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5% and 2.5 V ± 5%.

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period | $t_{TRR}$[1] | 7.5 | 8.0 | 8.5 | ns |
| RX_CLK duty cycle | $t_{TRRH}/t_{TRR}$ | 40 | 50 | 60 | % |
| RX_CLK peak-to-peak jitter | $t_{TRRJ}$ | — | — | 250 | ps |
| Rise time RX_CLK (20%–80%) | $t_{TRRR}$ | — | — | 1.0 | ns |
| Fall time RX_CLK (80%–20%) | $t_{TRRF}$ | — | — | 1.0 | ns |
| RCG[9:0] setup time to RX_CLK rising edge | $t_{TRRDVKH}$ | 2.0 | — | — | ns |
| RCG[9:0] hold time to RX_CLK rising edge | $t_{TRRDXKH}$ | 1.0 | — | — | ns |

1 ±100 ppm tolerance on RX_CLK frequency

A timing diagram for TBI receive appears in Figure 18.

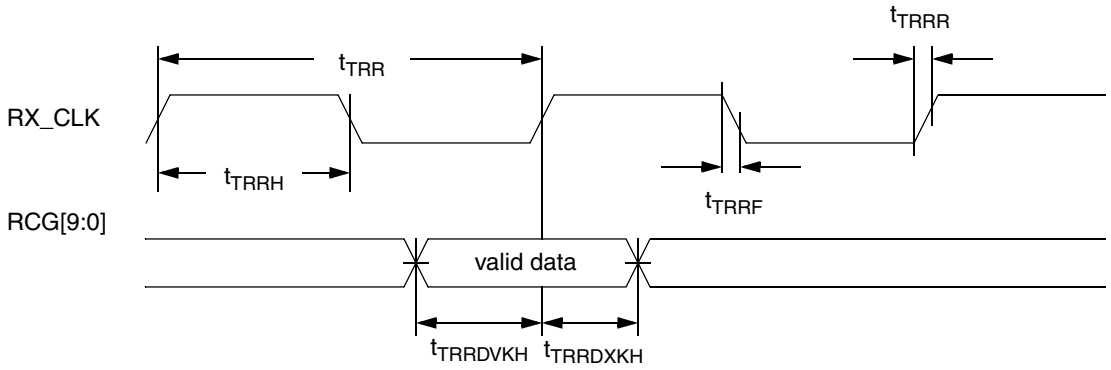



**Figure 18. TBI Single-Clock Mode Receive AC Timing Diagram**

## 8.2.6 RGMII and RTBI AC Timing Specifications

Table 35 presents the RGMII and RTBI AC timing specifications.

**Table 35. RGMII and RTBI AC Timing Specifications**

At recommended operating conditions with $L/TV_{DD}$ of 2.5 V ± 5%.

| Parameter | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Data to clock output skew (at transmitter) | $t_{SKRGT}$[5] | –500 | 0 | 500 | ps |
| Data to clock input skew (at receiver) [2] | $t_{SKRGT}$ | 1.0 | — | 2.8 | ns |
| Clock period duration [3] | $t_{RGT}$[5,6] | 7.2 | 8.0 | 8.8 | ns |
| Duty cycle for 10BASE-T and 100BASE-TX [3, 4] | $t_{RGTH}/t_{RGT}$[5] | 40 | 50 | 60 | % |
| Rise time (20%–80%) | $t_{RGTR}$[5] | — | — | 0.75 | ns |
| Fall time (80%–20%) | $t_{RGTF}$[5] | — | — | 0.75 | ns |

**Notes:**

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of $t_{RGT}$ represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, $t_{RGT}$ scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three $t_{RGT}$ of the lowest speed transitioned between.
5. Guaranteed by characterization
6. ±100 ppm tolerance on RX_CLK frequency.

Figure 19 shows the RGMII and RTBI AC timing and multiplexing diagrams.

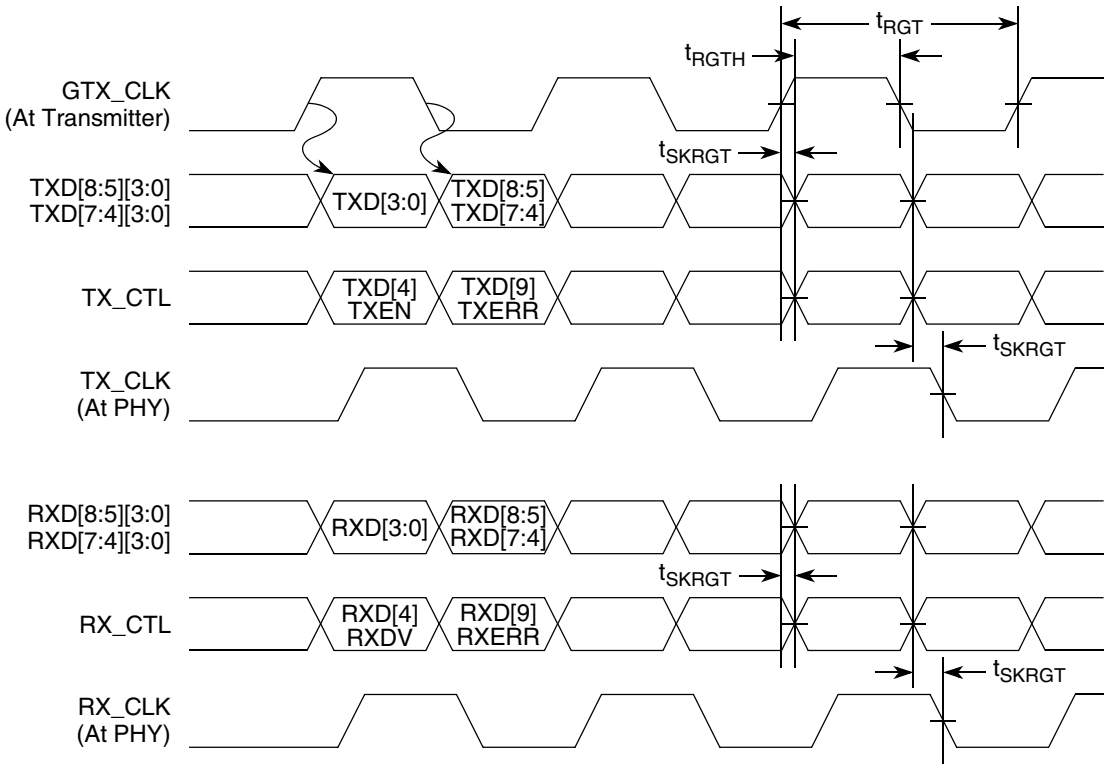



**Figure 19. RGMII and RTBI AC Timing and Multiplexing Diagrams**

## 8.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

### 8.2.7.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in Table 36.

**Table 36. RMII Transmit AC Timing Specifications**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5%.

| Parameter | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| REF_CLK clock period | $t_{RMT}$ | — | 20.0 | — | ns |
| REF_CLK duty cycle | $t_{RMTH}/t_{RMT}$ | 35 | 50 | 65 | % |
| REF_CLK peak-to-peak jitter | $t_{RMTJ}$ | — | — | 250 | ps |

**Table 36. RMII Transmit AC Timing Specifications (continued)**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5%.

| Parameter | Symbol [1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Rise time REF_CLK (20%–80%) | $t_{RMTR}$ | 1.0 | — | 2.0 | ns |
| Fall time REF_CLK (80%–20%) | $t_{RMTF}$ | 1.0 | — | 2.0 | ns |
| REF_CLK to RMII data TXD[1:0], TX_EN delay | $t_{RMTDX}$ | 1.0 | — | 10.0 | ns |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MTKHDX}$ symbolizes MII transmit timing (MT) for the time $t_{MTX}$ clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of $t_{MTX}$ represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 20 shows the RMII transmit AC timing diagram.

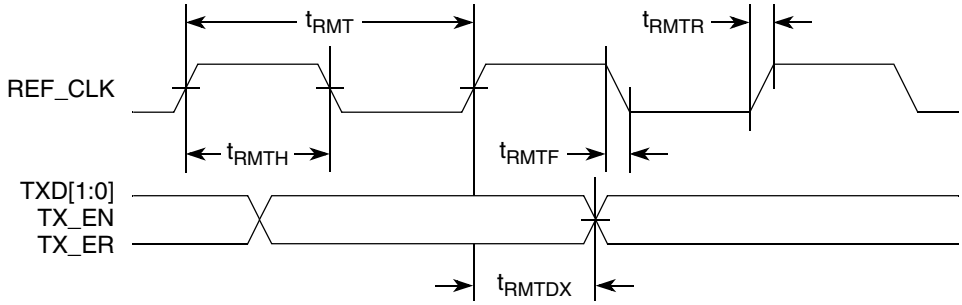



**Figure 20. RMII Transmit AC Timing Diagram**

### 8.2.7.2 RMII Receive AC Timing Specifications

Table 37 shows the RMII receive AC timing specifications.

**Table 37. RMII Receive AC Timing Specifications**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5%.

| Parameter | Symbol[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| REF_CLK clock period | $t_{RMR}$ | 15.0 | 20.0 | 25.0 | ns |
| REF_CLK duty cycle | $t_{RMRH}/t_{RMR}$ | 35 | 50 | 65 | % |
| REF_CLK peak-to-peak jitter | $t_{RMRJ}$ | — | — | 250 | ps |
| Rise time REF_CLK (20%–80%) | $t_{RMRR}$ | 1.0 | — | 2.0 | ns |

**Table 37. RMII Receive AC Timing Specifications (continued)**

At recommended operating conditions with $LV_{DD}$ of 3.3 V ± 5%.

| Parameter | Symbol[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Fall time REF_CLK (80%–20%) | $t_{RMRF}$ | 1.0 | — | 2.0 | ns |
| RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge | $t_{RMRDV}$ | 4.0 | — | — | ns |
| RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge | $t_{RMRDX}$ | 2.0 | — | — | ns |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MRDVKH}$ symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MRX}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{MRDXKL}$ symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{MRX}$ clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{MRX}$ represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 21 provides the AC test load for eTSEC.

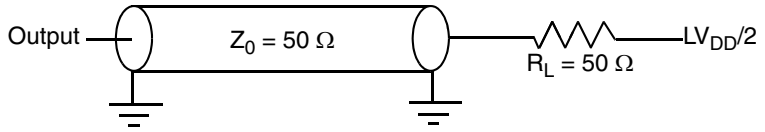



**Figure 21. eTSEC AC Test Load**

Figure 22 shows the RMII receive AC timing diagram.

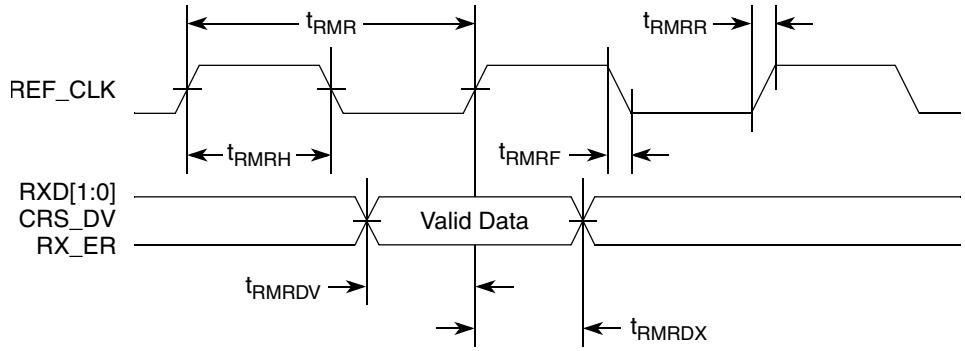



**Figure 22. RMII Receive AC Timing Diagram**

# 9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, RMII, TBI and RTBI are specified in "Section 8, "Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management."

## 9.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 38.

**Table 38. MII Management DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage (3.3 V) | $OV_{DD}$ | 3.135 | 3.465 | V |
| Output high voltage ($OV_{DD}$ = Min, $I_{OH}$ = –1.0 mA) | $V_{OH}$ | 2.10 | — | V |
| Output low voltage ($OV_{DD}$ = Min, $I_{OL}$ = 1.0 mA) | $V_{OL}$ | — | 0.50 | V |
| Input high voltage | $V_{IH}$ | 1.70 | — | V |
| Input low voltage | $V_{IL}$ | — | 0.90 | V |
| Input high current ($OV_{DD}$ = Max, $V_{IN}$ [1] = 2.1 V) | $I_{IH}$ | — | 40 | μA |
| Input low current ($OV_{DD}$ = Max, $V_{IN}$ = 0.5 V) | $I_{IL}$ | –600 | — | μA |

**Note:**
1. Note that the symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.

## 9.2 MII Management AC Electrical Specifications

Table 39 provides the MII management AC timing specifications.

**Table 39. MII Management AC Timing Specifications**

At recommended operating conditions with $OV_{DD}$ is 3.3 V ± 5%.

| Parameter | Symbol [1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| MDC frequency | $f_{MDC}$ | 2.5 | — | 9.3 | MHz | 2, 4 |
| MDC period | $t_{MDC}$ | 80 | — | 400 | ns | — |
| MDC clock pulse width high | $t_{MDCH}$ | 32 | — | — | ns | — |
| MDC to MDIO valid | $t_{MDKHDV}$ | $16 \times t_{MPXCLK}$ | — | — | ns | 5 |
| MDC to MDIO delay | $t_{MDKHDX}$ | 10 | — | $16 \times t_{MPXCLK}$ | ns | 3, 5 |
| MDIO to MDC setup time | $t_{MDDVKH}$ | 5 | — | — | ns | — |

**Table 39. MII Management AC Timing Specifications (continued)**

At recommended operating conditions with $OV_{DD}$ is 3.3 V ± 5%.

| Parameter | Symbol [1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| MDIO to MDC hold time | $t_{MDDXKH}$ | 0 | — | — | ns | — |
| MDC rise time | $t_{MDCR}$ | — | — | 10 | ns | 4 |
| MDC fall time | $t_{MDHF}$ | — | — | 10 | ns | 4 |

**Notes:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MDKHDX}$ symbolizes management data timing (MD) for the time $t_{MDC}$ from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, $t_{MDDVKH}$ symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MDC}$ clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the system clock speed. (The maximum frequency is the maximum platform frequency divided by 64.)
3. This parameter is dependent on the system clock speed. (That is, for a system clock of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a system clock of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz.)
4. Guaranteed by design.
5. $t_{MPXCLK}$ is the platform (MPX) clock

Figure 23 provides the AC test load for eTSEC.

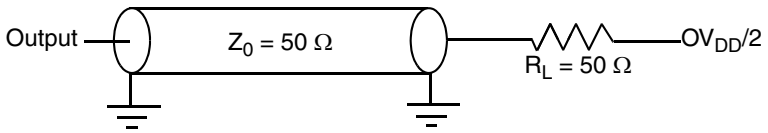



**Figure 23. eTSEC AC Test Load**

**NOTE**

Output will see a 50 Ω load since what it sees is the transmission line.

Figure 24 shows the MII management AC timing diagram.

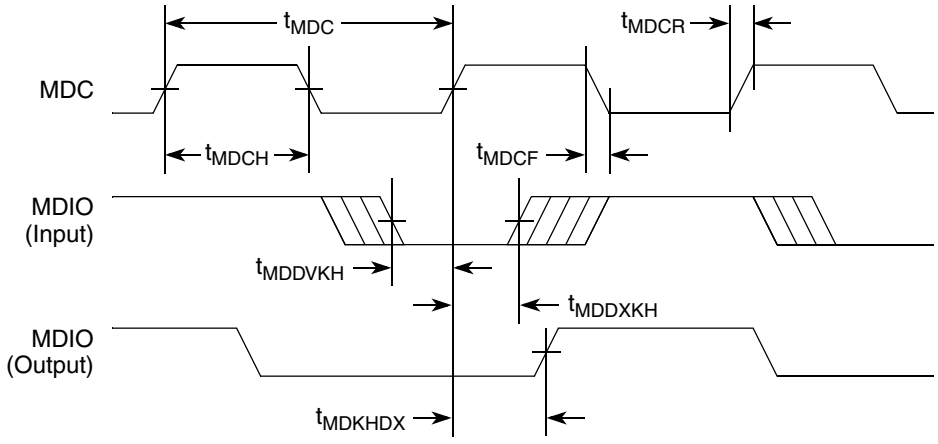



**Figure 24. MII Management Interface Timing Diagram**

# 10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8640.

## 10.1 Local Bus DC Electrical Characteristics

Table 40 provides the DC electrical characteristics for the local bus interface operating at $OV_{DD}$ = 3.3 V DC.

**Table 40. Local Bus DC Electrical Characteristics (3.3 V DC)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current ($V_{IN}$ [1] = 0 V or $V_{IN}$ = $OV_{DD}$) | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage ($OV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | $OV_{DD}$ – 0.2 | — | V |
| Low-level output voltage ($OV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.2 | V |

**Note:**
1. Note that the symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.

## 10.2 Local Bus AC Timing Specifications

Table 41 describes the timing parameters of the local bus interface at $OV_{DD}$ = 3.3 V with PLL enabled. For information about the frequency range of local bus see Section 18.1, "Clock Ranges."

**Table 41. Local Bus Timing Specifications ($OV_{DD}$ = 3.3 V)—PLL Enabled**

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus cycle time | $t_{LBK}$ | 7.5 | — | ns | 2 |
| Local bus duty cycle | $t_{LBKH}/t_{LBK}$ | 45 | 55 | % | — |
| LCLK[n] skew to LCLK[m] or LSYNC_OUT | $t_{LBKSKEW}$ | — | 150 | ps | 7, 8 |
| Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT) | $t_{LBIVKH1}$ | 1.8 | — | ns | 3, 4 |
| $\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock | $t_{LBIVKH2}$ | 1.7 | — | ns | 3, 4 |
| Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT) | $t_{LBIXKH1}$ | 1.0 | — | ns | 3, 4 |
| $\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock | $t_{LBIXKH2}$ | 1.0 | — | ns | 3, 4 |
| LALE output transition to LAD/LDP output transition (LATCH hold time) | $t_{LBOTOT}$ | 1.5 | — | ns | 6 |
| Local bus clock to output valid (except LAD/LDP and LALE) | $t_{LBKHOV1}$ | — | 2.0 | ns | — |
| Local bus clock to data valid for LAD/LDP | $t_{LBKHOV2}$ | — | 2.2 | ns | — |
| Local bus clock to address valid for LAD | $t_{LBKHOV3}$ | — | 2.3 | ns | — |
| Local bus clock to LALE assertion | $t_{LBKHOV4}$ | — | 2.3 | ns | 3 |
| Output hold from local bus clock (except LAD/LDP and LALE) | $t_{LBKHOX1}$ | 0.7 | — | ns | — |

**Table 41. Local Bus Timing Specifications ($OV_{DD}$ = 3.3 V)—PLL Enabled (continued)**

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Output hold from local bus clock for LAD/LDP | $t_{LBKHOX2}$ | 0.7 | — | ns | 3 |
| Local bus clock to output high Impedance (except LAD/LDP and LALE) | $t_{LBKHOZ1}$ | — | 2.5 | ns | 5 |
| Local bus clock to output high impedance for LAD/LDP | $t_{LBKHOZ2}$ | — | 2.5 | ns | 5 |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one(1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $OV_{DD} \div 2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. $t_{LBOTOT}$ is a measurement of the minimum time between the negation of LALE and any change in LAD. $t_{LBOTOT}$ is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[*n*]. Skew measured between complementary signals at $BV_{DD} \div 2$.
8. Guaranteed by design.

Figure 25 provides the AC test load for the local bus.

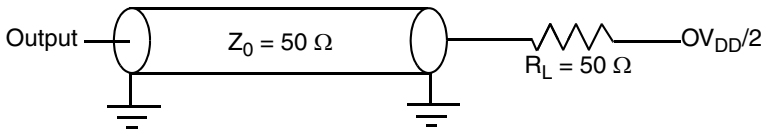



**Figure 25. Local Bus AC Test Load**

Figure 26 shows the local bus signals with PLL enabled.

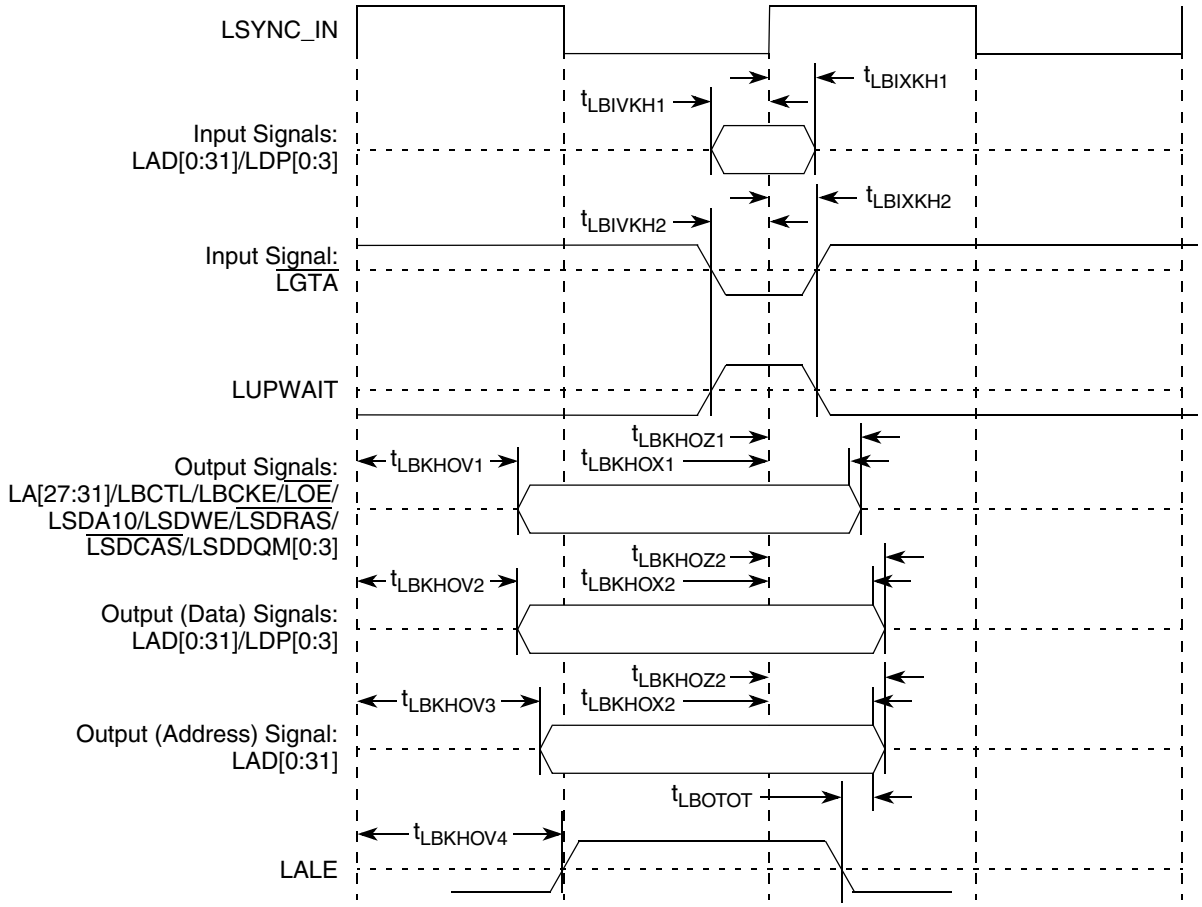



**Figure 26. Local Bus Signals (PLL Enabled)**

## NOTE

PLL bypass mode is recommended when LBIU frequency is at or below 83 MHz. When LBIU operates above 83 MHz, LBIU PLL is recommended to be enabled.

Table 42 describes the general timing parameters of the local bus interface at $OV_{DD}$ = 3.3 V with PLL bypassed.

**Table 42. Local Bus Timing Parameters—PLL Bypassed**

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus cycle time | $t_{LBK}$ | 12 | — | ns | 2 |
| Local bus duty cycle | $t_{LBKH}/t_{LBK}$ | 45 | 55 | % | — |
| Internal launch/capture clock to LCLK delay | $t_{LBKHKT}$ | 2.3 | 3.9 | ns | 8 |
| Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT) | $t_{LBIVKH1}$ | 5.7 | — | ns | 4, 5 |
| $\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock | $t_{LBIVKL2}$ | 5.6 | — | ns | 4, 5 |
| Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT) | $t_{LBIXKH1}$ | –1.8 | — | ns | 4, 5 |

**Table 42. Local Bus Timing Parameters—PLL Bypassed (continued)**

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock | $t_{LBIXKL2}$ | –1.3 | — | ns | 4, 5 |
| LALE output transition to LAD/LDP output transition (LATCH hold time) | $t_{LBOTOT}$ | 1.5 | — | ns | 6 |
| Local bus clock to output valid (except LAD/LDP and LALE) | $t_{LBKLOV1}$ | — | –0.3 | ns | |
| Local bus clock to data valid for LAD/LDP | $t_{LBKLOV2}$ | — | –0.1 | ns | 4 |
| Local bus clock to address valid for LAD | $t_{LBKLOV3}$ | — | 0 | ns | 4 |
| Local bus clock to LALE assertion | $t_{LBKLOV4}$ | — | 0 | ns | 4 |
| Output hold from local bus clock (except LAD/LDP and LALE) | $t_{LBKLOX1}$ | –3.2 | — | ns | 4 |
| Output hold from local bus clock for LAD/LDP | $t_{LBKLOX2}$ | –3.2 | — | ns | 4 |
| Local bus clock to output high Impedance (except LAD/LDP and LALE) | $t_{LBKLOZ1}$ | — | 0.2 | ns | 7 |
| Local bus clock to output high impedance for LAD/LDP | $t_{LBKLOZ2}$ | — | 0.2 | ns | 7 |

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one(1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which precedes LCLK by $t_{LBKHKT}$.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD} \div 2$.
4. All signals are measured from $BV_{DD} \div 2$ of the rising edge of local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. The value of $t_{LBOTOT}$ is the measurement of the minimum time between the negation of LALE and any change in LAD
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. Guaranteed by characterization.

Figure 27 shows the local bus signals in PLL bypass mode.

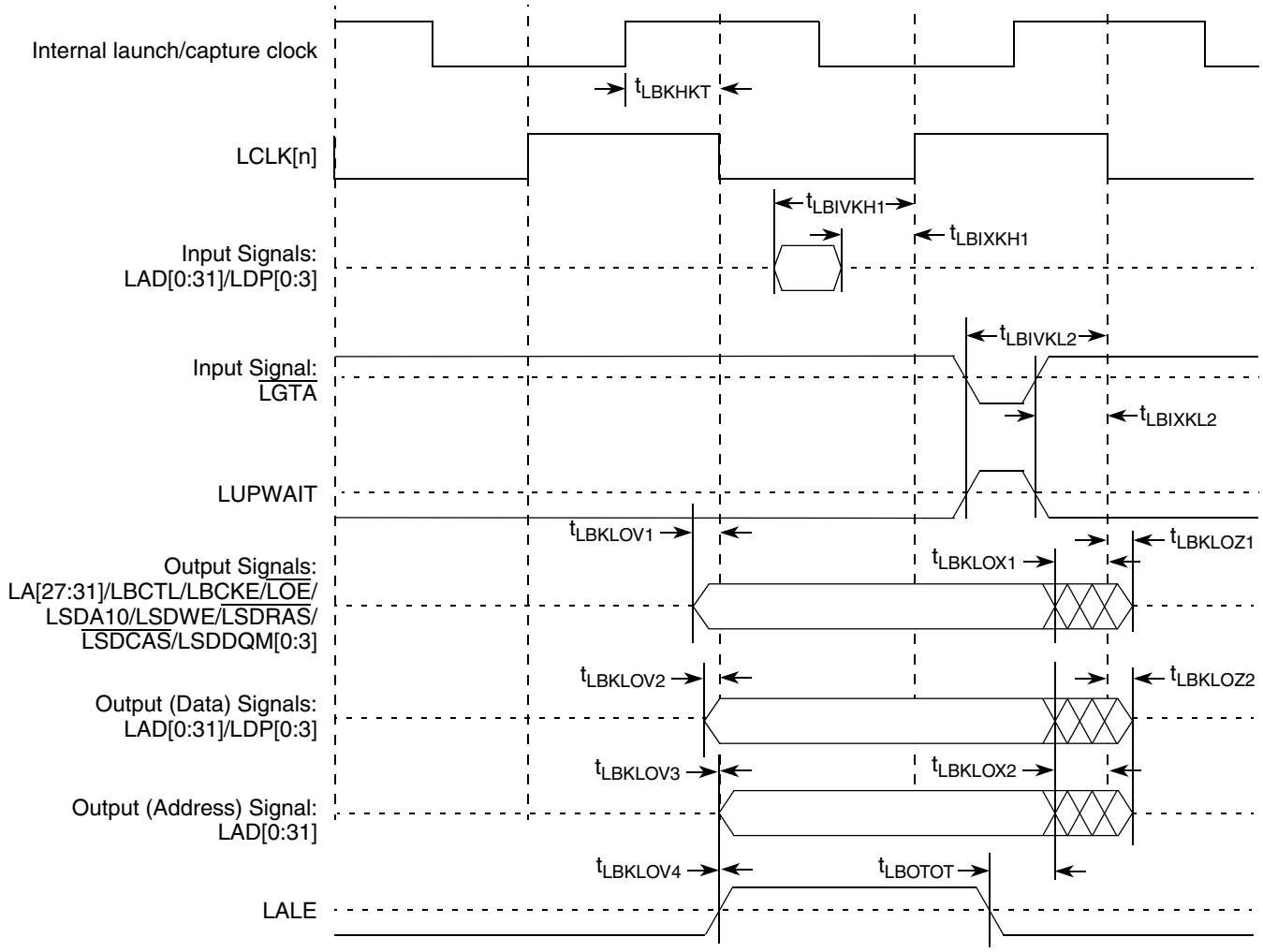



**Figure 27. Local Bus Signals (PLL Bypass Mode)**

## NOTE

In PLL bypass mode, LCLK[*n*] is the inverted version of the internal clock with the delay of $t_{LBKHKT}$. In this mode, signals are launched at the rising edge of the internal clock and are captured at falling edge of the internal clock, with the exception of the LGTA/LUPWAIT signal, which is captured at the rising edge of the internal clock.

Figure 28–Figure 31 show the local bus signals and GPCM/UPM signals for LCRR[CLKDIV] at clock ratios of 4, 8, and 16 with PLL enabled or bypassed.

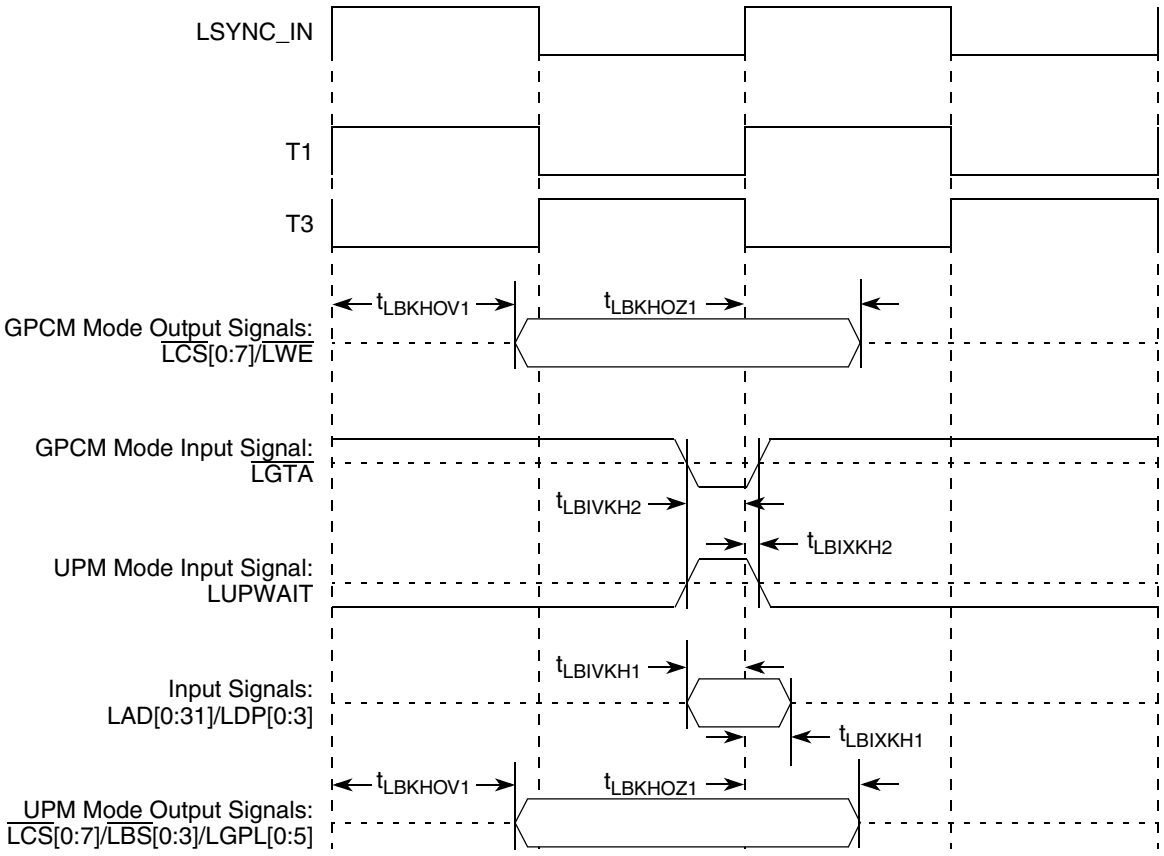



**Figure 28. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (clock ratio of 4) (PLL Enabled)**

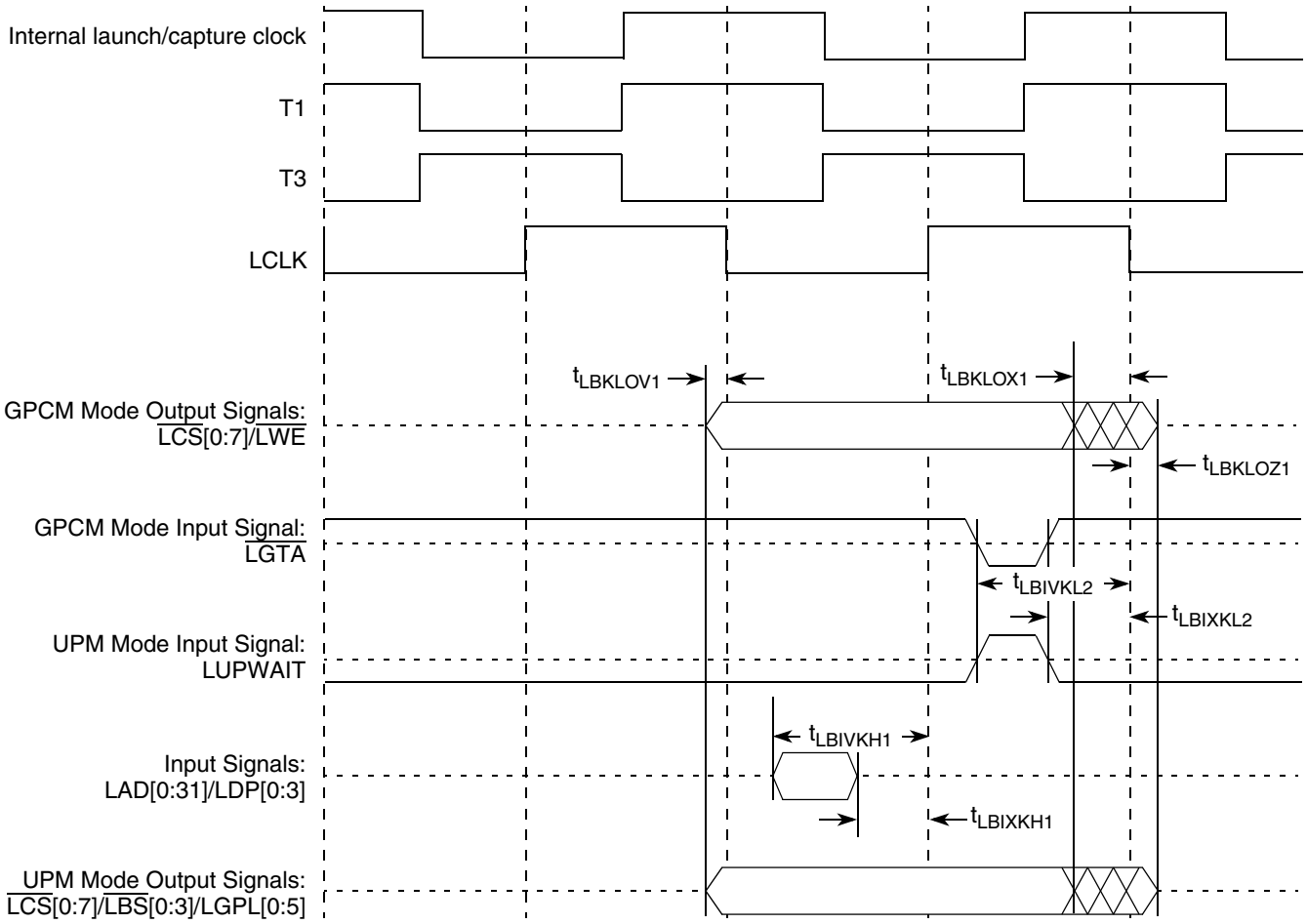



**Figure 29. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (clock ratio of 4) (PLL Bypass Mode)**

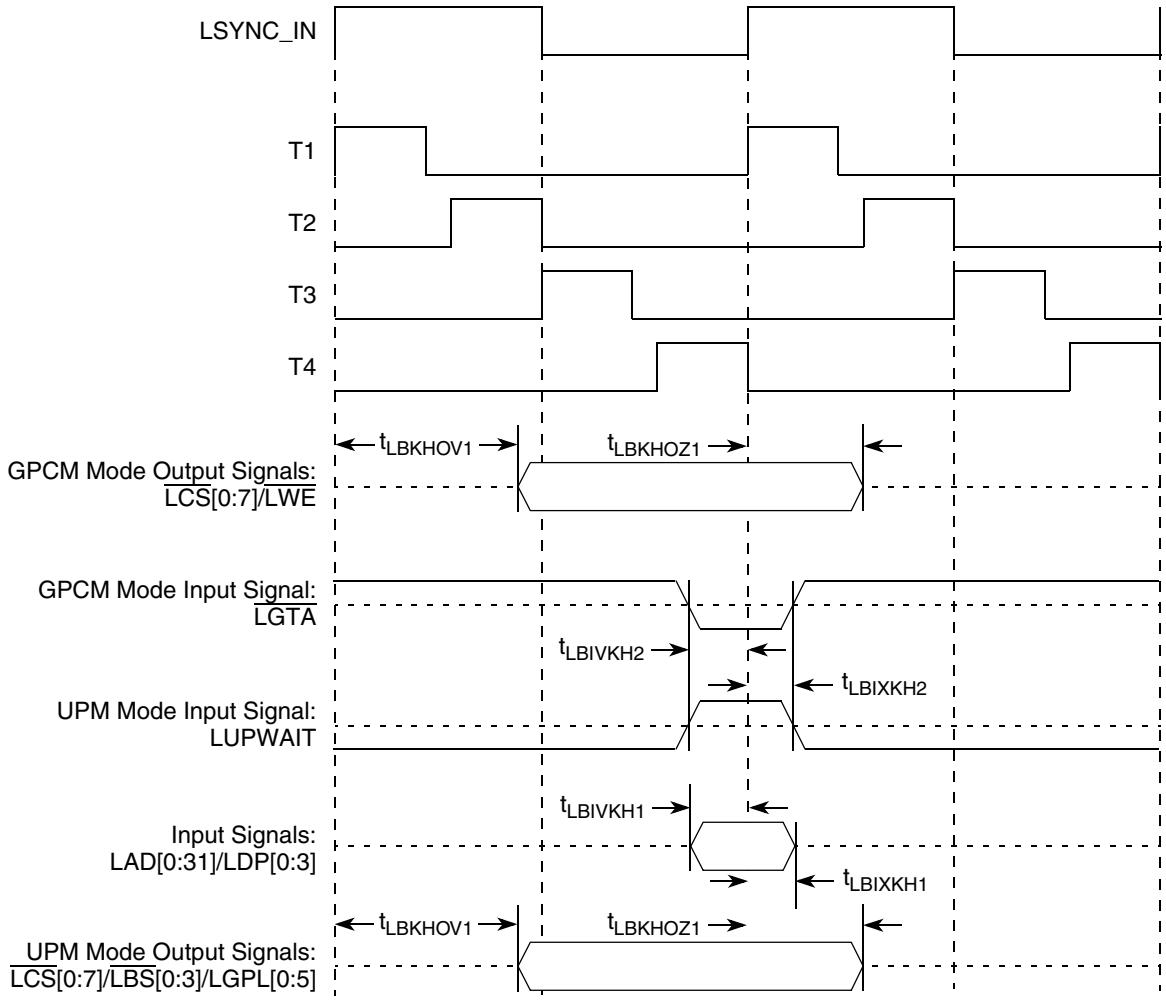



**Figure 30. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 or 8 (clock ratio of 8 or 16) (PLL Enabled)**

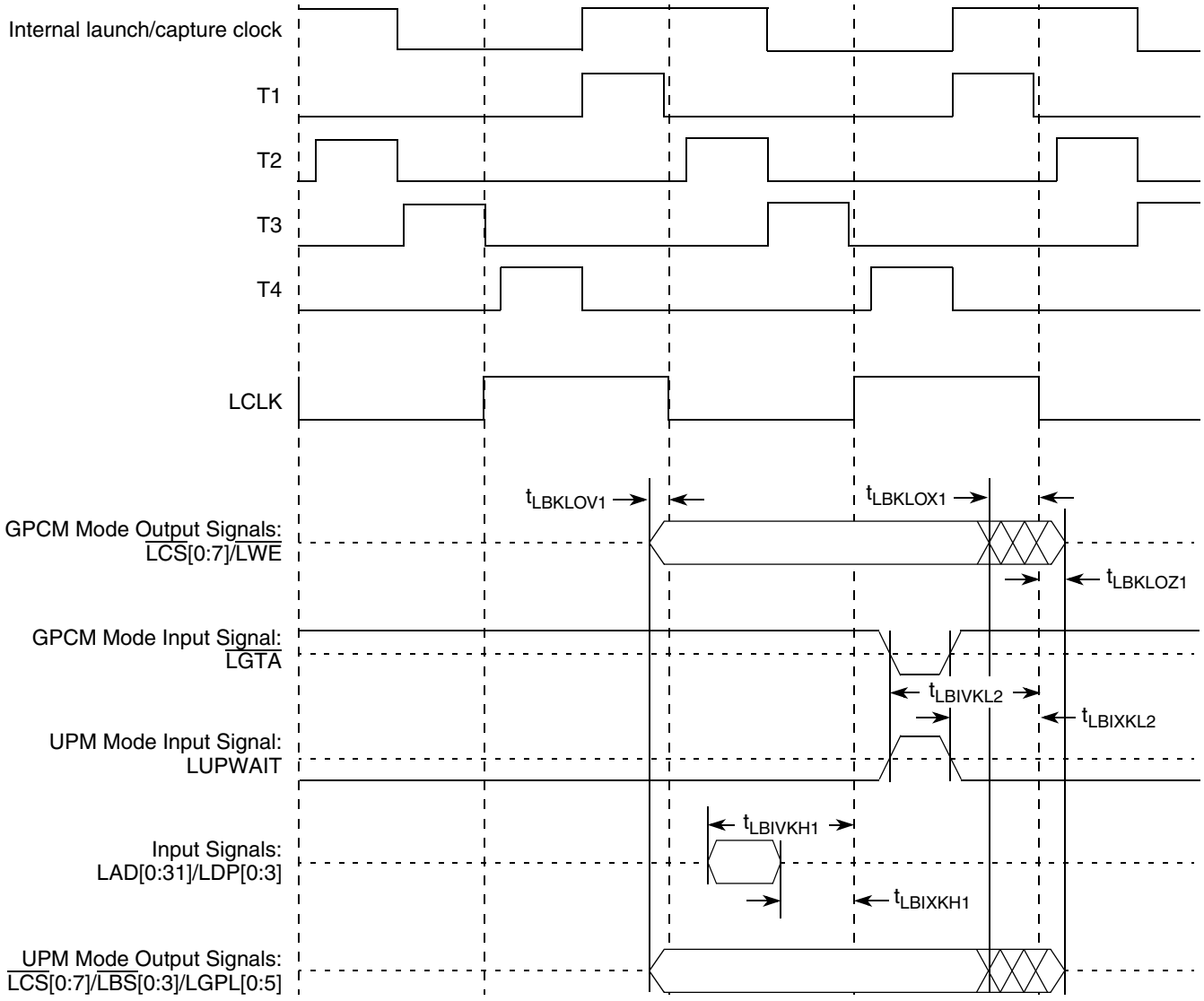



**Figure 31. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 or 8 (clock ratio of 8 or 16) (PLL Bypass Mode)**

# 11 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8640/D.

## 11.1 JTAG DC Electrical Characteristics

Table 43 provides the DC electrical characteristics for the JTAG interface.

**Table 43. JTAG DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current ($V_{IN}$ [1] = 0 V or $V_{IN}$ = $V_{DD}$) | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage ($OV_{DD}$ = min, $I_{OH}$ = –100 μA) | $V_{OH}$ | $OV_{DD}$ – 0.2 | — | V |
| Low-level output voltage ($OV_{DD}$ = min, $I_{OL}$ = 100 μA) | $V_{OL}$ | — | 0.2 | V |

**Note:**
1. Note that the symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.

## 11.2 JTAG AC Electrical Specifications

Table 44 provides the JTAG AC timing specifications as defined in Figure 33 through Figure 35.

**Table 44. JTAG AC Timing Specifications (Independent of SYSCLK)[1]**

At recommended operating conditions (see Table 3).

| Parameter | Symbol[2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| JTAG external clock frequency of operation | $f_{JTG}$ | 0 | 33.3 | MHz | — |
| JTAG external clock cycle time | $t_{JTG}$ | 30 | — | ns | — |
| JTAG external clock pulse width measured at 1.4 V | $t_{JTKHKL}$ | 15 | — | ns | — |
| JTAG external clock rise and fall times | $t_{JTGR}$ & $t_{JTGF}$ | 0 | 2 | ns | 6 |
| $\overline{TRST}$ assert time | $t_{TRST}$ | 25 | — | ns | 3 |
| Input setup times:<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDVKH}$<br>$t_{JTIVKH}$ | <br>4<br>0 | <br>—<br>— | ns | 4 |
| Input hold times:<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDXKH}$<br>$t_{JTIXKH}$ | <br>20<br>25 | <br>—<br>— | ns | 4 |
| Valid times:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDV}$<br>$t_{JTKLOV}$ | <br>4<br>4 | <br>20<br>25 | ns | 5 |
| Output hold times:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDX}$<br>$t_{JTKLOX}$ | <br>30<br>30 | <br>—<br>— | ns | 5, 6 |
| JTAG external clock to output high impedance:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDZ}$<br>$t_{JTKLOZ}$ | <br>3<br>3 | <br>19<br>9 | ns | 5, 6 |

**Table 44. JTAG AC Timing Specifications (Independent of SYSCLK)[1] (continued)**

At recommended operating conditions (see Table 3).

| Parameter | Symbol[2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|

**Notes:**

1. All outputs are measured from the midpoint voltage of the falling/rising edge of $t_{TCLK}$ to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 32). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{JTDVKH}$ symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{JTDXKH}$ symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to $t_{TCLK}$.
5. Non-JTAG signal output timing with respect to $t_{TCLK}$.
6. Guaranteed by design.

Figure 32 provides the AC test load for TDO and the boundary-scan outputs.

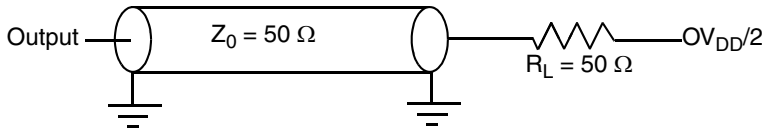



**Figure 32. AC Test Load for the JTAG Interface**

Figure 33 provides the JTAG clock input timing diagram.

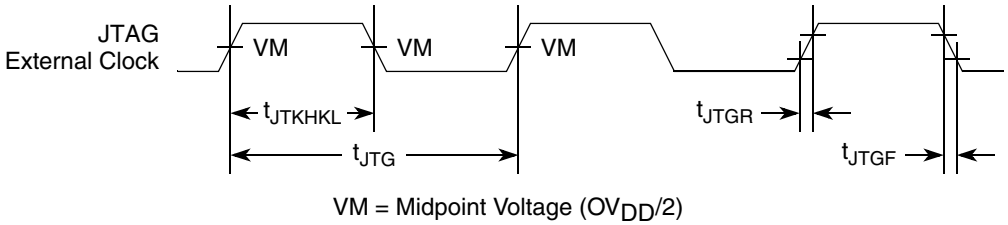



**Figure 33. JTAG Clock Input Timing Diagram**

Figure 34 provides the $\overline{\text{TRST}}$ timing diagram.

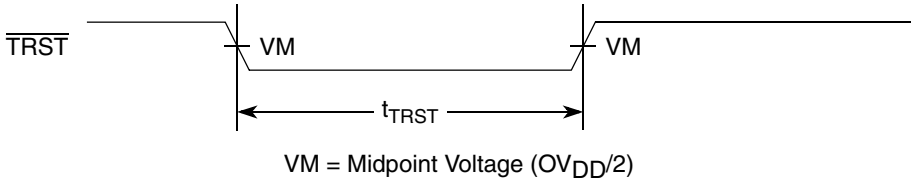



**Figure 34. $\overline{\text{TRST}}$ Timing Diagram**

Figure 35 provides the boundary-scan timing diagram.

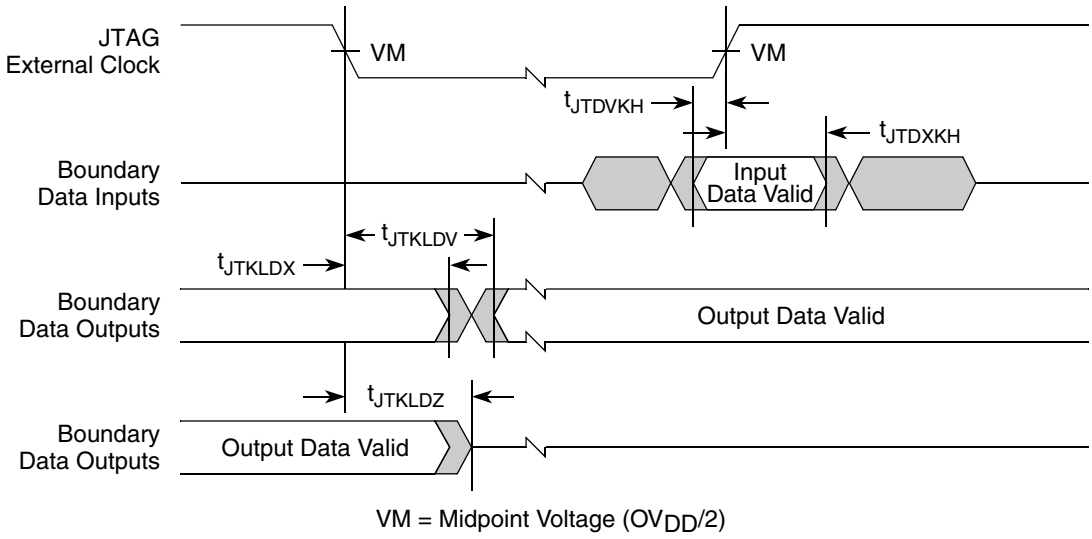



**Figure 35. Boundary-Scan Timing Diagram**

# 12 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8640.

## 12.1 I²C DC Electrical Characteristics

Table 45 provides the DC electrical characteristics for the I²C interfaces.

**Table 45. I²C DC Electrical Characteristics**

At recommended operating conditions with $OV_{DD}$ of 3.3 V ± 5%.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high voltage level | $V_{IH}$ | 0.7 × $OV_{DD}$ | $OV_{DD}$ + 0.3 | V | — |
| Input low voltage level | $V_{IL}$ | –0.3 | 0.3 × $OV_{DD}$ | V | — |
| Low level output voltage | $V_{OL}$ | 0 | 0.2 × $OV_{DD}$ | V | 1 |
| Pulse width of spikes which must be suppressed by the input filter | $t_{I2KHKL}$ | 0 | 50 | ns | 2 |
| Input current each I/O pin (input voltage is between 0.1 × $OV_{DD}$ and 0.9 × $OV_{DD}$ (max) | $I_I$ | –10 | 10 | μA | 3 |
| Capacitance for each I/O pin | $C_I$ | — | 10 | pF | — |

**Notes:**
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8641 Integrated Host Processor Reference Manual* for information on the digital filter used.
3. I/O pins will obstruct the SDA and SCL lines if $OV_{DD}$ is switched off.

## 12.2 I²C AC Electrical Specifications

Table 46 provides the AC timing parameters for the I²C interfaces.

## Table 46. I²C AC Electrical Specifications

All values refer to $V_{IH}$ (min) and $V_{IL}$ (max) levels (see Table 45).

| Parameter | Symbol[1] | Min | Max | Unit |
|---|---|---|---|---|
| SCL clock frequency | $f_{I2C}$ | 0 | 400 | kHz |
| Low period of the SCL clock | $t_{I2CL}$ [4] | 1.3 | — | μs |
| High period of the SCL clock | $t_{I2CH}$ [4] | 0.6 | — | μs |
| Setup time for a repeated START condition | $t_{I2SVKH}$ [4] | 0.6 | — | μs |
| Hold time (repeated) START condition (after this period, the first clock pulse is generated) | $t_{I2SXKL}$ [4] | 0.6 | — | μs |
| Data setup time | $t_{I2DVKH}$ [4] | 100 | — | ns |
| Data input hold time:<br>CBUS compatible masters<br>I²C bus devices | $t_{I2DXKL}$ | <br>—<br>0 [2] | <br>—<br>— | <br><br>μs |
| Rise time of both SDA and SCL signals | $t_{I2CR}$ | 20 + 0.1 $C_B$ [5] | 300 | ns |
| Fall time of both SDA and SCL signals | $t_{I2CF}$ | 20 + 0.1 $C_b$ [5] | 300 | ns |
| Data output delay time | $t_{I2OVKL}$ | — | 0.9 [3] | μs |
| Set-up time for STOP condition | $t_{I2PVKH}$ | 0.6 | — | μs |

**Table 46. I²C AC Electrical Specifications (continued)**

All values refer to $V_{IH}$ (min) and $V_{IL}$ (max) levels (see Table 45).

| Parameter | Symbol[1] | Min | Max | Unit |
|---|---|---|---|---|
| Bus free time between a STOP and START condition | $t_{I2KHDX}$ | 1.3 | — | μs |
| Noise margin at the LOW level for each connected device (including hysteresis) | $V_{NL}$ | $0.1 \times OV_{DD}$ | — | V |
| Noise margin at the HIGH level for each connected device (including hysteresis) | $V_{NH}$ | $0.2 \times OV_{DD}$ | — | V |

**Note:**

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{I2DVKH}$ symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{I2C}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{I2SXKL}$ symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the $t_{I2C}$ clock reference (K) going to the low (L) state or hold time. Also, $t_{I2PVKH}$ symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the $t_{I2C}$ clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. As a transmitter, the MPC8640 provides a delay time of at least 300 ns for the SDA signal (referred to the Vihmin of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of Start or Stop condition. When MPC8640 acts as the I²C bus master while transmitting, MPC8640 drives both SCL and SDA. As long as the load on SCL and SDA are balanced, MPC8640 would not cause unintended generation of Start or Stop condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for MPC8640 as transmitter, the following setting is recommended for the FDR bit field of the I2CFDR register to ensure both the desired I²C SCL clock frequency and SDA output delay time are achieved, assuming that the desired I²C SCL clock frequency is 400 KHz and the Digital Filter Sampling Rate Register (I2CDFSRR) is programmed with its default setting of 0x10 (decimal 16):

| I²C Source Clock Frequency | 333 MHz | 266 MHz | 200 MHz | 133 MHz |
|---|---|---|---|---|
| FDR Bit Setting | 0x2A | 0x05 | 0x26 | 0x00 |
| Actual FDR Divider Selected | 896 | 704 | 512 | 384 |
| Actual I²C SCL Frequency Generated | 371 KHz | 378 KHz | 390 KHz | 346 KHz |

   For the detail of I²C frequency calculation, refer to the application note AN2919 “Determining the I²C Frequency Divider Ratio for SCL.” Note that the I²C Source Clock Frequency is half of the MPX clock frequency for MPC8640.
3. The maximum $t_{I2DXKL}$ has only to be met if the device does not stretch the LOW period ($t_{I2CL}$) of the SCL signal.
4. Guaranteed by design.
5. $C_B$ = capacitance of one bus line in pF.

Figure 32 provides the AC test load for the I²C.

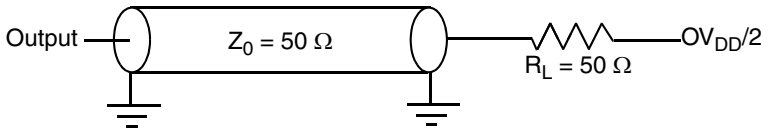



**Figure 36. I²C AC Test Load**

Figure 37 shows the AC timing diagram for the $I^2C$ bus.

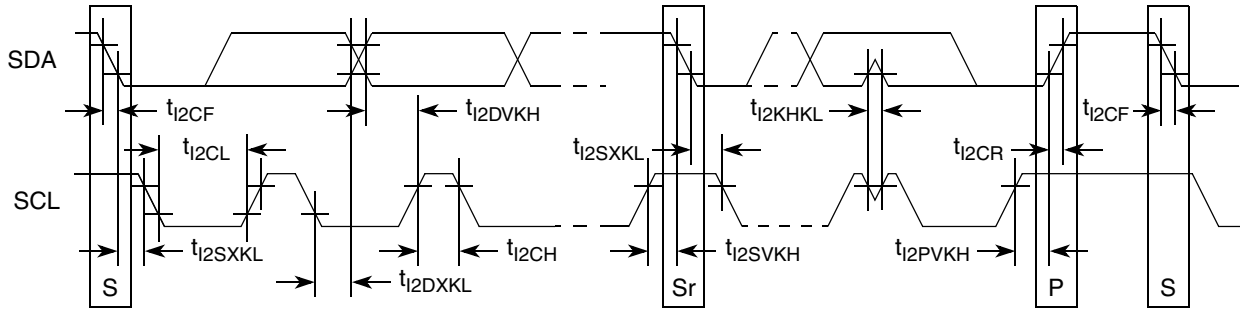



**Figure 37. $I^2C$ Bus AC Timing Diagram**

# 13 High-Speed Serial Interfaces (HSSI)

The MPC8640D features two Serializer/Deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes1 interface is dedicated for PCI Express data transfers. The SerDes2 can be used for PCI Express and/or serial RapidIO data transfers.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

## 13.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 38 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SD*n*_TX and $\overline{\text{SD}n\text{_TX}}$) or a receiver input (SD*n*_RX and $\overline{\text{SD}n\text{_RX}}$). Each signal swings between A volts and B volts where A > B.

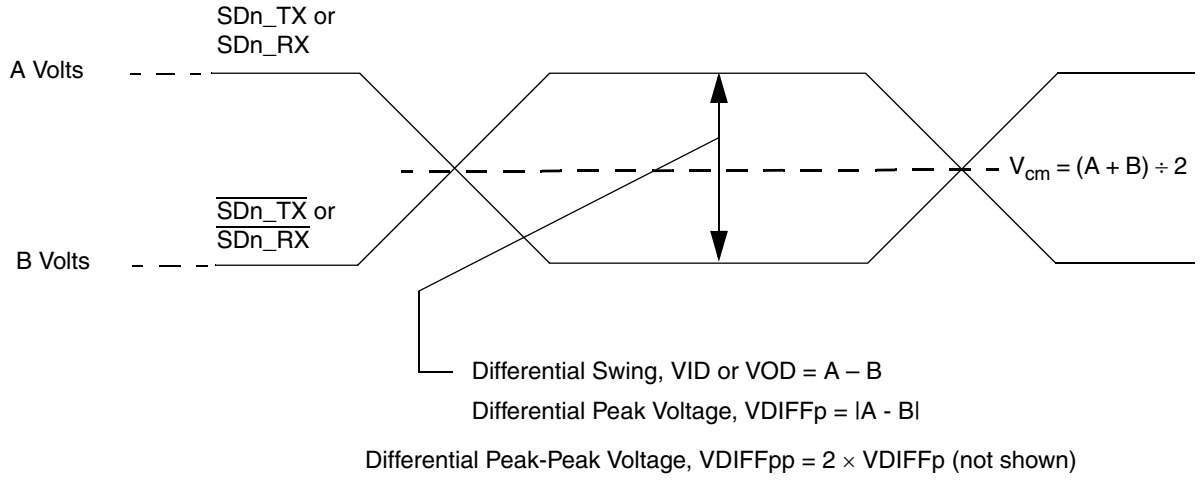



**Figure 38. Differential Voltage Definitions for Transmitter or Receiver**

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

**Single-Ended Swing**

The transmitter output signals and the receiver input signals SD*n*_TX, $\overline{\text{SD}n\text{_TX}}$, SD*n*_RX and $\overline{\text{SD}n\text{_RX}}$ each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's single-ended swing.

**Differential Output Voltage, $V_{OD}$** (or **Differential Output Swing**):

The differential output voltage (or swing) of the transmitter, $V_{OD}$, is defined as the difference of the two complimentary output voltages: $V_{SDn_TX} - V_{\overline{SDn_TX}}$. The $V_{OD}$ value can be either positive or negative.

**Differential Input Voltage, $V_{ID}$** (or **Differential Input Swing**):

The differential input voltage (or swing) of the receiver, $V_{ID}$, is defined as the difference of the two complimentary input voltages: $V_{SDn_RX} - V_{\overline{SDn_RX}}$. The $V_{ID}$ value can be either positive or negative.

**Differential Peak Voltage, $V_{DIFFp}$**

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak voltage, $V_{DIFFp} = |A - B|$ volts.

**Differential Peak-to-Peak, $V_{DIFFp-p}$**

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input

signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.

**Differential Waveform**

The differential waveform is constructed by subtracting the inverting signal ($\overline{SDn_TX}$, for example) from the non-inverting signal (SD*n*_TX, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 47 as an example for differential waveform.

**Common Mode Voltage, $V_{cm}$**

The common mode voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = (V_{SDn_TX} + V_{\overline{SDn_TX}}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasion.

To illustrate these definitions using real values, consider the case of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{TD}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing ($V_{OD}$) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, $V_{OD}$ is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage ($V_{DIFFp}$) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

## 13.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD*n*_REF_CLK and $\overline{SDn_REF_CLK}$ for PCI Express and Serial RapidIO.

The following sections describe the SerDes reference clock requirements and some application information.

### 13.2.1 SerDes Reference Clock Receiver Characteristics

Figure 39 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for $XV_{DD}$_SRDS*n* are specified in Table 1 and Table 2.
- SerDes Reference Clock Receiver Reference Circuit Structure
  - The SD*n*_REF_CLK and $\overline{\text{SD}n\text{_REF_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 39. Each differential clock input (SD*n*_REF_CLK or $\overline{\text{SD}n\text{_REF_CLK}}$) has a 50-Ω termination to SGND followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the Differential Mode and Single-ended Mode description below for further detailed requirements.
- The maximum average current requirement that also determines the common mode voltage range
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V ÷ 50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD*n*_REF_CLK and $\overline{\text{SD}n\text{_REF_CLK}}$ inputs cannot drive 50 Ω to SGND DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  - This requirement is described in detail in the following sections.

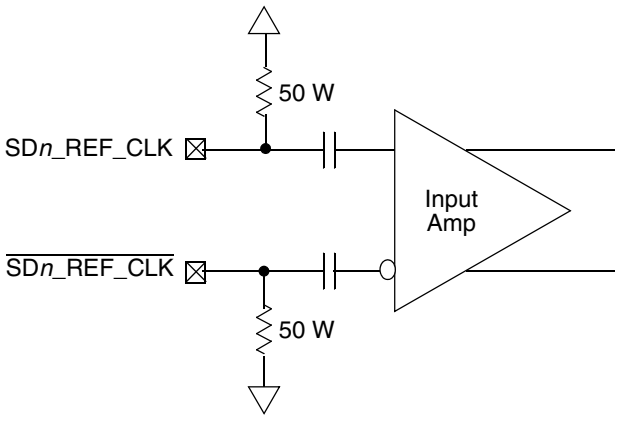



**Figure 39. Receiver of SerDes Reference Clocks**

### 13.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the MPC8640D SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For **external DC-coupled** connection, as described in section 13.2.1, the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. Figure 40 shows the SerDes reference clock input requirement for DC-coupled connection scheme.
  - For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND). Figure 41 shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- **Single-ended Mode**
  - The reference clock can also be single-ended. The SD*n*_REF_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from $V_{min}$ to $V_{max}$) with $\overline{\text{SD}n\text{_REF_CLK}}$ either left unconnected or tied to ground.
  - The SD*n*_REF_CLK input average voltage must be between 200 and 400 mV. Figure 42 shows the SerDes reference clock input requirement for single-ended signaling mode.
  - To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{\text{SD}n\text{_REF_CLK}}$) through the same source impedance as the clock input (SD*n*_REF_CLK) in use.

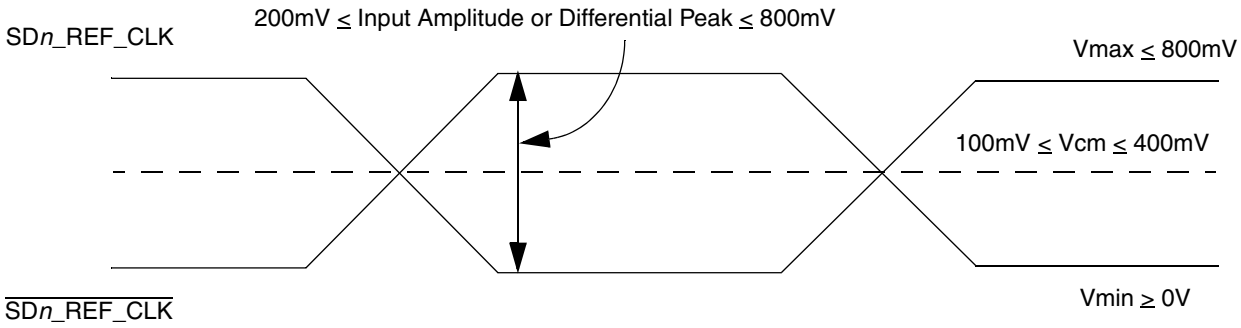



**Figure 40. Differential Reference Clock Input DC Requirements (External DC-Coupled)**

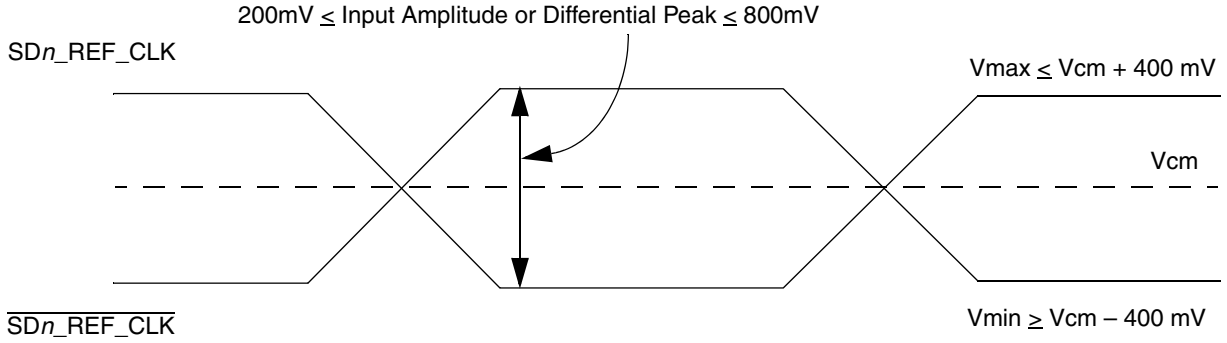



**Figure 41. Differential Reference Clock Input DC Requirements (External AC-Coupled)**

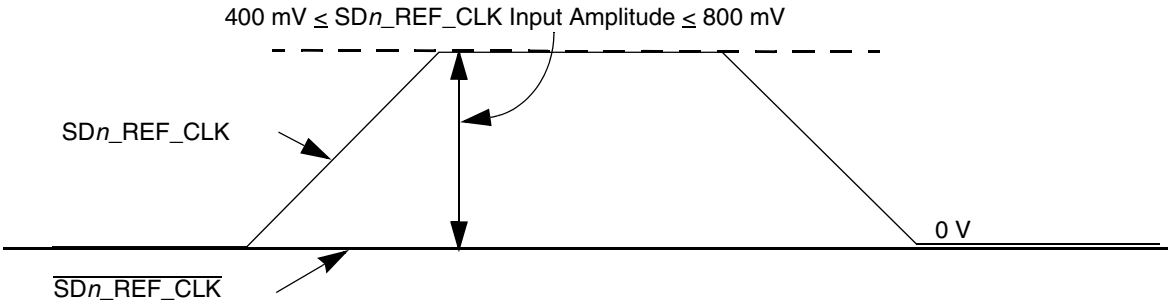



**Figure 42. Single-Ended Reference Clock Input DC Requirements**

### 13.2.3 Interfacing With Other Differential Signaling Levels

The following list explains characteristics of interfacing with other differential signaling levels.

- With on-chip termination to SGND, the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude. It may need to be DC-biased at clock driver output first and followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

Figure 43 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8640D SerDes reference clock input's DC requirement.

**NOTE**

Figure 43–Figure 46 are for conceptual reference only. Due to the differences in the clock driver chip's internal structure, output impedance, and termination requirements among various clock driver chip manufacturers, the clock circuit reference designs provided by clock driver chip vendor may be different from what is shown above. They may also vary from one vendor to the other. Therefore, NXP Semiconductors can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8640D SerDes reference clock receiver requirement provided in this document.

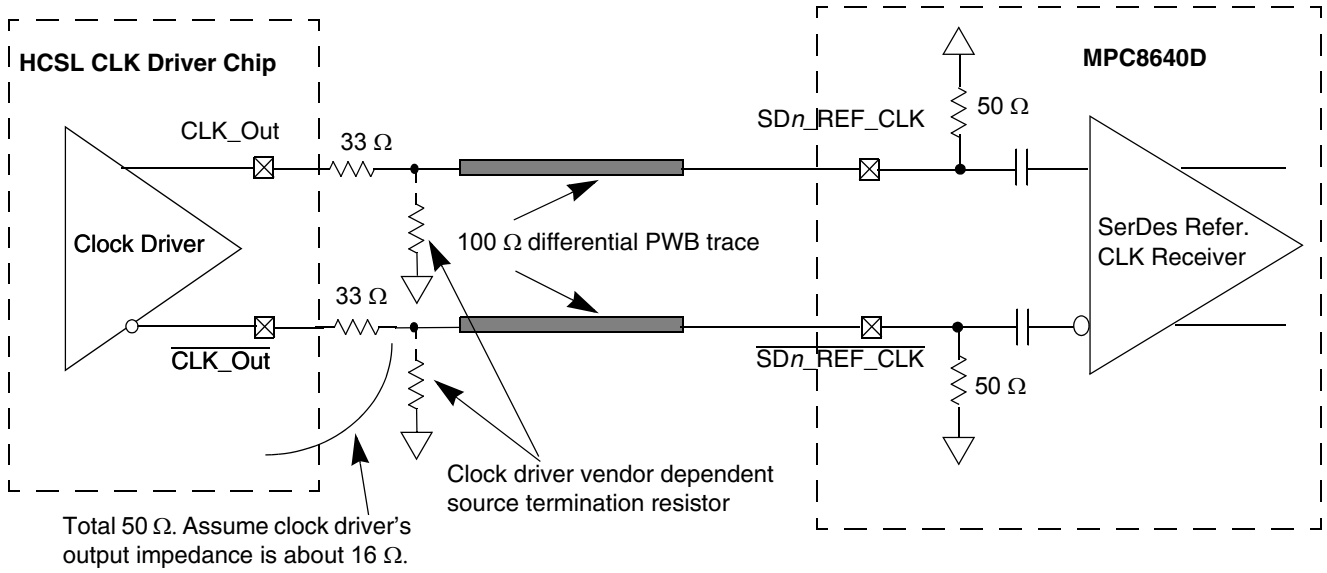



**Figure 43. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)**

Figure 44 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the MPC8640D SerDes reference clock input's allowed range (100 to 400mV), AC-coupled connection scheme must be used. It assumes the

LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

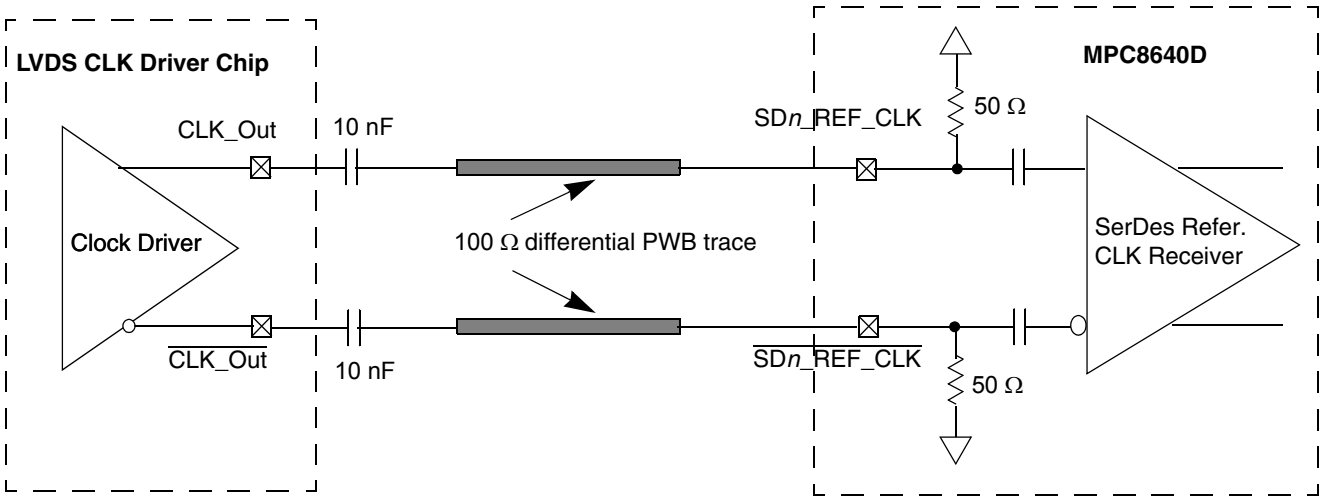



**Figure 44. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)**

Figure 45 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with MPC8640D SerDes reference clock input's DC requirement, AC-coupling has to be used. Figure 45 assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140 Ω to 240 Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8640D SerDes reference clock's differential input amplitude requirement (between 200 mV and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω.

Please consult with the clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

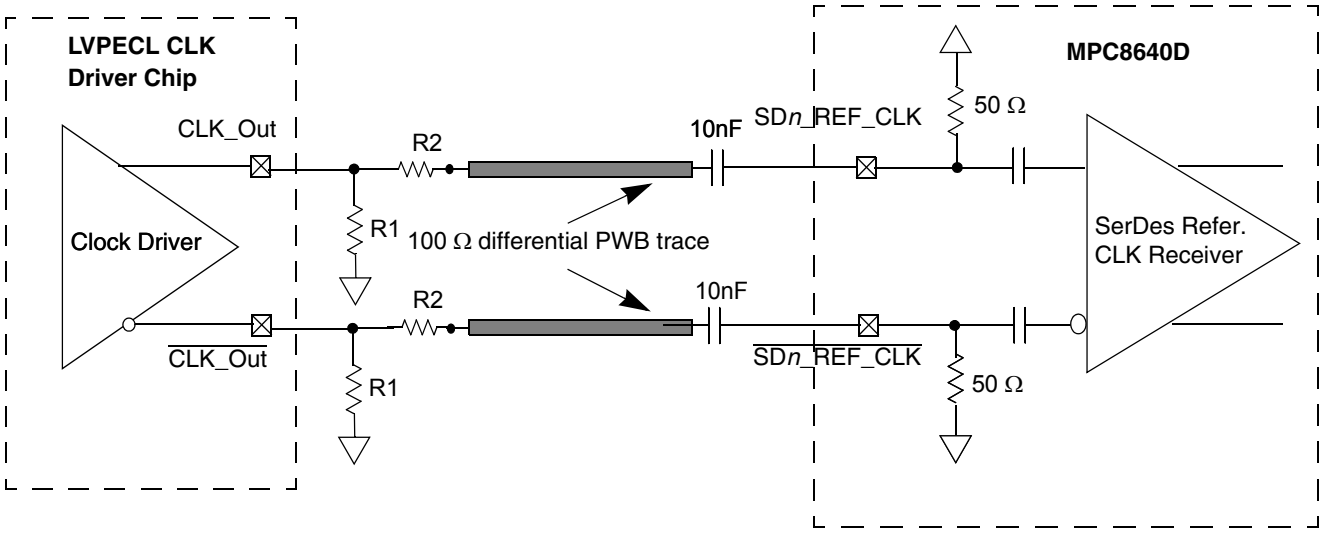



**Figure 45. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)**

Figure 46 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8640D SerDes reference clock input's DC requirement.

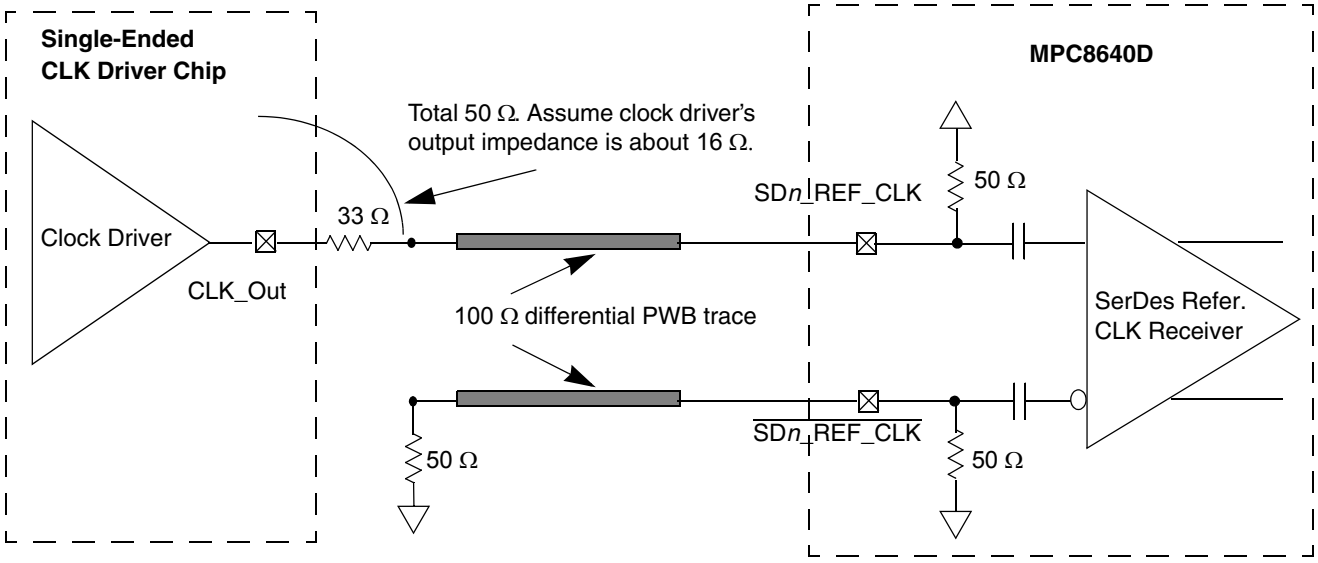



**Figure 46. Single-Ended Connection (Reference Only)**

## 13.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise

occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

Table 47 describes some AC parameters common to PCI Express and Serial RapidIO protocols.

**Table 47. SerDes Reference Clock Common AC Parameters**

At recommended operating conditions with $XV_{DD}$_SRDS1 or $XV_{DD}$_SRDS2 = 1.1 V ± 5% and 1.05 V ± 5%.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Rising Edge Rate | Rise Edge Rate | 1.0 | 4.0 | V/ns | 2, 3 |
| Falling Edge Rate | Fall Edge Rate | 1.0 | 4.0 | V/ns | 2, 3 |
| Differential Input High Voltage | $V_{IH}$ | +200 | — | mV | 2 |
| Differential Input Low Voltage | $V_{IL}$ | — | –200 | mV | 2 |
| Rising edge rate (SD*n*_REF_CLK) to falling edge rate ($\overline{\text{SD}n\text{_REF_CLK}}$) matching | Rise-Fall Matching | — | 20 | % | 1, 4 |

**Notes:**

1. Measurement taken from single-ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD*n*_REF_CLK minus $\overline{\text{SD}n\text{_REF_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 47.
4. Matching applies to the rising edge rate for SD*n*_REF_CLK and falling edge rate for $\overline{\text{SD}n\text{_REF_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLK rising meets $\overline{\text{SD}n\text{_REF_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rising edge rate of SD*n*_REF_CLK should be compared to the falling edge rate of $\overline{\text{SD}n\text{_REF_CLK}}$, and the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 48.

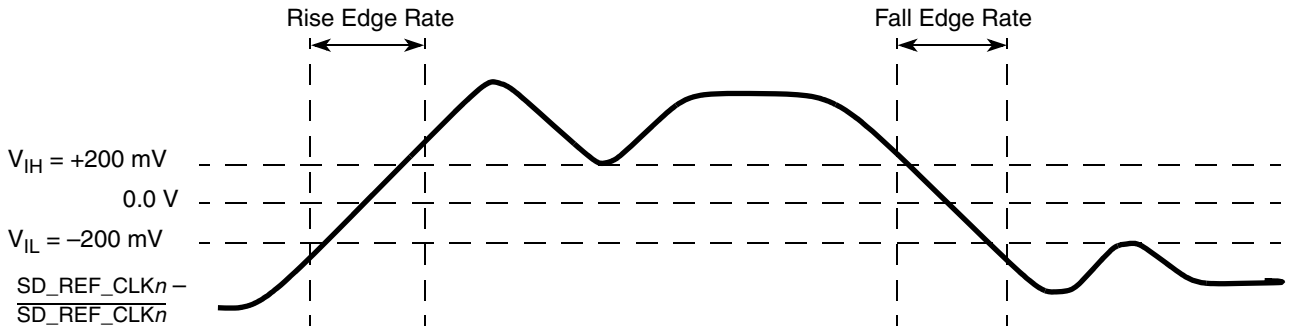



**Figure 47. Differential Measurement Points for Rise and Fall Time**

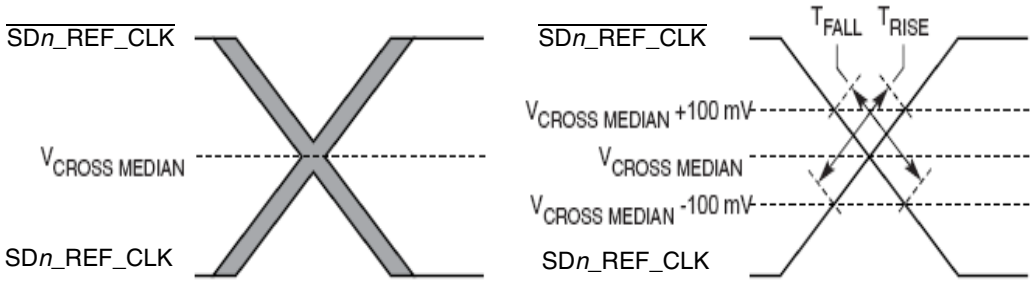



**Figure 48. Single-Ended Measurement Points for Rise and Fall Time Matching**

The other detailed AC requirements of the SerDes reference clocks is defined by each interface protocol based on application usage. Refer to the following sections for detailed information:

- Section 14.2, "AC Requirements for PCI Express SerDes Clocks"
- Section 15.2, "AC Requirements for Serial RapidIO SDn_REF_CLK and SDn_REF_CLK"

## 13.3 SerDes Transmitter and Receiver Reference Circuits

Figure 49 shows the reference circuits for SerDes data lane's transmitter and receiver.

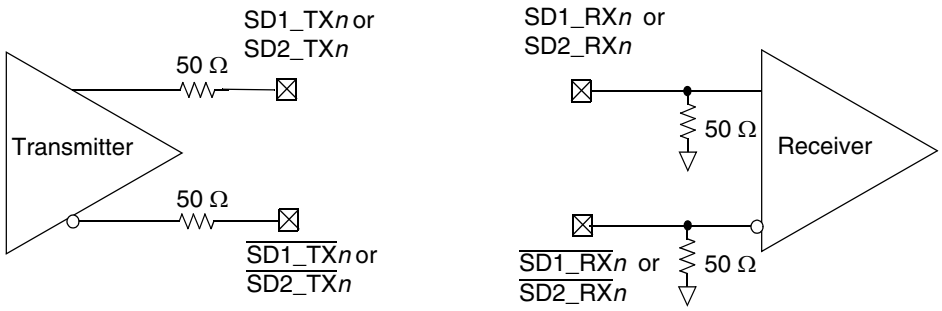



**Figure 49. SerDes Transmitter and Receiver Reference Circuits**

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express or Serial Rapid IO) in this document based on the application usage:

- Section 14, "PCI Express"
- Section 15, "Serial RapidIO"

Note that external AC Coupling capacitor is required for the above two serial transmission protocols with the capacitor value defined in specification of each protocol section.

# 14 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8640.

## 14.1 DC Requirements for PCI Express SD*n*_REF_CLK and $\overline{\text{SD}n\text{_REF_CLK}}$

For more information, see Section 13.2, "SerDes Reference Clocks."

## 14.2 AC Requirements for PCI Express SerDes Clocks

Table 48 lists AC requirements.

**Table 48. SD*n*_REF_CLK and $\overline{\text{SD}n\text{_REF_CLK}}$ AC Requirements**

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| REFCLK cycle time | $t_{REF}$ | — | 10 | — | ns | — |
| REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles | $t_{REFCJ}$ | — | — | 100 | ps | — |
| Phase jitter. Deviation in edge location with respect to mean edge location | $t_{REFPJ}$ | –50 | — | 50 | ps | — |

## 14.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ± 300 ppm tolerance.

## 14.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer please use the PCI Express Base Specification, Rev. 1.0a document.

### 14.4.1 Differential Transmitter (Tx) Output

Table 49 defines the specifications for the differential output at all transmitters. The parameters are specified at the component pins.

**Table 49. Differential Transmitter Output Specifications**

| Parameter | Symbol | Min | Nom | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Unit Interval | UI | 399.88 | 400 | 400.12 | ps | Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1. |
| Differential Peak-to-Peak Output Voltage | $V_{TX\text{-}DIFFp\text{-}p}$ | 0.8 | — | 1.2 | V | $V_{TX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{TX\text{-}D+} - V_{TX\text{-}D-} \rvert$ See Note 2. |

**Table 49. Differential Transmitter Output Specifications (continued)**

| Parameter | Symbol | Min | Nom | Max | Units | Notes |
|---|---|---|---|---|---|---|
| De- Emphasized Differential Output Voltage (Ratio) | $V_{TX\text{-}DE\text{-}RATIO}$ | –3.0 | –3.5 | –4.0 | dB | Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. See Note 2. |
| Minimum TX Eye Width | $T_{TX\text{-}EYE}$ | 0.70 | — | — | UI | The maximum Transmitter jitter can be derived as $T_{TX\text{-}MAX\text{-}JITTER} = 1 - T_{TX\text{-}EYE} = 0.3$ UI. See Notes 2 and 3. |
| Maximum time between the jitter median and maximum deviation from the median. | $T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ | — | — | 0.15 | UI | Jitter is defined as the measurement variation of the crossing points ($V_{TX\text{-}DIFFp\text{-}p}$ = 0 V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. See Notes 2 and 3. |
| D+/D– Tx Output Rise/Fall Time | $T_{TX\text{-}RISE}$, $T_{TX\text{-}FALL}$ | 0.125 | — | — | UI | See Notes 2 and 5 |
| RMS AC Peak Common Mode Output Voltage | $V_{TX\text{-}CM\text{-}ACp}$ | — | — | 20 | mV | $V_{TX\text{-}CM\text{-}ACp} = RMS(\lvert V_{TXD+} + V_{TXD-}\rvert/2 - V_{TX\text{-}CM\text{-}DC})$<br>$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $\lvert V_{TX\text{-}D+} + V_{TX\text{-}D-}\rvert/2$<br>See Note 2 |
| Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle | $V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$ | 0 | — | 100 | mV | $\lvert V_{TX\text{-}CM\text{-}DC\ (during\ L0)} - V_{TX\text{-}CM\text{-}Idle\text{-}DC\ (During\ Electrical\ Idle)}\rvert \le 100$ mV<br>$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $\lvert V_{TX\text{-}D+} + V_{TX\text{-}D-}\rvert/2$ [L0]<br>$V_{TX\text{-}CM\text{-}Idle\text{-}DC} = DC_{(avg)}$ of $\lvert V_{TX\text{-}D+} + V_{TX\text{-}D-}\rvert/2$ [Electrical Idle]<br>See Note 2. |
| Absolute Delta of DC Common Mode between D+ and D– | $V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$ | 0 | — | 25 | mV | $\lvert V_{TX\text{-}CM\text{-}DC\text{-}D+} - V_{TX\text{-}CM\text{-}DC\text{-}D-}\rvert \le 25$ mV<br>$V_{TX\text{-}CM\text{-}DC\text{-}D+} = DC_{(avg)}$ of $\lvert V_{TX\text{-}D+}\rvert$<br>$V_{TX\text{-}CM\text{-}DC\text{-}D-} = DC_{(avg)}$ of $\lvert V_{TX\text{-}D-}\rvert$<br>See Note 2. |
| Electrical Idle differential Peak Output Voltage | $V_{TX\text{-}IDLE\text{-}DIFFp}$ | 0 | — | 20 | mV | $V_{TX\text{-}IDLE\text{-}DIFFp} = \lvert V_{TX\text{-}IDLE\text{-}D+} - V_{TX\text{-}IDLE\text{-}D-}\rvert \le 20$ mV<br>See Note 2. |
| The amount of voltage change allowed during Receiver Detection | $V_{TX\text{-}RCV\text{-}DETECT}$ | — | — | 600 | mV | The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present. See Note 6. |
| The Tx DC Common Mode Voltage | $V_{TX\text{-}DC\text{-}CM}$ | 0 | — | 3.6 | V | The allowed DC common mode voltage under any conditions. See Note 6. |
| Tx Short Circuit Current Limit | $I_{TX\text{-}SHORT}$ | | — | 90 | mA | The total current the transmitter can provide when shorted to its ground |
| Minimum time spent in electrical idle | $T_{TX\text{-}IDLE\text{-}MIN}$ | 50 | — | | UI | Minimum time a transmitter must be in electrical idle. Utilized by the receiver to start looking for an electrical idle exit after successfully receiving an electrical idle ordered set. |

**Table 49. Differential Transmitter Output Specifications (continued)**

| Parameter | Symbol | Min | Nom | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set | $T_{TX\text{-}IDLE\text{-}SET\text{-}TO\text{-}IDLE}$ | — | — | 20 | UI | After sending an electrical idle ordered set, the transmitter must meet all electrical idle specifications within this time. This is considered a debounce time for the transmitter to meet electrical idle after transitioning from L0. |
| Maximum time to transition to valid Tx specifications after leaving an electrical idle condition | $T_{TX\text{-}IDLE\text{-}TO\text{-}DIFF\text{-}DATA}$ | — | — | 20 | UI | Maximum time to meet all Tx specifications when transitioning from electrical idle to sending differential data. This is considered a debounce time for the Tx to meet all Tx specifications after leaving electrical idle |
| Differential Return Loss | $RL_{TX\text{-}DIFF}$ | 12 | — | — | dB | Measured over 50 MHz to 1.25 GHz. See Note 4 |
| Common Mode Return Loss | $RL_{TX\text{-}CM}$ | 6 | — | — | dB | Measured over 50 MHz to 1.25 GHz. See Note 4 |
| DC Differential TX Impedance | $Z_{TX\text{-}DIFF\text{-}DC}$ | 80 | 100 | 120 | Ω | TX DC differential mode low impedance |
| Transmitter DC Impedance | $Z_{TX\text{-}DC}$ | 40 | — | — | Ω | Required TX D+ as well as D– DC impedance during all states |
| Lane-to-Lane Output Skew | $L_{TX\text{-}SKEW}$ | — | — | 500 + 2 UI | ps | Static skew between any two transmitter lanes within a single link |
| AC Coupling Capacitor | $C_{TX}$ | 75 | — | 200 | nF | All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 8. |
| Crosslink Random Timeout | $T_{crosslink}$ | 0 | — | 1 | ms | This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one downstream and one upstream port. See Note 7. |

**Notes:**
1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 52 and measured over any 250 consecutive Tx UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 50)
3. A $T_{TX\text{-}EYE}$ = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX\text{-}JITTER\text{-}MAX}$ = 0.30 UI for the transmitter collected over any 250 consecutive Tx UIs. The $T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a Vector Network Analyzer with 50 Ω probes—see Figure 52). Note that the series capacitors $C_{TX}$ is optional for the return loss measurement.
5. Measured between 20–80% at transmitter package pins into a test load as shown in Figure 52 for both $V_{TX\text{-}D+}$ and $V_{TX\text{-}D–}$.
6. See Section 4.3.1.8 of the PCI Express Base Specifications Rev 1.0a
7. See Section 4.2.6.3 of the PCI Express Base Specifications Rev 1.0a
8. MPC8640D SerDes transmitter does not have $C_{TX}$ built-in. An external AC coupling capacitor is required.

### 14.4.2 Transmitter Compliance Eye Diagrams

The Tx eye diagram in Figure 50 is specified using the passive compliance/test measurement load (see Figure 52) in place of any real PCI Express interconnect + Rx component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

**NOTE**

It is recommended that the recovered Tx UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).

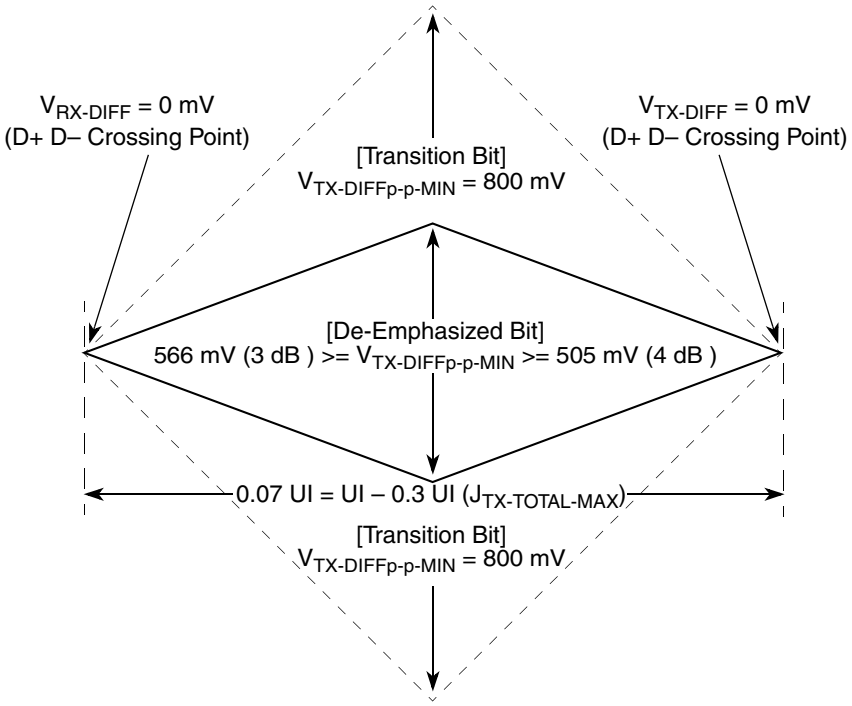



**Figure 50. Minimum Transmitter Timing and Voltage Output Compliance Specifications**

### 14.4.3 Differential Receiver (Rx) Input Specifications

Table 50 defines the specifications for the differential input at all receivers. The parameters are specified at the component pins.

**Table 50. Differential Receiver Input Specifications**

| Parameter | Symbol | Min | Nom | Max | Units | Comments |
|---|---|---|---|---|---|---|
| Unit Interval | UI | 399.88 | 400 | 400.12 | ps | Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1. |
| Differential Peak-to-Peak Output Voltage | $V_{RX-DIFFp-p}$ | 0.175 | — | 1.200 | V | $V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 2. |
| Minimum Receiver Eye Width | $T_{RX-EYE}$ | 0.4 | — | — | UI | The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3. |
| Maximum time between the jitter median and maximum deviation from the median. | $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ | — | — | 0.3 | UI | Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p} = 0$ V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. See Notes 2, 3 and 7. |
| AC Peak Common Mode Input Voltage | $V_{RX-CM-ACp}$ | — | — | 150 | mV | $V_{RX-CM-ACp} = \lvert V_{RXD+} - V_{RXD-} \rvert / 2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\lvert V_{RX-D+} - V_{RX-D-} \rvert / 2$ See Note 2 |
| Differential Return Loss | $RL_{RX-DIFF}$ | 15 | — | — | dB | Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at +300 mV and –300 mV, respectively. See Note 4 |
| Common Mode Return Loss | $RL_{RX-CM}$ | 6 | — | — | dB | Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at 0 V. See Note 4 |
| DC Differential Input Impedance | $Z_{RX-DIFF-DC}$ | 80 | 100 | 120 | Ω | Rx DC Differential mode impedance. See Note 5 |
| DC Input Impedance | $Z_{RX-DC}$ | 40 | 50 | 60 | Ω | Required Rx D+ as well as D– DC impedance (50 ± 20% tolerance). See Notes 2 and 5. |
| Powered Down DC Input Impedance | $Z_{RX-HIGH-IMP-DC}$ | 200 | — | — | kΩ | Required Rx D+ as well as D– DC impedance when the receiver terminations do not have power. See Note 6. |
| Electrical Idle Detect Threshold | $V_{RX-IDLE-DET-DIFFp-p}$ | 65 | — | 175 | mV | $V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver |

**Table 50. Differential Receiver Input Specifications (continued)**

| Parameter | Symbol | Min | Nom | Max | Units | Comments |
|---|---|---|---|---|---|---|
| Unexpected Electrical Idle Enter Detect Threshold Integration Time | $T_{RX-IDLE-DET-DIFF-ENTERTIME}$ | — | — | 10 | ms | An unexpected electrical Idle ($V_{RX-DIFFp-p}$ < $V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition. |
| Total Skew | $L_{TX-SKEW}$ | — | — | 20 | ns | Skew across all lanes on a link. This includes variation in the length of SKP ordered set (for example, COM and one to five symbols) at the Rx as well as any delay differences arising from the interconnect itself. |

**Notes:**
1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 52 should be used as the Rx device when taking measurements (also refer to the Receiver compliance eye diagram shown in Figure 51). If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A $T_{RX-EYE}$ = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D– line biased to –300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 52). Note that the series capacitors $C_{TX}$ is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
6. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit will not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.
7. It is recommended that the recovered Tx UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

## 14.5 Receiver Compliance Eye Diagrams

The Rx eye diagram in Figure 51 is specified using the passive compliance/test measurement load (see Figure 52) in place of any real PCI Express Rx component.

Note that in general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 52) is larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. A Rx component designer should provide

additional margin to adequately compensate for the degraded minimum Rx eye diagram (shown in Figure 51) expected at the input receiver based on some adequate combination of system simulations and the return loss measured looking into the Rx package and silicon. The Rx eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

**NOTE**

The reference impedance for return loss measurements is 50Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes—see Figure 52). Note that the series capacitors, $C_{TX}$, are optional for the return loss measurement.

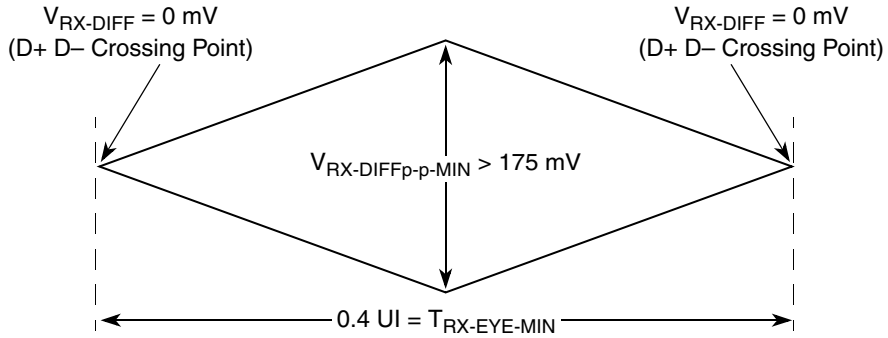



**Figure 51. Minimum Receiver Eye Timing and Voltage Compliance Specification**

### 14.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 52.

**NOTE**

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

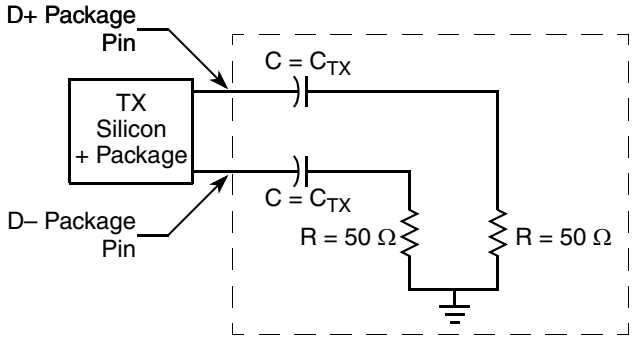



**Figure 52. Compliance Test/Measurement Load**

# 15 Serial RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8640, for the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitter types (short run and long run) on a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that will accept signals from both the short run and long run transmitter specifications.

The short run transmitter specifications should be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of ± 100 ppm. The worst case frequency difference between any transmit and receive clock will be 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

## 15.1 DC Requirements for Serial RapidIO SD*n*_REF_CLK and SD*n*_REF_CLK

For more information, see Section 13.2, "SerDes Reference Clocks."

## 15.2 AC Requirements for Serial RapidIO SD*n*_REF_CLK and SD*n*_REF_CLK

Table 51 lists AC requirements.

**Table 51. SD*n*_REF_CLK and $\overline{\text{SD}n\text{_REF_CLK}}$ AC Requirements**

| Symbol | Parameter Description | Min | Typical | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $t_{REF}$ | REFCLK cycle time | — | 10(8) | — | ns | 8 ns applies only to serial RapidIO with 125-MHz reference clock |
| $t_{REFCJ}$ | REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles | — | — | 80 | ps | — |
| $t_{REFPJ}$ | Phase jitter. Deviation in edge location with respect to mean edge location | –40 | — | 40 | ps | — |

## 15.3 Signal Definitions

LP-Serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 53 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input (RD and $\overline{\text{RD}}$). Each signal swings between A volts and B volts where A > B. Using these waveforms, the definitions are as follows:

1. The transmitter output signals and the receiver input signals TD, $\overline{\text{TD}}$, RD and $\overline{\text{RD}}$ each have a peak-to-peak swing of A – B volts
2. The differential output signal of the transmitter, $V_{OD}$, is defined as $V_{TD} - V_{\overline{TD}}$
3. The differential input signal of the receiver, $V_{ID}$, is defined as $V_{RD} - V_{\overline{RD}}$
4. The differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts

5. The peak value of the differential transmitter output signal and the differential receiver input signal is A – B volts
6. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is 2 × (A – B) volts

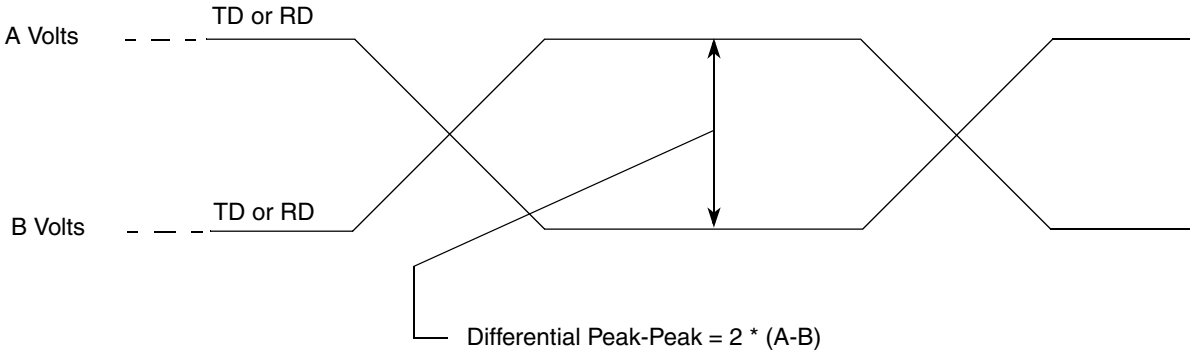



**Figure 53. Differential Peak-Peak Voltage of Transmitter or Receiver**

To illustrate these definitions using real values, consider the case of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{\text{TD}}$ is 500 mV p-p. The differential output signal ranges between 500 mV and –500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

## 15.4 Equalization

With the use of high speed serial links, the interconnect media causes degradation of the signal at the receiver. Effects such as inter-symbol interference (ISI) or data-dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver, often referred to as passive equalization.
- The use of active circuits in the receiver, often referred to as adaptive equalization.

## 15.5 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to the serial RapidIO interface. The goal of this standard is that electrical designs for the serial RapidIO interface can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

## 15.6 Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and Table 52 through Table 57.

The differential return loss, S11, of the transmitter in each case shall be better than

- –10 dB for (Baud Frequency)/10 < Freq(f) < 625 MHz
- –10 dB + 10log(f/625 MHz) dB for 625 MHz ≤ Freq(f) ≤ Baud Frequency

The reference impedance for the differential return loss measurements is 100-Ω resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%–80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-Serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB and 15 ps at 3.125 GB.

**Table 52. Short Run Transmitter AC Timing Specifications—1.25 GBaud**

| Parameter | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Output Voltage | $V_O$ | –0.40 | 2.30 | Volts | Voltage relative to COMMON of either signal comprising a differential pair |
| Differential Output Voltage | $V_{DIFFPP}$ | 500 | 1000 | mV p-p | — |
| Deterministic Jitter | $J_D$ | — | 0.17 | UI p-p | — |
| Total Jitter | $J_T$ | — | 0.35 | UI p-p | — |
| Multiple output skew | $S_{MO}$ | — | 1000 | ps | Skew at the transmitter output between lanes of a multilane link |
| Unit Interval | UI | 800 | 800 | ps | ± 100 ppm |

**Table 53. Short Run Transmitter AC Timing Specifications—2.5 GBaud**

| Parameter | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Output Voltage | $V_O$ | –0.40 | 2.30 | Volts | Voltage relative to COMMON of either signal comprising a differential pair |
| Differential Output Voltage | $V_{DIFFPP}$ | 500 | 1000 | mV p-p | — |

**Table 53. Short Run Transmitter AC Timing Specifications—2.5 GBaud (continued)**

| Parameter | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Deterministic Jitter | $J_D$ | — | 0.17 | UI p-p | — |
| Total Jitter | $J_T$ | — | 0.35 | UI p-p | — |
| Multiple Output skew | $S_{MO}$ | — | 1000 | ps | Skew at the transmitter output between lanes of a multilane link |
| Unit Interval | UI | 400 | 400 | ps | ± 100 ppm |

**Table 54. Short Run Transmitter AC Timing Specifications—3.125 GBaud**

| Parameter | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Output Voltage, | $V_O$ | –0.40 | 2.30 | Volts | Voltage relative to COMMON of either signal comprising a differential pair |
| Differential Output Voltage | $V_{DIFFPP}$ | 500 | 1000 | mV p-p | — |
| Deterministic Jitter | $J_D$ | — | 0.17 | UI p-p | — |
| Total Jitter | $J_T$ | — | 0.35 | UI p-p | — |
| Multiple output skew | $S_{MO}$ | — | 1000 | ps | Skew at the transmitter output between lanes of a multilane link |
| Unit Interval | UI | 320 | 320 | ps | ± 100 ppm |

**Table 55. Long Run Transmitter AC Timing Specifications—1.25 GBaud**

| Parameter | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Output Voltage, | $V_O$ | –0.40 | 2.30 | Volts | Voltage relative to COMMON of either signal comprising a differential pair |
| Differential Output Voltage | $V_{DIFFPP}$ | 800 | 1600 | mV p-p | — |
| Deterministic Jitter | $J_D$ | — | 0.17 | UI p-p | — |
| Total Jitter | $J_T$ | — | 0.35 | UI p-p | — |
| Multiple output skew | $S_{MO}$ | — | 1000 | ps | Skew at the transmitter output between lanes of a multilane link |
| Unit Interval | UI | 800 | 800 | ps | ± 100 ppm |

**Table 56. Long Run Transmitter AC Timing Specifications—2.5 GBaud**

| Parameter | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Output Voltage, | $V_O$ | –0.40 | 2.30 | Volts | Voltage relative to COMMON of either signal comprising a differential pair |
| Differential Output Voltage | $V_{DIFFPP}$ | 800 | 1600 | mV p-p | — |
| Deterministic Jitter | $J_D$ | — | 0.17 | UI p-p | — |
| Total Jitter | $J_T$ | — | 0.35 | UI p-p | — |
| Multiple output skew | $S_{MO}$ | — | 1000 | ps | Skew at the transmitter output between lanes of a multilane link |
| Unit Interval | UI | 400 | 400 | ps | ± 100 ppm |

**Table 57. Long Run Transmitter AC Timing Specifications—3.125 GBaud**

| Parameter | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Output Voltage, | $V_O$ | –0.40 | 2.30 | Volts | Voltage relative to COMMON of either signal comprising a differential pair |
| Differential Output Voltage | $V_{DIFFPP}$ | 800 | 1600 | mV p-p | — |
| Deterministic Jitter | $J_D$ | — | 0.17 | UI p-p | — |
| Total Jitter | $J_T$ | — | 0.35 | UI p-p | — |
| Multiple output skew | $S_{MO}$ | — | 1000 | ps | Skew at the transmitter output between lanes of a multilane link |
| Unit Interval | UI | 320 | 320 | ps | ± 100 ppm |

For each baud rate at which an LP-Serial transmitter is specified to operate, the output eye pattern of the transmitter shall fall entirely within the unshaded portion of the transmitter output compliance mask shown in Figure 54. This figure should be used with the parameters specified in Table 58 when measured at the output pins of the device and the device is driving a 100-Ω ± 5% differential resistive load.The output eye pattern of an LP-Serial transmitter that implements pre-emphasis (to equalize the link and reduce

inter-symbol interference) need only comply with the transmitter output compliance mask when pre-emphasis is disabled or minimized.

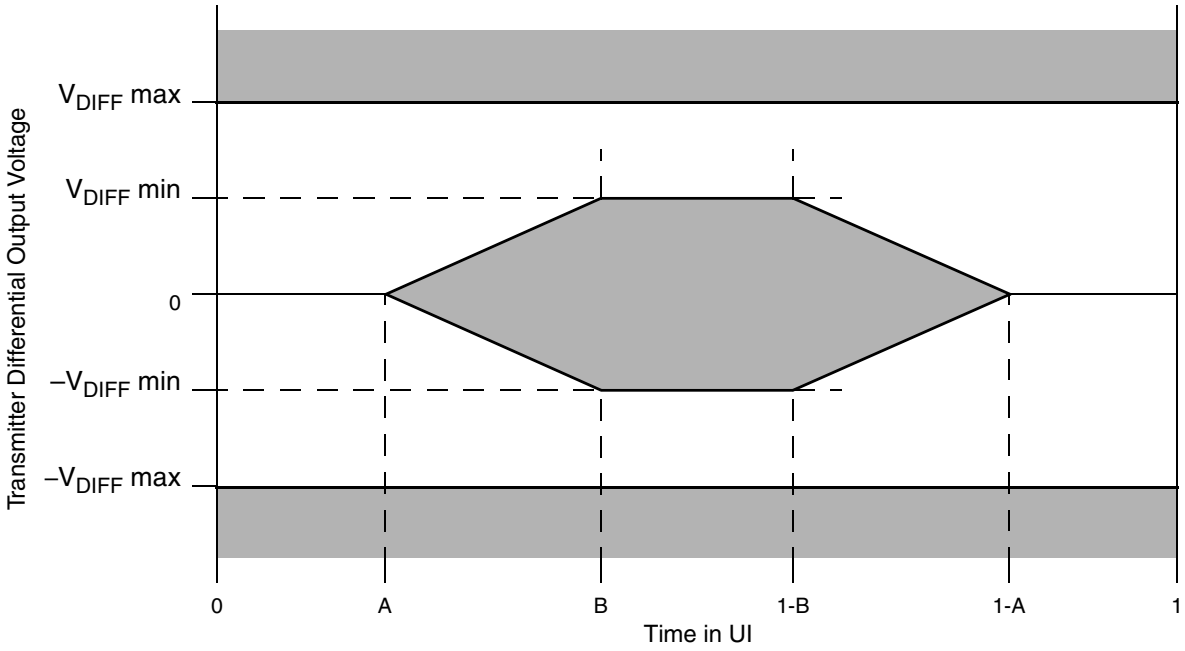



**Figure 54. Transmitter Output Compliance Mask**

Table 58 specifies the parameters for the transmitter differential output eye diagram.

**Table 58. Transmitter Differential Output Eye Diagram Parameters**

| Transmitter Type | $V_{DIFF}$min (mV) | $V_{DIFF}$max (mV) | A (UI) | B (UI) |
|---|---|---|---|---|
| 1.25 GBaud short range | 250 | 500 | 0.175 | 0.39 |
| 1.25 GBaud long range | 400 | 800 | 0.175 | 0.39 |
| 2.5 GBaud short range | 250 | 500 | 0.175 | 0.39 |
| 2.5 GBaud long range | 400 | 800 | 0.175 | 0.39 |
| 3.125 GBaud short range | 250 | 500 | 0.175 | 0.39 |
| 3.125 GBaud long range | 400 | 800 | 0.175 | 0.39 |

## 15.7 Receiver Specifications

LP-Serial receiver electrical and timing specifications are stated in the text and Table 59 through Table 61.

Receiver input impedance shall result in a differential return loss better that 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8) × (Baud Frequency). This includes contributions from on-chip circuitry, the chip package and any off-chip components related to the receiver. AC-coupling

components are included in this requirement. The reference impedance for return loss measurements is 100-Ω resistive for differential return loss and 25-Ω resistive for common mode.

**Table 59. Receiver AC Timing Specifications—1.25 GBaud**

| Parameter | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Differential Input Voltage | $V_{IN}$ | 200 | 1600 | mV p-p | Measured at receiver |
| Deterministic Jitter Tolerance | $J_D$ | 0.37 | — | UI p-p | Measured at receiver |
| Combined Deterministic and Random Jitter Tolerance | $J_{DR}$ | 0.55 | — | UI p-p | Measured at receiver |
| Total Jitter Tolerance[1] | $J_T$ | 0.65 | — | UI p-p | Measured at receiver |
| Multiple Input Skew | $S_{MI}$ | — | 24 | ns | Skew at the receiver input between lanes of a multilane link |
| Bit Error Rate | BER | — | $10^{-12}$ | — | — |
| Unit Interval | UI | 800 | 800 | ps | +/– 100 ppm |

**Note:**

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 55. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

**Table 60. Receiver AC Timing Specifications—2.5 GBaud**

| Parameter | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Differential Input Voltage | $V_{IN}$ | 200 | 1600 | mV p-p | Measured at receiver |
| Deterministic Jitter Tolerance | $J_D$ | 0.37 | — | UI p-p | Measured at receiver |
| Combined Deterministic and Random Jitter Tolerance | $J_{DR}$ | 0.55 | — | UI p-p | Measured at receiver |
| Total Jitter Tolerance[1] | $J_T$ | 0.65 | — | UI p-p | Measured at receiver |
| Multiple Input Skew | $S_{MI}$ | — | 24 | ns | Skew at the receiver input between lanes of a multilane link |
| Bit Error Rate | BER | — | $10^{-12}$ | — | — |
| Unit Interval | UI | 400 | 400 | ps | ± 100 ppm |

**Note:**

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 55. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

**Table 61. Receiver AC Timing Specifications—3.125 GBaud**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Differential Input Voltage | $V_{IN}$ | 200 | 1600 | mV p-p | Measured at receiver |
| Deterministic Jitter Tolerance | $J_D$ | 0.37 | — | UI p-p | Measured at receiver |
| Combined Deterministic and Random Jitter Tolerance | $J_{DR}$ | 0.55 | — | UI p-p | Measured at receiver |
| Total Jitter Tolerance[1] | $J_T$ | 0.65 | — | UI p-p | Measured at receiver |
| Multiple Input Skew | $S_{MI}$ | — | 22 | ns | Skew at the receiver input between lanes of a multilane link |
| Bit Error Rate | BER | — | $10^{-12}$ | — | — |
| Unit Interval | UI | 320 | 320 | ps | ± 100 ppm |

**Note:**

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 55. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

Figure 55 shows the single frequency sinusoidal jitter limits.

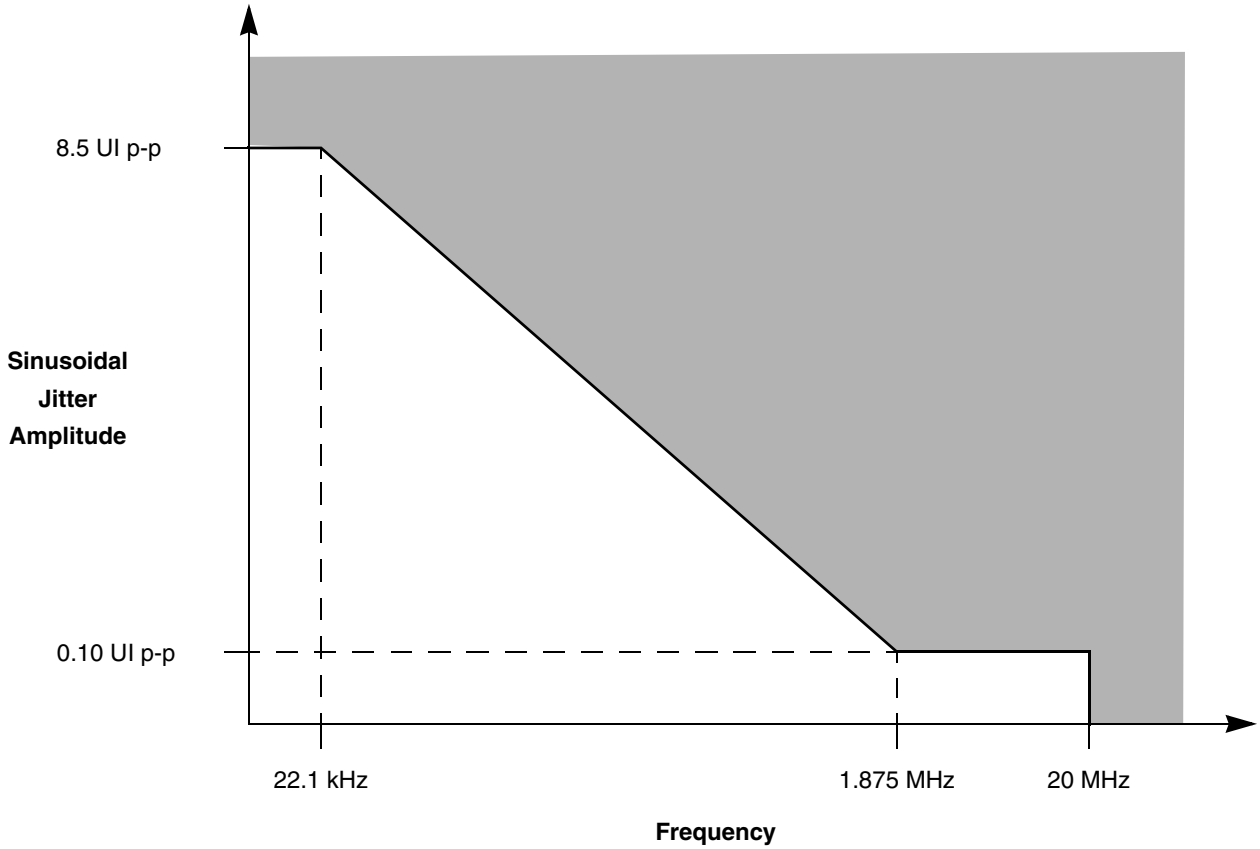



**Figure 55. Single Frequency Sinusoidal Jitter Limits**

## 15.8 Receiver Eye Diagrams

For each baud rate at which an LP-Serial receiver is specified to operate, the receiver shall meet the corresponding bit error rate specification (Table 59 through Table 61) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the shown in Figure 56 with the parameters specified in Table 62. The eye pattern of the receiver test signal is measured

at the input pins of the receiving device with the device replaced with a 100 Ω ± 5% differential resistive load.

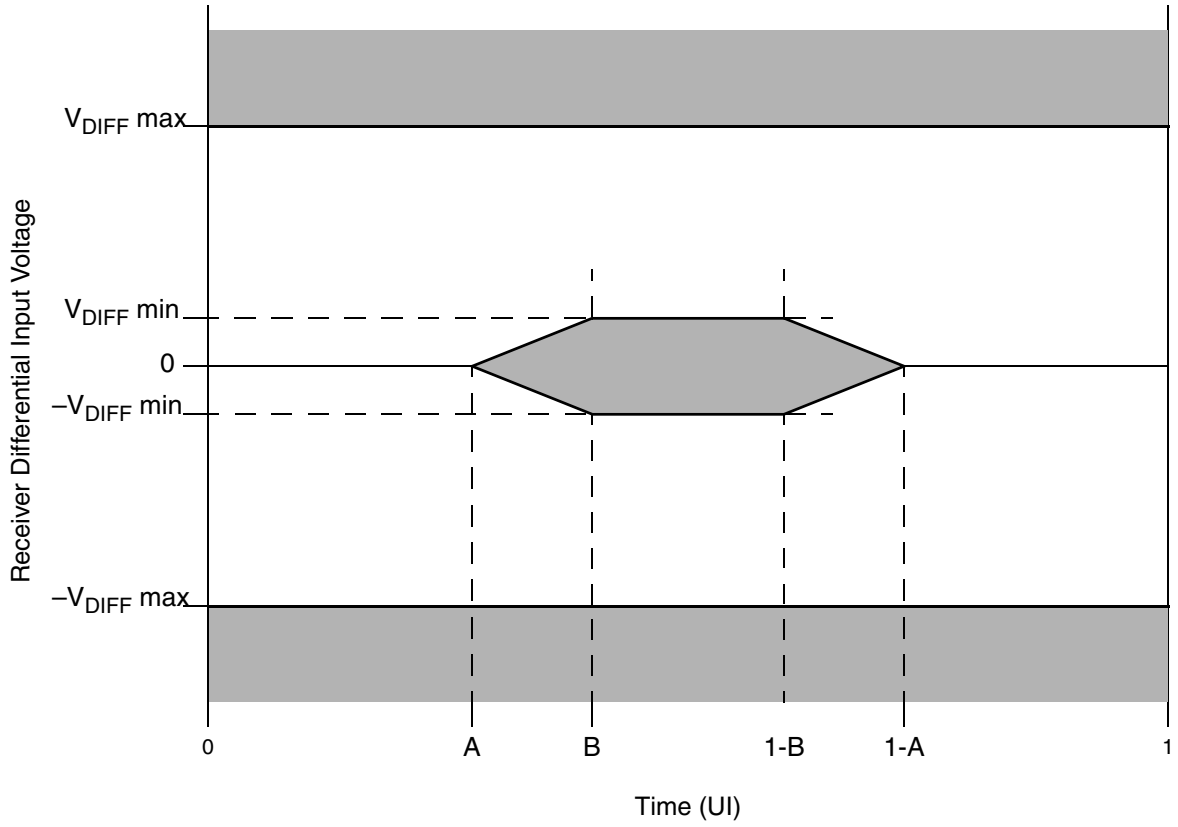



**Figure 56. Receiver Input Compliance Mask**

Table 62 shows the parameters for the receiver input compliance mask exclusive of sinusoidal jitter.

**Table 62. Receiver Input Compliance Mask Parameters Exclusive of Sinusoidal Jitter**

| Receiver Type | $V_{DIFF}$min (mV) | $V_{DIFF}$max (mV) | A (UI) | B (UI) |
|---|---|---|---|---|
| 1.25 GBaud | 100 | 800 | 0.275 | 0.400 |
| 2.5 GBaud | 100 | 800 | 0.275 | 0.400 |
| 3.125 GBaud | 100 | 800 | 0.275 | 0.400 |

## 15.9 Measurement and Test Requirements

Since the LP-Serial electrical specification are guided by the XAUI electrical interface specified in clause 47 of IEEE 802.3ae-2002, the measurement and test requirements defined here are similarly guided by clause 47. In addition, the CJPAT test pattern defined in Annex 48A of IEEE802.3ae-2002 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of IEEE802.3ae-2002 is recommended as a reference for additional information on jitter test methods.

### 15.9.1 Eye Template Measurements

For the purpose of eye template measurements, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency) ÷ 1667 is applied to the jitter. The data pattern for template measurements is the continuous jitter test pattern (CJPAT) defined in Annex 48A of IEEE802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than $10^{-12}$. The eye pattern shall be measured with AC coupling and the compliance template centered at 0 V differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be 100-Ω resistive ± 5% differential to 2.5 GHz.

### 15.9.2 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency) ÷ 1667 is applied to the jitter. The data pattern for jitter measurements is the continuous jitter test pattern (CJPAT) pattern defined in Annex 48A of IEEE802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 V differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of IEEE802.3ae.

### 15.9.3 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100-Ω resistive ± 5% differential to 2.5 GHz.

### 15.9.4 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in Section 15.7, “Receiver Specifications,” and then adjusting the signal amplitude until the data eye contacts the six points of the minimum eye opening of the receive template shown in Figure 56 and Table 62.Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in Section 15.7, “Receiver Specifications,” is then added to the signal and the test load is replaced by the receiver being tested.

# 16 Package

This section details package parameters and dimensions.

## 16.1 Package Parameters for the MPC8640

The package parameters are as provided in the following list. The package type is 33 mm × 33 mm, 1023 pins. There are four package options: high-lead flip chip-ceramic ball grid array (FC-CBGA) with lead C4 die bump and lead C5 solder balls, lead-free FC-CBGA with lead C4 bumps and lead-free solder balls (RoHS permitted exception in some cases), completely lead-free FC-CBGA, and otherwise lead-free FC-CBGA with lead solder balls for certain non-RoHS applications.

For all package types:

| | |
|---|---|
| Die size | 12.1 mm × 14.7 mm |
| Package outline | 33 mm × 33 mm |
| Interconnects | 1023 |
| Pitch | 1 mm |
| Total Capacitor count | 43 caps; 100 nF each |

For high-lead FC-CBGA (package option: HCTE[1] HX) or lead-free FC-CBGA with leaded solder balls (package option: HCTE[1] HJ)

| | |
|---|---|
| Maximum module height | 2.97 mm |
| Minimum module height | 2.47 mm |
| Solder Balls | 89.5% Pb 10.5% Sn |
| Ball diameter (typical[2]) | 0.60 mm |

For RoHS lead-free FC-CBGA (package option: HCTE[1] VU) and lead-free FC-CBGA (package option: HCTE[1] VJ)

| | |
|---|---|
| Maximum module height | 2.77 mm |
| Minimum module height | 2.27 mm |
| Solder Balls | 95.5% Sn 4.0% Ag 0.5% Cu |
| Ball diameter (typical[2]) | 0.60 mm |

[1] High-coefficient of thermal expansion

[2] Typical ball diameter is before reflow

## 16.2 Mechanical Dimensions of the MPC8640 FC-CBGA

The mechanical dimensions and bottom surface nomenclature of the MPC8640D (dual core) and MPC8640 (single core) high-lead FC-CBGA (package option: HCTE HX or HCTE HJ) and lead-free

FC-CBGA (package option: HCTE VU or HCTE VJ) are shown respectively Figure 57 and Figure 58.

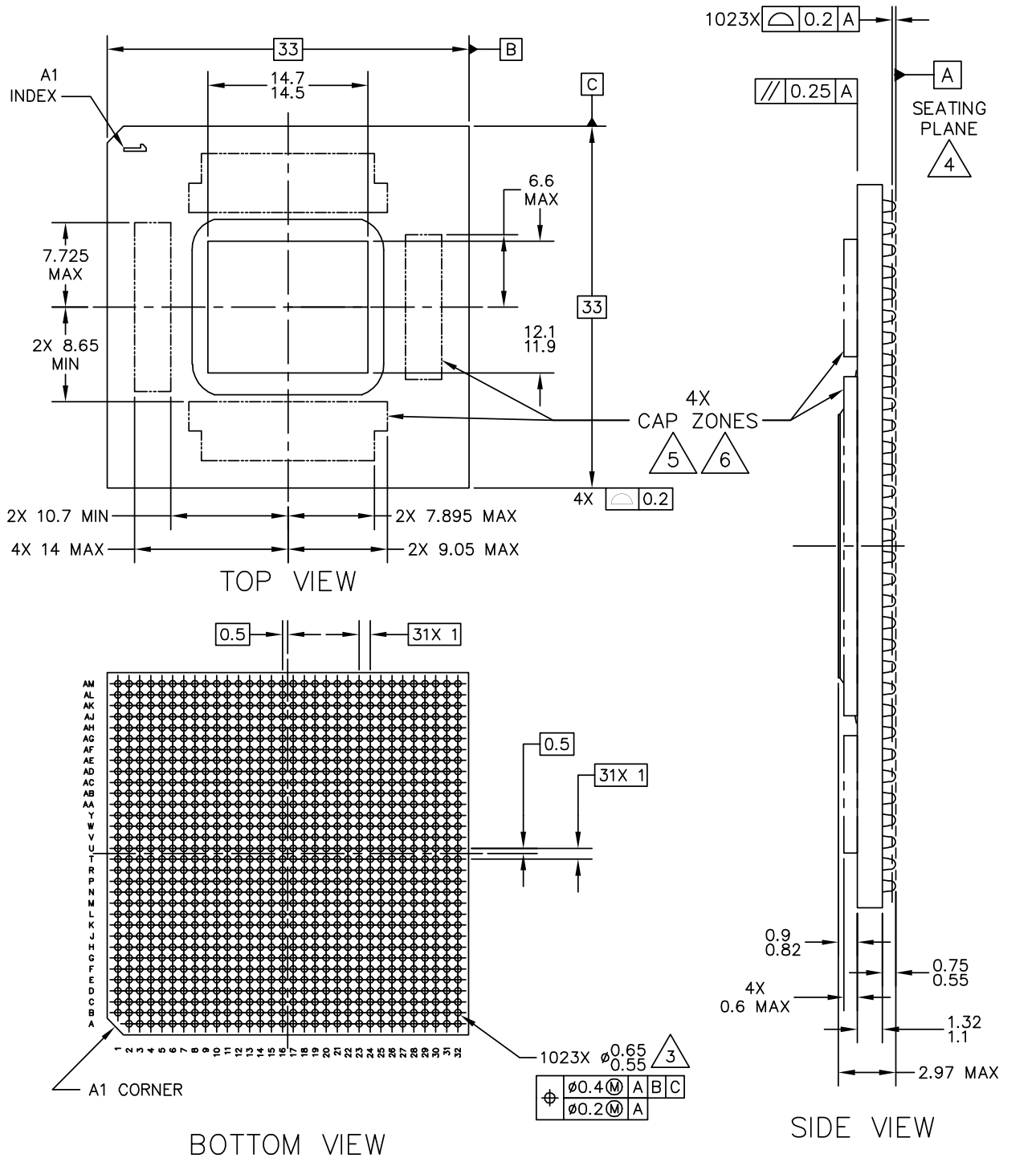



**Figure 57. MPC8640D High-Lead FC-CBGA Dimensions**

### NOTES for Figure 57

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.
5. Capacitors may not be present on all devices.
6. Caution must be taken not to short capacitors or expose metal capacitor pads on package top.
7. All dimensions symmetrical about centerlines unless otherwise specified.
8. Note that for MPC8640 (single core) the solder balls for the following signals/pins are not populated in the package: VDD_Core1 (R16, R18, R20, T17, T19, T21, T23, U16, U18, U22, V17, V19, V21, V23, W16, W18, W20, W22, Y17, Y19, Y21, Y23, AA16, AA18, AA20, AA22, AB23, AC24) and SENSEVDD_Core1 (U20).

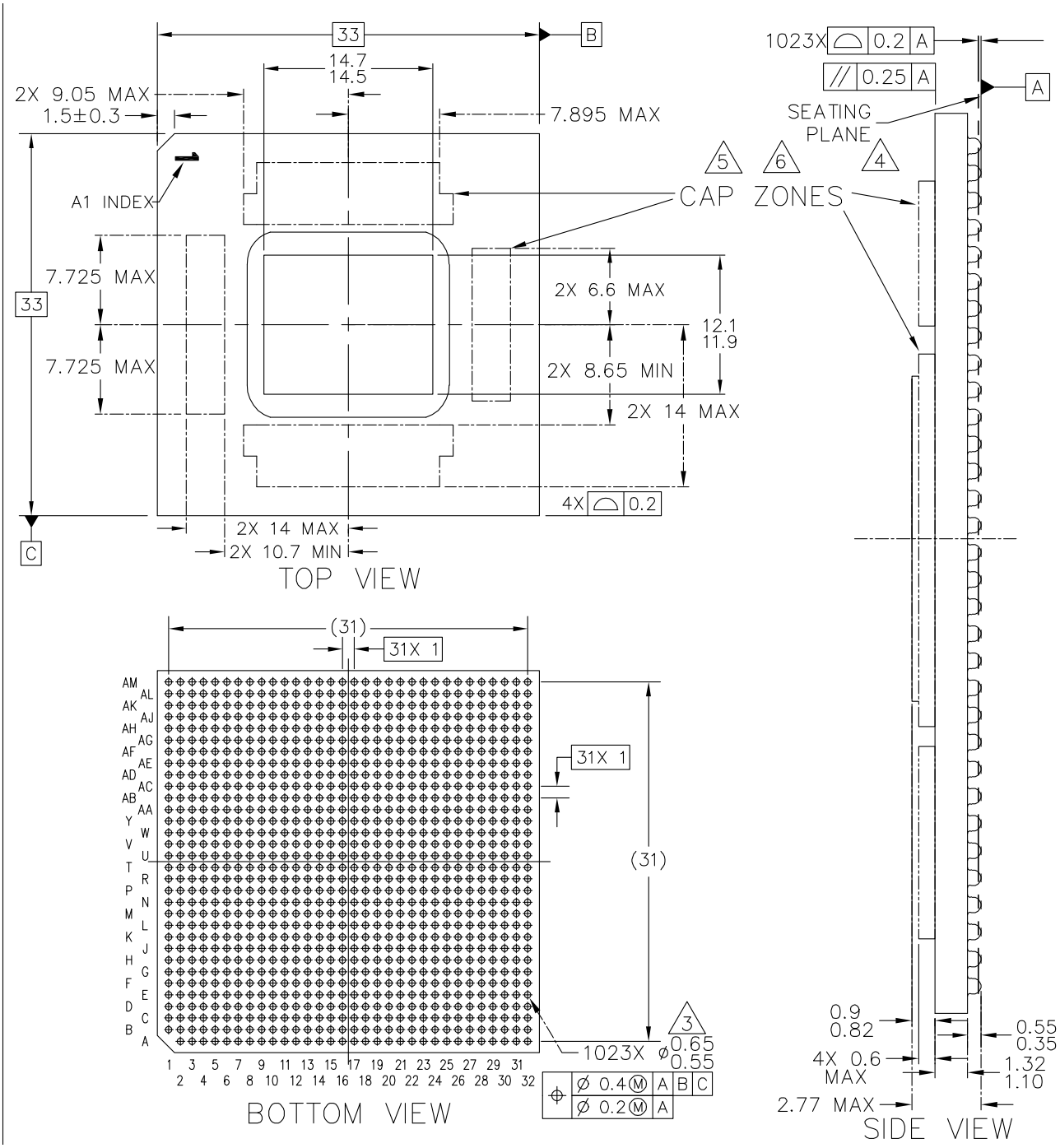



**Figure 58. MPC8640D Lead-Free FC-CBGA Dimensions**

**NOTES for Figure 58**

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.
5. Capacitors may not be present on all devices.
6. Caution must be taken not to short capacitors or expose metal capacitor pads on package top.
7. All dimensions symmetrical about centerlines unless otherwise specified.
8. Note that for MPC8640 (single core) the solder balls for the following signals/pins are not populated in the package: VDD_Core1 (R16, R18, R20, T17, T19, T21, T23, U16, U18, U22, V17, V19, V21, V23, W16, W18, W20, W22, Y17, Y19, Y21, Y23, AA16, AA18, AA20, AA22, AB23, AC24) and SENSEVDD_Core1 (U20).

# 17 Signal Listings

Table 63 provides the pin assignments for the signals. Notes for the signal changes on the single core device (MPC8640) are italicized and prefixed by *S*.

**Table 63. MPC8640 Signal Reference by Functional Block**

| Name[1] | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **DDR Memory Interface 1 Signals[2,3]** | | | | |
| D1_MDQ[0:63] | D15, A14, B12, D12, A15, B15, B13, C13, C11, D11, D9, A8, A12, A11, A9, B9, F11, G12, K11, K12, E10, E9, J11, J10, G8, H10, L9, L7, F10, G9, K9, K8, AC6, AC7, AG8, AH9, AB6, AB8, AE9, AF9, AL8, AM8, AM10, AK11, AH8, AK8, AJ10, AK10, AL12, AJ12, AL14, AM14, AL11, AM11, AM13, AK14, AM15, AJ16, AK18, AL18, AJ15, AL15, AL17, AM17 | I/O | $D1_GV_{DD}$ | — |
| D1_MECC[0:7] | M8, M7, R8, T10, L11, L10, P9, R10 | I/O | $D1_GV_{DD}$ | — |
| D1_MDM[0:8] | C14, A10, G11, H9, AD7, AJ9, AM12, AK16, N10 | O | $D1_GV_{DD}$ | — |
| D1_MDQS[0:8] | A13, C10, H12, J7, AE8, AM9, AK13, AK17, N9 | I/O | $D1_GV_{DD}$ | — |
| $\overline{\text{D1_MDQS}}$[0:8] | D14, B10, H13, J8, AD8, AL9, AJ13, AM16, P10 | I/O | $D1_GV_{DD}$ | — |
| D1_MBA[0:2] | AA8, AA10, T9 | O | $D1_GV_{DD}$ | — |
| D1_MA[0:15] | Y10, W8, W9, V7, V8, U6, V10, U9, U7, U10, Y9, T6, T8, AE12, R7, P6 | O | $D1_GV_{DD}$ | — |
| $\overline{\text{D1_MWE}}$ | AB11 | O | $D1_GV_{DD}$ | — |
| $\overline{\text{D1_MRAS}}$ | AB12 | O | $D1_GV_{DD}$ | — |
| $\overline{\text{D1_MCAS}}$ | AC10 | O | $D1_GV_{DD}$ | — |
| $\overline{\text{D1_MCS}}$[0:3] | AB9, AD10, AC12, AD11 | O | $D1_GV_{DD}$ | — |
| D1_MCKE[0:3] | P7, M10, N8, M11 | O | $D1_GV_{DD}$ | 23 |
| D1_MCK[0:5] | W6, E13, AH11, Y7, F14, AG10 | O | $D1_GV_{DD}$ | — |
| $\overline{\text{D1_MCK}}$[0:5] | Y6, E12, AH12, AA7, F13, AG11 | O | $D1_GV_{DD}$ | — |

**Table 63. MPC8640 Signal Reference by Functional Block (continued)**

| Name[1] | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| D1_MODT[0:3] | AC9, AF12, AE11, AF10 | O | $D1_GV_{DD}$ | — |
| D1_MDIC[0:1] | E15, G14 | IO | $D1_GV_{DD}$ | 27 |
| $D1_MV_{REF}$ | AM18 | DDR Port 1 reference voltage | $D1_GV_{DD}$ /2 | 3 |
| **DDR Memory Interface 2 Signals[2,3]** | | | | |
| D2_MDQ[0:63] | A7, B7, C5, D5, C8, D8, D6, A5, C4, A3, D3, D2, A4, B4, C2, C1, E3, E1, H4, G1, D1, E4, G3, G2, J4, J2, L1, L3, H3, H1, K1, L4, AA4, AA2, AD1, AD2, Y1, AA1, AC1, AC3, AD5, AE1, AG1, AG2, AC4, AD4, AF3, AF4, AH3, AJ1, AM1, AM3, AH1, AH2, AL2, AL3, AK5, AL5, AK7, AM7, AK4, AM4, AM6, AJ7 | I/O | $D2_GV_{DD}$ | — |
| D2_MECC[0:7] | H6, J5, M5, M4, G6, H7, M2, M1 | I/O | $D2_GV_{DD}$ | — |
| D2_MDM[0:8] | C7, B3, F4, J1, AB1, AE2, AK1, AM5, K6 | O | $D2_GV_{DD}$ | — |
| D2_MDQS[0:8] | B6, B1, F1, K2, AB3, AF1, AL1, AL6, L6 | I/O | $D2_GV_{DD}$ | — |
| $\overline{\text{D2_MDQS}}$[0:8] | A6, A2, F2, K3, AB2, AE3, AK2, AJ6, K5 | I/O | $D2_GV_{DD}$ | — |
| D2_MBA[0:2] | W5, V5, P3 | O | $D2_GV_{DD}$ | — |
| D2_MA[0:15] | W1, U4, U3, T1, T2, T3, T5, R2, R1, R5, V4, R4, P1, AH5, P4, N1 | O | $D2_GV_{DD}$ | — |
| $\overline{\text{D2_MWE}}$ | Y4 | O | $D2_GV_{DD}$ | — |
| $\overline{\text{D2_MRAS}}$ | W3 | O | $D2_GV_{DD}$ | — |
| $\overline{\text{D2_MCAS}}$ | AB5 | O | $D2_GV_{DD}$ | — |
| $\overline{\text{D2_MCS}}$[0:3] | Y3, AF6, AA5, AF7 | O | $D2_GV_{DD}$ | — |
| D2_MCKE[0:3] | N6, N5, N2, N3 | O | $D2_GV_{DD}$ | 23 |
| D2_MCK[0:5] | U1, F5, AJ3, V2, E7, AG4 | O | $D2_GV_{DD}$ | — |
| $\overline{\text{D2_MCK}}$[0:5] | V1, G5, AJ4, W2, E6, AG5 | O | $D2_GV_{DD}$ | — |
| D2_MODT[0:3] | AE6, AG7, AE5, AH6 | O | $D2_GV_{DD}$ | — |
| D2_MDIC[0:1] | F8, F7 | IO | $D2_GV_{DD}$ | 27 |
| $D2_MV_{REF}$ | A18 | DDR Port 2 reference voltage | $D2_GV_{DD}$ /2 | 3 |
| **High Speed I/O Interface 1 (SERDES 1)[4]** | | | | |
| SD1_TX[0:7] | L26, M24, N26, P24, R26, T24, U26, V24 | O | $SV_{DD}$ | — |
| $\overline{\text{SD1_TX}}$[0:7] | L27, M25, N27, P25, R27, T25, U27, V25 | O | $SV_{DD}$ | — |
| SD1_RX[0:7] | J32, K30, L32, M30, T30, U32, V30, W32 | I | $SV_{DD}$ | — |
| $\overline{\text{SD1_RX}}$[0:7] | J31, K29, L31, M29, T29, U31, V29, W31 | I | $SV_{DD}$ | — |
| SD1_REF_CLK | N32 | I | $SV_{DD}$ | — |
| $\overline{\text{SD1_REF_CLK}}$ | N31 | I | $SV_{DD}$ | — |

**Table 63. MPC8640 Signal Reference by Functional Block (continued)**

| Name[1] | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| SD1_IMP_CAL_TX | Y26 | Analog | $SV_{DD}$ | 19 |
| SD1_IMP_CAL_RX | J28 | Analog | $SV_{DD}$ | 30 |
| SD1_PLL_TPD | U28 | O | $SV_{DD}$ | 13, 17 |
| SD1_PLL_TPA | T28 | Analog | $SV_{DD}$ | 13, 18 |
| SD1_DLL_TPD | N28 | O | $SV_{DD}$ | 13, 17 |
| SD1_DLL_TPA | P31 | Analog | $SV_{DD}$ | 13, 18 |
| **High Speed I/O Interface 2 (SERDES 2)[4]** | | | | |
| SD2_TX[0:3] | Y24, AA27, AB25, AC27 | O | $SV_{DD}$ | — |
| SD2_TX[4:7] | AE27, AG27, AJ27, AL27 | O | $SV_{DD}$ | 34 |
| $\overline{\text{SD2_TX}}$[0:3] | Y25, AA28, AB26, AC28 | O | $SV_{DD}$ | — |
| $\overline{\text{SD2_TX}}$[4:7] | AE28, AG28, AJ28, AL28 | O | $SV_{DD}$ | 34 |
| SD2_RX[0:3] | Y30, AA32, AB30, AC32 | I | $SV_{DD}$ | 32 |
| SD2_RX[4:7] | AH30, AJ32, AK30, AL32 | I | $SV_{DD}$ | 32, 35 |
| $\overline{\text{SD2_RX}}$[0:3] | Y29, AA31, AB29, AC31 | I | $SV_{DD}$ | — |
| $\overline{\text{SD2_RX}}$[4:7] | AH29, AJ31, AK29, AL31 | I | $SV_{DD}$ | 35 |
| SD2_REF_CLK | AE32 | I | $SV_{DD}$ | — |
| $\overline{\text{SD2_REF_CLK}}$ | AE31 | I | $SV_{DD}$ | — |
| SD2_IMP_CAL_TX | AM29 | Analog | $SV_{DD}$ | 19 |
| SD2_IMP_CAL_RX | AA26 | Analog | $SV_{DD}$ | 30 |
| SD2_PLL_TPD | AF29 | O | $SV_{DD}$ | 13, 17 |
| SD2_PLL_TPA | AF31 | Analog | $SV_{DD}$ | 13, 18 |
| SD2_DLL_TPD | AD29 | O | $SV_{DD}$ | 13, 17 |
| SD2_DLL_TPA | AD30 | Analog | $SV_{DD}$ | 13, 18 |
| **Special Connection Requirement pins** | | | | |
| No Connects | K24, K25, P28, P29, W26, W27, AD25, AD26 | — | — | 13 |
| Reserved | H30, R32, V28, AG32 | — | — | 14 |
| Reserved | H29, R31, W28, AG31 | — | — | 15 |
| Reserved | AD24, AG26 | — | — | 16 |
| **Ethernet Miscellaneous Signals[5]** | | | | |
| EC1_GTX_CLK125 | AL23 | I | $LV_{DD}$ | 39 |
| EC2_GTX_CLK125 | AM23 | I | $TV_{DD}$ | 39 |
| EC_MDC | G31 | O | $OV_{DD}$ | — |
| EC_MDIO | G32 | I/O | $OV_{DD}$ | — |
| **eTSEC Port 1 Signals[5]** | | | | |

**Table 63. MPC8640 Signal Reference by Functional Block (continued)**

| Name[1] | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| TSEC1_TXD[0:7]/ GPOUT[0:7] | AF25, AC23,AG24, AG23, AE24, AE23, AE22, AD22 | O | $LV_{DD}$ | 6, 10 |
| TSEC1_TX_EN | AB22 | O | $LV_{DD}$ | 36 |
| TSEC1_TX_ER | AH26 | O | $LV_{DD}$ | — |
| TSEC1_TX_CLK | AC22 | I | $LV_{DD}$ | 40 |
| TSEC1_GTX_CLK | AH25 | O | $LV_{DD}$ | 41 |
| TSEC1_CRS | AM24 | I/O | $LV_{DD}$ | 37 |
| TSEC1_COL | AM25 | I | $LV_{DD}$ | — |
| TSEC1_RXD[0:7]/ GPIN[0:7] | AL25, AL24, AK26, AK25, AM26, AF26, AH24, AG25 | I | $LV_{DD}$ | 10 |
| TSEC1_RX_DV | AJ24 | I | $LV_{DD}$ | — |
| TSEC1_RX_ER | AJ25 | I | $LV_{DD}$ | — |
| TSEC1_RX_CLK | AK24 | I | $LV_{DD}$ | 40 |
| **eTSEC Port 2 Signals[5]** | | | | |
| TSEC2_TXD[0:3]/ GPOUT[8:15] | AB20, AJ23, AJ22, AD19 | O | $LV_{DD}$ | 6, 10 |
| TSEC2_TXD[4]/ GPOUT[12] | AH23 | O | $LV_{DD}$ | 6,10, 38 |
| TSEC2_TXD[5:7]/ GPOUT[13:15] | AH21, AG22, AG21 | O | $LV_{DD}$ | 6, 10 |
| TSEC2_TX_EN | AB21 | O | $LV_{DD}$ | 36 |
| TSEC2_TX_ER | AB19 | O | $LV_{DD}$ | 6, 38 |
| TSEC2_TX_CLK | AC21 | I | $LV_{DD}$ | 40 |
| TSEC2_GTX_CLK | AD20 | O | $LV_{DD}$ | 41 |
| TSEC2_CRS | AE20 | I/O | $LV_{DD}$ | 37 |
| TSEC2_COL | AE21 | I | $LV_{DD}$ | — |
| TSEC2_RXD[0:7]/ GPIN[8:15] | AL22, AK22, AM21, AH20, AG20, AF20, AF23, AF22 | I | $LV_{DD}$ | 10 |
| TSEC2_RX_DV | AC19 | I | $LV_{DD}$ | — |
| TSEC2_RX_ER | AD21 | I | $LV_{DD}$ | — |
| TSEC2_RX_CLK | AM22 | I | $LV_{DD}$ | 40 |
| **eTSEC Port 3 Signals[5]** | | | | |
| TSEC3_TXD[0:3] | AL21, AJ21, AM20, AJ20 | O | $TV_{DD}$ | 6 |
| TSEC3_TXD[4]/ | AM19 | O | $TV_{DD}$ | — |
| TSEC3_TXD[5:7] | AK21, AL20, AL19 | O | $TV_{DD}$ | 6 |
| TSEC3_TX_EN | AH19 | O | $TV_{DD}$ | 36 |

**Table 63. MPC8640 Signal Reference by Functional Block (continued)**

| Name[1] | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| TSEC3_TX_ER | AH17 | O | $TV_{DD}$ | — |
| TSEC3_TX_CLK | AH18 | I | $TV_{DD}$ | 40 |
| TSEC3_GTX_CLK | AG19 | O | $TV_{DD}$ | 41 |
| TSEC3_CRS | AE15 | I/O | $TV_{DD}$ | 37 |
| TSEC3_COL | AF15 | I | $TV_{DD}$ | — |
| TSEC3_RXD[0:7] | AJ17, AE16, AH16, AH14, AJ19, AH15, AG16, AE19 | I | $TV_{DD}$ | — |
| TSEC3_RX_DV | AG15 | I | $TV_{DD}$ | — |
| TSEC3_RX_ER | AF16 | I | $TV_{DD}$ | — |
| TSEC3_RX_CLK | AJ18 | I | $TV_{DD}$ | 40 |
| **eTSEC Port 4 Signals[5]** | | | | |
| TSEC4_TXD[0:3] | AC18, AC16, AD18, AD17 | O | $TV_{DD}$ | 6 |
| TSEC4_TXD[4] | AD16 | O | $TV_{DD}$ | 25 |
| TSEC4_TXD[5:7] | AB18, AB17, AB16 | O | $TV_{DD}$ | 6 |
| TSEC4_TX_EN | AF17 | O | $TV_{DD}$ | 36 |
| TSEC4_TX_ER | AF19 | O | $TV_{DD}$ | — |
| TSEC4_TX_CLK | AF18 | I | $TV_{DD}$ | 40 |
| TSEC4_GTX_CLK | AG17 | O | $TV_{DD}$ | 41 |
| TSEC4_CRS | AB14 | I/O | $TV_{DD}$ | 37 |
| TSEC4_COL | AC13 | I | $TV_{DD}$ | — |
| TSEC4_RXD[0:7] | AG14, AD13, AF13, AD14, AE14, AB15, AC14, AE17 | I | $TV_{DD}$ | — |
| TSEC4_RX_DV | AC15 | I | $TV_{DD}$ | — |
| TSEC4_RX_ER | AF14 | I | $TV_{DD}$ | — |
| TSEC4_RX_CLK | AG13 | I | $TV_{DD}$ | 40 |
| **Local Bus Signals[5]** | | | | |
| LAD[0:31] | A30, E29, C29, D28, D29, H25, B29, A29, C28, L22, M22, A28, C27, H26, G26, B27, B26, A27, E27, G25, D26, E26, G24, F27, A26, A25, C25, H23, K22, D25, F25, H22 | I/O | $OV_{DD}$ | 6 |
| LDP[0:3] | A24, E24, C24, B24 | I/O | $OV_{DD}$ | 6, 22 |
| LA[27:31] | J21, K21, G22, F24, G21 | O | $OV_{DD}$ | 6, 22 |
| $\overline{\text{LCS}}$[0:4] | A22, C22, D23, E22, A23 | O | $OV_{DD}$ | 7 |
| $\overline{\text{LCS}}$[5]/$\overline{\text{DMA_DREQ}}$[2] | B23 | O | $OV_{DD}$ | 7, 9, 10 |
| $\overline{\text{LCS}}$[6]/$\overline{\text{DMA_DACK}}$[2] | E23 | O | $OV_{DD}$ | 7, 10 |
| $\overline{\text{LCS}}$[7]/$\overline{\text{DMA_DDONE}}$[2] | F23 | O | $OV_{DD}$ | 7, 10 |

**Table 63. MPC8640 Signal Reference by Functional Block (continued)**

| Name[1] | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| $\overline{\text{LWE}}$[0:3]/ LSDDQM[0:3]/ $\overline{\text{LBS}}$[0:3] | E21, F21, D22, E20 | O | $OV_{DD}$ | 6 |
| LBCTL | D21 | O | $OV_{DD}$ | — |
| LALE | E19 | O | $OV_{DD}$ | — |
| LGPL0/LSDA10 | F20 | O | $OV_{DD}$ | 25 |
| LGPL1/$\overline{\text{LSDWE}}$ | H20 | O | $OV_{DD}$ | 25 |
| LGPL2/$\overline{\text{LOE}}$/ $\overline{\text{LSDRAS}}$ | J20 | O | $OV_{DD}$ | — |
| LGPL3/$\overline{\text{LSDCAS}}$ | K20 | O | $OV_{DD}$ | 6 |
| LGPL4/$\overline{\text{LGTA}}$/ LUPWAIT/LPBSE | L21 | I/O | $OV_{DD}$ | 42 |
| LGPL5 | J19 | O | $OV_{DD}$ | 6 |
| LCKE | H19 | O | $OV_{DD}$ | — |
| LCLK[0:2] | G19, L19, M20 | O | $OV_{DD}$ | — |
| LSYNC_IN | M19 | I | $OV_{DD}$ | — |
| LSYNC_OUT | D20 | O | $OV_{DD}$ | — |
| **DMA Signals[5]** | | | | |
| $\overline{\text{DMA_DREQ}}$[0:1] | E31, E32 | I | $OV_{DD}$ | — |
| $\overline{\text{DMA_DREQ}}$[2]/$\overline{\text{LCS}}$[5] | B23 | I | $OV_{DD}$ | 9, 10 |
| $\overline{\text{DMA_DREQ}}$[3]/IRQ[9] | B30 | I | $OV_{DD}$ | 10 |
| $\overline{\text{DMA_DACK}}$[0:1] | D32, F30 | O | $OV_{DD}$ | — |
| $\overline{\text{DMA_DACK}}$[2]/$\overline{\text{LCS}}$[6] | E23 | O | $OV_{DD}$ | 10 |
| $\overline{\text{DMA_DACK}}$[3]/IRQ[10] | C30 | O | $OV_{DD}$ | 9, 10 |
| $\overline{\text{DMA_DDONE}}$[0:1] | F31, F32 | O | $OV_{DD}$ | — |
| $\overline{\text{DMA_DDONE}}$[2]/$\overline{\text{LCS}}$[7] | F23 | O | $OV_{DD}$ | 10 |
| $\overline{\text{DMA_DDONE}}$[3]/IRQ[11] | D30 | O | $OV_{DD}$ | 9, 10 |
| **Programmable Interrupt Controller Signals[5]** | | | | |
| $\overline{\text{MCP_0}}$ | F17 | I | $OV_{DD}$ | — |
| $\overline{\text{MCP_1}}$ | H17 | I | $OV_{DD}$ | 12, *S4* |
| IRQ[0:8] | G28, G29, H27, J23, M23, J27, F28, J24, L23 | I | $OV_{DD}$ | — |
| IRQ[9]/$\overline{\text{DMA_DREQ}}$[3] | B30 | I | $OV_{DD}$ | 10 |
| IRQ[10]/$\overline{\text{DMA_DACK}}$[3] | C30 | I | $OV_{DD}$ | 9, 10 |
| IRQ[11]/$\overline{\text{DMA_DDONE}}$[3] | D30 | I | $OV_{DD}$ | 9, 10 |
| $\overline{\text{IRQ_OUT}}$ | J26 | O | $OV_{DD}$ | 7, 11 |

**Table 63. MPC8640 Signal Reference by Functional Block (continued)**

| Name[1] | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **DUART Signals[5]** | | | | |
| UART_SIN[0:1] | B32, C32 | I | $OV_{DD}$ | — |
| UART_SOUT[0:1] | D31, A32 | O | $OV_{DD}$ | — |
| $\overline{\text{UART_CTS}}$[0:1] | A31, B31 | I | $OV_{DD}$ | — |
| $\overline{\text{UART_RTS}}$[0:1] | C31, E30 | O | $OV_{DD}$ | — |
| **$I^2C$ Signals** | | | | |
| IIC1_SDA | A16 | I/O | $OV_{DD}$ | 7, 11 |
| IIC1_SCL | B17 | I/O | $OV_{DD}$ | 7, 11 |
| IIC2_SDA | A21 | I/O | $OV_{DD}$ | 7, 11 |
| IIC2_SCL | B21 | I/O | $OV_{DD}$ | 7, 11 |
| **System Control Signals[5]** | | | | |
| $\overline{\text{HRESET}}$ | B18 | I | $OV_{DD}$ | — |
| $\overline{\text{HRESET_REQ}}$ | K18 | O | $OV_{DD}$ | — |
| $\overline{\text{SMI_0}}$ | L15 | I | $OV_{DD}$ | — |
| $\overline{\text{SMI_1}}$ | L16 | I | $OV_{DD}$ | 12, *S4* |
| $\overline{\text{SRESET_0}}$ | C20 | I | $OV_{DD}$ | — |
| $\overline{\text{SRESET_1}}$ | C21 | I | $OV_{DD}$ | 12, *S4* |
| $\overline{\text{CKSTP_IN}}$ | L18 | I | $OV_{DD}$ | — |
| $\overline{\text{CKSTP_OUT}}$ | L17 | O | $OV_{DD}$ | 7, 11 |
| READY/TRIG_OUT | J13 | O | $OV_{DD}$ | 10, 25 |
| **Debug Signals[5]** | | | | |
| TRIG_IN | J14 | I | $OV_{DD}$ | — |
| TRIG_OUT/READY | J13 | O | $OV_{DD}$ | 10, 25 |
| D1_MSRCID[0:1]/LB_SRCID[0:1] | F15, K15 | O | $OV_{DD}$ | 6, 10 |
| D1_MSRCID[2]/LB_SRCID[2] | K14 | O | $OV_{DD}$ | 10, 25 |
| D1_MSRCID[3:4]/LB_SRCID[3:4] | H15, G15 | O | $OV_{DD}$ | 10 |
| D2_MSRCID[0:4] | E16, C17, F16, H16, K16 | O | $OV_{DD}$ | — |
| D1_MDVAL/LB_DVAL | J16 | O | $OV_{DD}$ | 10 |
| D2_MDVAL | D19 | O | $OV_{DD}$ | — |
| **Power Management Signals[5]** | | | | |
| ASLEEP | C19 | O | $OV_{DD}$ | — |
| **System Clocking Signals[5]** | | | | |
| SYSCLK | G16 | I | $OV_{DD}$ | — |

**Table 63. MPC8640 Signal Reference by Functional Block (continued)**

| Name[1] | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| RTC | K17 | I | $OV_{DD}$ | 32 |
| CLK_OUT | B16 | O | $OV_{DD}$ | 23 |
| **Test Signals[5]** | | | | |
| $\overline{\text{LSSD_MODE}}$ | C18 | I | $OV_{DD}$ | 26 |
| TEST_MODE[0:3] | C16, E17, D18, D16 | I | $OV_{DD}$ | 26 |
| **JTAG Signals[5]** | | | | |
| TCK | H18 | I | $OV_{DD}$ | — |
| TDI | J18 | I | $OV_{DD}$ | 24 |
| TDO | G18 | O | $OV_{DD}$ | 23 |
| TMS | F18 | I | $OV_{DD}$ | 24 |
| $\overline{\text{TRST}}$ | A17 | I | $OV_{DD}$ | 24 |
| **Miscellaneous[5]** | | | | |
| Spare | J17 | — | — | 13 |
| GPOUT[0:7]/ TSEC1_TXD[0:7] | AF25, AC23, AG24, AG23, AE24, AE23, AE22, AD22 | O | $OV_{DD}$ | 6, 10 |
| GPIN[0:7]/ TSEC1_RXD[0:7] | AL25, AL24, AK26, AK25, AM26, AF26, AH24, AG25 | I | $OV_{DD}$ | 10 |
| GPOUT[8:15]/ TSEC2_TXD[0:7] | AB20, AJ23, AJ22, AD19, AH23, AH21, AG22, AG21 | O | $OV_{DD}$ | 10 |
| GPIN[8:15]/ TSEC2_RXD[0:7] | AL22, AK22, AM21, AH20, AG20, AF20, AF23, AF22 | I | $OV_{DD}$ | 10 |
| **Additional Analog Signals** | | | | |
| TEMP_ANODE | AA11 | Thermal | — | — |
| TEMP_CATHODE | Y11 | Thermal | — | — |
| **Sense, Power and GND Signals** | | | | |
| $SENSEV_{DD}$_Core0 | M14 | $V_{DD}$_Core0 sensing pin | — | 31 |
| $SENSEV_{DD}$_Core1 | U20 | $V_{DD}$_Core1 sensing pin | — | 12,31, *S1* |
| $SENSEV_{SS}$_Core0 | P14 | Core0 GND sensing pin | — | 31 |
| $SENSEV_{SS}$_Core1 | V20 | Core1 GND sensing pin | — | 12, 31, *S3* |
| $SENSEV_{DD}$_PLAT | N18 | $V_{DD}$_PLAT sensing pin | — | 28 |
| $SENSEV_{SS}$_PLAT | P18 | Platform GND sensing pin | — | 29 |

**Table 63. MPC8640 Signal Reference by Functional Block (continued)**

| Name[1] | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| $D1_GV_{DD}$ | B11, B14, D10, D13, F9, F12, H8, H11, H14, K10, K13, L8, P8, R6, U8, V6, W10, Y8, AA6, AB10, AC8, AD12, AE10, AF8, AG12, AH10, AJ8, AJ14, AK12, AL10, AL16 | SDRAM 1 I/O supply | $D1_GV_{DD}$<br>• 2.5 DDR<br>• 1.8 DDR2 | — |
| $D2_GV_{DD}$ | B2, B5, B8, D4, D7, E2, F6, G4, H2, J6, K4, L2, M6, N4, P2, T4, U2, W4, Y2, AB4, AC2, AD6, AE4, AF2, AG6, AH4, AJ2, AK6, AL4, AM2 | SDRAM 2 I/O supply | $D2_GV_{DD}$<br>• 2.5 V DDR<br>• 1.8 V DDR2 | — |
| $OV_{DD}$ | B22, B25, B28, D17, D24, D27, F19, F22, F26, F29, G17, H21, H24, K19, K23, M21, AM30 | DUART, Local Bus, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, JTAG, Power management, $I^2C$, JTAG and Miscellaneous I/O voltage | $OV_{DD}$<br>3.3 V | — |
| $LV_{DD}$ | AC20, AD23, AH22 | TSEC1 and TSEC2 I/O voltage | $LV_{DD}$<br>2.5/3.3 V | — |
| $TV_{DD}$ | AC17, AG18, AK20 | TSEC3 and TSEC4 I/O voltage | $TV_{DD}$<br>2.5/3.3 V | — |
| $SV_{DD}$ | H31, J29, K28, K32, L30, M28, M31, N29, R30, T31, U29, V32, W30, Y31, AA29, AB32, AC30, AD31, AE29, AG30, AH31, AJ29, AK32, AL30, AM31 | Transceiver Power Supply SerDes | $SV_{DD}$<br>1.05/1.1 V | — |
| $XV_{DD}_SRDS1$ | K26, L24, M27, N25, P26, R24, R28, T27, U25, V26 | Serial I/O Power Supply for SerDes Port 1 | $XV_{DD}_SRDS1$<br>1.05/1.1 V | |
| $XV_{DD}_SRDS2$ | AA25, AB28, AC26, AD27, AE25, AF28, AH27, AK28, AM27, W24, Y27 | Serial I/O Power Supply for SerDes Port 2 | $XV_{DD}_SRDS2$<br>1.05/1.1 V | — |
| $V_{DD}_Core0$ | L12, L13, L14, M13, M15, N12, N14, P11, P13, P15, R12, R14, T11, T13, T15, U12, U14, V11, V13, V15, W12, W14, Y12, Y13, Y15, AA12, AA14, AB13 | Core 0 voltage supply | $V_{DD}_Core0$<br>0.95/1.05/1.1 V | — |
| $V_{DD}_Core1$ | R16, R18, R20, T17, T19, T21, T23, U16, U18, U22, V17, V19, V21, V23, W16, W18, W20, W22, Y17, Y19, Y21, Y23, AA16, AA18, AA20, AA22, AB23, AC24 | Core 1 voltage supply | $V_{DD}_Core1$<br>0.95/1.05/1.1 V | 12, *S1* |
| $V_{DD}_PLAT$ | M16, M17, M18, N16, N20, N22, P17, P19, P21, P23, R22 | Platform supply voltage | $V_{DD}_PLAT$<br>1.05/1.1 V | — |

**Table 63. MPC8640 Signal Reference by Functional Block (continued)**

| Name[1] | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| $AV_{DD}$_Core0 | B20 | Core 0 PLL Supply | $AV_{DD}$_Core0 0.95/1.05/ 1.1 V | — |
| $AV_{DD}$_Core1 | A19 | Core 1 PLL Supply | $AV_{DD}$_Core1 0.95/1.05/ 1.1 V | 12, *S2* |
| $AV_{DD}$_PLAT | B19 | Platform PLL supply voltage | $AV_{DD}$_PLAT 1.05/1.1 V | — |
| $AV_{DD}$_LB | A20 | Local Bus PLL supply voltage | $AV_{DD}$_LB 1.05/1.1 V | — |
| $AV_{DD}$_SRDS1 | P32 | SerDes Port 1 PLL & DLL Power Supply | $AV_{DD}$_SRDS1 1.05/1.1 V | — |
| $AV_{DD}$_SRDS2 | AF32 | SerDes Port 2 PLL & DLL Power Supply | $AV_{DD}$_SRDS2 1.05/1.1 V | — |
| GND | C3, C6, C9, C12, C15, C23, C26, E5, E8, E11, E14, E18, E25, E28, F3, G7, G10, G13, G20, G23, G27, G30, H5, J3, J9, J12, J15, J22, J25, K7, L5, L20, M3, M9, M12, N7, N11, N13, N15, N17, N19, N21, N23, P5, P12, P16, P20, P22, R3, R9, R11, R13, R15, R17, R19, R21, R23, T7, T12, T14, T16, T18, T20, T22, U5, U11,U13, U15, U17, U19, U21, U23, V3, V9, V12, V14, V16, V18, V22, W7, W11, W13, W15, W17, W19, W21, W23,Y5, Y14, Y16, Y18, Y20, Y22, AA3, AA9, AA13, AA15, AA17, AA19, AA21, AA23, AB7, AB24, AC5, AC11, AD3, AD9, AD15, AE7, AE13, AE18, AF5, AF11, AF21, AF24, AG3, AG9, AH7, AH13, AJ5, AJ11, AK3, AK9, AK15, AK19, AK23, AL7, AL13 | GND | — | — |
| AGND_SRDS1 | P30 | SerDes Port 1 Ground pin for $AV_{DD}$_SRDS1 | — | — |
| AGND_SRDS2 | AF30 | SerDes Port 2 Ground pin for $AV_{DD}$_SRDS2 | — | — |
| SGND | H28, H32, J30, K31, L28, L29, M32, N30, R29, T32, U30, V31, W29,Y32 AA30, AB31, AC29, AD32, AE30, AG29, AH32, AJ30, AK31, AL29, AM32 | Ground pins for $SV_{DD}$ | — | — |
| XGND | K27, L25, M26, N24, P27, R25, T26, U24, V27, W25, Y28, AA24, AB27, AC25, AD28, AE26, AF27, AH28, AJ26, AK27, AL26, AM28 | Ground pins for $XV_{DD}$_SRDS*n* | — | — |
| **Reset Configuration Signals**[20] | | | | |

**Table 63. MPC8640 Signal Reference by Functional Block (continued)**

| Name[1] | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| TSEC1_TXD[0] / cfg_alt_boot_vec | AF25 | — | $LV_{DD}$ | — |
| TSEC1_TXD[1]/ cfg_platform_freq | AC23 | — | $LV_{DD}$ | 21 |
| TSEC1_TXD[2:4]/ cfg_device_id[5:7] | AG24, AG23, AE24 | — | $LV_{DD}$ | — |
| TSEC1_TXD[5]/ cfg_tsec1_reduce | AE23 | — | $LV_{DD}$ | — |
| TSEC1_TXD[6:7]/ cfg_tsec1_prtcl[0:1] | AE22, AD22 | — | $LV_{DD}$ | — |
| TSEC2_TXD[0:3]/ cfg_rom_loc[0:3] | AB20, AJ23, AJ22, AD19 | — | $LV_{DD}$ | — |
| TSEC2_TXD[4], TSEC2_TX_ER/ cfg_dram_type[0:1] | AH23, AB19 | — | $LV_{DD}$ | 38 |
| TSEC2_TXD[5]/ cfg_tsec2_reduce | AH21 | — | $LV_{DD}$ | — |
| TSEC2_TXD[6:7]/ cfg_tsec2_prtcl[0:1] | AG22, AG21 | — | $LV_{DD}$ | — |
| TSEC3_TXD[0:1]/ cfg_spare[0:1] | AL21, AJ21 | O | $TV_{DD}$ | 33 |
| TSEC3_TXD[2]/ cfg_core1_enable | AM20 | O | $TV_{DD}$ | — |
| TSEC3_TXD[3]/ cfg_core1_lm_offset | AJ20 | — | $LV_{DD}$ | — |
| TSEC3_TXD[5]/ cfg_tsec3_reduce | AK21 | — | $LV_{DD}$ | — |
| TSEC3_TXD[6:7]/ cfg_tsec3_prtcl[0:1] | AL20, AL19 | — | $LV_{DD}$ | — |
| TSEC4_TXD[0:3]/ cfg_io_ports[0:3] | AC18, AC16, AD18, AD17 | — | $LV_{DD}$ | — |
| TSEC4_TXD[5]/ cfg_tsec4_reduce | AB18 | — | $LV_{DD}$ | — |
| TSEC4_TXD[6:7]/ cfg_tsec4_prtcl[0:1] | AB17, AB16 | — | $LV_{DD}$ | — |
| LAD[0:31]/ cfg_gpporcr[0:31] | A30, E29, C29, D28, D29, H25, B29, A29, C28, L22, M22, A28, C27, H26, G26, B27, B26, A27, E27, G25, D26, E26, G24, F27, A26, A25, C25, H23, K22, D25, F25, H22 | — | $OV_{DD}$ | — |
| $\overline{\text{LWE[0]}}$/ cfg_cpu_boot | E21 | — | $OV_{DD}$ | — |
| $\overline{\text{LWE[1]}}$/ cfg_rio_sys_size | F21 | — | $OV_{DD}$ | — |

**Table 63. MPC8640 Signal Reference by Functional Block (continued)**

| Name[1] | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| $\overline{\text{LWE[2:3]}}$/ cfg_host_agt[0:1] | D22, E20 | — | $OV_{DD}$ | — |
| LDP[0:3], LA[27] / cfg_core_pll[0:4] | A24, E24, C24, B24, J21 | — | $OV_{DD}$ | 22 |
| LA[28:31]/ cfg_sys_pll[0:3] | K21, G22, F24, G21 | — | $OV_{DD}$ | 22 |
| LGPL[3], LGPL[5]/ cfg_boot_seq[0:1] | K20, J19 | — | $OV_{DD}$ | — |

**Table 63. MPC8640 Signal Reference by Functional Block (continued)**

| Name[1] | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| D1_MSRCID[0]/ cfg_mem_debug | F15 | — | $OV_{DD}$ | — |
| D1_MSRCID[1]/ cfg_ddr_debug | K15 | — | $OV_{DD}$ | — |

**Table 63. MPC8640 Signal Reference by Functional Block (continued)**

| Name[1] | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|

**Note:**

1. Multi-pin signals such as D1_MDQ[0:63] and D2_MDQ[0:63] have their physical package pin numbers listed in order corresponding to the signal names.
2. Stub Series Terminated Logic (SSTL-18 and SSTL-25) type pins.
3. If a DDR port is not used, it is possible to leave the related power supply (Dn_GVDD, Dn_MVREF) turned off at reset. Note that these power supplies can only be powered up again at reset for functionality to occur on the DDR port.
4. Low Voltage Differential Signaling (LVDS) type pins.
5. Low Voltage Transistor-Transistor Logic (LVTTL) type pins.
6. This pin is a reset configuration pin and appears again in the Reset Configuration Signals section of this table. See the Reset Configuration Signals section of this table for config name and connection details.
7. Recommend a weak pull-up resistor (1–10 kΩ) be placed from this pin to its power supply.
8. Recommend a weak pull-down resistor (2–10 kΩ) be placed from this pin to ground.
9. This multiplexed pin has input status in one mode and output in another
10. This pin is a multiplexed signal for different functional blocks and appears more than once in this table.
11. This pin is open drain signal.
12. Functional only on the MPC8640D.
13. These pins should be left floating.
14. These pins should be connected to $SV_{DD}$.
15. These pins should be pulled to ground with a strong resistor (270-Ω to 330-Ω).
16. These pins should be connected to OVDD.
17. This is a SerDes PLL/DLL digital test signal and is only for factory use.
18. This is a SerDes PLL/DLL analog test signal and is only for factory use.
19. This pin should be pulled to ground with a 100-Ω resistor.
20. The pins in this section are reset configuration pins. Each pin has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
21. Should be pulled down at reset if platform frequency is at 400 MHz.
22. These pins require 4.7-kΩ pull-up or pull-down resistors and must be driven as they are used to determine PLL configuration ratios at reset.
23. This output is actively driven during reset rather than being released to high impedance during reset.
24 These JTAG pins have weak internal pull-up P-FETs that are always enabled.
25. This pin should NOT be pulled down (or driven low) during reset.
26. These are test signals for factory use only and must be pulled up (100-Ω to 1- kΩ.) to OVDD for normal machine operation.
27. Dn_MDIC[0] should be connected to ground with an 18-Ω resistor ± 1-Ω and Dn_MDIC[1] should be cLonnected Dn_GVDD with an 18-Ω resistor ± 1-Ω. These pins are used for automatic calibration of the DDR IOs.
28. Pin N18 is recommended as a reference point for determining the voltage of $V_{DD}$_PLAT and is hence considered as the $V_{DD}$_PLAT sensing voltage and is called SENSEVDD_PLAT.
29. Pin P18 is recommended as the ground reference point for SENSEVDD_PLAT and is called SENSEVSS_PLAT.
30. This pin should be pulled to ground with a 200-Ω resistor.
31. These pins are connected to the power/ground planes internally and may be used by the core power supply to improve tracking and regulation.
32. Must be tied low if unused
33. These pins may be used as defined functional reset configuration pins in the future. Please include a resistor pull-up/down option to allow flexibility of future designs.
34. Used as serial data output for serial RapidIO 1×/4× link.
35. Used as serial data input for serial RapidIO 1×/4× link.
36. This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid transmit enable before it is actively driven.

**Table 63. MPC8640 Signal Reference by Functional Block (continued)**

| Name[1] | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|

37.This pin is only an output in FIFO mode when used as Rx Flow Control.

38.This pin functions as cfg_dram_type[0 or 1] at reset. **Note:** This pin must be valid before HRESET assertion in device sleep mode.

39. Should be pulled to ground if unused (such as in FIFO, MII and RMII modes).

40. See Section 18.4.2, "Platform to FIFO Restrictions" for clock speed limitations for this pin when used in FIFO mode.

41. The phase between the output clocks TSEC1_GTX_CLK and TSEC2_GTX_CLK (ports 1 and 2) is no more than 100 ps. The phase between the output clocks TSEC3_GTX_CLK and TSEC4_GTX_CLK (ports 3 and 4) is no more than 100 ps.

42. For systems which boot from Local Bus (GPCM)-controlled flash, a pullup on LGPL4 is required.

**Special Notes for Single Core Device:**

*S1*. Solder ball for this signal will not be populated in the single core package.

*S2*. The PLL filter from $V_{DD}$_Core1 to $AV_{DD}$_Core1 should be removed. $AV_{DD}$_Core1 should be pulled to ground with a weak (2–10 kΩ) resistor. See Section 20.2.1, "PLL Power Supply Filtering" for more details.

*S3*. This pin should be pulled to GND for the single core device.

*S4*. No special requirement for this pin on single core device. Pin should be tied to power supply as directed for dual core.

# 18 Clocking

This section describes the PLL configuration of the MPC8640. Note that the platform clock is identical to the MPX clock.

## 18.1 Clock Ranges

Table 64 provides the clocking specifications for the processor cores, and Table 65 provides the clocking specifications for the memory bus. Table 66 provides the clocking for the Platform/MPX bus, and Table 67 provides the clocking for the local bus.

**Table 64. Processor Core Clocking Specifications**

| Parameter | Maximum Processor Core Frequency | | | | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| | 1000 MHz | | 1067 MHz | | 1250MHz | | | |
| | Min | Max | Min | Max | Min | Max | | |
| e600 core processor frequency | 800 | 1000 | 800 | 1067 | 800 | 1250 | MHz | 1, 2 |

**Notes**:

1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 18.2, "MPX to SYSCLK PLL Ratio," and Section 18.3, "e600 to MPX clock PLL Ratio," for ratio settings.
2. The minimum e600 core frequency is based on the minimum platform clock frequency of 400 MHz.

**Table 65. Memory Bus Clocking Specifications**

| Parameter | Maximum Processor Core Frequency | | Unit | Notes |
|---|---|---|---|---|
| | 1000, 1067, 1250 MHz | | | |
| | Min | Max | | |
| Memory bus clock frequency | 200 | 266 | MHz | 1, 2 |

**Notes:**
1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 18.2, "MPX to SYSCLK PLL Ratio," and Section 18.3, "e600 to MPX clock PLL Ratio," for ratio settings.
2. The memory bus clock speed is half the DDR/DDR2 data rate, hence, half the MPX clock frequency.

**Table 66. Platform/MPX bus Clocking Specifications**

| Parameter | Maximum Processor Core Frequency | | Unit | Notes |
|---|---|---|---|---|
| | 1000, 1067, 1250 MHz | | | |
| | Min | Max | | |
| Platform/MPX bus clock frequency | 400 | 533 | MHz | 1, 2 |

**Notes:**
1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 18.2, "MPX to SYSCLK PLL Ratio," and Section 18.3, "e600 to MPX clock PLL Ratio," for ratio settings.
2. Platform/MPX frequencies between 400 and 500 MHz are not supported.

**Table 67. Local Bus Clocking Specifications**

| Parameter | Maximum Processor Core Frequency | | Unit | Notes |
|---|---|---|---|---|
| | 1000, 1067, 1250 MHz | | | |
| | Min | Max | | |
| Local bus clock speed (for Local Bus Controller) | 25 | 133 | MHz | 1 |

**Notes:**
1. The Local bus clock speed on LCLK[0:2] is determined by MPX clock divided by the Local Bus PLL ratio programmed in LCRR[CLKDIV]. See the reference manual for the MPC8641D for more information on this.

## 18.2 MPX to SYSCLK PLL Ratio

The MPX clock is the clock that drives the MPX bus, and is also called the platform clock. The frequency of the MPX is set using the following reset signals, as shown in Table 68:

- SYSCLK input signal
- Binary value on LA[28:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that the DDR data rate is the determining factor in selecting the MPX bus frequency because the MPX frequency must equal the DDR data rate.

**Table 68. MPX:SYSCLK Ratio**

| Binary Value of LA[28:31] Signals | MPX:SYSCLK Ratio |
|---|---|
| 0000 | Reserved |
| 0001 | Reserved |
| 0010 | 2:1 |
| 0011 | 3:1 |
| 0100 | 4:1 |
| 0101 | 5:1 |
| 0110 | 6:1 |
| 0111 | Reserved |
| 1000 | 8:1 |
| 1001 | Reserved |

## 18.3 e600 to MPX clock PLL Ratio

Table 69 describes the clock ratio between the platform and the e600 core clock. This ratio is determined by the binary value of LDP[0:3], LA[27](cfg_core_pll[0:4] - reset config name) at power up, as shown in Table 69.

**Table 69. e600 Core to MPX Clock Ratio**

| Binary Value of LDP[0:3], LA[27] Signals | e600 core: MPX Clock Ratio |
|---|---|
| 01000 | 2:1 |
| 01100 | 2.5:1 |
| 10000 | 3:1 |
| 11100 | Reserved |
| 10100 | Reserved |
| 01110 | Reserved |

## 18.4 Frequency Options

This section discusses the frequency options for the MPC8640.

### 18.4.1 SYSCLK to Platform Frequency Options

Table 70 shows some SYSCLK frequencies and the expected MPX frequency values based on the MPX clock to SYSCLK ratio. Note that frequencies between 400 MHz and 500 MHz are not supported on the platform. See note regarding *cfg_platform_freq* in Section 17, “Signal Listings,” because it is a reset

configuration pin that is related to platform frequency.

**Table 70. Frequency Options of SYSCLK with Respect to Platform/MPX Clock Speed**

| MPX to SYSCLK Ratio | SYSCLK (MHz) | | | | |
|---|---|---|---|---|---|
| | 66 | 83 | 100 | 133 | 167 |
| | Platform/MPX Frequency (MHz)[1] | | | | |
| 2 | | | | | |
| 3 | | | | 400 | 500 |
| 4 | | | 400 | 533 | |
| 5 | | | 500 | | |
| 6 | 400 | 500 | | | |
| 8 | 533 | | | | |

1 SYSCLK frequency range is 66-167 MHz. Platform clock/MPX frequency range is 400 MHz, 500-533 MHz.

### 18.4.2 Platform to FIFO Restrictions

Please note the following FIFO maximum speed restrictions based on platform speed:

For FIFO GMII mode:

FIFO TX/RX clock frequency ≤ platform clock frequency ÷ 4.2

For example, if the platform frequency is 500 MHz, the FIFO Tx/Rx clock frequency should be no more than 119 MHz.

For FIFO encoded mode:

FIFO TX/RX clock frequency ≤ platform clock frequency ÷ 3.2

For example, if the platform frequency is 500 MHz, the FIFO Tx/Rx clock frequency should be no more than 156 MHz.

# 19 Thermal

This section describes the thermal specifications of the MPC8640.

## 19.1 Thermal Characteristics

Table 71 provides the package thermal characteristics for the MPC8640.

**Table 71. Package Thermal Characteristics[1]**

| Characteristic | Symbol | Value | Unit | Notes |
|---|---|---|---|---|
| Junction-to-ambient thermal resistance, natural convection, single-layer (1s) board | $R_{\theta JA}$ | 18 | °C/W | 1, 2 |
| Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board | $R_{\theta JA}$ | 13 | °C/W | 1, 3 |
| Junction-to-ambient thermal resistance, 200 ft/min airflow, single-layer (1s) board | $R_{\theta JMA}$ | 13 | °C/W | 1, 3 |
| Junction-to-ambient thermal resistance, 200 ft/min airflow, four-layer (2s2p) board | $R_{\theta JMA}$ | 9 | °C/W | 1, 3 |
| Junction-to-board thermal resistance | $R_{\theta JB}$ | 5 | °C/W | 4 |
| Junction-to-case thermal resistance | $R_{\theta JC}$ | < 0.1 | °C/W | 5 |

**Notes**:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. This is the thermal resistance between die and case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. Actual thermal resistance is less than 0.1 °C/W.

## 19.2 Thermal Management Information

This section provides thermal management information for the high coefficient of thermal expansion (HCTE) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The MPC8640 implements several features designed to assist with thermal management, including the temperature diode. The temperature diode allows an external device to monitor the die temperature in order to detect excessive temperature conditions and alert the system; see Section 19.2.4, “Temperature Diode,” for more information.

To reduce the die-junction temperature, heat sinks are required. Due to the potential large mass of the heat sink, attachment through the printed-circuit board is suggested. In any implementation of a heat sink solution, the force on the die should not exceed ten pounds force (45 newtons). Figure 59 shows a spring

clip through the board. Occasionally the spring clip is attached to soldered hooks or to a plastic backing structure. Screw and spring arrangements are also frequently used.

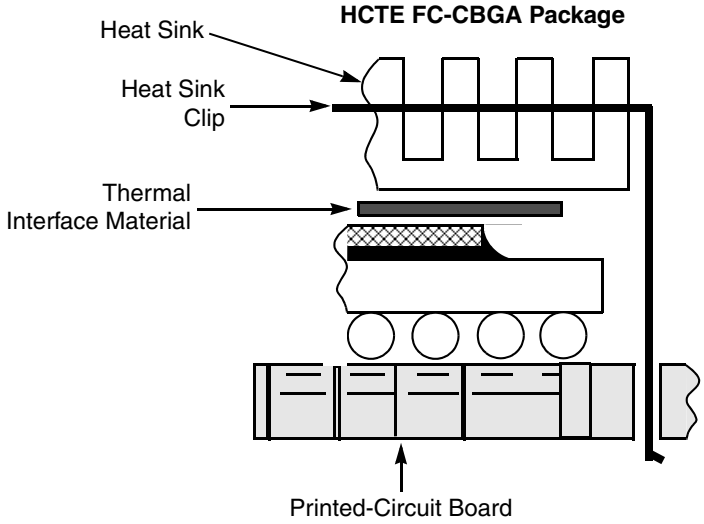



**Figure 59. FC-CBGA Package Exploded Cross-Sectional View with Several Heat Sink Options**

There are several commercially-available heat sinks for the MPC8640 provided by the following vendors:

| | |
|---|---|
| Aavid Thermalloy<br>80 Commercial St.<br>Concord, NH 03301<br>Internet: www.aavidthermalloy.com | 603-224-9988 |
| Advanced Thermal Solutions<br>89 Access Road #27.<br>Norwood, MA02062<br>Internet: www.qats.com | 781-769-2800 |
| Alpha Novatech<br>473 Sapena Ct. #12<br>Santa Clara, CA 95054<br>Internet: www.alphanovatech.com | 408-749-7601 |
| Calgreg Thermal Solutions<br>60 Alhambra Road, Suite 1<br>Warwick, RI 02886<br>Internet: www.calgreg.com | 888-732-6100 |
| International Electronic Research Corporation (IERC)<br>413 North Moss St.<br>Burbank, CA 91502<br>Internet: www.ctscorp.com | 818-842-7277 |

| | |
|---|---|
| Millennium Electronics (MEI)<br>Loroco Sites<br>671 East Brokaw Road<br>San Jose, CA 95112<br>Internet: www.mei-thermal.com | 408-436-8770 |
| Tyco Electronics<br>Chip Coolers™<br>P.O. Box 3668<br>Harrisburg, PA 17105-3668<br>Internet: www.chipcoolers.com | 800-522-6752 |
| Wakefield Engineering<br>33 Bridge St.<br>Pelham, NH 03076<br>Internet: www.wakefield.com | 603-635-5102 |

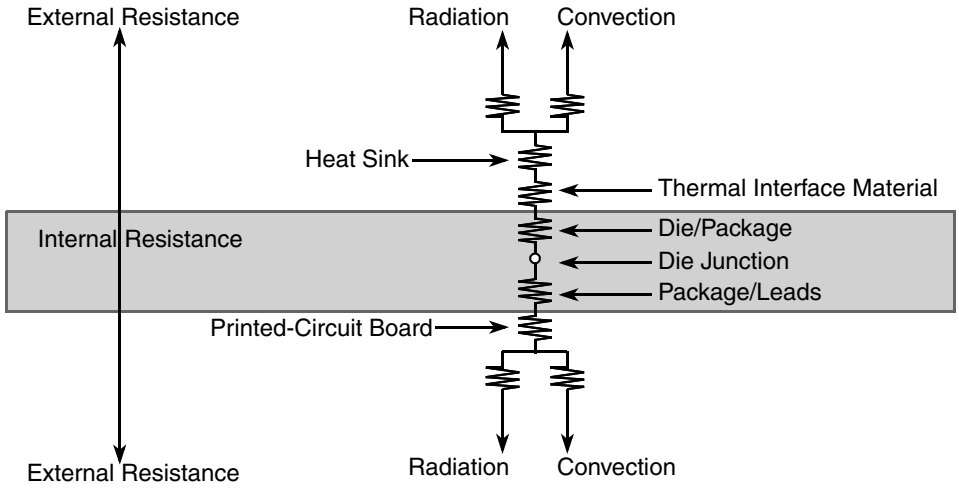
Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

### 19.2.1 Internal Package Conduction Resistance

For the exposed-die packaging technology described in Table 71, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance (the case is actually the top of the exposed silicon die)
- The die junction-to-board thermal resistance

Figure 60 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.




(Note the internal versus external package resistance.)

**Figure 60. C4 Package with Heat Sink Mounted to a Printed-Circuit Board**

Heat generated on the active side of the chip is conducted through the silicon, then the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Because the silicon thermal resistance is quite small, the temperature drop in the silicon may be neglected for a first-order analysis. Thus the thermal interface material and the heat sink conduction/convective thermal resistances are the dominant terms.

### 19.2.2 Thermal Interface Materials

A thermal interface material is recommended at the package-to-heat sink interface to minimize the thermal contact resistance. Figure 61 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 59). Therefore, synthetic grease offers the best thermal performance, considering the low interface pressure, and is recommended due to the high power dissipation of the MPC8640. Of course, the selection of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, and so on.

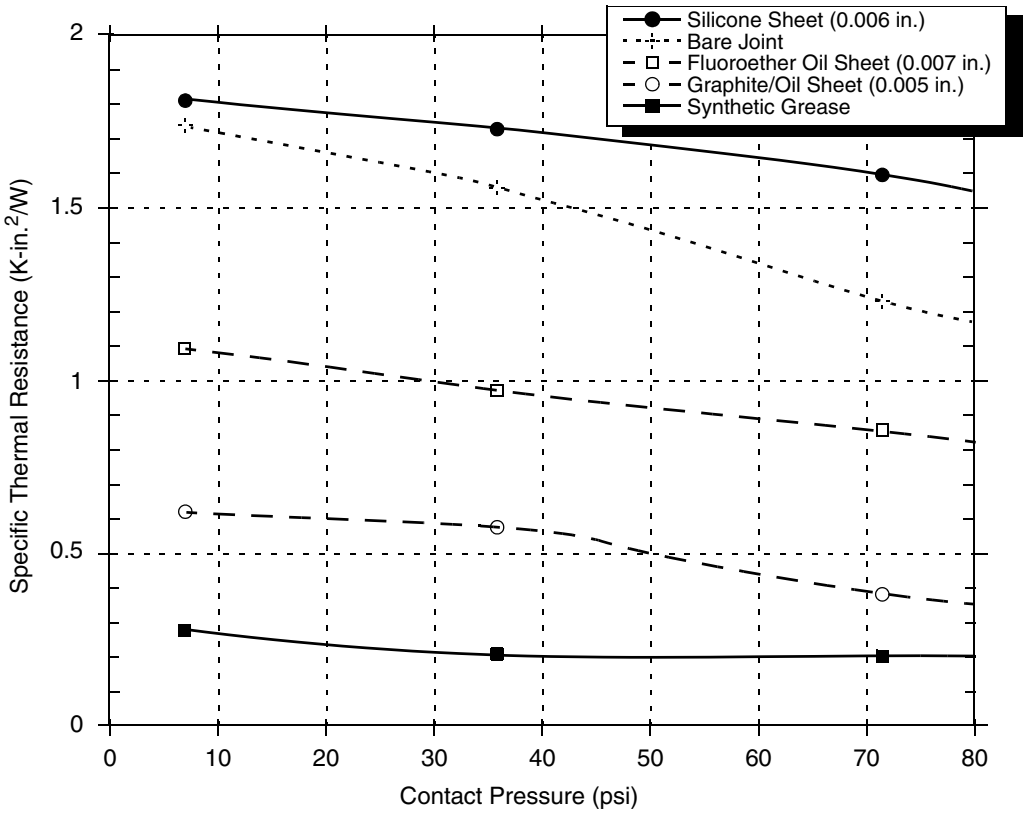



**Figure 61. Thermal Performance of Select Thermal Interface Material**

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based on high conductivity and mechanical strength to meet equipment shock/vibration requirements. There are several commercially available thermal interfaces and adhesive materials provided by the following vendors:

| | |
|---|---|
| The Bergquist Company<br>18930 West 78th St.<br>Chanhassen, MN 55317<br>Internet: www.bergquistcompany.com | 800-347-4572 |
| Chomerics, Inc.<br>77 Dragon Ct.<br>Woburn, MA 01801<br>Internet: www.chomerics.com | 781-935-4850 |
| Dow-Corning Corporation<br>Corporate Center<br>PO Box 994<br>Midland, MI 48686-0994<br>Internet: www.dowcorning.com | 800-248-2481 |
| Shin-Etsu MicroSi, Inc.<br>10028 S. 51st St.<br>Phoenix, AZ 85044<br>Internet: www.microsi.com | 888-642-7674 |
| Thermagon Inc.<br>4707 Detroit Ave.<br>Cleveland, OH 44102<br>Internet: www.thermagon.com | 888-246-9050 |

The following section provides a heat sink selection example using one of the commercially available heat sinks.

### 19.2.3 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_i + T_r + (R_{\theta JC} + R_{\theta int} + R_{\theta sa}) \times P_d$$

where:

$T_j$ is the die-junction temperature

$T_i$ is the inlet cabinet ambient temperature

$T_r$ is the air temperature rise within the computer cabinet

$R_{\theta JC}$ is the junction-to-case thermal resistance

$R_{\theta int}$ is the adhesive or interface material thermal resistance

$R_{\theta sa}$ is the heat sink base-to-ambient thermal resistance

$P_d$ is the power dissipated by the device

During operation, the die-junction temperatures ($T_j$) should be maintained less than the value specified in Table 2. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature ($T_i$) may range from 30 to 40 °C. The air temperature rise within a cabinet ($T_r$) may be in the range of 5 to 10 °C. The thermal resistance of the thermal interface material ($R_{\theta int}$) is typically about 0.2 °C/W. For example, assuming a $T_i$ of 30 °C, a $T_r$ of 5 °C, a package $R_{\theta JC}$ = 0.1, and a typical power consumption ($P_d$) of 43.4 W, the following expression for $T_j$ is obtained:

Die-junction temperature: $T_j = 30\ °C + 5\ °C + (0.1\ °C/W + 0.2\ °C/W + \theta_{sa}) \times 43.4\ W$

For this example, a $R_{\theta sa}$value of 1.32 °C/W or less is required to maintain the die junction temperature below the maximum value of Table 2.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, and so on.

Due to the complexity and variety of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board as well as system-level designs.

For system thermal modeling, the MPC8640 thermal model is shown in Figure 62. Four cuboids are used to represent this device. The die is modeled as 12.4 × 15.3 mm at a thickness of 0.86 mm. See Section 3, “Power Characteristics,” for power dissipation details. The substrate is modeled as a single block 33×33×1.2 mm with orthotropic conductivity: 13.5 W/(m • K) in the xy-plane and 5.3 W/(m • K) in the z-direction. The die is centered on the substrate. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate with a conductivity of 5.3 W/(m • K) in the thickness dimension of 0.07 mm. Because the bump/underfill is modeled with zero physical dimension (collapsed height), the die thickness was slightly enlarged to provide the correct height. The C5 solder layer is modeled as a cuboid with dimensions 33x33x0.4 mm and orthotropic thermal conductivity of 0.034 W/(m • K) in the xy-plane and 9.6 W/(m • K) in the z-direction. An LGA solder layer would be modeled as a collapsed thermal resistance with thermal conductivity of 9.6W/(m • K) and an effective height of 0.1 mm.

The thermal model uses approximate dimensions to reduce grid. Please refer to the case outline for actual dimensions.

| Conductivity | Value | Unit |
|---|---|---|
| **Die (12.4 × 15.3 × 0.86 mm)** | | |
| Silicon | Temperature dependent | |
| **Bump and Underfill (12.4 × 15.3 × 0.07 mm) Collapsed Resistance** | | |
| $k_z$ | 5.3 | W/(m • K) |
| **Substrate (33 × 33 × 1.2 mm)** | | |
| $k_x$ | 13.5 | W/(m • K) |
| $k_y$ | 13.5 | |
| $k_z$ | 5.3 | |
| **C5 Solder layer (33 × 33 × 0.4 mm)** | | |
| $k_x$ | 0.034 | W/(m • K) |
| $k_y$ | 0.034 | |
| $k_z$ | 9.6 | |

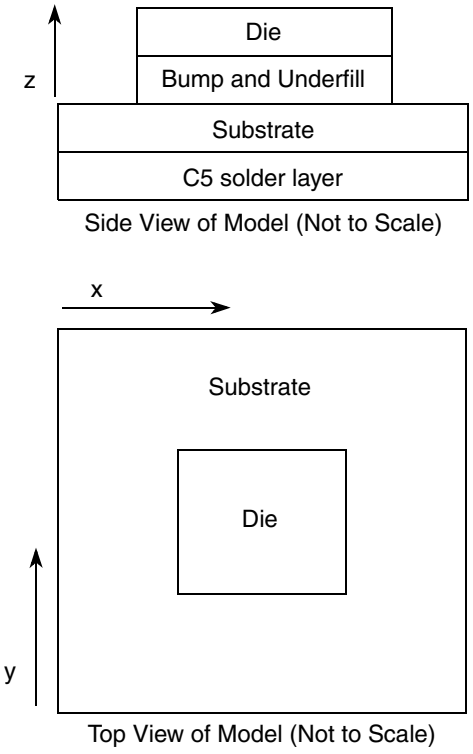



**Figure 62. Recommended Thermal Model of MPC8640**

## 19.2.4 Temperature Diode

The MPC8640 has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. It is recommended that each device be individually calibrated.

The following are the specifications of the MPC8640 on-board temperature diode:

$V_f > 0.40$ V

$V_f < 0.90$ V

An approximate value of the ideality may be obtained by calibrating the device near the expected operating temperature.

Ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fw} = I_s \left[ e^{\frac{qV_f}{nKT}} - 1 \right]$$

Another useful equation is:

$$V_H - V_L = n\frac{KT}{q}\left[ ln\frac{I_H}{I_L} \right]$$

Where:

$I_{fw}$ = Forward current
$I_s$ = Saturation current
$V_d$ = Voltage at diode
$V_f$ = Voltage forward biased
$V_H$ = Diode voltage while $I_H$ is flowing
$V_L$ = Diode voltage while $I_L$ is flowing
$I_H$ = Larger diode bias current
$I_L$ = Smaller diode bias current
q = Charge of electron ($1.6 \times 10^{-19}$ C)
n = Ideality factor (normally 1.0)
K = Boltzman's constant ($1.38 \times 10^{-23}$ Joules/K)
T = Temperature (Kelvins)

The ratio of $I_H$ to $I_L$ is usually selected to be 10:1. The above simplifies to the following:

$$V_H - V_L = 1.986 \times 10^{-4} \times nT$$

Solving for T, the equation becomes:

$$nT = \frac{V_H - V_L}{1.986 \times 10^{-4}}$$

# 20 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8640.

## 20.1 System Clocking

This device includes six PLLs, as follows:

- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 18.2, "MPX to SYSCLK PLL Ratio."
- The dual e600 Core PLLs generate the e600 clock from the externally supplied input.
- The local bus PLL generates the clock for the local bus.
- There are two internal PLLs for the SerDes block.

## 20.2 Power Supply Design and Sequencing

This section describes the power supply design and sequencing.

### 20.2.1 PLL Power Supply Filtering

Each of the PLLs listed in Section 20.1, "System Clocking," is provided with power through independent power supply pins.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 64, one to each of the $AV_{DD}$ type pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific $AV_{DD}$ type pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the $AV_{DD}$ type pin, which is on the periphery of the footprint, without the inductance of vias.

Figure 63 and Figure 64 show the PLL power supply filter circuits for the platform and cores, respectively.

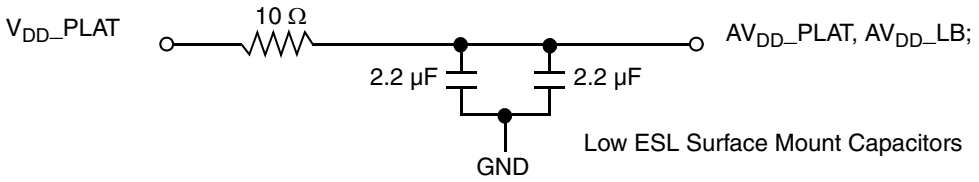
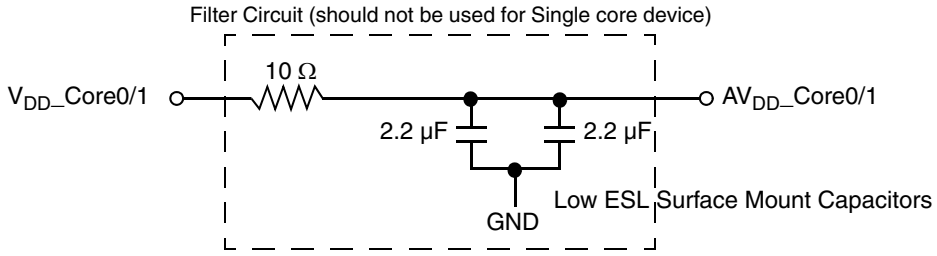


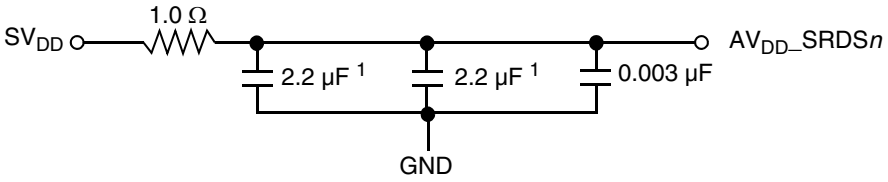

**Figure 63. MPC8640 PLL Power Supply Filter Circuit (for platform and Local Bus)**




**Note:** For single core device the filter circuit (in the dashed box) should be removed and $AV_{DD}$_Core1 should be tied to ground with a weak (2–10 kΩ) pull-down resistor.

**Figure 64. MPC8640 PLL Power Supply Filter Circuit (for cores)**

The $AV_{DD}$_SRDS*n* signals provide power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the $AV_{DD}$_SRDS*n* balls to ensure it filters out as much noise as possible. The ground connection should be near the $AV_{DD}$_SRDS*n* balls. The 0.003-µF capacitor is closest to the balls, followed by the two 2.2-µF capacitors, and finally the 1-Ω resistor to the board supply plane. The capacitors are connected from $AV_{DD}$_SRDS*n* to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.




1. An 0805 sized capacitor is recommended for system initial bring-up.

**Figure 65. SerDes PLL Power Supply Filter**

Note the following:

- $AV_{DD}$_SRDS*n* should be a filtered version of $SV_{DD}$.
- Signals on the SerDes interface are fed from the $SV_{DD}$ power plan.

### 20.2.2 PLL Power Supply Sequencing

For details on power sequencing for the $AV_{DD}$ type and supplies refer to Section 2.2, "Power-Up/Down Sequence."

## 20.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8640 system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system

designer place at least one decoupling capacitor at each $OV_{DD}$, D*n*_$GV_{DD}$, $LV_{DD}$, $TV_{DD}$, $V_{DD}$_Core*n*, and $V_{DD}$_PLAT pin of the device. These decoupling capacitors should receive their power from separate $OV_{DD}$, D*n*_$GV_{DD}$, $LV_{DD}$, $TV_{DD}$, $V_{DD}$_Core*n*, and $V_{DD}$_PLAT and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 μF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the $OV_{DD}$, D*n*_$GV_{DD}$, $LV_{DD}$, $TV_{DD}$, $V_{DD}$_Core*n*, and $V_{DD}$_PLAT planes, to enable quick recharging of the smaller chip capacitors. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 μF (AVX TPS tantalum or Sanyo OSCON).

## 20.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power ($SV_{DD}$ and $XV_{DD}$_SRDS*n*) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 × 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a 1-μF ceramic chip capacitor on each side of the device. This should be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there should be a 10-μF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100-μF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

## 20.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. In general all unused active low inputs should be tied to $OV_{DD}$, D*n*_$GV_{DD}$, $LV_{DD}$, $TV_{DD}$, $V_{DD}$_Core*n*, and $V_{DD}$_PLAT, $XV_{DD}$_SRDS*n*, and $SV_{DD}$ as required and unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

The following list explains the special cases:

- DDR—If one of the DDR ports is not being used the power supply pins for that port can be connected to ground so that there is no need to connect the individual unused inputs of that port to ground. Note that these power supplies can only be powered up again at reset for functionality to occur on the DDR port. Power supplies for other functional buses should remain powered.

- Local Bus—If parity is not used, tie LDP[0:3] to ground via a 4.7-kΩ resistor, tie LPBSE to $OV_{DD}$ via a 4.7-kΩ resistor (pull-up resistor). For systems which boot from Local Bus (GPCM)-controlled flash, a pull-up on LGPL4 is required.
- SerDes—Receiver lanes configured for PCI Express are allowed to be disconnected (as would occur when a PCI Express slot is connected but not populated). Directions for terminating the SerDes signals is discussed in Section 20.5.1, "Guidelines for High-Speed Interface Termination."

## 20.5.1 Guidelines for High-Speed Interface Termination

This section provides the guidelines for high-speed interface termination.

### 20.5.1.1 SerDes Interface

The high-speed SerDes interface can be disabled through the POR input cfg_io_ports[0:3] and through the DEVDISR register in software. If a SerDes port is disabled through the POR input the user cannot enable it through the DEVDISR register in software. However, if a SerDes port is enabled through the POR input the user can disable it through the DEVDISR register in software. Disabling a SerDes port through software should be done on a temporary basis. Power is always required for the SerDes interface, even if the port is disabled through either mechanism. Table 72 describes the possible enabled/disabled scenarios for a SerDes port. The termination recommendations must be followed for each port.

**Table 72. SerDes Port Enabled/Disabled Configurations**

| | Disabled Through POR Input | Enabled Through POR Input |
|---|---|---|
| **Enabled through DEVDISR** | SerDes port is disabled (and cannot be enabled through DEVDISR)<br><br>Complete termination required (Reference Clock not required) | SerDes port is enabled<br><br>Partial termination may be required[1] (Reference Clock is required) |
| **Disabled through DEVDISR** | SerDes port is disabled (through POR input)<br><br>Complete termination required (Reference Clock not required) | SerDes port is disabled after software disables port<br><br>Same termination requirements as when the port is enabled through POR input[2] (Reference Clock is required) |

**Note:**

1 Partial Termination when a SerDes port is enabled through both POR input and DEVDISR is determined by the SerDes port mode. If the port is in ×8 PCI Express mode, no termination is required because all pins are being used. If the port is in ×1/×2/×4 PCI Express mode, termination is required on the unused pins. If the port is in ×4 serial RapidIO mode, termination is required on the unused pins.

2 If a SerDes port is enabled through the POR input and then disabled through DEVDISR, no hardware changes are required. Termination of the SerDes port should follow what is required when the port is enabled through both POR input and DEVDISR. See Note 1 for more information.

If the high-speed SerDes port requires complete or partial termination, the unused pins should be terminated as described in this section.

The following pins must be left unconnected (floating):

- SD*n*_TX[7:0]
- $\overline{\text{SD}n\text{_TX}}$[7:0]

The following pins must be connected to GND:

- SD*n*_RX[7:0]
- $\overline{\text{SD}n\text{_RX}}$[7:0]
- SD*n*_REF_CLK
- $\overline{\text{SD}n\text{_REF_CLK}}$

**NOTE**

It is recommended to power down the unused lane through SRDS1CR1[0:7] register (offset = 0xE_0F08) and SRDS2CR1[0:7] register (offset = 0xE_0F44.) (This prevents the oscillations and holds the receiver output in a fixed state.) that maps to SERDES lane 0 to lane 7 accordingly.

For other directions on reserved or no-connects pins see Section 17, "Signal Listings."

## 20.6 Pull-Up and Pull-Down Resistor Requirements

The MPC8640 requires weak pull-up resistors (2–10 kΩ is recommended) on all open drain type pins.

The following pins must not be pulled down during power-on reset: TSEC4_TXD[4], LGPL0/LSDA10, LGPL1/$\overline{\text{LSDWE}}$, TRIG_OUT/READY, and D1_MSRCID[2].

The following are factory test pins and require strong pull-up resistors (100Ω –1 kΩ) to $\text{OV}_{\text{DD}}$

$\overline{\text{LSSD_MODE}}$, TEST_MODE[0:3].The following pins require weak pull-up resistors (2–10 kΩ) to their specific power supplies: $\overline{\text{LCS}}$[0:4], $\overline{\text{LCS}}$[5]/$\overline{\text{DMA_DREQ2}}$, $\overline{\text{LCS}}$[6]/$\overline{\text{DMA_DACK}}$[2], $\overline{\text{LCS}}$[7]/$\overline{\text{DMA_DDONE}}$[2], IRQ_OUT, IIC1_SDA, IIC1_SCL, IIC2_SDA, IIC2_SCL, and $\overline{\text{CKSTP_OUT}}$.

The following pins should be pulled to ground with a 100-Ω resistor: SD1_IMP_CAL_TX, SD2_IMP_CAL_TX. The following pins should be pulled to ground with a 200-Ω resistor:

SD1_IMP_CAL_RX, SD2_IMP_CAL_RX

TSEC*n*_TX_EN signals require an external 4.7-kΩ pull down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.

When the platform frequency is 400 MHz, TSEC1_TXD[1] must be pulled down at reset.

TSEC2_TXD[4] and TSEC2_TX_ER pins function as cfg_dram_type[0 or 1] at reset and MUST BE VALID BEFORE HRESET ASSERTION when coming out of device sleep mode.

### 20.6.1 Special instructions for Single Core device

The mechanical drawing for the single core device does not have all the solder balls that exist on the single core device. This includes all the balls for VDD_Core1 and $\text{SENSEV}_{\text{DD}}$_Core1 which exist on the package for the dual core device, but not on the single core package. A solder ball is present for

$SENSEV_{SS}$_Core1 and needs to be connected to ground with a weak (2–10 kΩ) pull down resistor. Likewise, $AV_{DD}$_Core1 needs to be pulled to ground as shown in Figure 64.

The mechanical drawing for the single core device is located in Section 16.2, "Mechanical Dimensions of the MPC8640 FC-CBGA."

For other pin pull-up or pull-down recommendations of signals, please see Section 17, "Signal Listings."

## 20.7 Output Buffer DC Impedance

The MPC8640 drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for $I^2C$).

To measure $Z_0$ for the single-ended drivers, an external resistor is connected from the chip pad to $OV_{DD}$ or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 66). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and $R_P$ is trimmed until the voltage at the pad equals $OV_{DD}/2$. $R_P$ then becomes the resistance of the pull-up devices. $R_P$ and $R_N$ are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N) \div 2$.

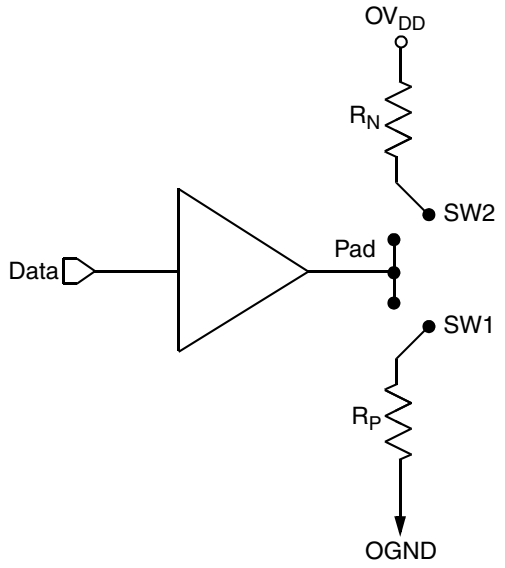



**Figure 66. Driver Impedance Measurement**

Table 73 summarizes the signal impedance targets. The driver impedances are targeted at minimum $V_{DD}$, nominal $OV_{DD}$, 105 °C.

**Table 73. Impedance Characteristics**

| Impedance | DUART, Control, Configuration, Power Management | PCI Express | DDR DRAM | Symbol | Unit |
|---|---|---|---|---|---|
| $R_N$ | 43 Target | 25 Target | 20 Target | $Z_0$ | W |
| $R_P$ | 43 Target | 25 Target | 20 Target | $Z_0$ | W |

**Note:** Nominal supply voltages. See Table 1, $T_j$ = 105 °C.

## 20.8 Configuration Pin Muxing

The MPC8640 provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform/system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled, the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e600 PLL ratio configuration pins are not equipped with these default pull-up devices.

## 20.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 68. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP port connects primarily through the JTAG interface of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 67 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 67, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header shown in Figure 67; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 67 is common to all known emulators.

For a multi-processor non-daisy chain configuration, Figure 68, can be duplicated for each processor. The recommended daisy chain configuration is shown in Figure 69. Please consult with your tool vendor to determine which configuration is supported by their emulator.

### 20.9.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, NXP recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. NXP recommends that the COP header be designed into the system as shown in Figure 68. If this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to $OV_{DD}$ through a 10 kΩ resistor. This will prevent TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.

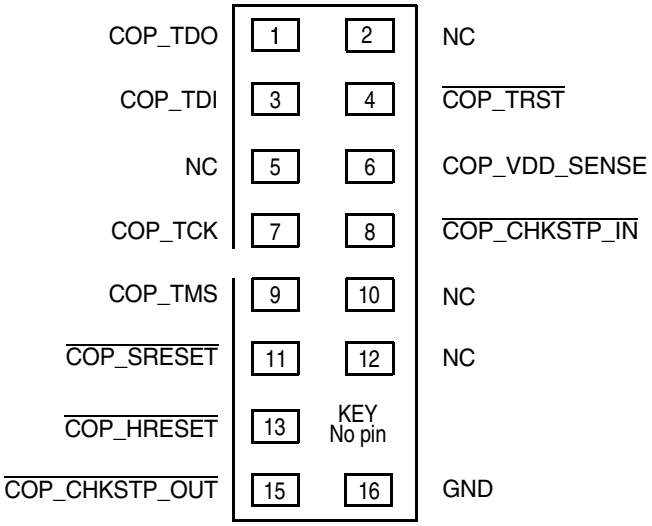
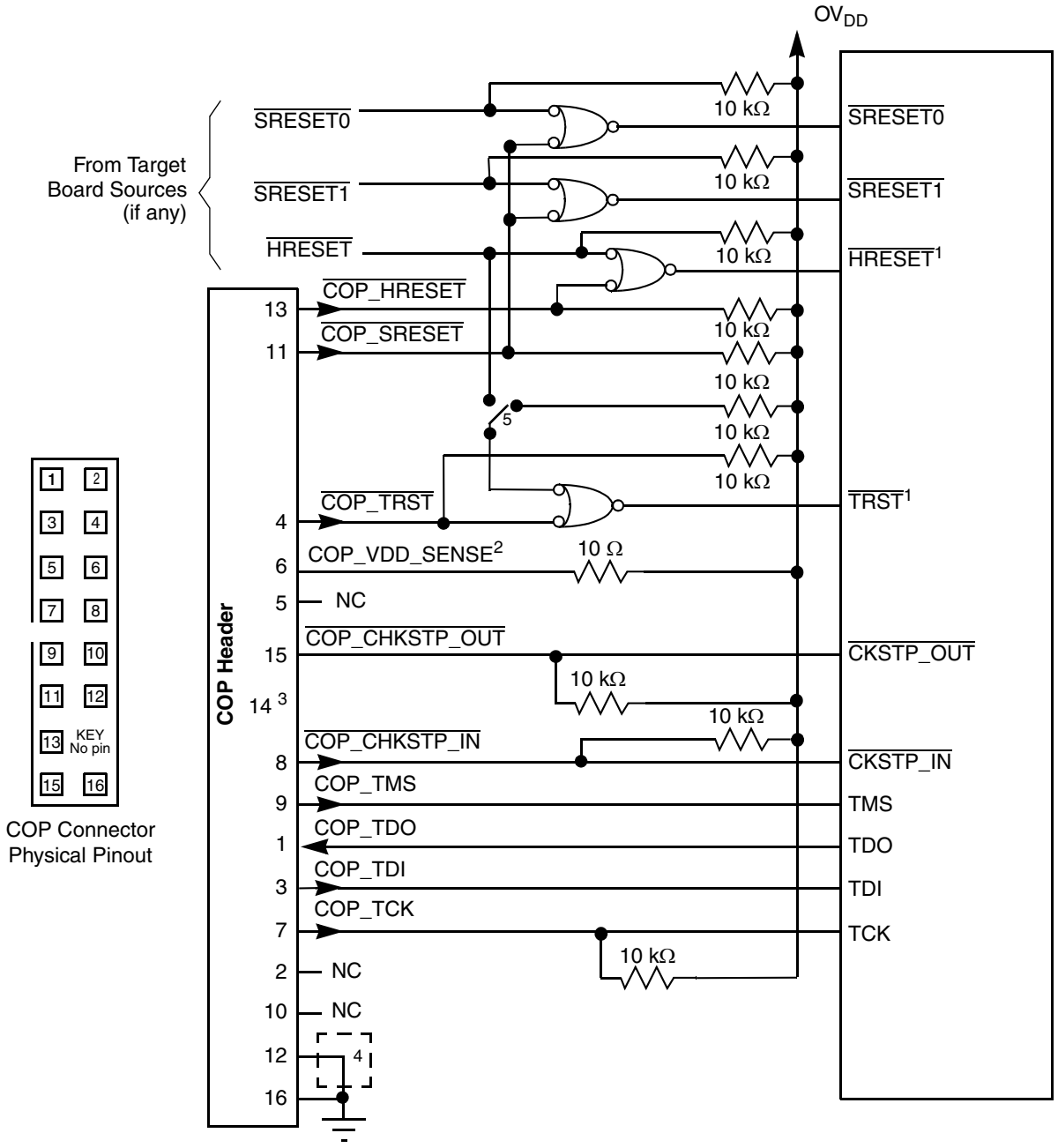


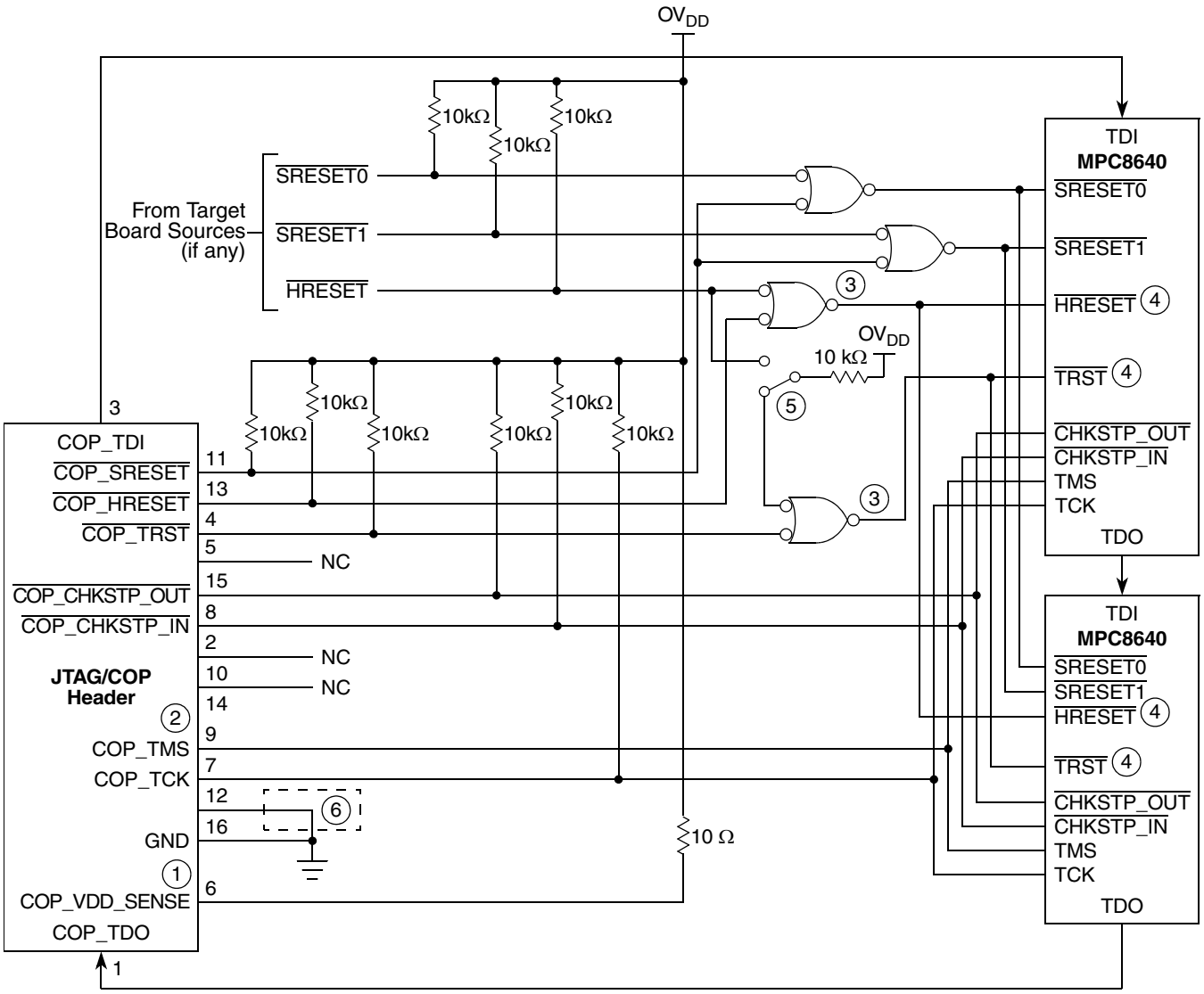

**Figure 67. COP Connector Physical Pinout**




**Notes:**

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed or removed.

**Figure 68. JTAG/COP Interface Connection for one MPC8640 device**




**Notes:**

1. Populate this with a 10-Ω resistor for short circuit/current-limiting protection.
2. KEY location; pin 14 is not physically present on the COP header.
3. Use a AND gate with sufficient drive strength to drive two inputs.
4. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown above.
5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed or removed.
6. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.

**Figure 69. JTAG/COP Interface Connection for Multiple MPC8640 Devices in Daisy Chain Configuration**

# 21 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 21.1, "Part Numbers Fully Addressed by This Document."

## 21.1 Part Numbers Fully Addressed by This Document

Table 74 provides the NXP part numbering nomenclature for the MPC8640. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local NXP sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

**Table 74. Part Numbering Nomenclature**

| *uu* | *nnnn* | *D* | *w* | *xx* | *yyyy* | *a* | *z* |
|---|---|---|---|---|---|---|---|
| **Product Code** | **Part Identifier** | **Core Count** | **Temp** | **Package[1]** | **Core Processor Frequency [2] (MHz)** | **DDR speed (MHz)** | **Product Revision Level** |
| MC[5] | 8640 | Blank = Single Core<br>D = Dual Core | Blank: 0°C to 105°C<br>T: –40 °C to 105 °C | HX = High-lead HCTE FC-CBGA<br>VU = RoHS lead-free HCTE FC-CBGA[6]<br>VJ = Lead-free HCTE FC-CBGA[7]<br>HJ = Leaded balls HCTE FC-CBGA[8] | 1000, 1067, 1250 | N = 533 MHz[4]<br>H = 500 MHz | Revision C = 2.1<br>System Version Register Value for Rev C:<br>0x8090_0021 MPC8640<br>0x8090_0121 MPC8640D<br><br>Revision E = 3.0<br>System Version Register Value for Rev E:<br>0x8090_0030 MPC8640<br>0x8090_0130 MPC8640D |

**Notes:**

1. See Section 16, “Package,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
3. The P prefix in a NXP part number designates a “Pilot Production Prototype” as defined by NXP SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.
4. Part Number MC8640xxx1067Nz is our low $V_{DD}$_Core*n* device. $V_{DD}$_Core*n* = 0.95 V and $V_{DD}$_PLAT = 1.05 V.
5. MC - Qualified production
6. VU part number is RoHS compliant with the permitted exception of the C4 die bumps.
7. VJ part number is entirely lead-free including the C4 die bumps.
8. HJ part number is entirely lead-free except for the C5 solder balls.

Table 75 shows the parts that are available for ordering and their operating conditions.

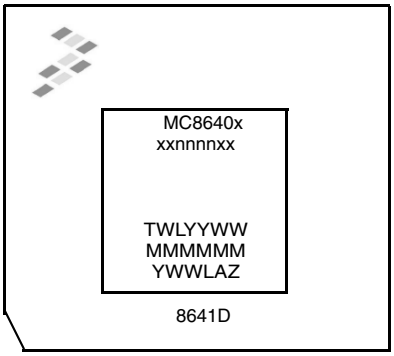
**Table 75. Part Offerings and Operating Conditions**

| Part Offerings[1] | Operating Conditions |
|---|---|
| MC8640Dwxx1250Hz | Dual core<br>Max CPU speed = 1250 MHz,<br>Max DDR = 500 MHz<br>Core Voltage = 1.05 volts |
| MC8640Dwxx1000Hz | Dual core<br>Max CPU speed = 1000 MHz,<br>Max DDR = 500 MHz<br>Core Voltage = 1.05 volts |
| MC8640Dwxx1067Nz | Dual core<br>MAX CPU speed = 1067 MHz,<br>MAX DDR = 533 MHz<br>Core Voltage = 0.95 volts |
| MC8640wxx1250Hz | Single core<br>Max CPU speed = 1250 MHz,<br>Max DDR = 500 MHz<br>Core Voltage = 1.05 volts |
| MC8640wxx1000Hz | Single core<br>Max CPU speed = 1000 MHz,<br>Max DDR = 500 MHz<br>Core Voltage = 1.05 volts |
| MC8640wxx1067Nz | Single core<br>Max CPU speed = 1067 MHz,<br>Max DDR = 533 MHz<br>Core Voltage = 0.95 volts |

1 Note that the “w” represents the operating temperature range. The “xx” in the part marking represents the package option. The “z” represents the product revision level. For more information see Table 74.

## 21.2 Part Marking

Parts are marked as the example shown in Figure 70.




NOTE:
TWLYYWW is the test code
MMMMMM is the M00 (mask) number.
YWWLAZ is the assembly traceability code.

**Figure 70. Part Marking for FC-CBGA Device**

# 22 Document Revision History

Table 76 provides a revision history for the MPC8640D hardware specification.

**Table 76. Document Revision History**

| Revision | Date | Substantive Change(s) |
|---|---|---|
| 5 | 02/2017 | • Updated Section 16.1, “Package Parameters for the MPC8640” with information related to package options.<br>• Updated Section 16.2, “Mechanical Dimensions of the MPC8640 FC-CBGA” with information related to package options.<br>• Updated Table 74, “Part Numbering Nomenclature,” to add package type HJ and related footnote 8.<br>• Updated the template for NXP.<br>• Replaced all “Freescale” instances to “NXP”. |
| 4 | 05/2014 | • Updated Serial RapidIO equation in Section 4.4, “Platform Frequency Requirements for PCI-Express and Serial RapidIO”<br>• In Table 41, “Local Bus Timing Specifications ($OV_{DD}$ = 3.3 V)—PLL Enabled,” changed the value for Local bus cycle time from 8 to 7.5 ns.<br>• Updated Section 19.2.4, “Temperature Diode,” by removing the ideality factor value.<br>• Updated Figure 70 such that the marking on the substrate is 8641D instead of 8640D.<br>• Added VJ package description and footnotes to Table 74., “Part Numbering Nomenclature” and Section 16, “Package.” |
| 3 | 07/2009 | • Updated Table 74, “Part Numbering Nomenclature,” and Table 75, “Part Offerings and Operating Conditions,” to include silicon revision 3.0 part markings. |
| 2 | 06/2009 | • Added Table 5, “MPC8640D Individual Supply Maximum Power Dissipation 1.”<br>• Added Note 8 to Table 49, “Differential Transmitter Output Specifications.” |

**Table 76. Document Revision History**

| Revision | Date | Substantive Change(s) |
|---|---|---|
| 1 | 11/2008 | • Removed voltage option of 1.10 V from Table 2 because it is not supported by MPC8640D or MPC8640<br>• Updated Table 4 and Table 6 with the new 1067/533 MHz device offering. This includes updated Power Specifications.<br>• Added Section 4.4, “Platform Frequency Requirements for PCI-Express and Serial RapidIO”<br>• Updated Section 6, “DDR and DDR2 SDRAM” to include 533 MHz.<br>• Added core frequency of 1067 to Table 64, Table 65, Table 66 and Table 67<br>• Changed Max Memory clock frequency from 250 MHz to 266 MHz in Table 65<br>• Changed Max MPX/Platform clock Frequency from 500 MHz to 533 MHz in Table 66<br>• Changed Max Local Bus clock speed from 1 MHz to 133 MHz in Table 67<br>• Added MPX:Sysclk Ratio of 8:1 to Table 68<br>• Added Core:MPX Ratio of 3:1 to Table 69<br>• Updated Table 70 to include 533 MPX clock frequency<br>• Changed the Extended Temp range part numbering ‘w’ to be T instead of an H in Table 74<br>• Changed the DDR speed part numbering N to stand for 533 MHz instead of 500 MHz in Table 74<br>• Removed the statement “Note that core processor speed of 1500 MHz is only available for the MPC8640D (dual core)” from Note 2 in Table 74 because MPC8640D is not offered at 1500 MHz core.<br>• Removed the part offering MC8640Dwxx1000NC which is replaced with MC8640Dwxx1067NC and removed MC8640wxx1000NC replaced with MC8640wxx1067NC in Table 75<br>• Added Note 8 to Figure 57 and Figure 58. |
| 0 | 07/2008 | • Initial Release |

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