FS26

Safety system basis chip with low power for ASIL D / ASIL B

Rev. 4 — 16 July 2024 **Product brief**



1 About this document

This product brief is intended to provide overview/summary information for the purpose of evaluating a product for design suitability. It is intended for quick reference only and should not be relied upon to contain detailed and full information.

Some of the content in this product brief is extracted from the product's full data sheet. In case of any inconsistency or conflict, the full data sheet shall prevail.

For detailed and full information, see the relevant FS26 full data sheet, available via the NXP Secure Files content interface.

2 General description

Devices in the FS26 automotive safety system basis chip (SBC) family are designed to support entry and mid-range safety microcontrollers, like those in the S32K3 series. FS26 devices have multiple power supplies and the flexibility to work with other microcontrollers targeting automotive electrification. Possible FS26 applications include power train, chassis, safety and low-end gateway technology.

This family of devices consist of several versions that are pin to pin and software compatible. These versions support a wide range of applications with automotive safety integrity levels (ASIL) B or D, offering choices in number of output rails, output voltage settings, operating frequencies, power up sequencing, and integrated system level features.

The FS26 features multiple switch mode regulators and low dropout (LDO) voltage regulators to supply the microcontroller, sensors, peripheral ICs and communication interfaces. It offers a high precision reference voltage supply for the system, and for two independent tracking regulators. The FS26 also offers various functionality for system control and diagnostics, including an analog multiplexer, general purpose input/outputs (GPIOs), and selectable wakeup events from I/O, long duration timer or serial-peripheral interface (SPI) communication.

The FS26 is developed in compliance with the ISO26262 standard, and includes enhanced safety features with multiple fail-safe outputs. It uses the latest on-demand latent fault monitoring, and can be part of a safety-oriented system partitioning scheme covering both ASIL B and ASIL D safety integrity levels.

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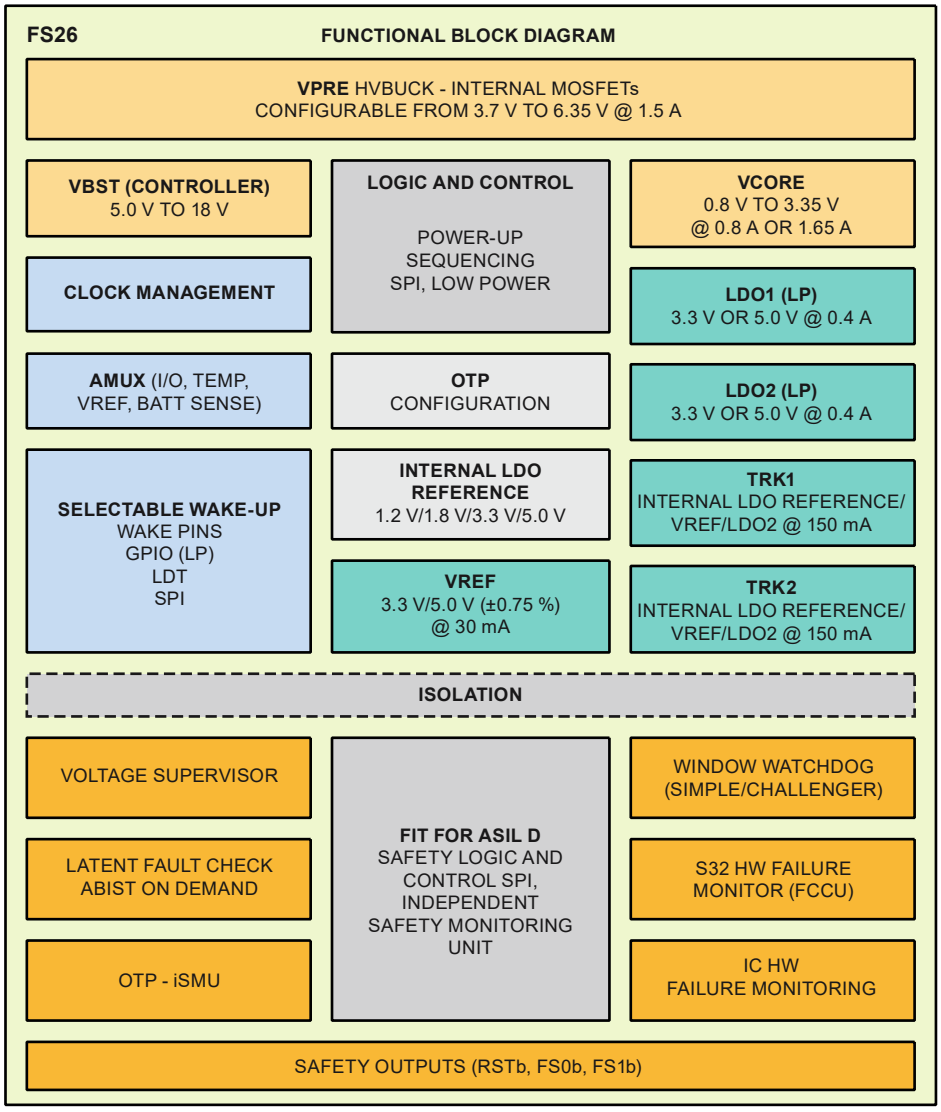


Figure 1. Functional block diagram

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3 Features and benefits

Operating range

- 40 V DC maximum input voltage
- Supports operating voltage range down to battery 3.2 V with VBST in front-end
- Supports operating voltage range down to battery 6 V without VBST in front-end
- Low Power *LPOFF mode* with 30 µA quiescent current
- Low Power *standby mode* with 29 µA quiescent current with VPRE active. LDO1 or LDO2 activation selectable via OTP configuration. GPIO1 or GPIO2 activation selectable via SPI communication.

Power supplies

- VPRE: Synchronous buck converter with integrated FETs. Configurable output voltage and switching frequency, output DC current capability up to 1.5 A and PFM mode for Low Power *standby mode* operation.
- VCORE: Synchronous buck converter with integrated FETs. VCORE is dedicated for microcontroller core supply. Output DC current up to 0.8 A or 1.65 A (depending on part number), output voltage range setting from 0.8 V to 3.35 V.
- VBST: Asynchronous boost controller with external low-side switch, diode, and current sense resistor. VBST is configurable as front-end supply to withstand low voltage cranking profiles or in back-end supply with configurable output voltage and scalable output DC current capability.
- LDO1: LDO regulator for microcontroller I/O support with selectable output voltage between 3.3 V and 5.0 V and up to 400 mA current capability.
- LDO2: LDO regulator for system peripheral support with selectable output voltage between 3.3 V and 5.0 V and up to 400 mA current capability.
- VREF: High-precision reference voltage with 0.75 % accuracy for External ADC reference and internal tracking reference.
- TRK1 and TRK2: Voltage tracking regulators with selectable output voltage between VREF, LDO2, or Internal LDO reference. Supports high-voltage protection for ECU off- board operation. Each tracker has a current capability up to 150 mA.

System support

- Two wake-up inputs with high-voltage support for system robustness
- Two programmable GPIO with wake-up capability or HS/LS driver
- Programmable long duration timer (LDT) for system shutdown and wake-up control
- Monitoring of system voltages (Including Battery voltage monitoring) through the analog multiplexer
- Selectable wake-up sources from: WAKE/GPIO pins, LDT, or SPI activity
- Device control via 32-bit SPI interface with cyclic redundancy checks (CRC)

Compliance

- Electromagnetic compatibility (EMC) optimization techniques for switching regulators, including spread spectrum, slew rate control, and manual frequency tuning.
- Electromagnetic interference (EMI) robustness supporting various automotive EMI test standards.

Functional safety

- Scalable portfolio from Automotive Safety Integrity Levels (ASIL) B to D
- Independent monitoring circuitry, dedicated interface for microcontroller monitoring, simple or challenger watchdog function
- Analog built-in self-test (ABIST1) and logical built-in self-test (LBIST) at startup
- Analog built-in self-test (ABIST2) on demand
- Safety outputs with latent fault detection mechanism (RSTB, FS0B, FS1B)

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Configuration and enablement

- LQFP48 pins with exposed pad for optimized thermal management
- Permanent device customization via one time programmable (OTP) fuse memory
- OTP Emulation mode for hardware development and evaluation
- *Debug mode* for software development, MCU programming, and debugging

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4 Applications

xEV and powertrain market

- Inverter
- Onboard charger (OBC), DCDC
- Battery management system (BMS)
- Belt starter generator (BSG)

Body market

- Gateway
- Zonal control
- Body controller
- Smart junction box

Safety and chassis

- Suspension
- Power steering

MCU attach

- NXP S32K3 family
- Infineon AURIX family (TC2xx and TC3xx)
- Renesas RH850 family
- Cypress Traveo family

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5 Ordering information

This section describes the part numbers available for purchase, with their main differences. It also depicts how the part number reference is built.

5.1 Part number definition

Figure 2 shows how the FS26xyz part number is used to describe the available feature set of each device.

FS26xx
Product Numbering Scheme

P	FS	26 X Y	A	M	Zzz	AD
Release Type	Family	Product Core	Release Version	Temperature	Funct. or Param. variant	Package
M Production	FS High Voltage Power Management	2600-2633 Core	A Initial Release	M -40 to 125 °C	A0 No OTP	AD LQFP48
P Pre-release			B-Z as required		A1-ZZ Unique part identification	
S Customer special						

FS 2 6 X Y Z

Z	ASIL
B	Fit for ASIL B (Simple W/D, UV/OV, ABIST, VMON)
D	Fit for ASIL D (Challenger WD, FCCU, ABIST/LBIST, VMON)

Y	FS1b	LDT	Use case
0	no	no	Base
1	yes	no	FS1b
2	no	yes	LDT
3	yes	yes	FS1b and LDT

X	PMIC Solution
0	Vcore 0.8 A, Vboost, 1 MV Buck, 2 LDOs 1 Tracker
1	Vcore 0.8 A, Vboost, 1 MV Buck, 2 LDOs 2 Trackers
2	Vcore 1.6 A, Vboost, 1 MV Buck, 2 LDOs 1 Tracker
3	Vcore 1.6 A, Vboost, 1 MV Buck, 2 LDOs 2 Trackers

aaa-045498

Figure 2. Part number breakdown

Figure 3 maps FS26 part numbers vs. product feature sets.

Vcore	0.8 A core				1.6 A core			
EXT Supply	1 TRK		2 TRK		1 TRK		2 TRK	
ASIL Level	ASIL B	ASIL D	ASIL B	ASIL D	ASIL B	ASIL D	ASIL B	ASIL D
Base	FS2600B	FS2600D	FS2610B	FS2610D	FS2620B	FS2620D	FS2630B	FS2630D
FS1b	FS2601B	FS2601D	FS2611B	FS2611D	FS2621B	FS2621D	FS2631B	FS2631D
LDT	FS2602B	FS2602D	FS2612B	FS2612D	FS2622B	FS2622D	FS2632B	FS2632D
FS1b + LDT	FS2603B	FS2603D	FS2613B	FS2613D	FS2623B	FS2623D	FS2633B	FS2633D

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Figure 3. Part number mapping versus features set

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5.2 Part number list

Table 1. Device segmentation

Part Number	DEV_ID[5:0]	Tracker 2	Core Current Capability	Long Duration Timer	Tracker 2 Monitoring	FS1B	ABIST on demand	Watchdog Type	Fault Recovery	FCCU Monitoring	LBIST
FS2600B	0x01	NO	0.8 A	NO	NO	NO	YES	Simple	NO	Optional	NO
FS2601B	0x02	NO	0.8 A	NO	NO	YES	YES	Simple	NO	Optional	NO
FS2602B	0x03	NO	0.8 A	YES	NO	NO	YES	Simple	NO	Optional	NO
FS2603B	0x04	NO	0.8 A	YES	NO	YES	YES	Simple	NO	Optional	NO
FS2600D	0x05	NO	0.8 A	NO	NO	NO	YES	Challenger	YES	YES	YES
FS2601D	0x06	NO	0.8 A	NO	NO	YES	YES	Challenger	YES	YES	YES
FS2602D	0x07	NO	0.8 A	YES	NO	NO	YES	Challenger	YES	YES	YES
FS2603D	0x08	NO	0.8 A	YES	NO	YES	YES	Challenger	YES	YES	YES
FS2610B	0x09	YES	0.8 A	NO	YES	NO	YES	Simple	NO	Optional	NO
FS2611B	0x0A	YES	0.8 A	NO	YES	YES	YES	Simple	NO	Optional	NO
FS2612B	0x0B	YES	0.8 A	YES	YES	NO	YES	Simple	NO	Optional	NO
FS2613B	0x0C	YES	0.8 A	YES	YES	YES	YES	Simple	NO	Optional	NO
FS2610D	0x0D	YES	0.8 A	NO	YES	NO	YES	Challenger	YES	YES	YES
FS2611D	0x0E	YES	0.8 A	NO	YES	YES	YES	Challenger	YES	YES	YES
FS2612D	0x0F	YES	0.8 A	YES	YES	NO	YES	Challenger	YES	YES	YES
FS2613D	0x10	YES	0.8 A	YES	YES	YES	YES	Challenger	YES	YES	YES
FS2620B	0x11	NO	1.65 A	NO	NO	NO	YES	Simple	NO	Optional	NO
FS2621B	0x12	NO	1.65 A	NO	NO	YES	YES	Simple	NO	Optional	NO
FS2622B	0x13	NO	1.65 A	YES	NO	NO	YES	Simple	NO	Optional	NO
FS2623B	0x14	NO	1.65 A	YES	NO	YES	YES	Simple	NO	Optional	NO
FS2620D	0x15	NO	1.65 A	NO	NO	NO	YES	Challenger	YES	YES	YES
FS2621D	0x16	NO	1.65 A	NO	NO	YES	YES	Challenger	YES	YES	YES
FS2622D	0x17	NO	1.65 A	YES	NO	NO	YES	Challenger	YES	YES	YES
FS2623D	0x18	NO	1.65 A	YES	NO	YES	YES	Challenger	YES	YES	YES
FS2630B	0x19	YES	1.65 A	NO	YES	NO	YES	Simple	NO	Optional	NO
FS2631B	0x1A	YES	1.65 A	NO	YES	YES	YES	Simple	NO	Optional	NO
FS2632B	0x1B	YES	1.65 A	YES	YES	NO	YES	Simple	NO	Optional	NO
FS2633B	0x1C	YES	1.65 A	YES	YES	YES	YES	Simple	NO	Optional	NO
FS2630D	0x1D	YES	1.65 A	NO	YES	NO	YES	Challenger	YES	YES	YES
FS2631D	0x1E	YES	1.65 A	NO	YES	YES	YES	Challenger	YES	YES	YES
FS2632D	0x1F	YES	1.65 A	YES	YES	NO	YES	Challenger	YES	YES	YES
FS2633D	0x20	YES	1.65 A	YES	YES	YES	YES	Challenger	YES	YES	YES

Table 2. Orderable part numbers

Part number	Description	Package
MFS2613AMDA2AD	S32K344 + FS26 EVB ASIL D S32K3X4EVB-x257	LQFP48
MFS2613AMDA3AD	S32K344 400 V HVBMS Reference design	
MFS2613AMDA4AD	S32K344 Body Control Module Reference design (white board)	
MFS2613AMDA6AD	S32K344 48 V MC Development platform	
MFS2621AMDABAD	Aurix TC38, TC29	

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Table 2. Orderable part numbers*...continued*

Part number	Description	Package
MFS2613AMDDCAD	S32K324 5G T-BOX + Gateway	
MFS2633AMDALAD	S32K3x8 and S32K396 MCU attach	
MFS2633AMDE4AD	S32K396 Reference design	
MFS2613AMDH3AD	S32K344 400 V HVBMS Reference design (No VBST)	
MFS2633AMDAHAD	S32K396 BMS Reference design	
MFS2633AMDAJAD	S32K358 400 V & 800 V HVBMS Reference design	
MFS2633AMDC3AD	S32K358 400 V & 800 V HVBMS Reference design (wireless)	
MFS2633AMDAKAD	S32K358 400 V & 800 V HVBMS Reference design (No VBST)	
MFS2633AMDADAD	RH850UA2x for BMS and ZCU applications (VCORE = 1.09 V)	
MFS2621AMDAEAD	RH850C, RH850Por RH850F for EPS, BMS, Motor control and DCDC applications (VCORE = 1.25 V)	
MFS2633AMDAMAD	RH850UA2x for ADAS, Smart cockpit and 3.3V applications (VCORE = 1.09 V)	
MFS2600AMBA0AD	Superset covering FS2600B devices	
MFS2600AMDA0AD	Superset covering FS2600D devices	
MFS2601AMBA0AD	Superset covering FS2601B devices	
MFS2601AMDA0AD	Superset covering FS2601D devices	
MFS2602AMBA0AD	Superset covering FS2602B devices	
MFS2602AMDA0AD	Superset covering FS2602D devices	
MFS2603AMBA0AD	Superset covering FS2603B devices	
MFS2603AMDA0AD	Superset covering FS2603D devices	
MFS2610AMBA0AD	Superset covering FS2610B devices	
MFS2610AMDA0AD	Superset covering FS2610D devices	
MFS2611AMBA0AD	Superset covering FS2611B devices	
MFS2611AMDA0AD	Superset covering FS2611D devices	
MFS2612AMBA0AD	Superset covering FS2612B devices	
MFS2612AMDA0AD	Superset covering FS2612D devices	
MFS2613AMBA0AD	Superset covering FS2613B devices	
MFS2613AMDA0AD	Superset covering FS2613D devices	
MFS2620AMBA0AD	Superset covering FS2620B devices	
MFS2620AMDA0AD	Superset covering FS2620D devices	
MFS2621AMBA0AD	Superset covering FS2621B devices	
MFS2621AMDA0AD	Superset covering FS2621D devices	
MFS2622AMBA0AD	Superset covering FS2622B devices	
MFS2622AMDA0AD	Superset covering FS2622D devices	
MFS2623AMBA0AD	Superset covering FS2623B devices	
MFS2623AMDA0AD	Superset covering FS2623D devices	

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Table 2. Orderable part numbers*...continued*

Part number	Description	Package
MFS2630AMDA0AD	Superset covering FS2630D devices	
MFS2630AMBA0AD	Superset covering FS2630B devices	
MFS2631AMBA0AD	Superset covering FS2631B devices	
MFS2631AMDA0AD	Superset covering FS2631D devices	
MFS2632AMBA0AD	Superset covering FS2632B devices	
MFS2632AMDA0AD	Superset covering FS2632D devices	
MFS2633AMBA0AD	Superset covering FS2633B devices	

Empty OTP samples can be ordered for engineering purposes using part numbers MFS2633AMDA0AD or MFS2633AMBA0AD.

Refer to the associated OTP configuration report in the website product page.

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6 Simplified application diagrams

Figure 4 shows a simplified block diagram for a typical system with an FS26, using the boost controller to support battery cold-crank events.

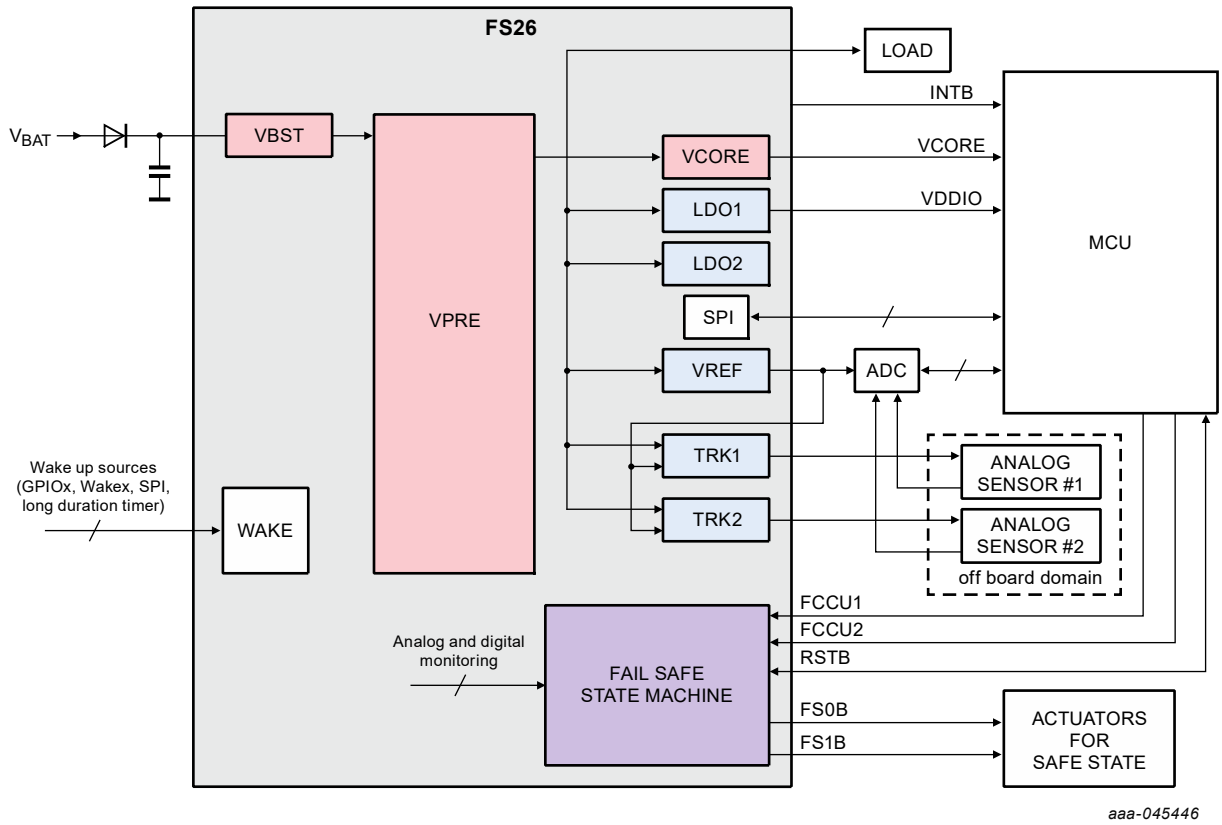


Figure 4. Example of application diagram (with VBST as a front-end regulator)

Figure 5 shows a simplified block diagram for a typical system with an FS26, using the boost controller to generate a voltage above the high-voltage buck output voltage.

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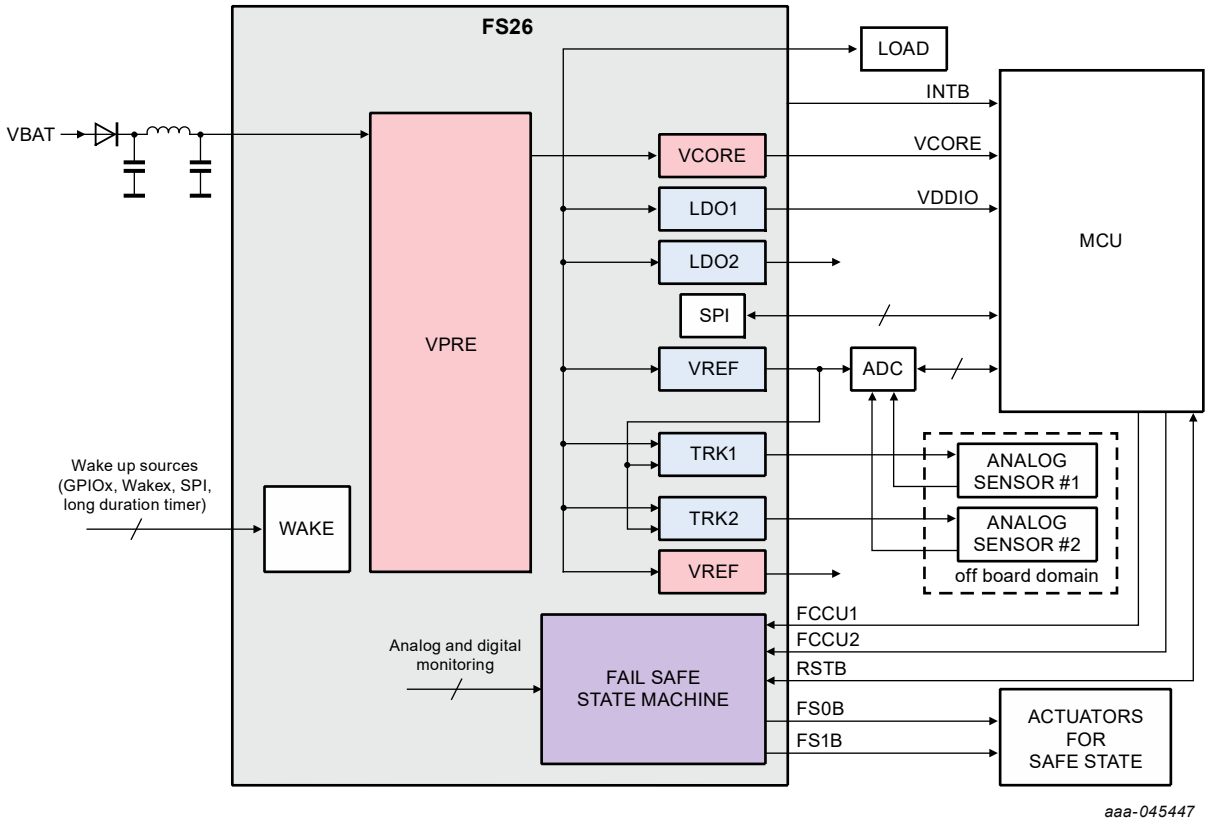


Figure 5. Example of application diagram (with VBST as a back-end regulator)

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7 Block diagram

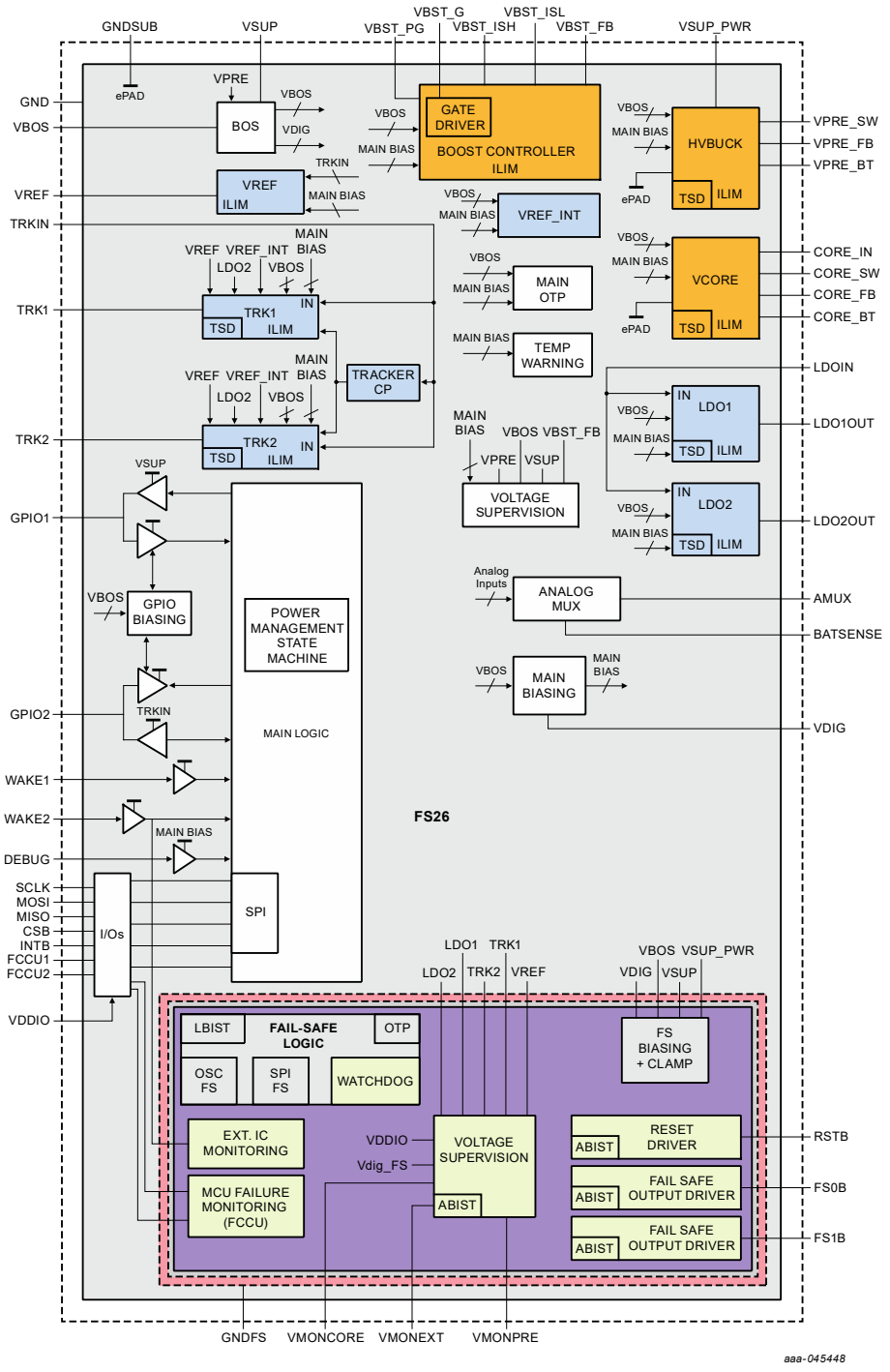


Figure 6. Block diagram of the FS26

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8 Pinning Information

8.1 Pinning

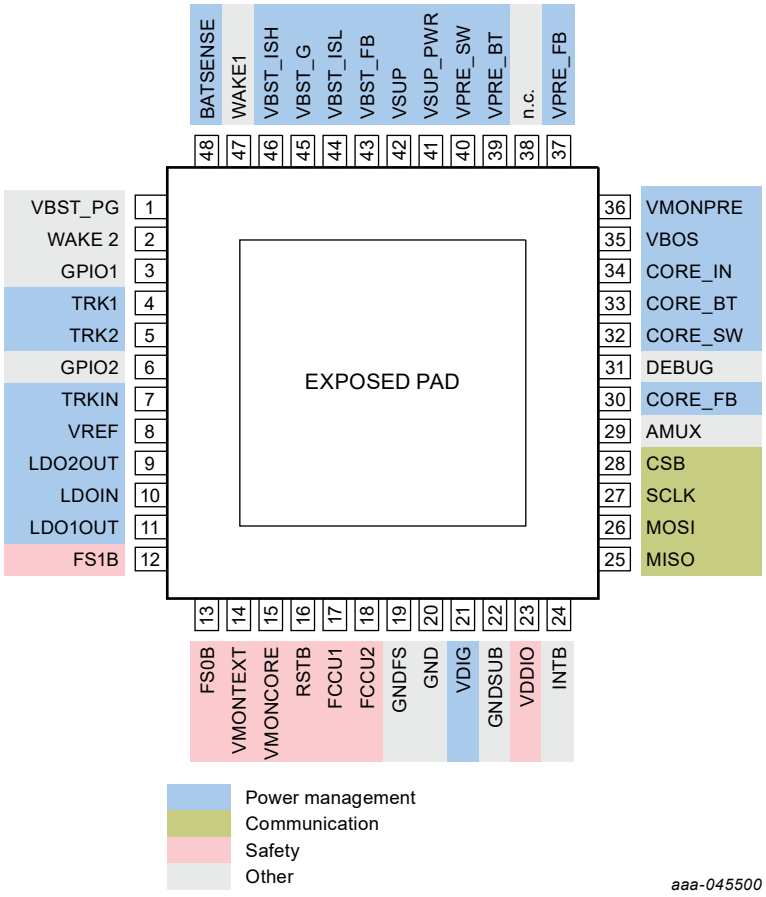


Figure 7. Pin assignment in LQFP48 package with exposed pad

8.2 Pin descriptions

Table 3. Pin descriptions

Symbol	Pin Number	Type	Description
VBST_PG	1	Digital output	Power good signal for boost controller
WAKE2	2	Analog input	WAKE2 input pin or ERROR monitoring input
GPIO1	3	Analog output / Digital Input	General purpose I/O 1
TRK1	4	Analog output	TRK1 output
TRK2	5	Analog output	TRK2 output
GPIO2	6	Analog output / Digital Input	General purpose I/O 2
TRKIN	7	Analog input	Tracker input
VREF	8	Analog output	Voltage reference output
LDO2OUT	9	Analog output	LDO2 output
LDOIN	10	Analog input	LDO input voltage supply
LDO1OUT	11	Analog output	LDO1 output
FS1B	12	Digital output	Safety output #1

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Table 3. Pin descriptions*...continued*

Symbol	Pin Number	Type	Description
FS0B	13	Digital output	Safety output #0
VMONEXT	14	Analog input	External voltage monitoring input
VMONCORE	15	Analog input	VCORE voltage monitoring input
RSTB	16	Digital input/output	Reset input/output
FCCU1	17	Digital input	Fault control collection unit 1
FCCU2	18	Digital input	Fault control collection unit 2
GNDFS	19	Ground connection	GND for fail-safe circuitry
GND	20	Ground connection	GND for main circuitry
VDIG	21	Analog output	1.6 V digital supply
GNDSUB	22	Ground connection	Substrate ground
VDDIO	23	Analog input	I/O input supply
INTB	24	Digital output	Interrupt output
MISO	25	Digital output	SPI primary in secondary out
MOSI	26	Digital input	SPI primary out secondary input
SCLK	27	Digital input	SPI clock input
CSB	28	Digital input	SPI chip select
AMUX	29	Analog output	Analog multiplexer output
CORE_FB	30	Analog input	VCORE feedback node
DEBUG	31	Digital input	DEBUG input pin
CORE_SW	32	Analog output	VCORE switching node
CORE_BT	33	Analog input	VCORE bootstrap supply
CORE_IN	34	Analog input	VCORE input supply
VBOS	35	Analog output	Best of supply decoupling output
VMONPRE	36	Analog input	VPRE monitoring pin
VPRE_FB	37	Analog input	VPRE feedback node
NC	38	Not connected pin	Not connected pin
VPRE_BT	39	Analog output	VPRE boot strap capacitor
VPRE_SW	40	Analog output	VPRE switching node
VSUP_PWR	41	Analog input	VPRE converter supply pin
VSUP	42	Analog input	Supply pin for internal biasing
VBST_FB	43	Analog input	VBST feedback node
VBST_ISL	44	Analog input	VBST current sense low
VBST_G	45	Analog output	VBST low-side gate drive
VBST_ISH	46	Analog input	VBST current sense high
WAKE1	47	Analog input	WAKE1 input pin
BATSENSE	48	Analog input	Battery sense terminal
EP	49	Ground connection	Exposed pad (to be connected to GND)

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9 Maximum ratings

Table 4. Maximum ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (Rating)	Min	Max	Unit
Voltage ratings				
VPRE_BT	DC voltage at VPRE_BT pin	-0.3	45.5	V
GPIO1, GPIO2, FS1B, FS0B, VMONEXT, VMONCORE, VMONPRE, WAKE1, WAKE2, VPRE_SW, VBST_FB	DC voltage at GPIO1, GPIO2, FS1B, FS0B, VMONEXT, VMONCORE, VMONPRE, WAKE1, WAKE2, VPRE_SW, VBST_FB pins	-0.3	40	V
BATSENSE	DC voltage at BATSENSE pin with -10 mA maximum reverse current (recommended 5.1 kΩ serial resistor)	-18.0	40	V
TRK1, TRK2, VSUP, VSUP_PWR	DC voltage at TRK1, TRK2, VSUP_PWR, VSUP pins	-1.2	40	V
CORE_BT	DC voltage at CORE_BT pin	-0.3	12.5	V
DEBUG	DC voltage at DEBUG pin	-0.3	10	V
TRKIN, LDOIN, CORE_IN, VPRE_FB, CORE_SW	DC voltage at TRKIN, LDOIN, CORE_IN, VPRE_FB, CORE_SW pins	-0.3	8.5	V
VBOS	DC voltage at VBOS pin	-0.3	5.6	V
VREF, LDO2OUT, LDO1OUT, RSTB, FCCU1, FCCU2, VDDIO, INTB, MISO, MOSI, SCLK, CSB, AMUX, CORE_FB, VBST_ISH, VBST_ISL, VBST_G, VBST_PG	DC voltage at VREF, LDO2OUT, LDO1OUT, RSTB, FCCU1, FCCU2, VDDIO, INTB, MISO, MOSI, SCLK, CSB, AMUX, CORE_FB, VBST_ISH, VBST_ISL, VBST_G and VBST_PG pins	-0.3	5.5	V
VDIG	DC voltage at VDIG pin	-0.3	2	V
GNDFS, GND, GNDSUB, EP	DC voltage at GNDFS, GND, GNDSUB pins, and exposed pad (EP)	-0.3	0.3	V
WAKE1, WAKE2, GPIO1, GPIO2	DC maximum reverse current at WAKE1, WAKE2, GPIO1, GPIO2 pins	-5	—	mA

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10 Electrostatic discharge

Table 5. ESD

Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (Rating)	Min	Max	Unit
ESD ratings				
Human body model: AEC-Q-100 Rev H.				
V_{ESD_HBM}	All pins	-2.0	2.0	kV
Charged device model: AEC-Q-100 Rev H				
V_{ESD_CDM1}	All pins	-500	500	V
V_{ESD_CDM2}	Corner pins	-750	750	V
Gun Test				
V_{ESD_CDT1}	ESD - GUN discharged contact test 330 Ω/150 pF unpowered according to IEC61000-4-2 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
V_{ESD_CDT2}	ESD - GUN discharged contact test 2 kΩ/150 pF unpowered according to ISO10605.2008 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
V_{ESD_CDT3}	ESD - GUN discharged contact test 2 kΩ/330 pF powered according to ISO10605.2008 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
V_{ESD_CDT4}	ESD - GUN discharged contact test 330 Ω/150 pF powered according to ISO10605.2008 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
V_{ESD_CDT5}	Operating ESD- GUN discharged contact test 330 Ω/150 pF powered according to ISO10605.2008 Global pins (GND, BATSENSE, FS0B, FS1B). Criteria: CLASS A	-8	8	kV

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11 Thermal ratings

Table 6. Temperatures ranges

Symbol	Description	Min	Typ	Max	Unit
T_A	Ambient temperature	-40	—	125	°C
T_J	Junction temperature	-40	—	150	°C
T_{STG}	Storage temperature	-55	—	150	°C
T_{WARN}	Temperature warning threshold to set TWARN_S SPI bit	145	155	170	°C

Table 7. Thermal resistance (per JEDEC JESD51-2)

Symbol	Description	Value	Unit
$R_{\theta JA}$	Thermal resistance Junction to Ambient[1]	25	°C/W
$R_{\theta JCBOTTOM}$	Thermal resistance Junction to Case Bottom[2][3] (with uniform power dissipation on the silicon die)	1.7	°C/W
$R_{\theta JCTOP}$	Thermal resistance Junction to Case Top[1][3]	13.5	°C/W
Ψ_{JT}	Thermal characterization parameter Junction to Top[4]	0.8	°C/W

[1] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
[2] Thermal resistance between the die and the printed circuit board. Board temperature is measured on the top surface of the board near the package.
[3] For exposed pad packages where the pad would be expected to be soldered, junction to case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.
[4] Thermal test board meets JEDEC specification for this package (JESD51-7).

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12 Packaging

12.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

Table 8. Package mechanical dimensions

Package	Suffix	Package outline drawing number
7.0 × 7.0, 48–Pin LQFP exposed pad, with 0.5 mm pitch, and a 4.5 × 4.5 exposed pad	AE	98ASA00945D

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12.2 Package outline

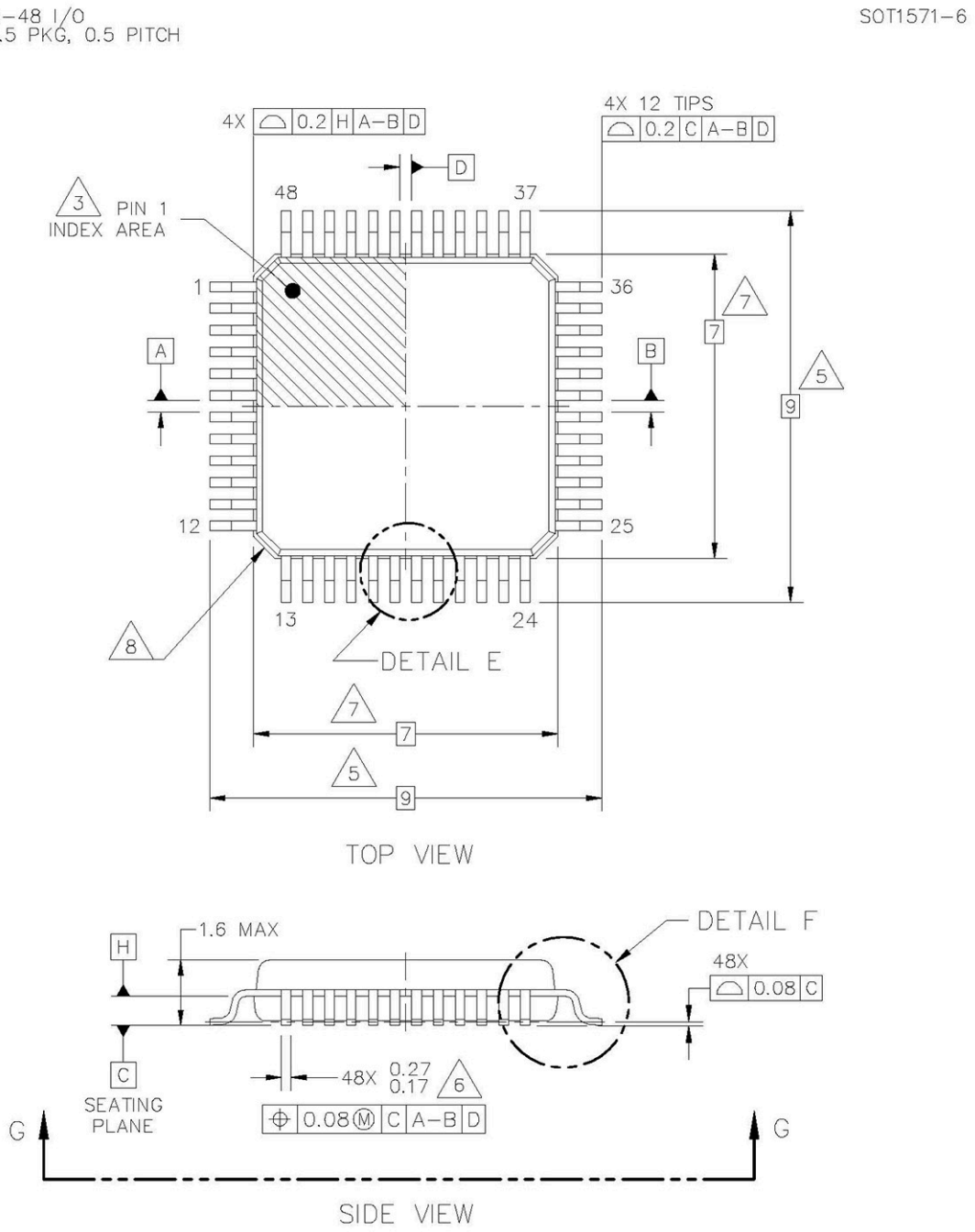


Figure 8. SOT1571-6

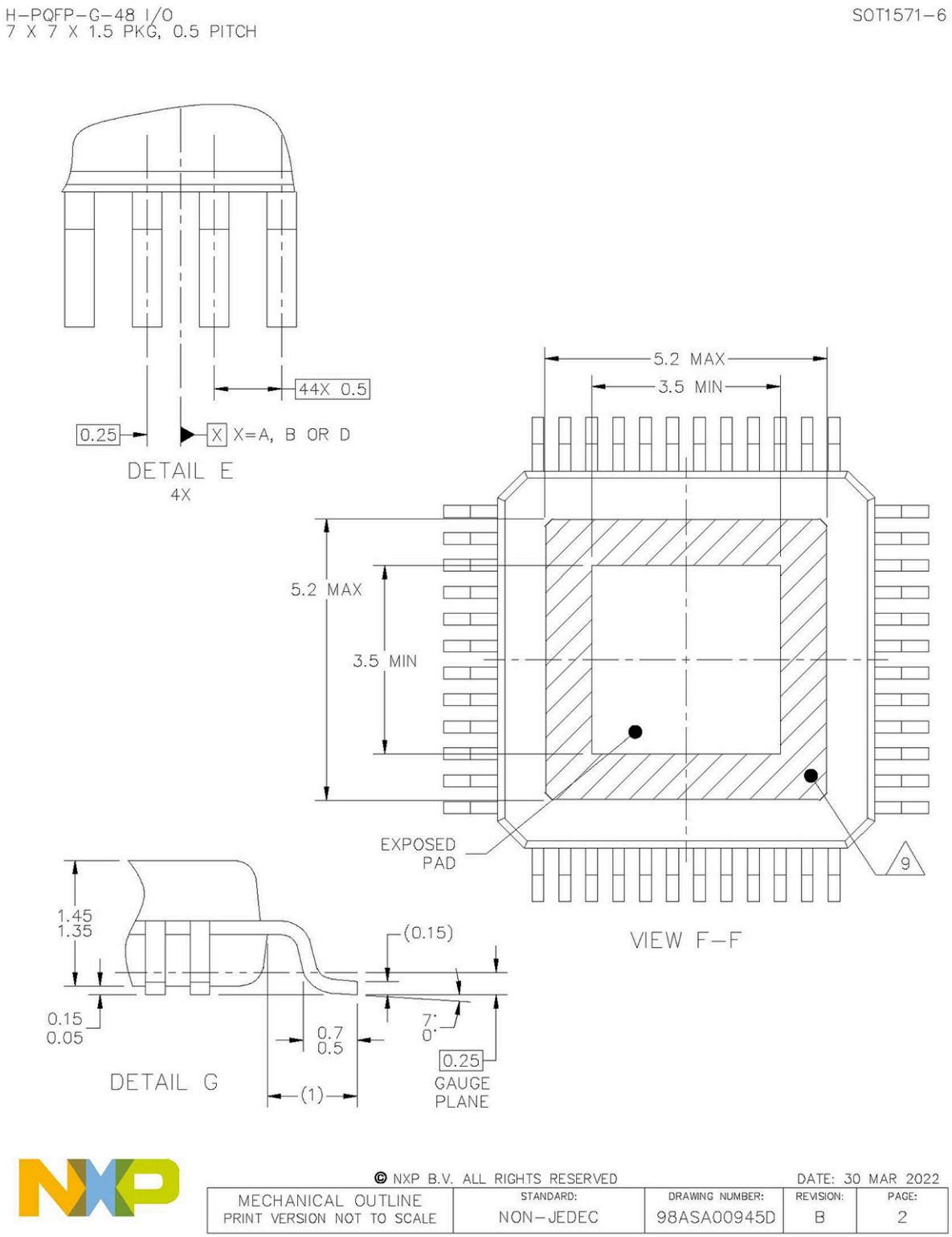


Figure 9. Package outline details (SOT1571-6)

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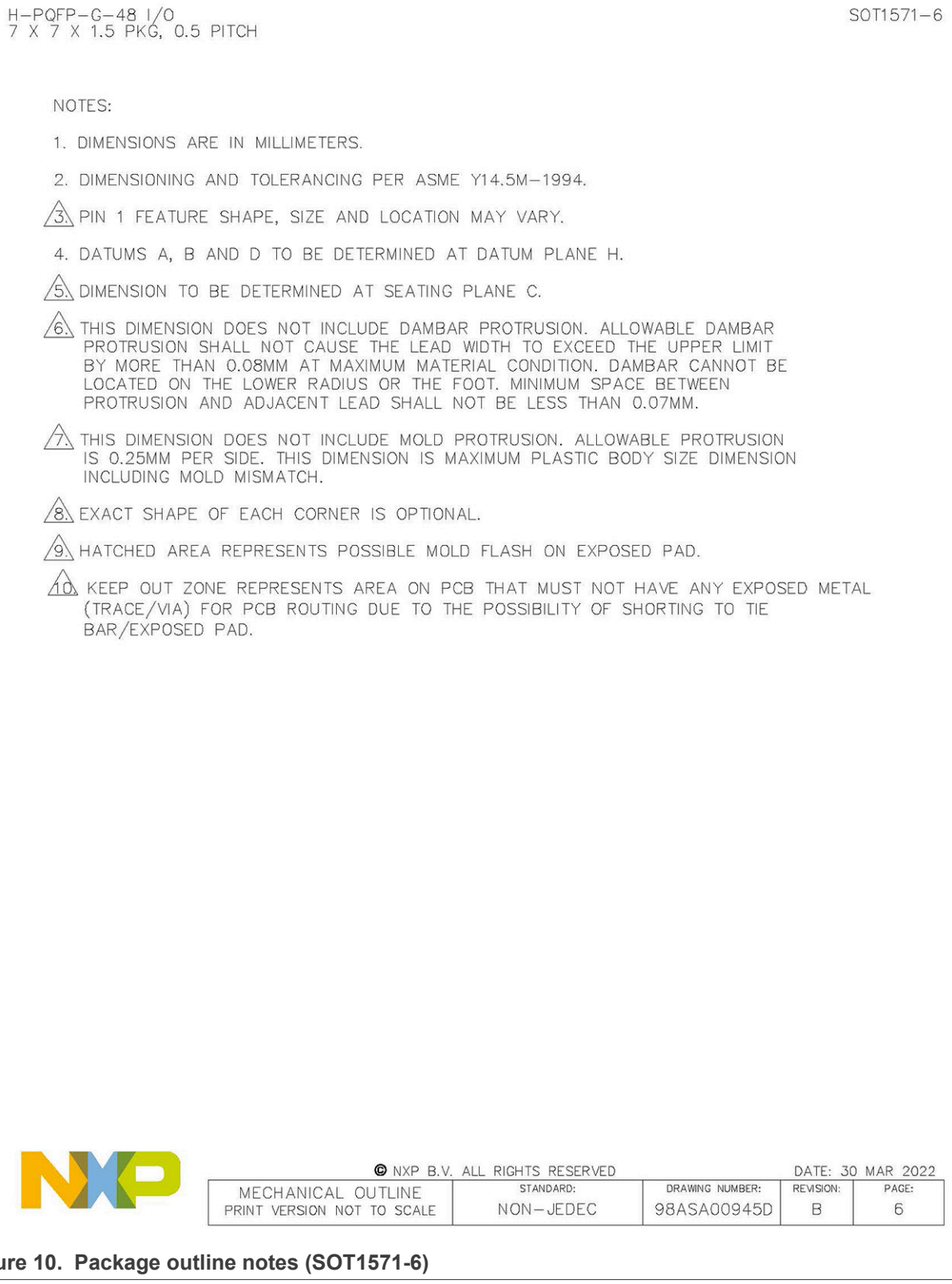


Figure 10. Package outline notes (SOT1571-6)

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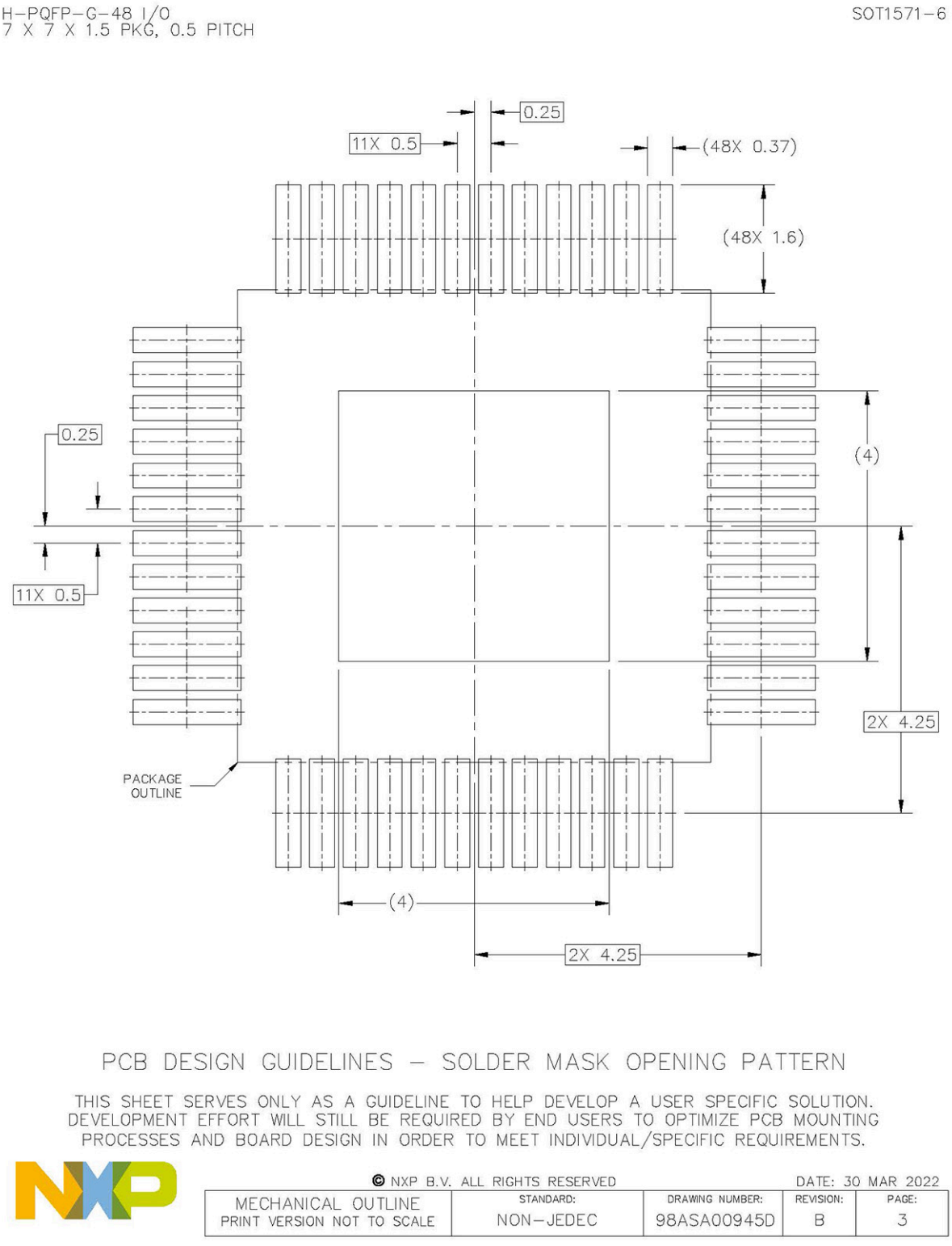


Figure 11. PCB design guidelines - solder mask opening pattern (SOT1571-6)

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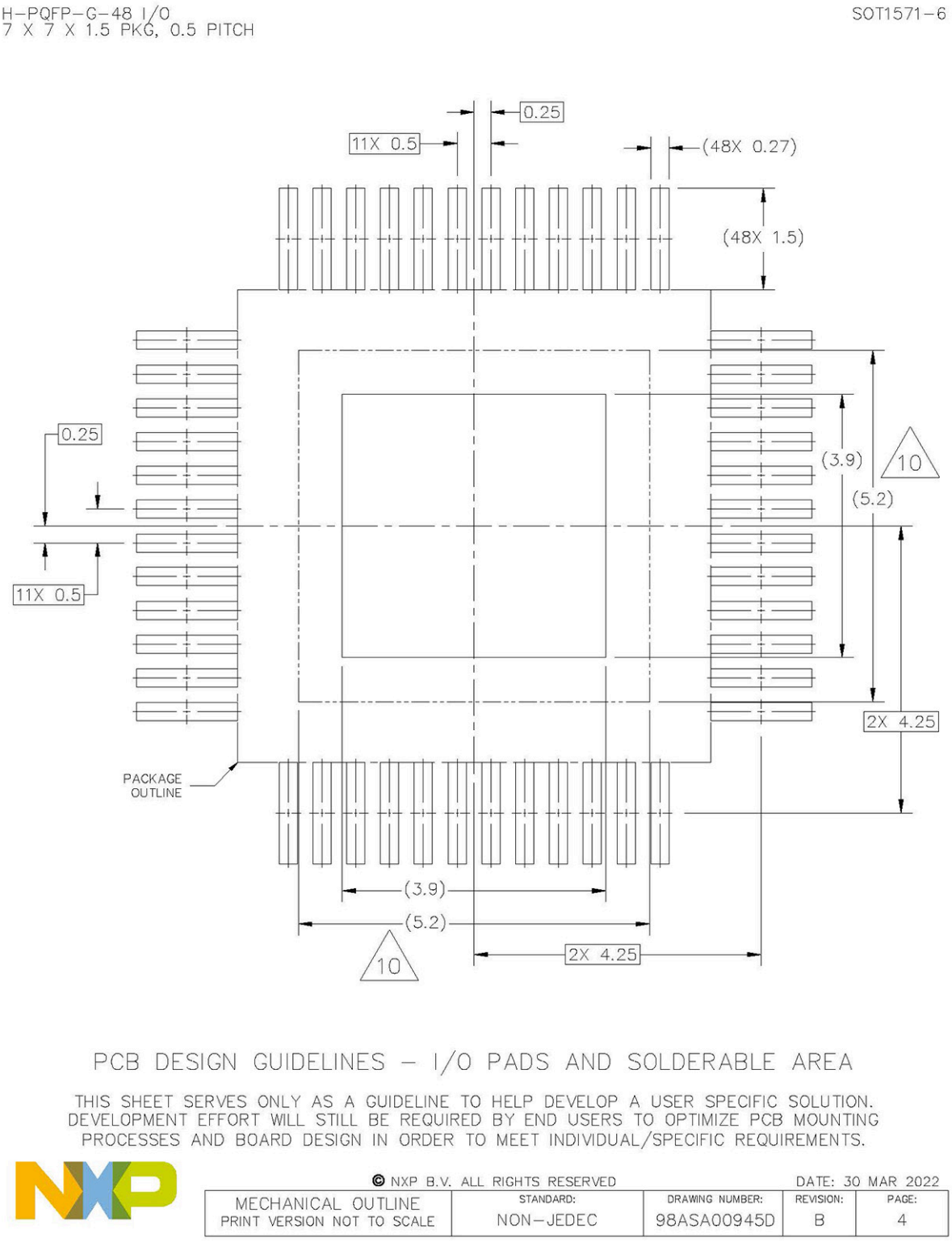


Figure 12. PCB design guidelines - I/O pads and solderable area (SOT1571-6)

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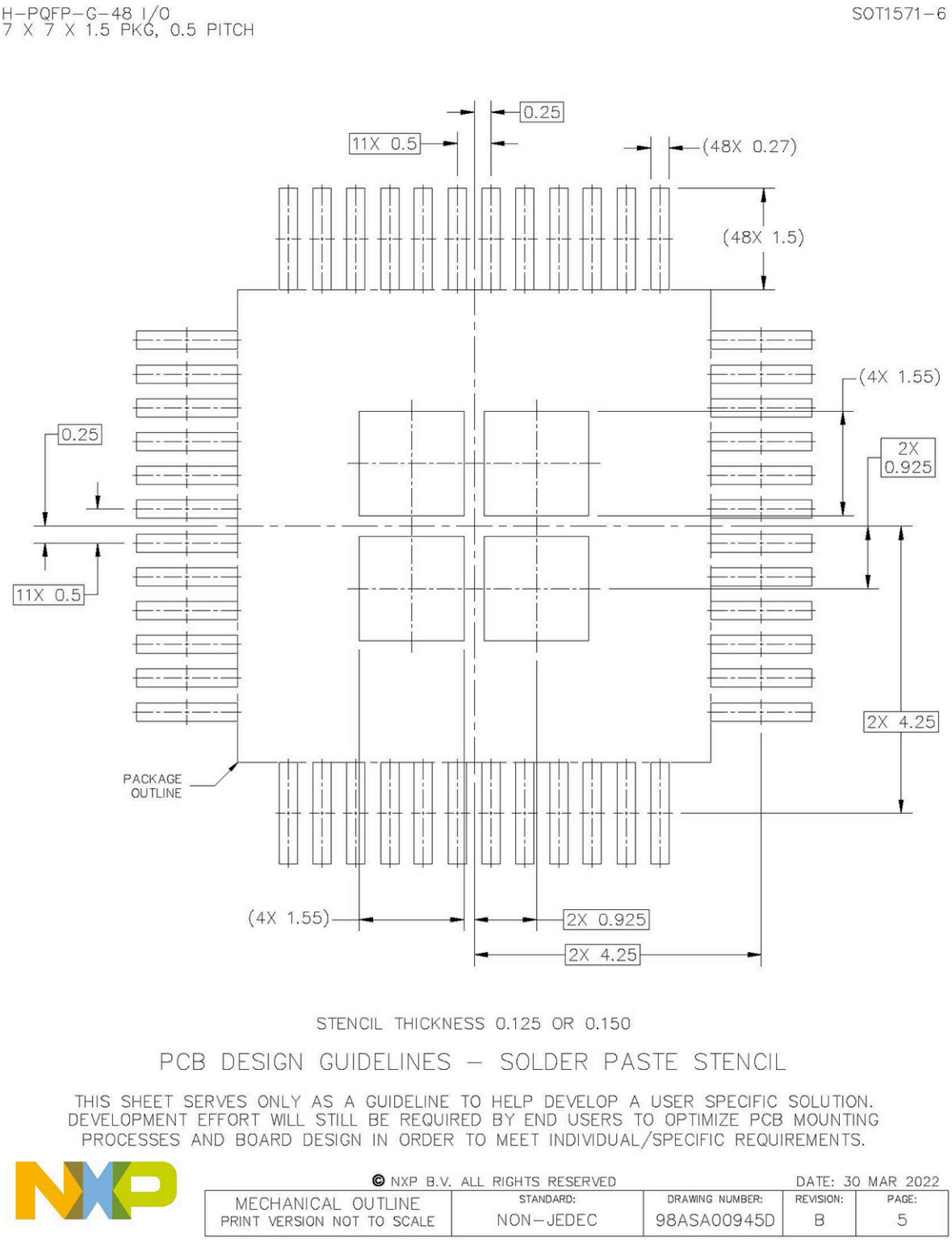


Figure 13. PCB design guidelines - solder paste stencil (SOT1571-6)

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13 References

Table 9. References

Documents, Tools, Enablement	URL
FS26 Functional Safety Manual	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
FS26 Dynamic FMEDA	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
AN12995 - FS26 Product Guidelines	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
FS26_SMPS_Calculator.xls	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
FS26 SMPS Simplis models	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
FS26 Graphical User Interface • To calculate the power dissipation • To create an OTP configuration • To interface an EVB KIT with a computer	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
FS26 Product Overview	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
KITFS26AEEVM: FS26 Evaluation Board	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/fs26-safety-sbc-evaluation-board:KITFS26AEEVM
KITFS26SKTEVM: FS26 Socket Board	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/fs26-safety-sbc-programming-socket-board:KITFS26SKTEVM

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14 Revision history

Revision	Date	Description of changes
4	16 July 2024	• Corrected picture of chip on the front page • Revised Section 3 to match FS26 data sheet • Revised Section 5.2 to removed the sentence below Table 1 • Revised Table 2 and instructions below the table • Revised Figure 4 • Revised Figure 5 • Updated legal information
3	14 March 2023	• Revised Figure *Functional block diagram* • Revised *Features and benefits* • Revised *Applications* • Revised Table *Device segmentation* and Table *Orderable part numbers* • Revised *Simplified application diagram*, including Figure *Example of application diagram (with VBST as a front-end regulator)* and Figure *Example of application diagram (with VBST as a back-end regulator)* • Revised Figure *Block diagram of the FS26* • Revised Table *Pin descriptions* • Revised Table *Maximum ratings* • Revised Table *Thermal resistance (per JEDEC JESD51-2)* • Revised Table *References* • Revised legal information
2	1 June 2022	• Revised *About this document* • Revised *General description* • Revised *Features and benefits* • Revised *Ordering information* including adding subsections *Part number definition* and *Part number list* • Revised *Simplified application diagam* • Revised *Block diagram* • Revised *Pinning* and *Pin descriptions* • Revised *Maximum ratings* • Revised *Electrostatic discharge* • Revised *Thermal ratings* • Revised *Package mechanical dimensions* and *Package outline* • Revised *References* • Revised legal information
1	13 Sept 2021	Initial version

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