PF5024

Power management integrated circuit (PMIC) for high performance applications

Rev. 3.2 — 5 March 2024 Product data sheet

1 Overview

The PF5024 integrates multiple high performance buck regulators. It can operate as a stand-alone point-of-load regulator IC, or as a companion chip to a larger PMIC.

Built-in one-time programmable (OTP) memory stores key startup configurations, drastically reducing external components typically used to set output voltage and sequence of regulators. Regulator parameters are adjustable through high-speed I^2C after start up offering flexibility for different system states.

2 Features

- Four high efficiency buck converters
- Watchdog timer/monitor
- Monitoring circuit to fit ASIL B safety level
- One-time programmable device configuration
- 3.4 MHz I^2C communication interface
- 40-pin QFN package with wettable flank and exposed pad

3 Simplified application diagram

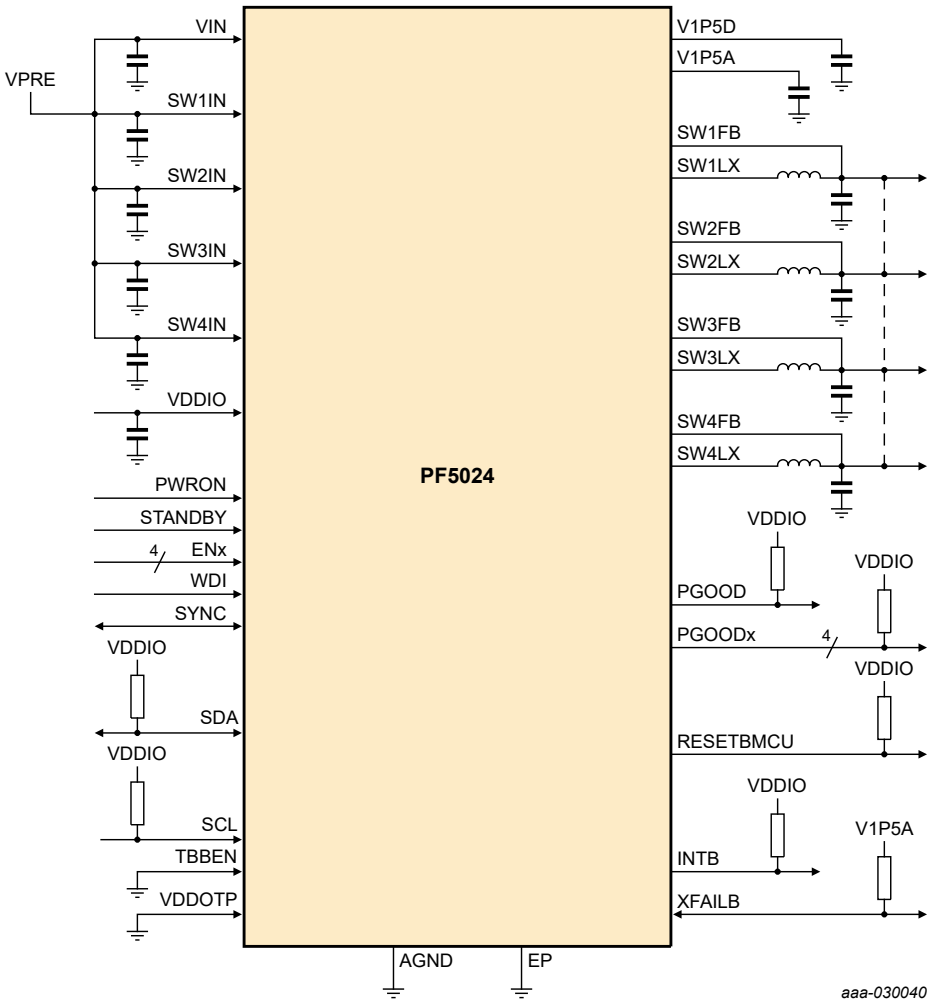

Figure 1. Simplified application diagram

4 Ordering information

Table 1. Ordering information

Type number [1]	Package		
	Name	Description	Version
MPF5024CMBA0ES [2]	HVQFN40	Plastic thermal enhanced very thin quad flat pack; no leads, wettable flank, Dimple cut, 40 terminals, 0.5 mm pitch, 6 mm x 6 mm x 0.9 mm body Temperature grade: 125 °C	SOT618-17(D)
MPF5024CMMA0ES [3]			
MPF5024CVNA0ES [4]		Plastic thermal enhanced very thin quad flat pack; no leads, wettable flank, Dimple cut, 40 terminals, 0.5 mm pitch, 6 mm x 6 mm x 0.9 mm body Temperature grade: 105 °C	

[1] To order parts in tape and reel, add the R2 suffix to the part number.
[2] Automotive part, Safety grade: ASIL B
[3] Automotive part, Safety grade: QM
[4] Industrial part

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OTP emulation and programming performed by the customer is allowed during engineering development using NXP's latest graphical user interface and socketed evaluation board.

Customer is not allowed to perform OTP programming for production purposes. Only NXP or a recommended third party are allowed to program the device for production purposes.

5 Applications

- Automotive Infotainment
- High-end consumer and industrial

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6 Internal block diagram

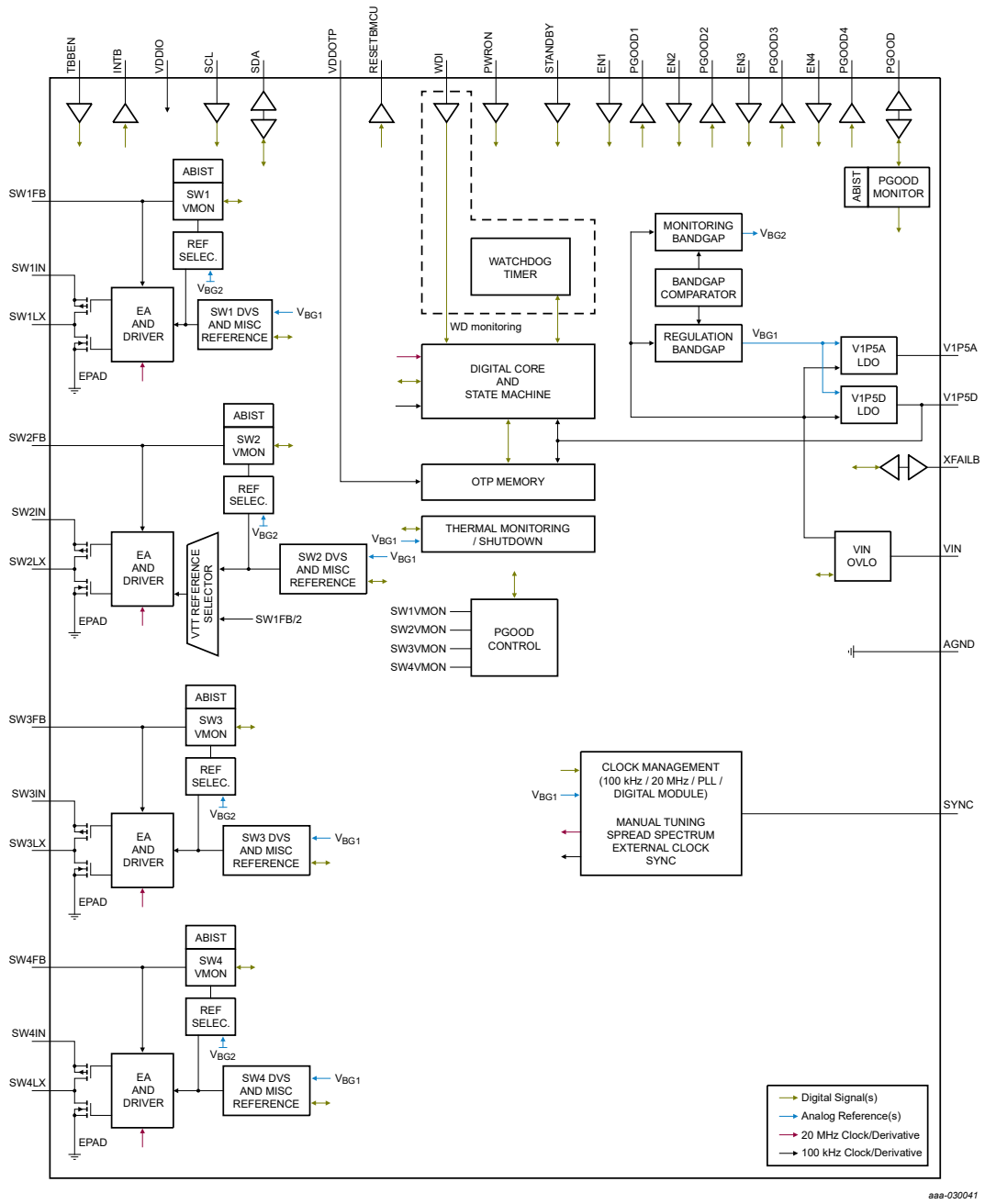

Figure 2. Internal block diagram

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7 Pinning information

7.1 Pinning

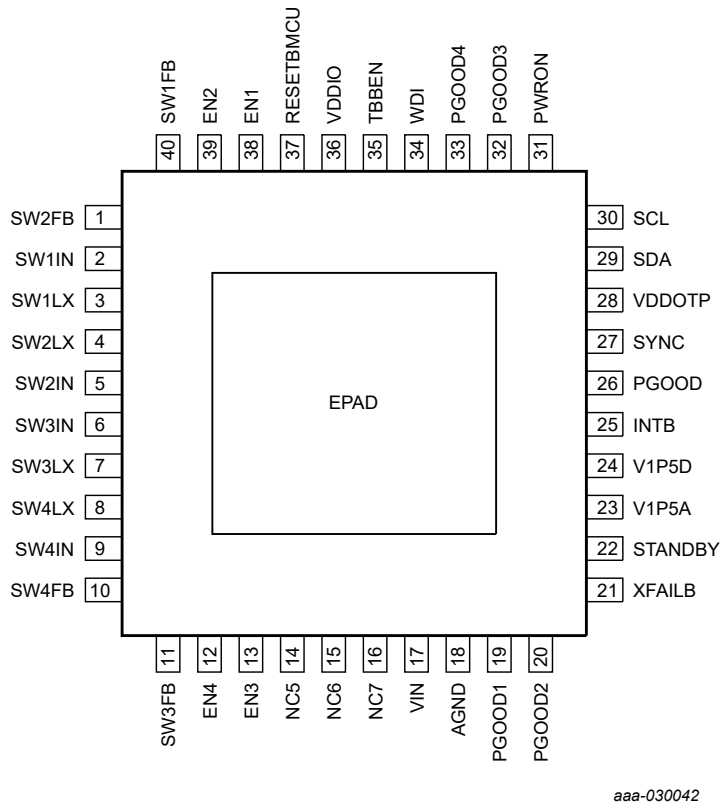

Figure 3. Pin configuration for 40-pin QFN

7.2 Pin description

Table 2. Pin description

QFN pin number	Pin name	Pin description	Min	Max	Units
1	SW2FB	SW2 feedback input	−0.3	6.0	V
2	SW1IN	SW1 input supply	−0.3	6.0	V
3	SW1LX	SW1 switching node	−0.3	6.0	V
4	SW2LX	SW2 switching node	−0.3	6.0	V
5	SW2IN	SW2 input supply	−0.3	6.0	V
6	SW3IN	SW3 input supply	−0.3	6.0	V
7	SW3LX	SW3 switching node	−0.3	6.0	V
8	SW4LX	SW4 switching node	−0.3	6.0	V
9	SW4IN	SW4 input supply	−0.3	6.0	V
10	SW4FB	SW4 feedback input	−0.3	6.0	V
11	SW3FB	SW3 feedback input	−0.3	6.0	V
12	EN4	SW4 enable input	−0.3	6.0	V
13	EN3	SW3 enable input	−0.3	6.0	V
14	NC5	not connected	−0.3	6.0	V

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Table 2. Pin description*...continued*

QFN pin number	Pin name	Pin description	Min	Max	Units
15	NC6	not connected	−0.3	6.0	V
16	NC7	not connected	−0.3	6.0	V
17	VIN	Main input voltage	−0.3	6.0	V
18	AGND	Ground	−0.3	6.0	V
19	PGOOD1	SW1 PGOOD output	−0.3	6.0	V
20	PGOOD2	SW2 PGOOD output	−0.3	6.0	V
21	XFAILB	XFAILB bidirectional IO	−0.3	6.0	V
22	STANDBY	STANDBY input	−0.3	6.0	V
23	V1P5A	1.6 V regulator output or internal analog	−0.3	2.0	V
24	V1P5D	1.6 V regulator output or internal digital	−0.3	2.0	V
25	INTB	Interrupt open-drain output	−0.3	6.0	V
26	PGOOD	Global PGOOD output	−0.3	6.0	V
27	SYNC	External clock input/output for synchronization	−0.3	6.0	V
28	VDDOTP	Power supply for programming block	−0.3	10	V
29	SDA	I^2C SDA	−0.3	6.0	V
30	SCL	I^2C SCL	−0.3	6.0	V
31	PWRON	PWRON input	−0.3	6.0	V
32	PGOOD3	SW3 PGOOD output	−0.3	6.0	V
33	PGOOD4	SW4 PGOOD output	−0.3	6.0	V
34	WDI	External watchdog reset input	−0.3	6.0	V
35	TBBEN	TBBEN mode control input	−0.3	6.0	V
36	VDDIO	I/O supply voltage. Connect to voltage rail at 1.8 V or 3.3 V	−0.3	6.0	V
37	RESETBMCU	RESETBMCU open-drain output	−0.3	6.0	V
38	EN1	SW1 enable input	−0.3	6.0	V
39	EN2	SW2 enable input	−0.3	6.0	V
40	SW1FB	SW1 feedback input	−0.3	6.0	V
	EPAD	Exposed pad. Connect to ground	−0.3	0.3	V

8 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Unit
VIN	Main input supply voltage [1]	−0.3	—	6.0	V
SWxVIN	Regulator input supply voltage [1]	−0.3	—	6.0	V
VDDOTP	OTP programming input supply voltage	−0.3	—	10	V

[1] Pin reliability may be affected if system voltages are above the maximum operating range of 5.5 V for extended period of time. To minimize system reliability impact, system must not operate above 5.5 V for more than 1800 sec over the lifetime of the device.

9 ESD ratings

Table 4. ESD ratings

All ESD specifications are compliant with AEC-Q100 specification.

Symbol	Parameter	Min	Typ	Max	Unit
V_{ESD}	Human body model [1]	—	—	2000	V

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Table 4. ESD ratings*...continued*

All ESD specifications are compliant with AEC-Q100 specification.

Symbol	Parameter	Min	Typ	Max	Unit
V_{ESD}	Charge device model [1] All pins	— —	— —	 500	V
$I_{LATCHUP}$	Latch-up current	—	—	100	mA

[1] ESD testing is performed in accordance with the human body model (HBM) (CZAP = 100 pF, RZAP = 1500 Ω), and the charge device model (CDM), robotic (CZAP = 4.0 pF).

10 Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient operating temperature	−40	—	125	°C
T_J	Junction temperature	−40	—	150	°C
T_{ST}	Storage temperature range	−55	—	150	°C
T_{PPRT}	Peak package reflow temperature	—	—	260	°C

Table 6. QFN40 thermal resistance and package dissipation ratings

Symbol	Parameter	Typ	Unit
$R_{\theta JA}$	Junction to Ambient Thermal Resistance [1] [2] [3] JESD51-7, 2s2p	32.6	°C/W
$R_{\theta JA}$	Junction to Ambient Thermal Resistance [1] [2] [4] JESD51-7, 2s6p	26.8	°C/W
Ψ_{JT}	Junction to Top of Package Thermal Parameter [1] [2] [3] JESD51-7, 2s2p	0.46	°C/W
Ψ_{JT}	Junction to Top of Package Thermal Parameter [1] [2] [4] JESD51-7, 2s6p	0.39	°C/W
Ψ_{JB}	Junction to Board Thermal Parameter [1] [2] [3] JESD51-7, 2s2p	13.9	°C/W
Ψ_{JB}	Junction to Board Thermal Parameter [1] [2] [4] JESD51-7, 2s6p	12.3	°C/W

[1] Determined in accordance to JEDEC JESD51-2A natural convection environment and uniform power.
[2] Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment
[3] Thermal test board meets JEDEC specification for this package (JESD51-7, 2s2p). PCB has a 3×3 array of thermal via under the exposed pad.
[4] 2s6p PCB identical to 51-7 but with four additional internal layers at 35 µm thickness.

11 Operating conditions

Table 7. Operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Main input supply voltage	UVDET	—	5.5	V

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12 General description

12.1 Features

The PF5024 is a power management integrated circuit (PMIC) designed to be the primary power management building block for NXP high-end multimedia application processors from the i.MX 8 and S32V series. It is also capable of providing power solution to the high end i.MX 6 series as well as several non-NXP processors.

- Buck regulators
  - SW1 to SW4: 0.4 V to 1.8 V; 2500 mA
  - Dynamic voltage scaling
  - Configurable as a multiphase regulator
  - VTT termination mode on SW2
  - Programmable current limit
  - Spread-spectrum and manual tuning of switching frequency
- PGOOD output and monitor
  - Global PGOOD output and PGOOD monitor
  - Independent PGOOD output for each regulator
- Independent enable input for each regulator
- Clock synchronization through configurable input/output sync pin
- System features
  - Fast PMIC startup
  - Advanced state machine for seamless processor interface
  - High speed I^2C interface support (up to 3.4 MHz)
  - User programmable Standby and Off modes
  - Programmable soft start sequence and power down sequence
  - Programmable regulator configuration
- OTP (One-time programmable) memory for device configuration
- Monitoring circuit to fit ASIL B safety level
  - Independent voltage monitoring with programmable fault protection
  - Advance thermal monitoring and protection
  - External watchdog monitoring and programmable internal watchdog counter
  - I^2C CRC and write protection mechanism
  - Analog built-in self-test (ABIST)

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12.2 Functional block diagram

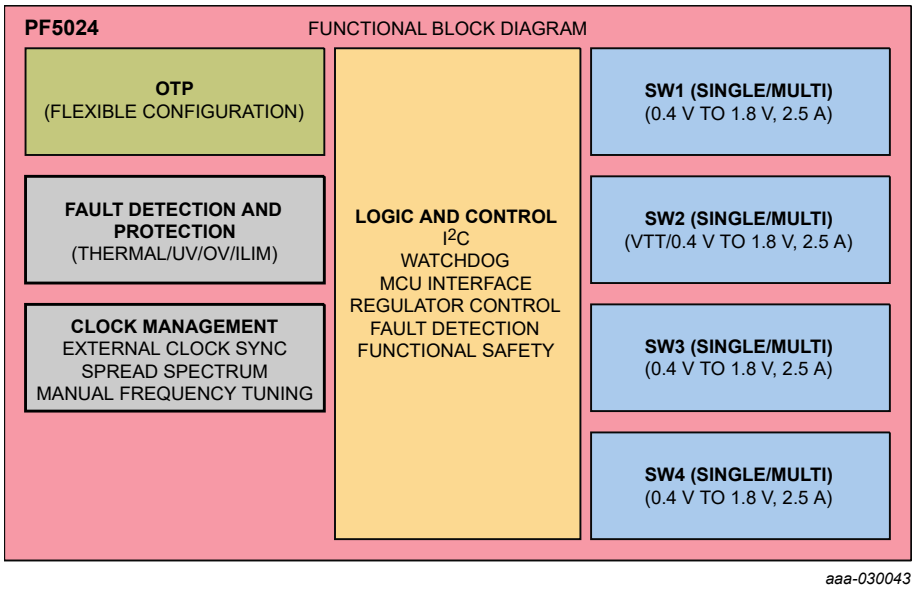

Figure 4. Functional block diagram

12.3 Power tree summary

The following table provides a summary of the voltage regulators in the PF5024.

Table 8. Voltage supply summary

Regulator	Type	Input supply	Regulated output range (V)	VOUT programmable step (mV)	IRATED (mA)
SW1	Buck	SW1IN	0.4 V to 1.8 V	6.25	2500
SW2	Buck	SW2IN	VTT/0.4 V to 1.8 V	6.25	2500
SW3	Buck	SW3IN	0.4 V to 1.8 V	6.25	2500
SW4	Buck	SW4IN	0.4 V to 1.8 V	6.25	2500

12.4 Device differences

Table 9. Device differences

Description	PF5024 non-safety	PF5024 ASIL B	Bits not available on PF5024 non-safety
During the self-test, the device checks: • The high speed oscillator circuit is operating within a maximum of 15 % tolerance • A CRC is performed on the mirror registers during the self-test routine to ensure the integrity of the registers before powering up • The output of both the voltage generation bandgap and the monitoring bandgap are not more than 5 % to 12 % apart from each other • ABIST test on all voltage monitors and toggling signals	Not available	Available	AB_SWx_OV AB_SWx_UV STEST_NOK AB_RUN

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Table 9. Device differences*...continued*

Description	PF5024 non-safety	PF5024 ASIL B	Bits not available on PF5024 non-safety
Fail-safe state: to lock down the system in case of critical failures cycling the PMIC ON/OFF.	Not available	Available	FS_CNT[3:0] OTP_FS_BYPASS OTP_FS_MAX_CNT[3:0] OTP_FS_OK_TIMER[2:0]
Secure I^2C write: I^2C write procedure to modify registers dedicated to safety features (I^2C CRC is still available).	Not available	Available	I2C_SECURE_EN OTP_I2C_SECURE _EN (always 0) RANDOM_GEN[7:0] RANDOM_CHK[7:0]

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13 State machine

The PF5024 features a state of the art state machine for seamless processor interface. The state machine handles the IC start up, provides fault monitoring and reporting, and protects the IC and the system during fault conditions.

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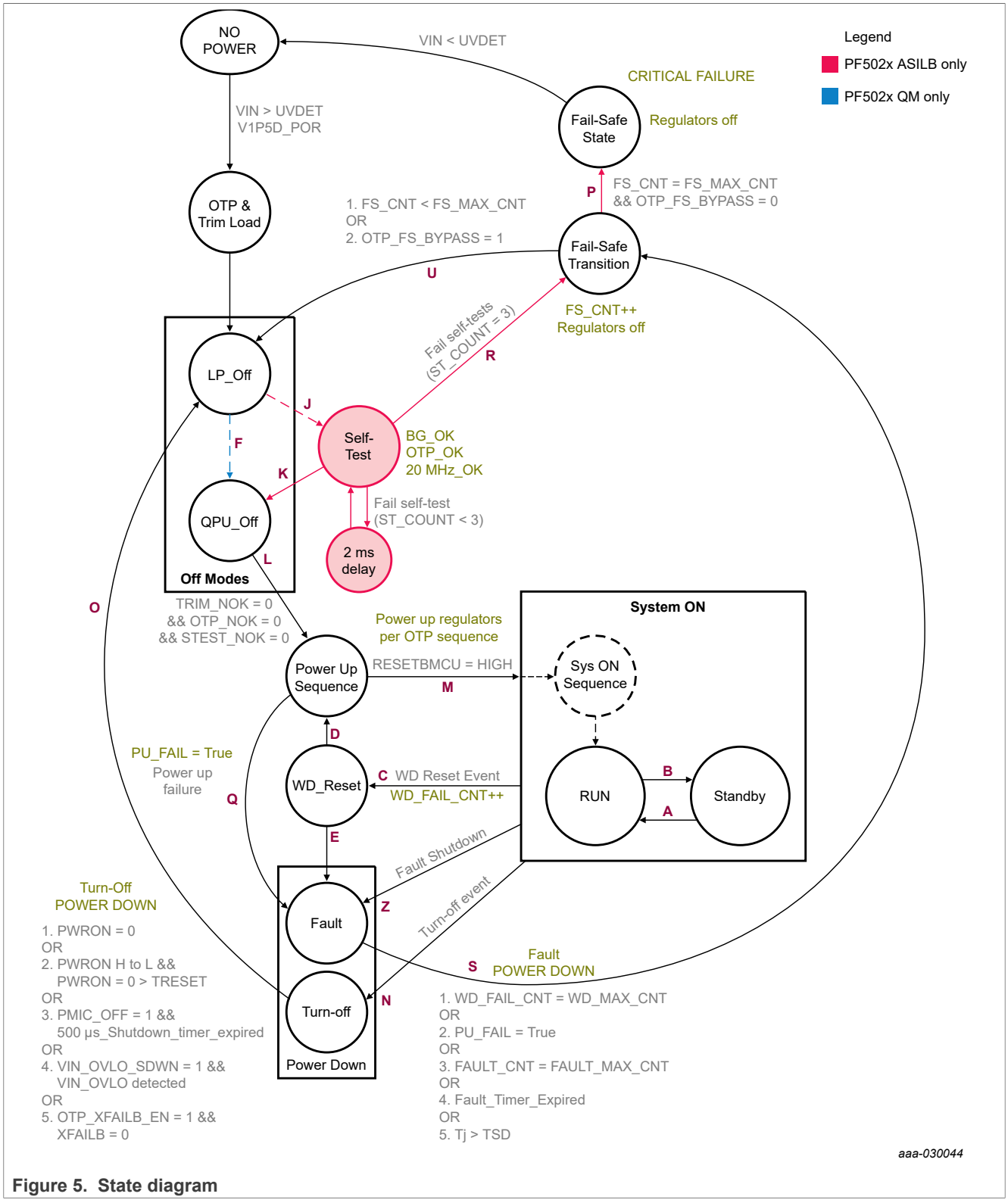

Figure 5. State diagram

Table 10 lists the conditions for the different state machine transitions.

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Table 10. State machine transition definition

Symbol	Description	Conditions
Transition A	Standby to run	1. (STANDBY = 0 && STANDBYINV bit = 0)
		2. (STANDBY = 1 && STANDBYINV bit = 1)
Transition B	Run to standby	1. (STANDBY = 1 && STANDBYINV bit = 0)
		2. (STANDBY = 0 && STANDBYINV bit = 1)
Transition C	System on to WD reset	1. Hard WD Reset event
Transition D	WD reset to system ON	1. 30 µs delay passed && WD_EVENT_CNT < WD_MAX_CNT
Transition E	WD reset to power down (fault)	1. WD_EVENT_CNT = WD_MAX_CNT
Transition J	LP_Off to self-test **(PF5024 ASIL B only)**	Transitory off state: device pass through LP_Off to self-test to QPU_Off (no power up event present) 1. LPM_OFF = 1 && TBBEN = Low
		Power up event from LP_Off state 2. LPM_OFF = 0 && TBBEN = Low && (PWRON = 1 && OTP_PWRON_MODE = 0) && UVDET< VIN < VIN_OVLO (or VIN_OVLO disabled) && T_J < TSD && TRIM_NOK = 0 && OTP_NOK = 0
		Power up event from LP_Off state 3. LPM_OFF = 0 && TBBEN = Low && (PWRON H to L && OTP_PWRON_MODE = 1 && UVDET < VIN < VIN_OVLO (or VIN_OVLO disabled) && T_J < TSD && TRIM_NOK = 0 && OTP_NOK = 0
		Conditions: Transitory OFF state to go into TBB mode. Device pass through LP_Off to self-test to QPU_Off (no power up event present) 4. TBBEN = high (V1P5D)
Transition K	Self-test to QPU_Off **(PF5024 ASIL B only)**	1. Pass self-tests
		2. TBBEN = high (V1P5D)
Transition F	LP_Off to QPU_Off **(PF5024 QM only)**	Transitory OFF state: device pass through LP_Off to QPU_Off (no power up event present) 1. LPM_OFF = 1 && TBBEN = Low
		Power up event from LP_Off state 2. LPM_OFF = 0 && TBBEN = Low && (PWRON = 1 && OTP_PWRON_MODE = 0) && UVDET< VIN < VIN_OVLO (or VIN_OVLO disabled) && T_J < TSD && TRIM_NOK = 0 && OTP_NOK = 0
		Power up event from LP_Off state 3. LPM_OFF =0 && TBBEN = Low && (PWRON H to L && OTP_PWRON_MODE = 1) && UVDET < VIN < VIN_OVLO (or VIN_OVLO disabled) && T_J < TSD&& TRIM_NOK = 0 && OTP_NOK = 0
		Transitory OFF state: device pass through LP_Off to QPU_Off (no power up event present) 4. TBBEN = High (V1P5D)

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Table 10. State machine transition definition*...continued*

Symbol	Description	Conditions
		Transitory QPU_Off state, power on event occurs from LP_Off state, after self-test is passed, QPU_Off is just a transitory state until power up sequence starts. 1. LPM_OFF = 0 && TBBEN = Low && TRIM_NOK = 0 && OTP_NOK = 0 && STEST_NOK = 0 && OTP_XFAILB_EN = 0
		Power up event from QPU_Off state 2. LPM_OFF = 0 && TBBEN = Low && TRIM_NOK = 0 && OTP_NOK = 0 && STEST_NOK = 0 && OTP_XFAILB_EN = 0
		Power up event from QPU_Off state 3. LPM_OFF = 1 && (PWRON = 1 && OTP_PWRON_MODE = 0) && UVDET < VIN < VIN_OVLO (or VIN_OVLO disabled) && $T_J < T_{SD}$ && TRIM_NOK = 0 && OTP_NOK = 0 && STEST_NOK=0 && OTP_XFAILB_EN = 0
		Power up event from QPU_Off state 4. LPM_OFF = 1 && (PWRON = 1 && OTP_PWRON_MODE = 0) && UVDET < VIN < VIN_OVLO (or VIN_OVLO disabled) && $T_J < T_{SD}$ && TRIM_NOK = 0 && OTP_NOK = 0 && STEST_NOK = 0 && OTP_XFAILB_EN=1 && XFAILB = 1
Transition L	QPU_Off to power up	Power up event from QPU_Off state 5. LPM_OFF = 1 && (PWRON H to L && OTP_PWRON_MODE = 1) && UVDET < VIN < VIN_OVLO (or VIN_OVLO disabled) && $T_J < T_{SD}$ && TRIM_NOK = 0 && OTP_NOK = 0 && STEST_NOK = 0 && OTP_XFAILB_EN = 0
		Power up event from QPU_Off state 6. LPM_OFF = 1 && (PWRON H to L && OTP_PWRON_MODE = 1) && UVDET < VIN < VIN_OVLO (or VIN_OVLO disabled) && TRIM_NOK = 0 && OTP_NOK = 0 && STEST_NOK = 0 && OTP_XFAILB_EN = 1 && XFAILB = 1
		Power up event from QPU_Off state 7. TBBEN = High && (PWRON = 1 && OTP_PWRON_MODE = 0) && UVDET < VIN < VIN_OVLO (or VIN_OVLO disabled) && $T_J < T_{SD}$ && TRIM_NOK = 0 && OTP_NOK = 0 && STEST_NOK = 0 && OTP_XFAILB_EN = 0
		Power up event from QPU_Off state 8. TBBEN = High && (PWRON = 1 && OTP_PWRON_MODE = 0) && UVDET < VIN < VIN_OVLO (or VIN_OVLO disabled) && $T_J < T_{SD}$ && TRIM_NOK = 0 && OTP_NOK = 0 && STEST_NOK = 0 && OTP_XFAILB_EN = 1 && XFAILB = 1

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Table 10. State machine transition definition*...continued*

Symbol	Description	Conditions
		Power up event from QPU_Off state 9. TBBEN = High && (PWRON H to L && OTP_PWRON_MODE = 1) && UVDET < VIN < VIN_OVLO (or VIN_OVLO disabled) && $T_J < T_{SD}$ && TRIM_NOK = 0 && OTP_NOK = 0 && STEST_NOK = 0 && OTP_XFAILB_EN = 0
		Power up event from QPU_Off state 10. TBBEN = High && (PWRON H to L && OTP_PWRON_MODE = 1) && UVDET < VIN < VIN_OVLO (or VIN_OVLO disabled) && $T_J < T_{SD}$ && TRIM_NOK = 0 && OTP_NOK = 0 && STEST_NOK = 0 && OTP_XFAILB_EN = 1 && XFAILB = 1
Transition M	Power up sequence to system ON	1. RESETBMCU is released as part of the power up sequence
Transition N	System ON to power down (turn off)	Requested turn off event 1. OTP_PWRON_MODE = 0 && PWRON = 0
		Requested turn off event 2. OTP_PWRON_MODE = 1 && (PWRON H to L && PWRON = low for t > TRESET)
		Requested turn off event 3. PMIC_OFF = 1 && 500µs_Shutdown_Timer_Expired
		Protective turn off event (no PMIC fault) 4. VIN_OVLO_SDWN = 1 && VIN_OVLO detected for longer than VIN_OVLO_DBNC time
		External turn off event 5. OTP_XFAILB_EN = 1 && XFAILB = 0
Transition Z	System ON to power down (fault)	Turn off event due to PMIC fault 1. Fault Timer expired
		Turn off event due to PMIC fault 2. FAULT_CNT = FAULT_MAX_CNT
		Turn off event due to PMIC fault 3. Thermal shutdown T_J > TSD
Transition O	Power down (turn off) to LP_Off	Requested turn off event moves directly to LP_Off 1. Power down sequences finished
Transition Q	Power up to power down (fault)	Power up failure 1. Failure during power up sequence
Transition R	Self-test to fail-safe transition	1. Self-tests fail 3 times && TBBEN = low
Transition S	Power down (fault) to fail-safe transition	Turn off event due to a fault condition moves to fail-safe transition 1. Power down sequence is finished
Transition U	Fail-safe transition to LP_Off	1. FS_CNT < FS_MAX_CNT
		2. OTP_FS_BYPASS = 1
Transition P	Fail-safe transition to fail-safe state **(PF5024 ASIL B only)**	1. FS_CNT = FS_MAX_CNT && OTP_FS_BYPASS = 0

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13.1 State descriptions

13.1.1 OTP/TRIM load

Upon VIN application, the V1P5D and V1P5A regulators are turned on automatically. Once the V1P5D and V1P5A cross their respective POR thresholds, the fuses (for trim and OTP) are loaded into the mirror registers and into the functional I^2C registers if configured by the voltage on the VDDOTP pin.

The fuse circuits have a CRC error check routine which reports and protects against register loading errors on the mirror registers. If a register loading error is detected, the corresponding TRIM_NOK or OTP_NOK flag is asserted. See Section 17 "OTP/TBB and hardwire default configurations" for details on handling fuse load errors.

If no fuse load errors are present, the state machine moves to the LP_off state.

13.1.2 LP_Off state

The LP_Off state is a low power off mode selectable by the LPM_OFF bit during the system On mode. By default, the LPM_OFF = 0 when VIN crosses the UVDET threshold, therefore the state machine stops at the LP_Off state until a valid power up event is present. When LPM_OFF = 1, the state machine transitions automatically to the QPU_Off state if no power up event has been present and waits in the QPU_Off until a valid power up event is present.

The selection of the LPM_OFF bit is based on whether prioritizing low quiescent current (stay in the LP_Off state) or quick power up (move to the QPU_Off state).

If a power up event is started in LP_Off state with LPM_OFF = 0 and a fuse loading error is detected, the PF5024 ignores the power up event and remains in the LP_Off state to avoid any potential damage to the system.

13.1.3 Self-test routine (PF5024 ASIL B only)

When the device transitions from the LP_Off state, it turns on all necessary internal circuits as it moves into the self-test routine and performs a self-check routine to verify the integrity of the internal circuits.

During the self-test routine the following blocks are verified:

- The high speed clock circuit is operating within a maximum of 15 % tolerance
- The output of both the voltage generation bandgap and the monitoring bandgap are not more than 5 % to 12 % apart from each other
- A CRC is performed on the mirror registers during the self-test routine, to ensure the integrity of the registers before powering up
- ABIST test on all voltage monitors.

To allow for varying settling times for the internal bandgap and clocks, the self-test block is executed up to three times (with 2.0 ms between each test) if a failure is encountered, the state machine proceeds to the fail-safe transition.

A failure in the ABIST test is not interpreted as a self-test failure and it only sets the corresponding ABIST flag for system information. The MCU is responsible for reading the information and deciding whether it can continue with a safe operation. See Section 18.1 "System safety strategy" for the functional safety strategy of PF5024.

Upon a successful self-test, the state machine proceeds to the QPU_Off state.

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13.1.4 QPU_Off state

The QPU_Off state is a higher power consumption Off mode, in which all internal circuitry required for a power on is biased and ready to start a power up sequence.

If LPM_OFF = 1 and no turn on event is present, the device stops at the QPU_Off state, and waits until a valid turn on event is present.

In this state, if VDDIO supply is provided externally, the device is able to communicate through I^2C to access and modify the mirror registers in order to operate the device in TBB mode or to program the OTP registers as described in Section 17 "OTP/TBB and hardwire default configurations".

If a power up event is started and any of the TRIM_NOK, OTP_NOK or STEST_NOK flags are asserted, the device ignores the power up event and remains in the QPU_Off state. See Section 17 "OTP/TBB and hardwire default configurations" for debugging a fuse loading failure.

Upon a power up event, the default configuration from OTP or hardwire is loaded into their corresponding I^2C functional register in the transition from QPU_Off to power up state.

13.1.5 Power up sequence

During the power up sequence, the external regulators are turned on in a predefined order as programmed by the default (OTP or hardwire) sequence.

The RESETBMCU is also programmed as part of the power up sequence, and it is used as the condition to enter the system On state. The RESETBMCU may be released in the middle of the power up sequence, in this case, the remaining supplies in the power up continues to power up as the device is in the run state. See Section 14.5.2 "Power up sequencing" for details.

13.1.6 System On state

During the system On state, the MCU is powered and out of reset and the system is fully operational.

The system On is a virtual state composed by two modes of operations:

- Run state
- Standby state

Register to control the regulators output voltage, regulator enable, interrupt masks, and other miscellaneous functions can be written to or read from the functional I^2C register map during the system On state.

13.1.6.1 Run state

If the power up state is successfully completed, the state machine transitions to the run state. In this state, RESETBMCU is released high, and the MCU is expected to boot up and set up specific registers on the PMIC as required during the system boot up process.

The Run mode is intended to be used as the normal mode of operation for the system.

Each regulator has specific registers to control its output voltage, operation mode and/or enable/disable state during the run state.

By default, the VSWx_RUN[7:0] register is loaded with the data stored in the OTP_VSWx[7:0] bit.

Upon power up, if the switching regulator is part of the power up sequence, the SWx_RUN_MODE[1:0] bits will be loaded as needed by the system:

- When OTP_SYNC_MODE = 1, default SWx_RUN_MODE at power up is always set to PWM (0b01)
- When OTP_SYNC_MODE = 0 and OTP_SYNCOUT_EN = 1, default SWx_RUN_MODE at power up is always set to PWM (0b01)

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- When OTP_FSS_EN = 1, default SWx_RUN_MODE at power up shall always set to PWM (0b01)
- If none of the above conditions are met, the default value of the SWx_RUN_MODE bits at power up will be set by the OTP_SW_MODE bits.

When OTP_SW_MODE = 0, the default value of the SWx_RUN_MODE bits are set to 0b11 (autoskip).

When OTP_SW_MODE = 1, the default value of the SWx_RUN_MODE bits are set to 0b01 (PWM).

If the switching regulator is not part of the power up sequence, the SWx_RUN_MODE[1:0] bits are loaded with 0b00 (Off mode).

In a typical system, each time the processor boots up (PMIC transitions from Off mode to run state), all output voltage configurations are reset to the default OTP configuration, and the MCU should configure the PMIC to its desired usage in the application.

13.1.6.2 Standby state

The standby state is intended to be used as a low power (state retention) mode of operation. In this state, the voltage regulators can be preset to a specific low power configuration in order to reduce the power consumption during system's sleep or state retention modes of operations.

The standby state is entered when the STANDBY pin is pulled high or low as defined by the STANBYINV bit. The STANDBY pin is pulled high/low by the MCU to enter/exit system low power mode. See Section 14.9.2 "STANDBY" for detailed configuration of the STANDBY pin.

Each regulator has specific registers to control its output voltage, operation mode and/or enable/disable state during the standby state.

By default, the VSWx_STBY[7:0] register is loaded with the data stored in the OTP_VSWx[7:0] bit.

Upon power up, if the switching regulator is part of the power up sequence, the SWx_STBY_MODE[1:0] bits will be loaded as needed by the system:

- When OTP_SYNC_MODE = 1, default SWx_STBY_MODE at power up is always set to PWM (0b01)
- When OTP_SYNC_MODE = 0 and OTP_SYNCOUT_EN = 1, default SWx_STBY_MODE at power up is always set to PWM (0b01)
- When OTP_FSS_EN = 1, default SWx_STBY_MODE at power up shall always set to PWM (0b01)
- If none of the above conditions are met, the default value of the SWx_STBY_MODE bits at power up will be set by the OTP_SW_MODE bits.

When OTP_SW_MODE = 0, the default value of the SWx_STBY_MODE bits are set to 0b11 (autoskip).

When OTP_SW_MODE = 1, the default value of the SWx_STBY_MODE bits are set to 0b01 (PWM).

If the switching regulator is not part of the power up sequence, the SWx_STBY_MODE[1:0] bits are loaded with 0b00 (Off mode).

Upon power up, the standby registers are loaded with the same default OTP values as the run mode. The MCU is expected to program the desired standby values during boot up.

If any of the external regulators are disabled in the standby state, the power down sequencer is engaged as described in Section 14.6.2 "Power down sequencing".

13.1.7 WD_Reset

When a hard watchdog reset is present, the state machine increments the WD_EVENT_CNT[3:0] register and compares against the WD_MAX_CNT[3:0] register. If WD_EVENT_CNT[3:0] = WD_MAX_CNT[3:0], the state machine detects a cyclic watchdog failure, it powers down the external regulators and proceeds to the fail-safe transition.

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If WD_EVENT_CNT[3:0] < WD_MAX_CNT[3:0], the state machine performs a hard WD reset.

A hard WD reset can be generated from either a transition in the WDI pin or a WD event initiated by the internal watchdog counter as described in Section 15.7.2 "Watchdog reset behaviors".

13.1.8 Power down state

During power down state, all regulators are disabled as configured in the power down sequence. The power down sequence is programmable as defined in Section 14.6.2 "Power down sequencing".

Two types of events may lead to the power down sequence:

- Non faulty turn off events: move directly into LP_Off state as soon as power down sequence is finalized.
- Turn off events due to a PMIC fault: move to the fail-safe transition as soon as the power down sequence is finalized.

13.1.9 Fail-safe transition

The fail-safe transition is entered if the PF5024 initiates a turn off event due to a PMIC fault.

If the fail-safe transition is entered, the PF5024 provides four FAIL bits to indicate the source of the failure:

- The PU_FAIL is set to 1 when the device shuts down due to a power up failure
- The WD_FAIL is set to 1 when the device shuts down due to a watchdog event counter max out
- The REG_FAIL is set to 1 when the device shuts down due to a regulator failure (fault counter maxed out or fault timer expired)
- The TSD_FAIL is set to 1 when the device shuts down due to a thermal shutdown

The value of the FAIL bits is retained as long as VIN > UVDET.

The MCU can read the FAIL bits during the system On state in order to obtain information about the previous failure and can clear them by writing a 1 to them, provided the state machine is able to power up successfully after such failure.

In the PF5024, when the state machine enters the fail-safe transition, a fail-safe counter is compared and increased, if the FS_CNT[3:0] reaches the maximum count, the device can be programmed to move directly to the fail-safe state to prevent a cyclic failure from happening.

13.1.10 Fail-safe state (PF5024 ASIL B only)

The fail-safe state works as a safety lock-down upon a critical device/system failure. It is reached when the FS_CNT [3:0] = FS_MAX_CNT [3:0].

A bit is provided to enable or disable the device to enter the fail-safe state upon a cyclic failure. When the OTP_FS_BYPASS = 1, the fail-safe bypass operation is enabled and the device always move to the LP_Off state, regardless of the value of the FS_CNT[3:0]. If the OTP_FS_BYPASS = 0, the fail-safe bypass is disabled, and the device moves to the fail-safe state when the proper condition is met.

The maximum number of times the device can pass through the fail-safe transition continuously prior to moving to a fail state is programmed by the OTP_FS_MAX_CNT[3:0] bits. If the FS_MAX_CNT[3:0] = 0x00, the device moves into the fail-safe state as soon as it fails for the very first time.

The device can exit the fail-safe state only after a power cycle (VIN crossing UVDET) event is present.

To avoid reaching the fail-safe state due to isolated fail-safe transition events, the FS_CNT [3:0] is gradually decreased based on a fail-safe OK timer. The OTP_FS_OK_TIME[2:0] bits select the default time configuration for the fail-safe OK timer between 1 to 60 min.

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Table 11. Fail-safe OK timer configuration

OTP_FS_OK_TIME[2:0]	FS_CNT decrease period (min)
000	1
001	5
010	10
011	15
100	20
101	30
110	45
111	60

When the fail-safe OK timer reaches the configured time during the system On state, the state machine decreases the FS_CNT[3:0] bits by one and starts a new count until the FS_CNT[3:0] is 0x00. The FS_CNT[3:0] may be manually cleared during the system on state if the system wants to control this counter manually.

14 General device operation

14.1 UVDET

UVDET works as the main operation threshold for the PF5024. Crossing UVDET on the rising edge is a mandatory condition for OTP fuses to be loaded into the mirror registers and allows the main PF5024 operation.

If VIN is below the UVDET threshold, the device remains in an unpowered state. A 200 mV hysteresis is implemented on the UVDET comparator to set the falling threshold.

Table 12. UVDET threshold

Symbol	Parameter	Min	Typ	Max	Unit
UVDET	Rising UVDET	2.7	2.8	2.9	V
UVDET	Falling UVDET	2.5	2.6	2.7	V

14.2 VIN OVLO condition

The VIN_OVLO circuit monitors the main input supply of the PF5024. When this block is enabled, the PF5024 monitors its input voltage and can be programmed to react to an overvoltage in two ways:

- When the VIN_OVLO_SDWN = 0, the VIN_OVLO event triggers an OVLO interrupt but does not turn off the device
- When the VIN_OVLO_SDWN = 1, the VIN_OVLO event initiates a power down sequence

When the VIN_OVLO_EN = 0, the OVLO monitor is disabled and when the VIN_OVLO_EN = 1, the OVLO monitor is enabled. The default configuration of the VIN_OVLO_EN bit is set by the OTP_VIN_OVLO_EN bit in OTP. Likewise, the default value of the VIN_OVLO_SDWN bit is set by the OTP_VIN_OVLO_SDWN upon power up.

During a power up transition, if the OTP_VIN_OVLO_SDWN = 0 the device allows the external regulators to come up and the PF5024 announces the VIN_OVLO condition through an interrupt. If the OTP_VIN_OVLO_SDWN = 1, the device stops the power up sequence and returns to the corresponding Off mode.

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Debounce on the VIN_OVLO comparator is programmable to 10 µs, 100 µs or 1.0 ms, by the VIN_OVLO_DBNC[1:0] bits. The default value for the VIN_OVLO debounce is set by the OTP_VIN_OVLO_DBNC[1:0] bits upon power up.

Table 13. VIN_OVLO debounce configuration

VIN_OVLO_DBNC[1:0]	VIN OVLO debounce value (µs)
00	10
01	100
10	1000
11	Reserved

Table 14. VIN_OVLO specifications

Symbol	Parameter	Min	Typ	Max	Unit
VIN_OVLO	VIN overvoltage lockout rising [1]	5.6	5.8	6.0	V
VIN_OVLO_HYS	VIN overvoltage lockout hysteresis [1]	—	—	200	mV

[1] Operating the device above the maximum VIN = 5.5 V for extended period of time may degrade and cause permanent damage to the device.

14.3 IC startup timing with PWRON pulled up

The PF5024 features a fast internal core power up sequence to fulfill system power up timings of 5.0 ms or less, from power application until MCU is out of reset. Such requirement needs a maximum ramp up time of 1.5 ms for VIN to cross the UVDET threshold in the rising edge.

A maximum core biasing time of 1.5 ms from VIN crossing to UVDET until the beginning of the power up sequence is ensured to allow up to 1.5 ms time frame for the voltage regulators power up sequence.

Timing for the external regulators to start up is programmed by default in the OTP fuses.

The 5.0 ms power up timing requirement is only applicable when the PWRON pin operates in level sensitive mode OTP_PWRON_MODE = 0, however turn on timing is expected to be the same for both level or edge sensitive modes after the power on event is present.

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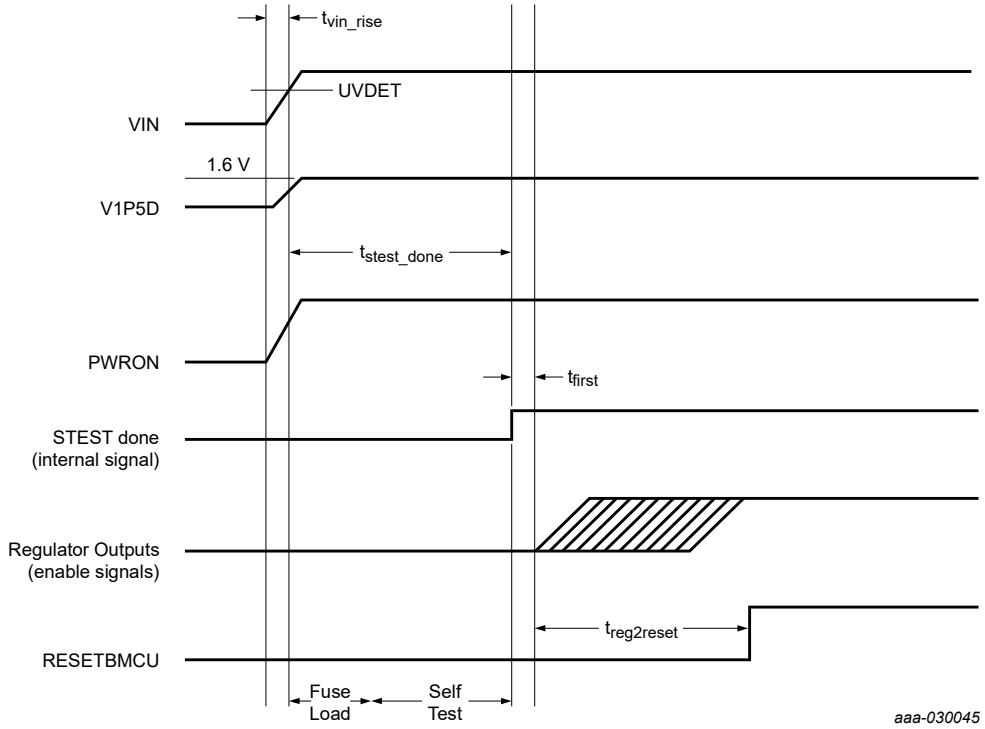

Figure 6. Startup with PWRON pulled up

Table 15. Startup timing requirements (PWRON pulled up)

Symbol	Parameter	Min	Typ	Max	Unit
t_{vin_rise}	Rise time of VIN from VPWR application to UVDET (system dependent)	10	—	1500	µs
t_{stest_done}	Time from VIN crossing UVDET to fist slot of power up sequence	—	—	1.5	ms

14.4 IC startup timing with PWRON pulled low during VIN application

It is possible that PWRON is held low when VIN is applied. By default, LPM_OFF bit is reset to 0 upon crossing UVDET, therefore the PF5024 remains in the LP_Off state as described in Section 13.1.2 "LP_Off state". In this scenario, the quiescent current in the LP_Off state is kept to a minimum. When PWRON goes high with LPM_OFF = 0, the PMIC startup is expected to take longer, since it has to enable most of the internal circuits and perform the self-test before starting a power up sequence.

Figure 7 shows startup timing with LPM_OFF = 0.

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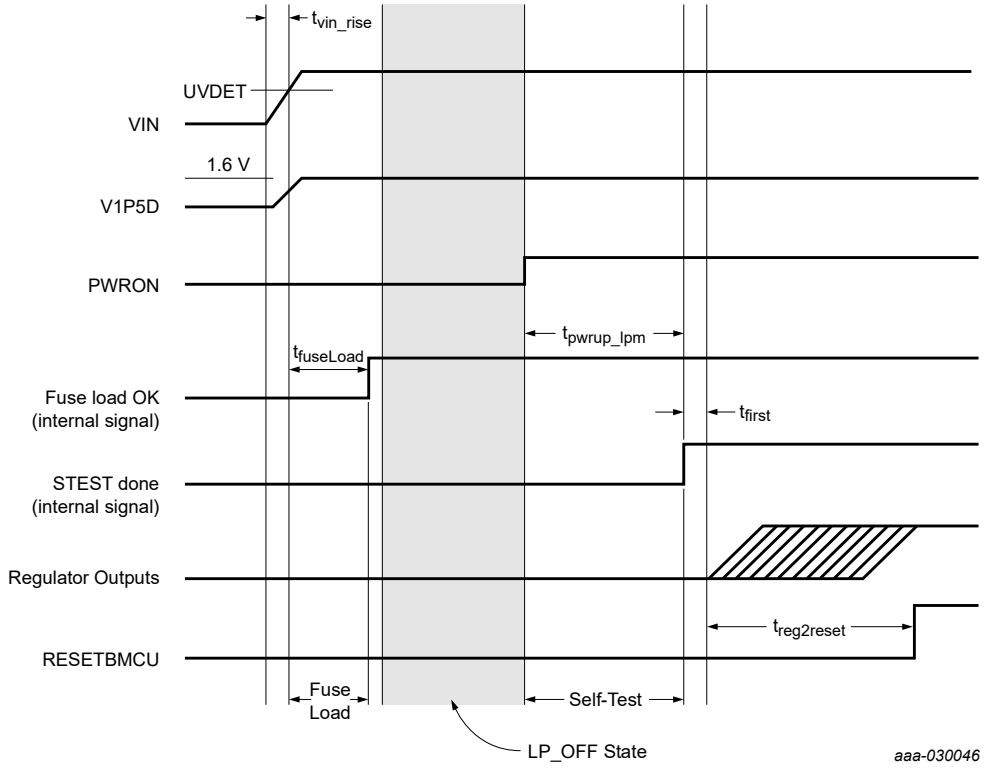

Figure 7. Startup with PWRON driven high externally and bit LPM_OFF = 0

Table 16. Startup with PWRON driven high externally and LPM_OFF = 0

Symbol	Parameter	Min	Typ	Max	Unit
t_{vin_rise}	Rise time of VIN from VPWR application to UVDET (system dependent)	10	—	1500	µs
$t_{fuseload}$	Time from VIN crossing UVDET to Fuse_Load_done (fuse loaded correctly)	—	—	600	µs
t_{pwrup_lpm}	Time from PWRON going high to the first slot of the power up sequence	—	—	800	µs

14.5 Power up

14.5.1 Power up events

Upon a power cycle (VIN > UVDET), the LPM_OFF bit is reset to 0, therefore the device moves to the LP_Off state by default. The actual value of the LPM_OFF bit can be changed during the Run mode and is maintained until VIN crosses the UVDET threshold.

In either one of the Off modes, the PF5024 can be enabled by the following power up events:

1. When OTP_PWRON_MODE = 0, PWRON pin is pulled high.
2. When OTP_PWRON_MODE = 1, PWRON pin experiences a high to low transition and remains low for as long as the PWRON_DBNC timer.

A power up event is valid only if:

- VIN > UVDET
- VIN < VIN_OVLO (unless the OVLO is disabled or OTP_VIN_OVLO_SDWN = 0)
- Tj < thermal shutdown threshold

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- TRIM_NOK = 0 && OTP_NOK = 0 && STEST_NOK = 0

14.5.2 Power up sequencing

The power up sequencer controls the time and order in which the voltage regulators and other controlling I/O are enabled when going from the Off mode into the run state.

The OTP_SEQ_TBASE[1:0] bits set the default time base for the power up and power down sequencer.

The SEQ_TBASE[1:0] bits can be modified during the system On state in order to change the sequencer timing during run/standby transitions as well as the power down sequence.

Table 17. Power up time base register

OTP bits OTP_SEQ_TBASE[1:0]	Functional bits SEQ_TBASE[1:0]	Sequencer time base (µs)
00	00	30
01	01	120
10	10	250
11	11	500

The power up sequence may include any of the following:

- Switching regulators
- PGOOD pin if programmed as a GPO
- RESETBMCU

The default sequence slot for each one of these signals is programmed via the OTP configuration registers. They can be modified in the functional I^2C register map to change the order in which the sequencer behaves during the run/standby transitions as well as the power down sequence.

The x_SEQ[7:0] bits set the regulator/pin sequence from 0 to 254. Sequence code 0x00 indicates that the particular output is not part of the startup sequence and remains in OFF (in case of a regulator) or remains low/disabled (in case PGOOD pin used as a GPO).

Table 18. Power up sequence registers

OTP bits OTP_SWx_SEQ[7:0]/ OTP_PGOOD_SEQ[7:0]/ OTP_RESETBMCU_SEQ[7:0]	Functional bits SWx_SEQ[7:0]/ PGOOD_SEQ[7:0]/ RESETBMCU_SEQ[7:0]	Sequence slot	Startup time (µs)
00000000	00000000	Off	Off
00000001	00000001	0	SLOT0 (right after PWRON event is valid)
00000010	00000010	1	SEQ_TBASE x SLOT1
. . .	. . .	. . .	. . .
11111111	11111111	254	SEQ_TBASE x SLOT254

If RESETBMCU is not programmed in the OTP sequence, it will be enabled by default after the last regulator programmed in the power up sequence.

When the _SEQ[7:0] bits of all regulators and PGOOD used as a GPIO are set to 0x00 (OFF) and a power on event is present, the device moves to the run state in companion mode. In this mode, the device is enabled without any voltage regulator or GPO enabled. If the RESETBMCU is not programed in a power up sequence slot, it is released when the device enters the run state.

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The companion mode is a special case of the power up sequence to address the scenario where the PF5024 is working as a secondary PMIC, and supplies are meant to be enabled by the MCU during the system operation. In this scenario, if RESETBMCU is used, it is connected to the primary device RESETBMCU pin.

Figure 8 provides an example of the power up/down sequence coming from the Off modes.

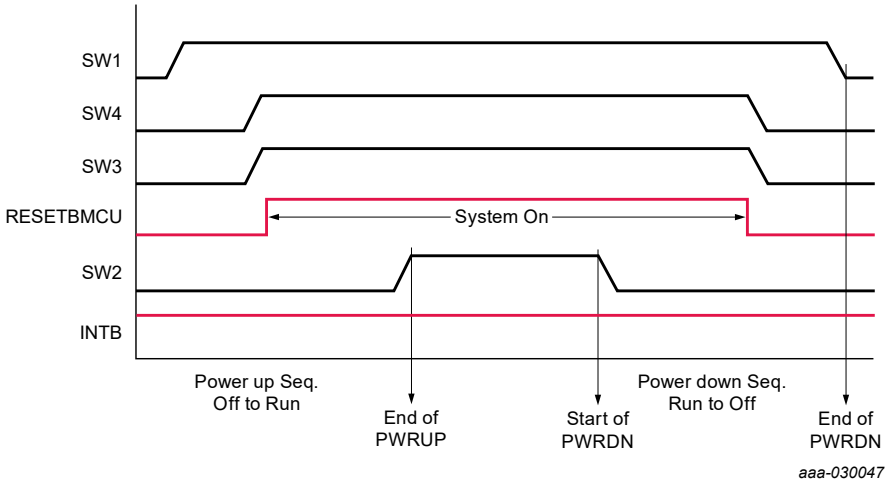

Figure 8. Power up/down sequence between Off and system On state

When transitioning from Standby mode to Run mode, the power up sequencer is activated only if any of the external regulators is re-enabled during this transition. If none of the regulators toggle from Off to On and only voltage changes are being performed when entering or exiting Standby mode, the changes for the voltage regulators are made simultaneously rather than going through the power up sequencer.

Figure 9 shows an example of the power up/down sequence when transitioning between Run and Standby modes.

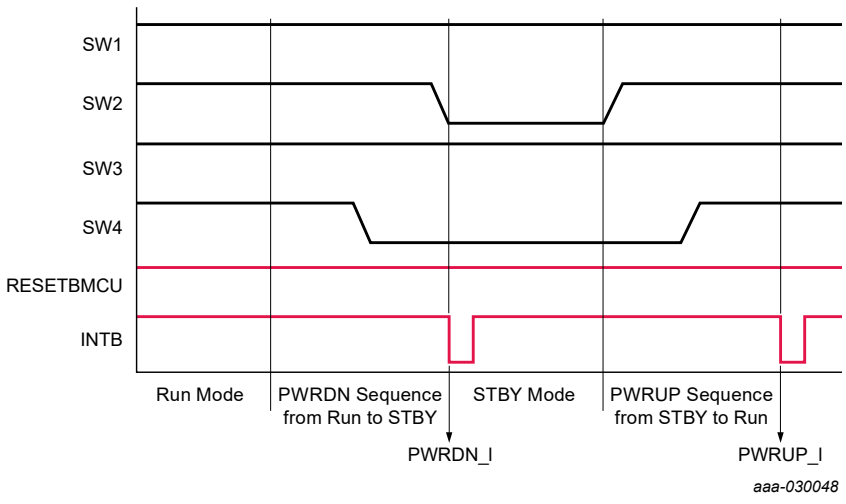

Figure 9. Power up/down sequence between run and standby

The PWRUP_I interrupt is set while transitioning from standby to run, even if the sequencer is not used. This is used to indicate that the transition is complete and device is ready to perform proper operation.

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14.6 Power down

14.6.1 Turn off events

Turn off events may be requested by the MCU (non-PMIC fault related) or due to a critical failure of the PMIC (hard fault condition).

The following are considered non-PMIC failure turn off events:

1. When OTP_PWRON_MODE = 0, the device starts a power down sequence when the PWRON pin is pulled low.
2. When OTP_PWRON_MODE = 1, the device starts a power down sequence when the PWRON pin sees a transition from high to low and remains low for longer than TRESET.
3. When bit PMIC_OFF is set to 1, the device starts a 500 µs shutdown timer. When the shutdown timer is started, the PF5024 sets the SDWN_I interrupt and asserts the INTB pin provided it is not masked. At this point, the MCU can read the interrupt and decide whether to continue with the turn off event or stop it in case it was sent by mistake.
   If the SDWN_I bit is cleared before the 500 µs shutdown timer is expired, the shutdown request is canceled and the shutdown timer is reset; otherwise, if the shutdown timer is expired, the PF5024 starts a power down sequence.
   The PMIC_OFF bit self-clears after SDWN_I flag is cleared.
4. When VIN_OVLO_EN = 1 and VIN_OVLO_SDWN = 1, and a VIN_OVLO event is present.

Turn off events due to a hard fault condition:

1. If an OV, UV or ILIM condition is present long enough for the fault timer to expire.
2. In the event that an OV, UV or ILIM condition appears and clears cyclically, and the FAULT_CNT[3:0] = FAULT_MAX_CNT[3:0].
3. If the watchdog fail counter is overflown, that is WD_EVENT_CNT = WD_MAX_CNT.
4. When Tj crosses the thermal shutdown threshold as the temperature rises.

When the PF5024 experiences a turn off event due to a hard fault condition, the device pass through the fail-safe transition after regulators have been powered down.

14.6.2 Power down sequencing

During a power down sequence, output voltage regulators can be turned off in two different modes as defined by the PWRDWN_MODE bit.

1. When PWRDWN_MODE = 0, the regulators power down in sequential mode.
2. When PWRDWN_MODE = 1, the regulators power down by groups.

During transition from run to standby, the power down sequencer is activated in the corresponding mode, if any of the external regulators are turned off in the standby configuration. If external regulators are not turned off during this transition, the power down sequencer is bypassed and the transition happens at once (any associated DVS transitions could still take time).

The PWRDN_I interrupt is set at the end of the transition from run to standby when the last regulator has reached its final state, even if external regulators are not turned off during this transition.

14.6.2.1 Sequential power down

When the device is set to the sequential power down, it uses the same _SEQ[7:0] registers as the power up sequence to power down in reverse order.

All regulators with the _SEQ[7:0] bits set to 0x00, power down immediately and the remaining regulators power down one OTP_SEQ_TBASE[1:0] delay after, in reverse order as defined in the _SEQ[7:0] bits.

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If PGOOD pin is used as a GPO, it is de-asserted as part of the power down sequence as indicated by the PGOOD_SEQ[7:0] bits.

If the MCU requires a different power down sequence, it can change the values of the SEQ_TBASE[1:0] and the _SEQ[7:0] bits during the system On state.

When the state machine passes through any of the Off modes, the contents of the SEQ_TBASE[1:0] and _SEQ[7:0] bits are reloaded with the corresponding mirror register (OTP) values before it starts the next power up sequence.

14.6.2.2 Group power down

When the device is configured to power down in groups, the regulators are assigned to a specific power down group. All regulators assigned to the same group are disabled at the same time when the corresponding group is due to be disabled.

Power down groups shut down in decreasing order starting from the lowest hierarchy group with a regulator shutting down (for instance Group 4 being the lowest hierarchy and Group 1 the highest hierarchy group). If no regulators are set to the lowest hierarchy group, the power down sequence timer starts off the next available group that contains a regulator to power down.

Each regulator has its own _PDGRP[1:0] bits to set the power down group it belongs to as shown in Table 19.

Table 19. Power down regulator group bits

OTP_SWx_PDGRP[1:0] OTP_PGOOD_PDGRP[1:0] OTP_RESETBMCU_PDGRP[1:0]	SWx_PDGRP[1:0] PGOOD_PDGRP[1:0] RESETBMCU_PDGRP[1:0]	Description
00	00	Regulator belongs to Group 4
01	01	Regulator belongs to Group 3
10	10	Regulator belongs to Group 2
11	11	Regulator belongs to Group 1

If PGOOD pin is used as a GPO, the PGOOD_PDGRP[1:0] is used to turn off the PGOOD pin in a specific group during the power down sequence. If PGOOD pin is used in power good mode, it is recommended that the OTP_PGOOD_PDGRP bits are set to 11 to ensure the group power down sequencer does not detect these bits as part of Group 4.

Each one of power down groups have programmable time delay registers to set the time delay after the regulators in this group have been turned off, and the next group can start to power down.

Table 20. Power down counter delay

OTP bits OTP_GRPx_DLY[1:0]	Functional bits GRPx_DLY[1:0]	Power down delay (µs)
00	00	120
01	01	250
10	10	500
11	11	1000

If RESETBMCU is required to be asserted first before any of the external regulators from the corresponding group, the RESETBMCU_DLY provides a selectable delay to disable the regulators after RESETBMCU is asserted.

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Table 21. Programmable delay after RESETBMCU is asserted

OTP bits OTP_RESETBMCU_DLY[1:0]	Functional bits RESETBMCU_DLY[1:0]	RESETBMCU delay (µs)
00	00	No delay
01	01	10
10	10	100
11	11	500

If RESETBMCU_DLY is set to 0x00, all regulators in the same power down group as RESETBMCU is disabled at the same time RESETBMCU is asserted.

Figure 10 shows an example of the power down sequence when PWRDWN_MODE = 1.

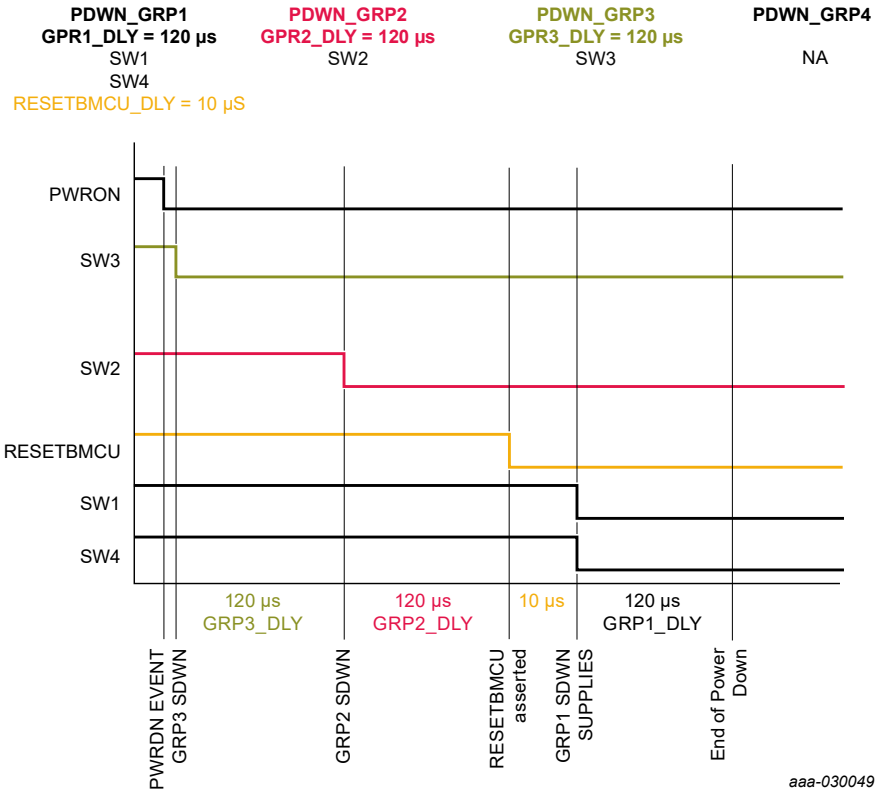

Figure 10. Group power down sequence example

14.6.2.3 Power down delay

After a power down sequence is started, the PWRON pin shall be masked until the sequence is finished and the programmable power down delay is reached. The device can power up again if a power up event is present. The power down delay time can be programmed on an OTP via the OTP_PD_SEQ_DLY[1:0] bits.

Table 22. Power down delay selection

OTP_PD_SEQ_DLY[1:0]	Delay after power down sequence
00	No delay
01	1.5 ms
10	5.0 ms
11	10 ms

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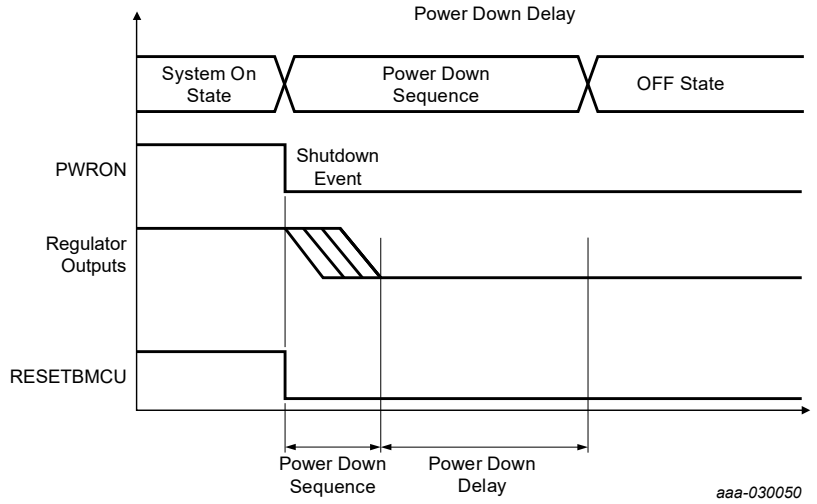

Figure 11. Power down delay

The default value of the OTP_PD_SEQ_DLY[1:0] bits on an unprogrammed OTP device shall be 00.

14.7 Fault detection

Three types of faults are monitored per regulator: UV, OV and ILIM. Faults are monitored during power up sequence, run, standby and WD reset states. A fault event is notified to the MCU through the INTB pin if the corresponding fault is not masked.

The fault configuration registers are reset to their default value after the power up sequences, and system must configure them as required during the boot-up process via I^2C commands.

For each type of fault, there is an I^2C bit that is used to select whether the regulator is kept enabled or disabled when the corresponding regulator experience a fault event.

SWx_ILIM_STATE

- 0 = regulator disables upon an ILIM fault event
- 1 = regulator remains on upon an ILIM fault event

SWx_OV_STATE

- 0 = regulator disables upon an OV fault event
- 1 = regulator remains on upon an OV fault event

SWx_UV_STATE

- 0 = regulator disables upon an UV fault event
- 1 = regulator remains on upon an UV fault event

The following table lists the functional bits associated with enabling/disabling the external regulators when they experience a fault.

Table 23. Regulator control during fault event bits

Regulator	Bit to disable the regulator during current limit	Bit to disable the regulator during undervoltage	Bit to disable the regulator during overvoltage
SWx	SWx_ILIM_STATE	SWx_UV_STATE	SWx_OV_STATE

ILIM faults are debounced for 1.0 ms before they can be detected as a fault condition. If the regulator is programed to disable upon an ILIM condition, the regulator turns off as soon as the ILIM condition is detected.

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OV/UV faults are debounced for defined filter time before they are detected as a fault condition. If the regulator is programmed to disable upon an OV or UV, the regulator will turn off if the fault persist for longer than 300 µs after the OV/UV fault has been detected.

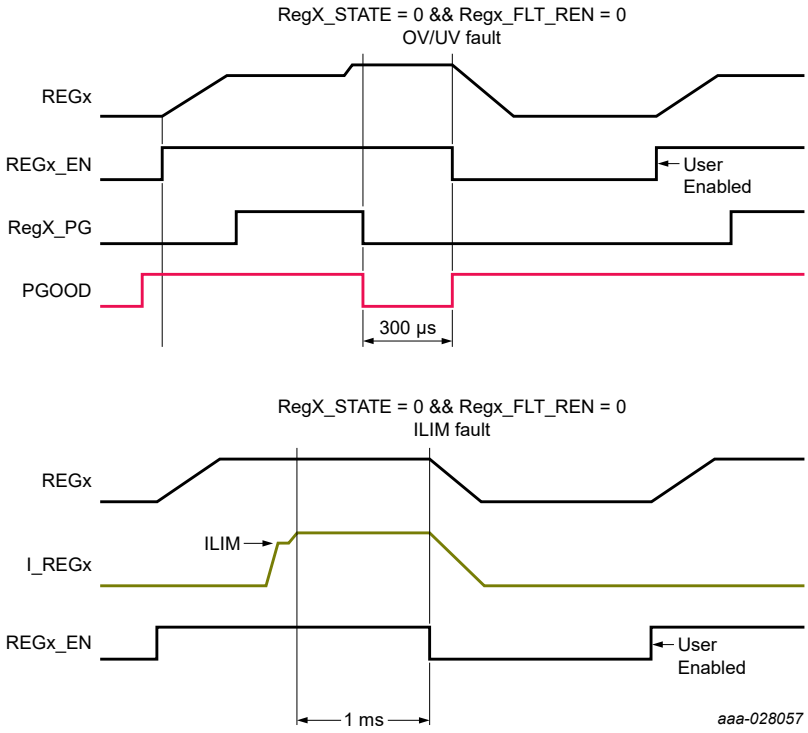

Figure 12. Regulator turned off upon with RegX_STATE = 0 and FLT_REN = 0

When a regulator is programmed to disable upon an OV, UV, or ILIM fault, a bit is provided to decide whether a regulator can return to its previous configuration or remain disabled when the fault condition is cleared.

SWx_FLT_REN

- 0 = regulator remains disabled after the fault condition is cleared or no longer present
- 1 = regulator returns to its previous state if fault condition is cleared

If a regulator is programmed to remain disabled after clearing the fault condition, the MCU can turn it back ON during the system On state by toggling OFF and ON the corresponding mode/enable bits.

When the bit SWx_FLT_REN = 1, if a regulator is programmed to turn off upon an OV, UV or ILIM condition, the regulator returns to its previous state 500 µs after the fault condition is cleared. If the regulator is programmed to turn off upon an ILIM condition, the device may take up to 1.0 ms to debounce the ILIM condition removal, in addition to the 500 µs wait period to re-enable the regulator.

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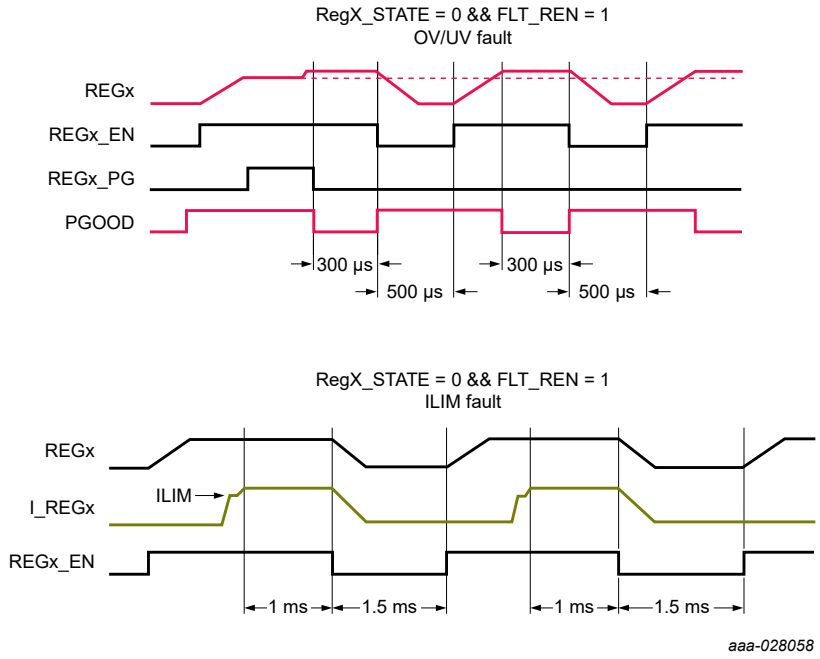

Figure 13. Regulator turned off upon with RegX_STATE = 0 and FLT_REN = 1

When any of the regulators is controlled by hardware using the ENx pins and programmed to turn off upon an OV, UV or ILIM fault, the _FLT_REN bit still controls whether the regulator returns to its previous state or not regardless the state of the ENx pin.

To avoid fault cycling, a global fault counter is provided. Each time any of the external regulators encounter a fault event, the PF5024 compares the value of the FAULT_CNT[3:0] against the FAULT_MAX_CNT, and if it not equal, it increments the FAULT_CNT[3:0] and proceeds with the fault protection mechanism.

The processor is expected to read the counter value and reset it when the faults have been cleared and the device returns to a normal operation. If the processor does not reset the fault counter and it equals the FAULT_MAX_CNT[3:0] value, the state machine initiates a power down sequence.

The default value of the FAULT_MAX_CNT[3:0] is loaded from the OTP_FAULT_MAX_CNT[3:0] bits during the power up sequence.

When the FAULT_MAX_CNT[3:0] is set to 0x00, the system disables the turn-off events due to a fault counter maxing out.

When a regulator experiences a fault event, a fault timer is started. While this timer is in progress, the expectation is that the processor takes actions to clear the fault. For example, it could reduce its load in the event of a current limit fault, or turn off the regulator in the event of an overvoltage fault.

If the fault clears before the timer expires, the state machine resumes the normal operation, and the fault timer gets reset. If the fault does not clear before the timer expires, a power down sequence is initiated to turn off the voltage regulators.

The default value of the fault timer is set by the OTP_TIMER_FAULT[3:0], however the duration of the fault timer can be changed during the system On state by modifying the TIMER_FAULT[3:0] bits in the I^2C registers.

Table 24. Fault timer register configuration

OTP bits OTP_TIMER_FAULT [3:0]	Functional bits TIMER_FAULT [3:0]	Timer value (ms)
0000	0000	1
0001	0001	2

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Table 24. Fault timer register configuration*...continued*

OTP bits OTP_TIMER_FAULT [3:0]	Functional bits TIMER_FAULT [3:0]	Timer value (ms)
0010	0010	4
0011	0011	8
0100	0100	16
0101	0101	32
0110	0110	64
0111	0111	128
1000	1000	256
1001	1001	512
1010	1010	1024
1011	1011	2056
1100	1100	Reserved
1101	1101	Reserved
1110	1110	Reserved
1111	1111	Disabled

Each voltage regulator has a dedicated I^2C bit that is used to bypass the fault detection mechanism for each specific fault.

SWx_ILIM_BYPASS

- 0 = ILIM protection enabled
- 1 = ILIM fault bypassed

SWx_OV_BYPASS

- 0 = OV protection enabled
- 1 = OV fault bypassed

SWx_UV_BYPASS

- 0 = UV protection enabled
- 1 = UV fault bypassed

Table 25. Fault bypass bits

Regulator	Bit to bypass a current limit	Bit to bypass an undervoltage	Bit to bypass an overvoltage
SWx	SWx_ILIM_BYPASS	SWx_UV_BYPASS	SWx_OV_BYPASS

The default value of the OV_BYPASS, UV_BYPASS and ILIM_BYPASS bits upon power up can be configured by their corresponding OTP bits.

Bypassing the fault detection prevents the specific fault from starting any of the protective mechanism:

- Increment the counter
- Start the fault timer
- Disable the regulator if the corresponding _STATE bit is 0
- OV/UV condition asserting the PGOOD and PGOODx pins low

When a fault is bypassed, the corresponding interrupt bit is still set and the INTB pin is asserted, provided the interrupt has not been masked.

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14.7.1 Fault monitoring during power up state

An OTP bit is provided to select whether the output of the switching regulators is verified during the power up sequence and used as a gating condition to release the RESETBMCU or not.

- When OTP_PG_CHECK = 0, the output voltage of the regulators is not checked during the power up sequence and power good indication is not required to de-assert the RESETBMCU. In this scenario, the OV/UV monitors are masked until RESETBMCU is released; after this event, all regulators may start checking for faults after their corresponding blanking period.
- When OTP_PG_CHECK = 1, the output voltage of the regulators is verified during the power up sequence and a power good condition is required to release the RESETBMCU.

When OTP_PG_CHECK = 1, OV and UV faults during the power up sequence are reported based on the internal PG (Power Good) signals of the corresponding external regulator. The PGOOD pin can be used as an external indicator of an OV/UV failure when the RESETBMCU is ready to be de-asserted and it has been configured in the PGOOD mode. See Section 14.9.6 "PGOOD" for details on PGOOD pin operation and configuration.

Regardless of the PGOOD pin configured as a power good indicator or not, the PF5024 masks the detection of an OV/UV failure until RESETBMCU is ready to be released, at this point the device checks for any OV/UV condition for the regulators turned on so far. If all regulators powered up before or in the same sequence slot than RESETBMCU are in regulation, RESETBMCU is de-asserted and the power up sequence can continue as shown in Figure 14.

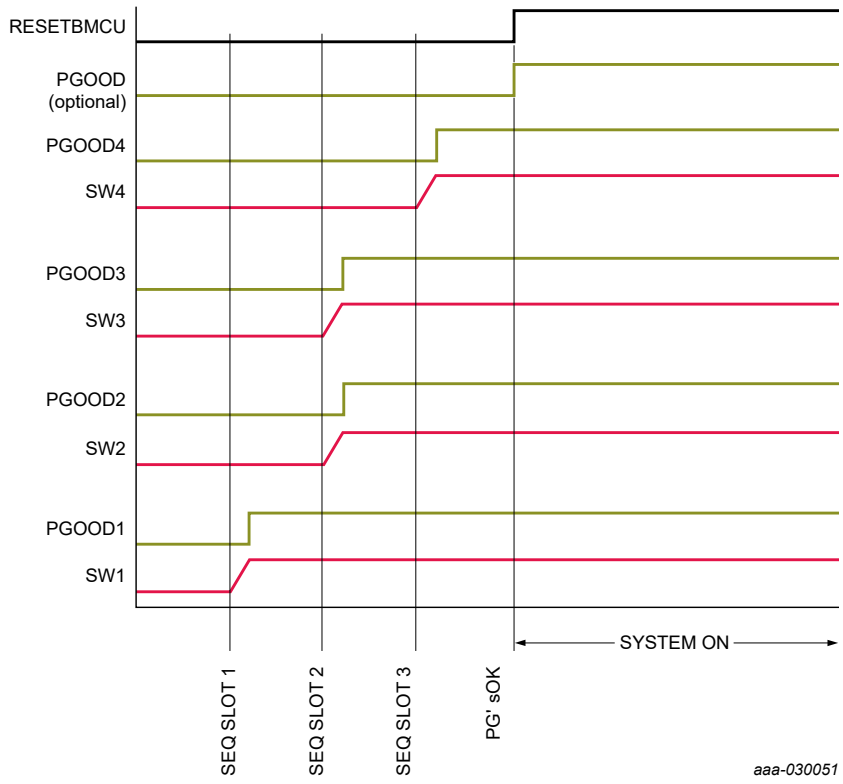

Figure 14. Correct power up (no fault during power up)

If any of the regulators are powered up before RESETBMCU is out of regulator, RESETBMCU is not de-asserted and the power up sequence is stopped for up to 2.0 ms. If the fault is cleared and all internal PG signals are asserted within the 2.0 ms timer, RESETBMCU is de-asserted and the power up sequence continues where it stopped as shown in Figure 15.

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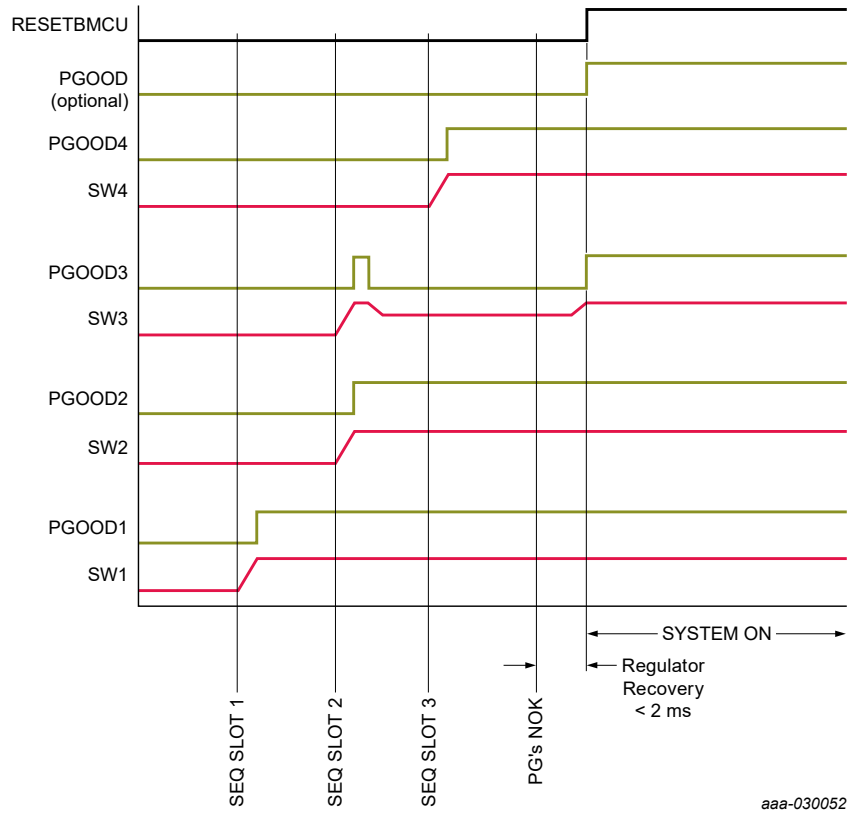

Figure 15. Power up sequencer with a temporary failure

If the faulty condition is not cleared within the 2.0 ms timer, the power up sequence is aborted and the PF5024 turns off all voltage regulators enabled so far as shown in Figure 16.

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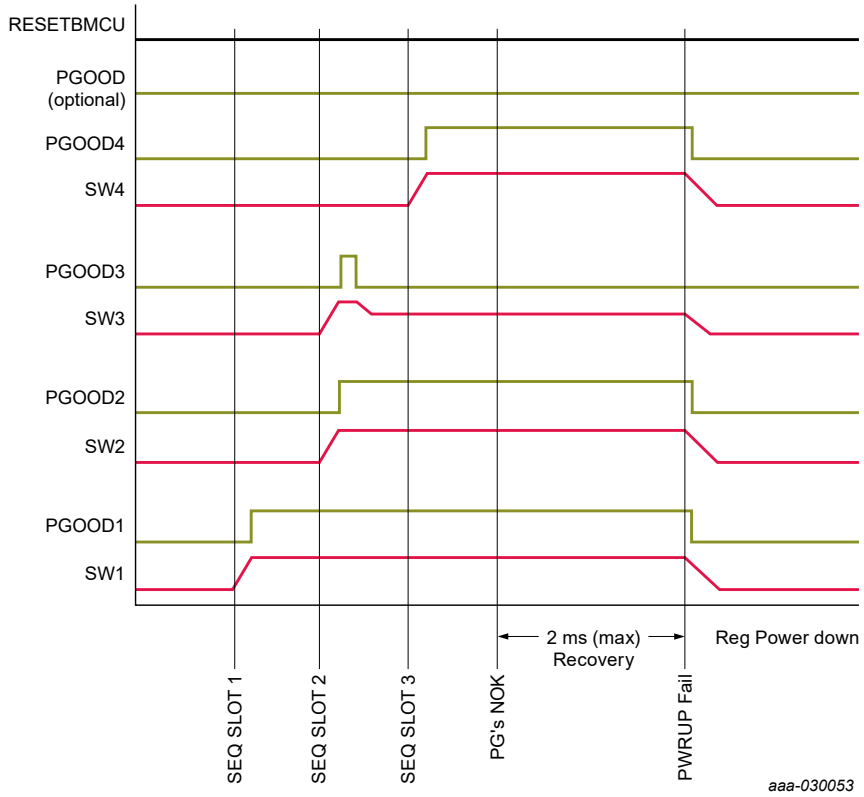

Figure 16. Power up sequencer aborted as fault persists for longer than 2.0 ms

Supplies enabled after RESETBMCU are checked for OV, UV and ILIM faults after each of them are enabled. If an OV, UV or ILIM condition is present, the PF5024 starts a fault detection and protection mechanism as described in Section 14.7 "Fault detection". At this point, the MCU should be able to read the interrupt and react upon a fault event as defined by the system.

When OTP_PG_CHECK=1, If PGOOD is used as a GPIO, it may be released at any time in the power up sequence as long as the RESETBMCU is released after one or more of the SW regulators.

If a regulator fault occurs after RESETBMCU is de-asserted but before the power up sequence is finalized, the power up sequences continue to turn on the remaining regulators as configured, even if a fault detection mechanism is active on an earlier regulator.

14.8 Interrupt management

The MCU is notified of any interrupt through the INTB pin and various interrupt registers.

The interrupt registers are composed by three types of bits to help manage all the interrupt requests in the PF5024:

- The interrupt latch XXXX_I: this bit is set when the corresponding interrupt event occurs. It can be read at any time, and is cleared by writing a 1 to the bit.
- The mask bit XXXX_M: this bit controls whether a given interrupt latch pulls the INTB pin low or not.
- When the mask bit is 1, the interrupt latch does not control the INTB pin.
- When the mask bit is 0, the INTB pin is pulled low as long as the corresponding latch bit is set.
- The sense bit XXXX_S: if available, the sense bit provides the actual status of the signal triggering the interrupt.

The INTB pin is a reflection of an “OR” logic of all the interrupt status bits which control the pin.

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Interrupts are stored in two levels on the interrupts registers. At first level, the SYS_INT register provides information about the Interrupt register that originated the interrupt event.

The corresponding SYS_INT bits is set as long as the INTB pin is programmed to assert with any of the interrupt bits of the respective interrupt registers.

- STATUS1_I: this bit is set when the interrupt is generated within the INT STATUS1 register
- STATUS2_I: this bit is set when the interrupt is generated within the INT STATUS2 register
- MODE_I: this bit is set when the interrupt is generated within the SW MODE INT register
- ILIM_I: this bit is set when the interrupt is generated within any of the SW ILIM INT register
- UV_I: this bit is set when the interrupt is generated within any of the SW UV INT
- OV_I: this bit is set when the interrupt is generated within any of the SW OV register
- PWRON_I: this bit is set when the interrupt is generated within the PWRON INT register
- EWARN_I (EWARN time set by OTP_EWARN_TIME[1:0]): is set when an early warning event occurs to indicate an imminent shutdown

Table 26. EWARN configuration

OTP_EWARN_TIME[1:0]	EWARN delay time
00	100 µs
01	5.0 ms
10	20 ms
11	50 ms

The SYS_INT bits are set when the INTB pin is asserted by any of the second level interrupt bits that have not been masked in their corresponding mask registers. When the second level interrupt bit is cleared, the corresponding first level interrupt bit on the SYS_INT register will be cleared automatically.

The INTB pin will remain asserted if any of the first level interrupts bit is set, and it will be de-asserted only when all the unmasked second level interrupts are cleared and thus all the first level interrupts are cleared as well.

At second level the remaining registers provide the exact source for the interrupt event.

Table 27 shows a summary of the interrupt latch, mask and sense pins available on the PF5024.

Table 27. Interrupt registers

Register name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
INT STATUS1	SDWN_I	FREQ_RDY_I	CRC_I	PWRUP_I	PWRDN_I	—	PGOOD_I	VIN_OVLO_I
INT MASK1	SDWN_M	FREQ_RDY_M	CRC_M	PWRUP_M	PWRDN_M	—	PGOOD_M	VIN_OVLO_M
INT SENSE1	—	—	—	—	—	—	PGOOD_S	VIN_OVLO_S
THERM INT	WDI_I	FSYNC_FLT_I	THERM_155_I	THERM_140_I	THERM_125_I	THERM_110_I	THERM_95_I	THERM_80_I
THERM MASK	WDI_M	FSYNC_FLT_M	THERM_155_M	THERM_140_M	THERM_125_M	THERM_110_M	THERM_95_M	THERM_80_M
THERM SENSE	WDI_S	FSYNC_FLT_S	THERM_155_S	THERM_140_S	THERM_125_S	THERM_110_S	THERM_95_S	THERM_80_S
SW MODE INT	—	—	—	—	SW4_MODE_I	SW3_MODE_I	SW2_MODE_I	SW1_MODE_I
SW MODE MASK	—	—	—	—	SW4_MODE_M	SW3_MODE_M	SW2_MODE_M	SW1_MODE_M
SW ILIM INT	—	—	—	—	SW4_ILIM_I	SW3_ILIM_I	SW2_ILIM_I	SW1_ILIM_I
SW ILIM MASK	—	—	—	—	SW4_ILIM_M	SW3_ILIM_M	SW2_ILIM_M	SW1_ILIM_M
SW ILIM SENSE	—	—	—	—	SW4_ILIM_S	SW3_ILIM_S	SW2_ILIM_S	SW1_ILIM_S
SW UV INT	—	—	—	—	SW4_UV_I	SW3_UV_I	SW2_UV_I	SW1_UV_I
SW UV MASK	—	—	—	—	SW4_UV_M	SW3_UV_M	SW2_UV_M	SW1_UV_M
SW UV SENSE	—	—	—	—	SW4_UV_S	SW3_UV_S	SW2_UV_S	SW1_UV_S
SW OV INT	—	—	—	—	SW4_OV_I	SW3_OV_I	SW2_OV_I	SW1_OV_I
SW OV MASK	—	—	—	—	SW4_OV_M	SW3_OV_M	SW2_OV_M	SW1_OV_M
SW OV SENSE	—	—	—	—	SW4_OV_S	SW3_OV_S	SW2_OV_S	SW1_OV_S
PWRON INT	BGMON_I	PWRON_8S_I	PWRON_4S_I	PRON_3S_I	PWRON_2S_I	PWRON_1S_I	PWRON_REL_I	PWRON_PUSH_I
PWRON MASK	BGMON_M	PWRON_8S_M	PWRON_4S_M	PRON_3S_M	PWRON_2S_M	PWRON_1S_M	PWRON_REL_M	PWRON_PUSH_M
PWRON SENSE	BGMON_S	—	—	—	—	—	—	PWRON_S
EN_SENSE	—	—	—	—	EN4_S	EN3_S	EN2_S	EN1_S

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Table 27. Interrupt registers*...continued*

Register name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
SYS INT	EWARN_I	PWRON_I	OV_I	UV_I	ILIM_I	MODE_I	STATUS2_I	STATUS1_I

14.9 I/O interface pins

The PF5024 PMIC is fully programmable via the I^2C interface. Additional communication between MCU, PF5024 and other companion PMIC is provided by direct logic interfacing including INTB, RESETBMCU, PGOOD, among other pins.

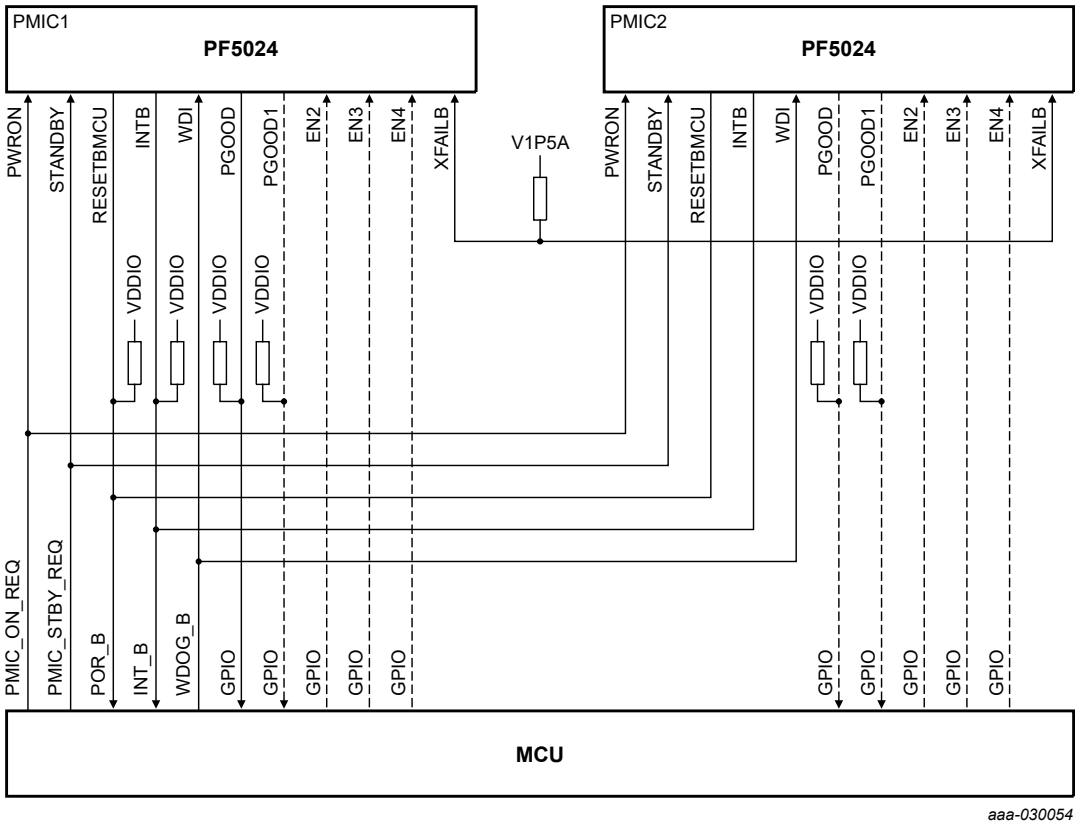

Figure 17. I/O interface diagram

Table 28. I/O electrical specifications

Symbol	Parameter	Min	Typ	Max	Unit
PWRON_V_{IL}	PWRON low input voltage	—	—	0.4	V
PWRON_V_{IH}	PWRON high input voltage	1.4	—	5.5	V
STANDBY_V_{IL}	STANDBY low input voltage	—	—	0.4	V
STANDBY_V_{IH}	STANDBY high input voltage	1.4	—	5.5	V
RESETBMCU_V_{OL}	RESETBMCU low output voltage −2.0 mA load current	 0	 —	 0.4	V
INTB_V_{OL}	INTB low output voltage −2.0 mA load current	 0	 —	 0.4	V
ENx_V_{IL}	ENx low input voltage	—	—	0.4	V
ENx_V_{IH}	ENx high input voltage	1.4	—	5.5	V
WDI_V_{IL}	WDI low input voltage	—	—	0.3*VDDIO	V
WDI_V_{IH}	WDI high input voltage	0.7*VDDIO	—	5.5	V
R_{WDI_PD}	WDI internal pull-down resistance	0.475	1.0	—	MΩ

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Table 28. I/O electrical specifications...*continued*

Symbol	Parameter	Min	Typ	Max	Unit
PGOOD_V_{OL}	PGOOD low output voltage −2.0 mA load current	0	—	0.4	V
PGOODx_V_{OL}	PGOODx low output voltage −2.0 mA load current	0	—	0.4	V
TBBEN_V_{IL}	TBBEN low input voltage	—	—	0.4	V
TBBEN_V_{IH}	TBBEN high input voltage	1.4	—	5.5	V
R_{TBBEN_PD}	TBBEN internal pull-down resistance	0.475	1.0	—	MΩ
XFAILB_V_{IL}	XFAILB low input voltage	—	—	0.4	V
XFAILB_V_{IH}	XFAILB high input voltage	1.4	—	5.5	V
XFAILB_V_{OH}	XFAILB high output voltage Pulled-up to V1P5A	V1P5A − 0.5	—	—	V
XFAILB_V_{OL}	XFAILB low output voltage −2.0 mA load current	0	—	0.4	V
SCL_V_{IL}	SCL low input voltage	—	—	0.3*VDDIO	V
SCL_V_{IH}	SCL high input voltage	0.7*VDDIO	—	VDDIO	V
SDA_V_{IL}	SDA low input voltage	—	—	0.3*VDDIO	V
SDA_V_{IH}	SDA high input voltage	0.7*VDDIO	—	VDDIO	V
SDA_V_{OL}	SDA low output voltage −20 mA load current	0	—	0.4	V

14.9.1 PWRON

PWRON is an input signal to the IC that acts as a power up event signal in the PF5024.

The PWRON pin has two modes of operation as programed by the OTP_PWRON_MODE bit.

When OTP_PWRON_MODE = 0, the PWRON pin operates in level sensitive mode. In this mode, the device is in the corresponding off mode when the PWRON pin is pulled low. Pulling the PWRON pin high is a necessary condition to generate a power on event.

PWRON may be pulled up to VIN with an external 100 kΩ resistor if device is intended to come up automatically with VIN application. See Section 14.5 "Power up" for details on power up requirements.

When OTP_PWRON_MODE = 1, the PWRON pin operates in edge sensitive mode. In this mode, PWRON is used as an input from a push button connected to the PMIC.

When the switch is not pressed, the PWRON pin is pulled up to VIN externally through a 100 kΩ resistor. When the switch is pressed, the PWRON pin should be shorted to ground. The PWRON_S bit is low whenever the PWRON pin is at logic 0 and is high whenever the PWRON pin is at logic 1.

The PWRON pin has a programmable debounce on the rising and falling edges as shown in Table 29.

Table 29. PWRON debounce configuration in edge detection mode

Bits	Value	Falling edge debounce (ms)	Rising edge debounce (ms)
PWRON_DBNC[1:0]	00	32	32
PWRON_DBNC[1:0]	01	32	32
PWRON_DBNC[1:0]	10	125	32
PWRON_DBNC[1:0]	11	750	32

The default value for the power on debounce is set by the OTP_PWRON_DBNC[1:0] bits.

Pressing the PWRON switch for longer than the debounce time starts a power on event as well as generate interrupts which the processor may use to initiate PMIC state transitions.

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During the system On state, when the PWRON button is pushed (logic 0) for longer than the debounce setting, the PWRON_PUSH_I interrupt is generated. When the PWRON button is released (logic 1) for longer than the debounce setting, the PWRON_REL_I interrupt is generated.

The PWRON_1S_I, PWRON_2S_I, PWRON_3S_I, PWRON_4S_I and PWRON_8S_I interrupts are generated when the PWRON pin is held low for longer than 1, 2, 3, 4 and 8 seconds respectively.

If PWRON_RST_EN = 1, pressing the PWRON for longer than the delay programmed by TRESET[1:0] forces a PMIC reset. A PMIC reset initiates a power down sequence, wait for 30 µs to allow all supplies to discharge and then it powers back up with the default OTP configuration.

If PWRON_RST_EN = 0, the device starts a turn off event after push button is pressed for longer than TRESET[1:0].

Table 30. TRESET configuration

TRESET[1:0]	Time to reset
00	2 s
01	4 s
10	8 s
11	16 s

The default value of the TRESET delay is programmable through the OTP_TRESET[1:0] bits.

14.9.2 STANDBY

STANDBY is an input signal to the IC, when this pin is asserted, the device enters the standby mode and when de-asserted, the part exits Standby mode.

STANDBY can be configured as active high or active low using the STANDBYINV bit.

Table 31. Standby pin polarity control

STANDBY (pin)	STANDBYINV (I^2C bit)	STANDBY control
0	0	Not in Standby mode
0	1	In Standby mode
1	0	In Standby mode
1	1	Not in Standby mode

14.9.3 RESETBMCU

RESETBMCU is an open-drain, active low output used to bring the processor (and peripherals) in and out of reset.

The time slot RESETBMCU is de-asserted during the power up sequence is programmed by the OTP_RESETBMCU_SEQ[7:0] bits, and it is a condition to enter the system On state.

During the system On state, the RESETBMCU is de-asserted (pulled high), and it is asserted (pulled low) as indicated in the power down sequence, when a system power down or reset is initiated.

In the application, RESETBMCU can be pulled up to VDDIO by a 10 kΩ external resistor.

It is also recommended to add a 10 nF bypass capacitor close to the pin to improve the EM immunity performance.

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14.9.4 INTB

INTB is an open-drain, active low output. This pin is asserted (pulled low) when any interrupt occurs, provided that the interrupt is not masked.

INTB is de-asserted after the corresponding interrupt latch is cleared by software, which requires writing a “1” to the interrupt bit.

An INTB_TEST bit is provided to allow a manual test of the INTB pin. When INTB_TEST is set to 1, the interrupt pin asserts for 100 µs and then de-asserts to its normal state. The INTB_TEST bit self-clears to 0 automatically after the test pulse is generated.

In the application, INTB can be pulled up to VDDIO with an external 100 kΩ resistor.

14.9.5 WDI

WDI is an input pin to the PF5024 and is intended to operate as an external watchdog monitor.

When the WDI pin is connected to the watchdog output of the processor, this pin is used to detect a pulse to indicate a watchdog event is requested by the processor. When the WDI pin is asserted, the device starts a watchdog event to place the PMIC outputs in a default known state.

The WDI pin is monitored during the system On state. In the Off modes and during the power up sequence, the WDI pin is masked until RESETBMCU is de-asserted.

The WDI can be configured to assert on the rising or the falling edge using the OTP_WDI_INV bit.

- When OTP_WDI_INV = 0, the device starts a WD event on the falling edge of the WDI.
- When OTP_WDI_INV = 1, the device starts a WD event on the rising edge of the WDI.

A 10 µs debounce filter is implemented on either rising or falling edge detection to prevent false WDI signals to start a watchdog event.

The WDI_MODE bit allows the WDI pin to react in two different ways:

- When WDI_MODE = 1, a WDI asserted performs a hard WD reset.
- When WDI_MODE = 0, a WDI asserted performs a soft WD reset.

The default value of the WDI_MODE bit is set by the OTP _WDI_MODE bit in the OTP register space.

The WDI_STBY_ACTIVE bit allows the WDI pin to generate a watchdog event during the standby state.

- When WDI_STBY_ACTIVE = 0, asserting the WDI will not generate a watchdog event during the standby state.
- When WDI_STBY_ACTIVE = 1, asserting the WDI will start a watchdog event during the standby state.

The OTP_WDI_STBY_ACTIVE is used to configure whether the WDI is active in the standby state or not by default upon power up.

See Section 15.7 "Watchdog event management" for details on watchdog event.

14.9.6 PGOOD

PGOOD is an open drain output programmable as a power good indicator pin or GPO. In the application, PGOOD can be pulled up to VDDIO with a 100 kΩ resistor.

When OTP_PG_ACTIVE = 0, the PGOOD pin is used as a general purpose output.

As a GPO, during the run state, the state of the pin is controlled by the RUN_PG_GPO bit in the functional I^2C registers:

- When RUN_PG_GPO = 1, the PGOOD pin is high

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- When RUN_PG_GPO = 0, the PGOOD pin is low

During the standby state, the state of the pin is controlled by the STBY_PG_GPO bit in the functional I^2C registers:

- When STBY_PG_GPO = 1, the PGOOD pin is high
- When STBY_PG_GPO = 0, the PGOOD pin is low

When used as a GPO, the PGOOD pin can be enabled high as part of the power up sequence as programmed by the OTP_SEQ_TBASE[1:0] and the OTP_PGOOD_SEQ[7:0] bits. If enabled as part of the power up sequence, both the RUN_PG_GPO and STBY_PG_GPO bits are loaded with 1, otherwise they are loaded with 0 upon power up.

When OTP_PG_ACTIVE = 1, the PGOOD pin is in Power good (PG) mode and it acts as a PGOOD indicator for the selected output voltages in the PF5024.

There is an individual PG monitor for every regulator. Each monitor provides an internal PG signal that can be selected to control the status of the PGOOD pin upon an OV or UV condition when the corresponding SWxPG_EN bit is set. The status of the PGOOD pin is a logic AND function of the internal PG signals of the selected monitors.

- When the PG_EN = 1, the corresponding regulator becomes part of the AND function that controls the PGOOD pin.
- When the PG_EN = 0, the corresponding regulator does not control the status of the PGOOD pin.

The PGOOD pin is pulled low when any of the selected regulator outputs falls above or below the programmed OV/UV thresholds and the corresponding OV/UV interrupt is generated. If the faulty condition is removed, the corresponding OV_S/UV_S bit goes low to indicate the output is back in regulation, however, the interrupt remains latched until it is cleared.

The actual condition causing the interrupt (OV, UV) can be read in the fault interrupt registers. For more details on handling interrupts, see Section 14.8 "Interrupt management".

When a particular regulator is disabled (via OTP, or I^2C, or by change in state of PMIC such as going to standby mode), it no longer controls the PGOOD pin.

In the Off mode and during the power up sequence, the PGOOD pin is held low until RESETBMCU is ready to be released, at this point, the PG monitors are unmasked and the PGOOD pin is released high if all the internal PG monitors are in regulation. In the event that one or more outputs are not in regulation by the time RESETBMCU is ready to de-assert, the PGOOD pin is held low and the PF5024 performs the corresponding fault protection mechanism as described in Section 14.7.1 "Fault monitoring during power up state".

14.9.7 PGOODx

The PGOODx pins are open drain outputs to provide the power good status of each regulator. In the application, PGOODx can be pulled up to VDDIO with a 100 kΩ resistor.

The PGOODx pin is pulled low when the corresponding regulator output falls above or below the programmed OV/UV thresholds.

The actual condition causing the interrupt (OV, UV) can be read in the fault interrupt registers. For more details on handling interrupts, see Section 14.8 "Interrupt management".

Table 32. PGOODx assignment

Pin	PF5024 regulator
PGOOD1	SW1
PGOOD2	SW2
PGOOD3	SW3

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Table 32. PGOODx assignment*...continued*

Pin	PF5024 regulator
PGOOD4	SW4

14.9.8 ENx

The ENx input pin is used to enable or disable the dedicated regulator via hardware.

When the ENx pin is asserted high, the corresponding regulator is controlled by SWx_RUN_MODE.

When the ENx pin is asserted low, the corresponding regulator is turned off.

During power up and power down sequence, after the sequencing starts, the ENx pins are masked. Any change in the ENx pin will not reflect on the status of the particular regulator.

Table 33. ENx assignment

Pin	PF5024 regulator
EN1	SW1
EN2	SW2
EN3	SW3
EN4	SW4

The status of the ENx pin can be monitored via the corresponding ENx_S flag bit in the EN SENSE register.

- When ENx is in low state, ENx_S flag is set to 0.
- When ENx is in high state, ENx_S flag is set to 1.

14.9.9 TBBEN

The TBBEN is an input pin provided to allow the user to program the mirror registers in order to operate the device with a custom configuration as well as programming the default values on the OTP fuses.

- When TBBEN pin is pulled low to ground, the device is operating in normal mode.
- When TBBEN pin is pulled high to V1P5D, the device enables the TBB configuration mode.

See Section 17 "OTP/TBB and hardwire default configurations" for details on TBB and OTP operation.

When TBBEN pin is pulled high to V1P5D the following conditions apply:

- The device uses a fixed I^2C device address (0x08)
- Disable the watchdog operation, including WDI monitoring and internal watchdog timer
- Disable the CRC and I^2C secure write mechanism while no power up event is present (TBB/OTP programming mode).

Disabling the watchdog operation may be required for in-line MCU programming where output voltages are required but watchdog operation should be completely disabled.

14.9.10 XFAILB

XFAILB is a bidirectional pin with an open drain output used to synchronize the power up and power down sequences of two or more PMICs. It should normally be pulled up externally to V1P5A supply.

The OTP_XFAILB_EN bit is used to enable or disable the XFAILB mode of operation.

- When OTP_XFAILB_EN = 0, the XFAILB mode is disabled and any events on this pin are ignored.
- When OTP_XFAILB_EN = 1, the XFAILB mode is enabled

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When the XFAILB mode is enabled, and the PF5024 has a turn off event generated by an internal fault, the XFAILB pin is asserted low 20 µs before starting the power down sequence.

A power down event caused by the following conditions will assert the XFAILB pin:

- Fault timer expired
- FAULT_CNT = FAULT_MAX_CNT (Regulator fault counter max out)
- WD_EVENT_CNT = WD_MAX_CNT (Watchdog event counter max out)
- Power up failure
- Thermal shutdown
- Hard WD event

The XFAILB pin is forced low during the Off mode.

During the system On state, if the XFAILB pin is externally pulled low, it will detect an XFAIL event after a 20 µs debounce. When an XFAIL event is detected, the XFAILB pin is asserted low internally and the device starts a power down sequence.

If a PWRON event is present, the device will start a turn on event and proceed to release the XFAILB pin when its ready to start the power up sequence state. If the XFAILB pin is pulled down externally during the power up event, the PF5024 will stop the power up sequence until the pin is no longer pulled down externally. This will help both PMICs to synchronize the power up sequence allowing it to continue only when both PMICs are ready to initiate the power up sequence.

A hard WD event will set the XFAILB pin 20 µs before it starts its power down sequence. After all regulator outputs have been turned off, the device will release the XFAILB pin internally after a 30 µs delay, proceed to load the default OTP configuration and wait for the XFAILB pin to be released externally before it can restart the power up sequence.

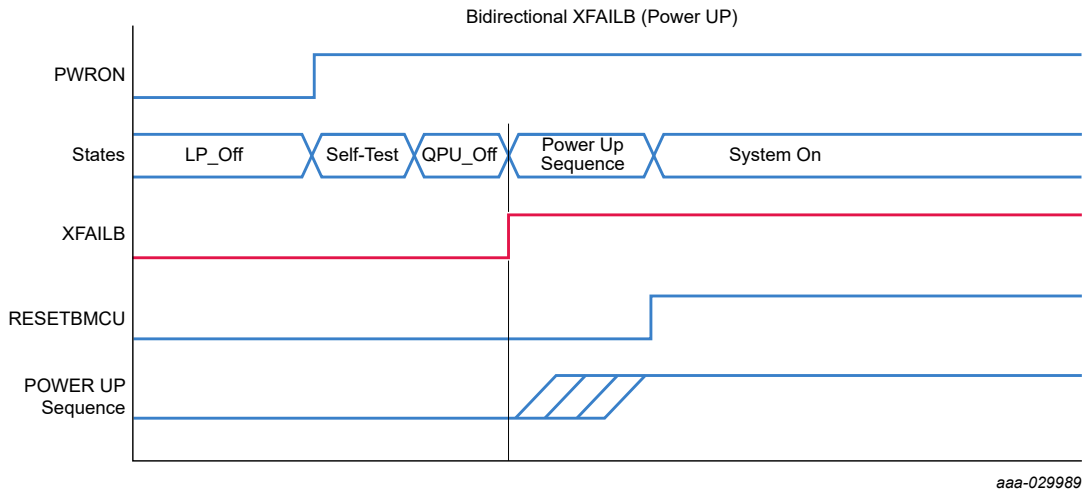

Figure 18. XFAILB behavior during a power up sequence

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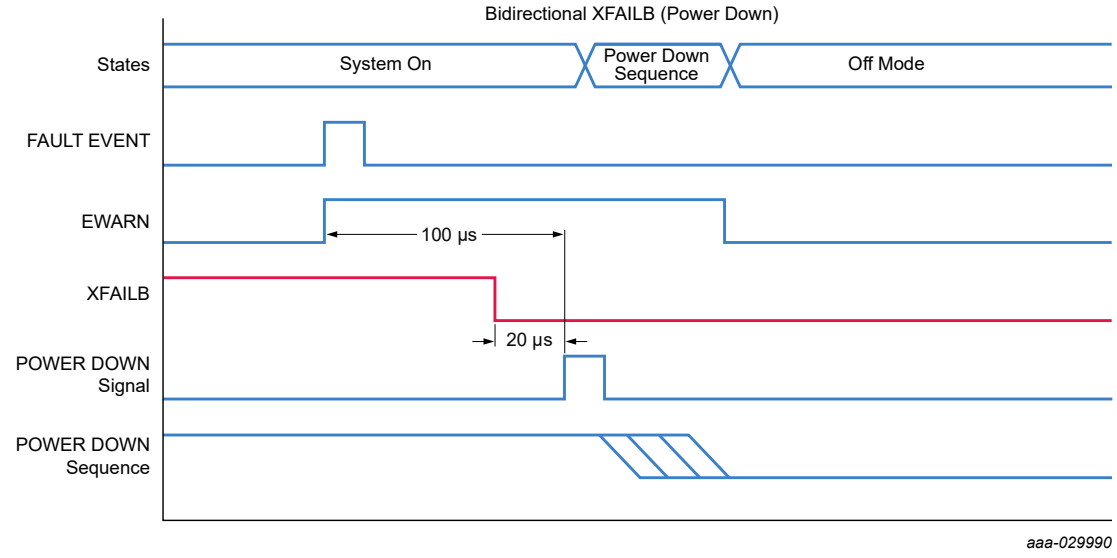

Figure 19. XFAILB behavior during a power down sequence

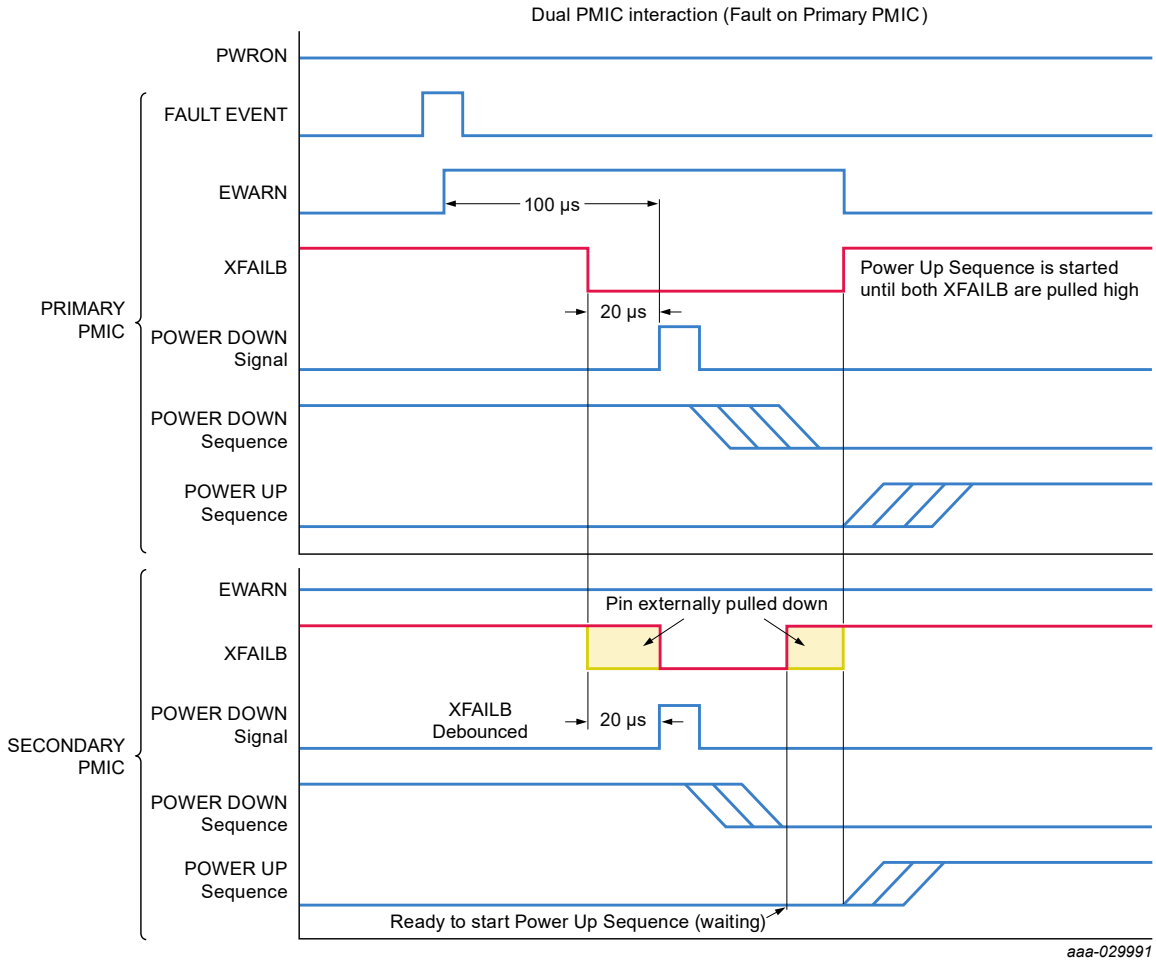

Figure 20. Behavior during an external XFAILB event

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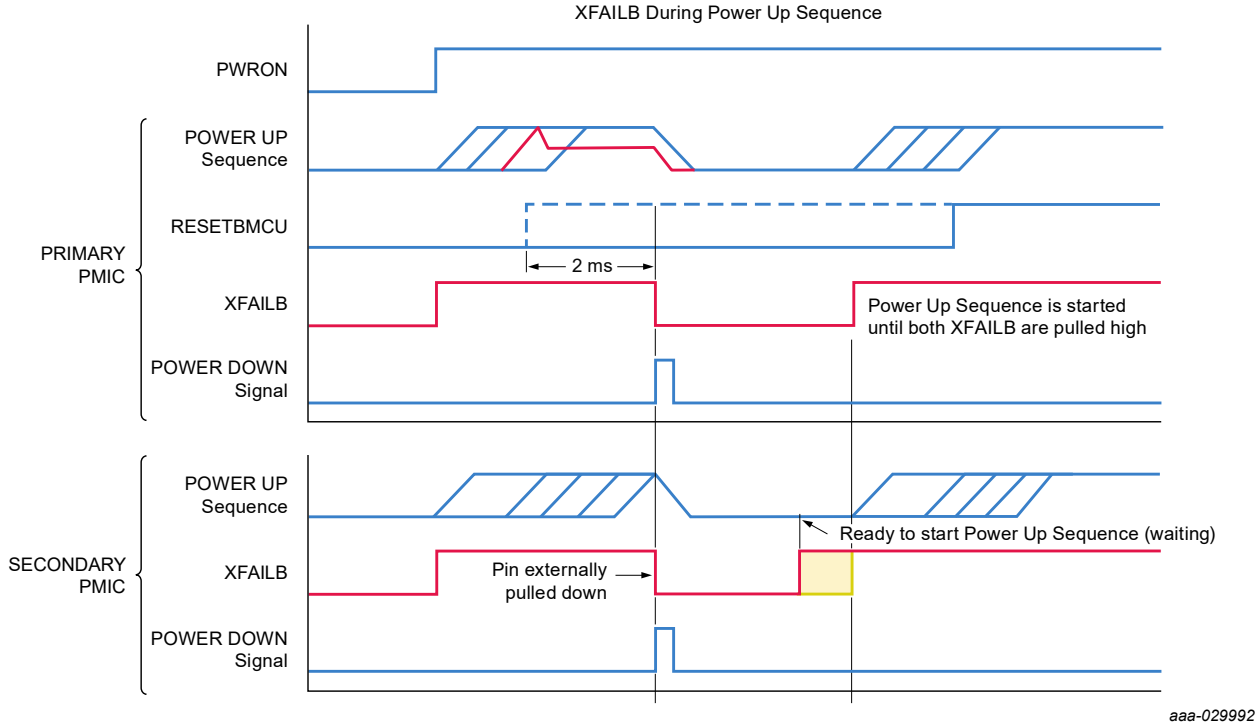

Figure 21. External XFAILB event during a power up sequence

14.9.11 SDA and SCL (I^2C bus)

Communication with the PF5024 is done through I^2C and it supports high-speed operation mode with up to 3.4 MHz operation. SDA and SCL are pulled up to VDDIO with 1.5 kΩ resistors.

The PF5024 is designed to operate as a secondary device during I^2C communication. The default I^2C device address is set by the OTP_I2C_ADD[2:0].

Table 34. I^2C address configuration

OTP_I2C_ADD[2:0]	Device address
000	0x08
001	0x09
010	0x0A
011	0x0B
100	0x0C
101	0x0D
110	0x0E
111	0x0F

See http://www.nxp.com/documents/user_manual/UM10204.pdf for detailed information on the digital I^2C communication protocol implementation.

During an I^2C transaction, the communication will latch after the 8th bit sent. If the data sent is not a multiple of 8 bit, any word with less than 8 bits will be ignored. If only 7 bits are sent, no data is written and the logic will not provide an ACK bit to the MCU.

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From an IC level, a wrong I^{2}C command can create a system level safety issue. For example, though the MCU may have intended to set a given regulator's output to 1.0 V, it may be erroneously registered as 1.1 V due to noise in the bus.

To prevent a wrong I^{2}C configuration, various protective mechanisms are implemented.

14.9.11.1 I^{2}C CRC verification

When this feature is enabled, a selectable CRC verification is performed on each I^{2}C transaction.

- When OTP_I2C_CRC_EN = 0, the CRC verification mechanism is disabled.
- When OTP_I2C_CRC_EN = 1, the CRC verification mechanism is enabled.

After each I^{2}C transaction, the device calculates the corresponding CRC byte to ensure the configuration command has not been corrupted.

When a CRC fault is detected, the PF5024 ignores the erroneous configuration command and triggers a CRC_I interrupt asserting the INTB pin, provided the interrupt is not masked.

The PF5024 implements a CRC-8-SAE, per the SAE J1850 specification.

- Polynomial = 0x11D
- Initial value = 0xFF

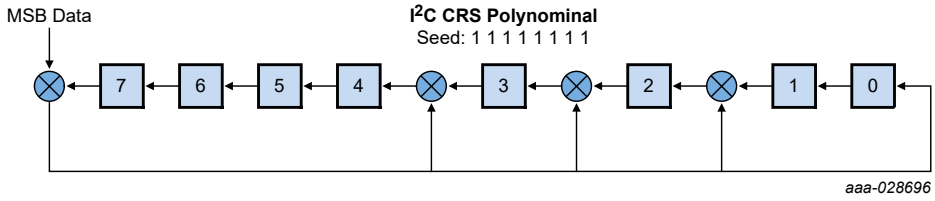

Figure 22. 8 bit SAE J1850 CRC polynomial

14.9.11.2 I^{2}C secure write

A secure write mechanism is implemented for specific registers critical to the functional safety of the device.

- When OTP_I2C_ SECURE_EN = 0, the secure write is disabled.
- When OTP_I2C_ SECURE_EN = 1, the secure write is enabled.

When the secure write is enabled, a specific sequence must be followed in order to grant writing access on the corresponding secure register.

Secure write sequence is as follows:

- MCU sends command to modify the secure registers
- PMIC generates a random code in the RANDOM_GEN register
- MCU reads the random code from the RANDOM_GEN register and writes it back on the RANDOM_CHK register

The PMIC compares the RANDOM_CHK against the RANDOM_GEN register:

- If RANDOM_CHK [7:0] = RANDOM_GEN[7:0], the device applies the configuration on the corresponding secure register, and self-clears both the RANDOM_GEN and RANDOM_CHK registers.
- If RANDOM_CHK[7:0] different from RANDOM_GEN[7:0], the device ignores the configuration command and self-clears both the RANDOM_GEN and RANDOM_CHK registers.

In the event the MCU sends any other command instead of providing a value for the RANDOM_CHK register, the state machine cancels the ongoing secure write transaction and performs the new I^{2}C command.

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In the event the MCU does not provide a value for the RANDOM_CHK register, the I^2C transaction will time out 10 ms after the RANDOM_GEN code is generated, and device is ready for a new transaction.

Table 35. Secure bits

Register	Bit	Description
ABIST OV1	AB_SWx_OV	Writing a 1 to this flag to clear the ABIST fault notification
ABIST UV1	AB_SWx_UV	Writing a 1 to this flag to clear the ABIST fault notification
ABIST RUN	AB_RUN	Writing a 1 starts an ABIST on demand
CTRL1	TMP_MON_EN	Writing a 0 disables the thermal monitor, preventing the thermal interrupts and thermal shutdown event from being detected
CTRL1	VIN_OVLO_EN	Writing a 0 disables the VIN overvoltage lockout monitor completely
CTRL1	WDI_MODE	Writing a 0 set the WDI event to soft WD reset Writing a 1 set the WDI event to hard WD reset
CTRL1	VIN_OVLO_SDWN	Writing a 0 disables a shutdown event upon a VIN overvoltage condition (only interrupts are provided)
CTRL1	WD_EN	Writing a 0 disables the watchdog counter block
CTRL1	WD_STBY_EN	Writing a 0 disables the watchdog counter during the standby mode
CTRL1	WDI_STBY_ACTIVE	Writing a 0 disables the monitoring of WDI input during standby mode
CTRL1	I2C_SECURE_EN	Writing a 0 disables de I^2C secure write mode
VMONENx	SWxVMON_EN	Writing a 0 disables the OV/UV monitor for SWx

15 Functional blocks

15.1 Analog core and internal voltage references

All regulators use the main bandgap as the reference for the output voltage generations, this bandgap is also used as reference for the internal analog core and digital core supplies. The performance of the regulators is directly dependent on the performance of the bandgap.

No external DC loading is allowed on V1P5A and V1P5D. V1P5D is kept powered as long as there is a valid supply and it may be used as a reference voltage for the VDDOTP and TBBEN pins during system power on.

The analog reference supply V1P5A is used as the internal reference supply for the voltage regulators. it is disabled in the LP_OFF state to achieve low quiescent currents. In applications where there is two or more PMICs supplying a system, the V1P5A may be used to pull up the XFAILB pin to achieve proper power up and power down synchronization during system operation.

A second bandgap is provided as the reference for all the monitoring circuits. This architecture allows the PF5024 to provide a reliable way to detect not only single point but also latent faults in order to meet the metrics required by an ASIL B level application.

Table 36. Internal supplies electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{1P5D}	V1P5D output voltage	1.50	1.60	1.65	V
C_{1P5D}	V1P5D output capacitor	—	1.0	—	µF
V_{1P5A}	V1P5A output voltage	1.50	1.60	1.65	V
C_{1P5A}	V1P5A output capacitor	—	1.0	—	µF

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15.2 Type 1 buck regulators (SWx)

The PF5024 features four low voltage regulators with input supply range from 2.5 V to 5.5 V and output voltage range from 0.4 V to 1.8 V in 6.25 mV steps. Each voltage regulator is capable to supply 2.5 A and features a programmable soft-start and DVS ramp for system power optimization.

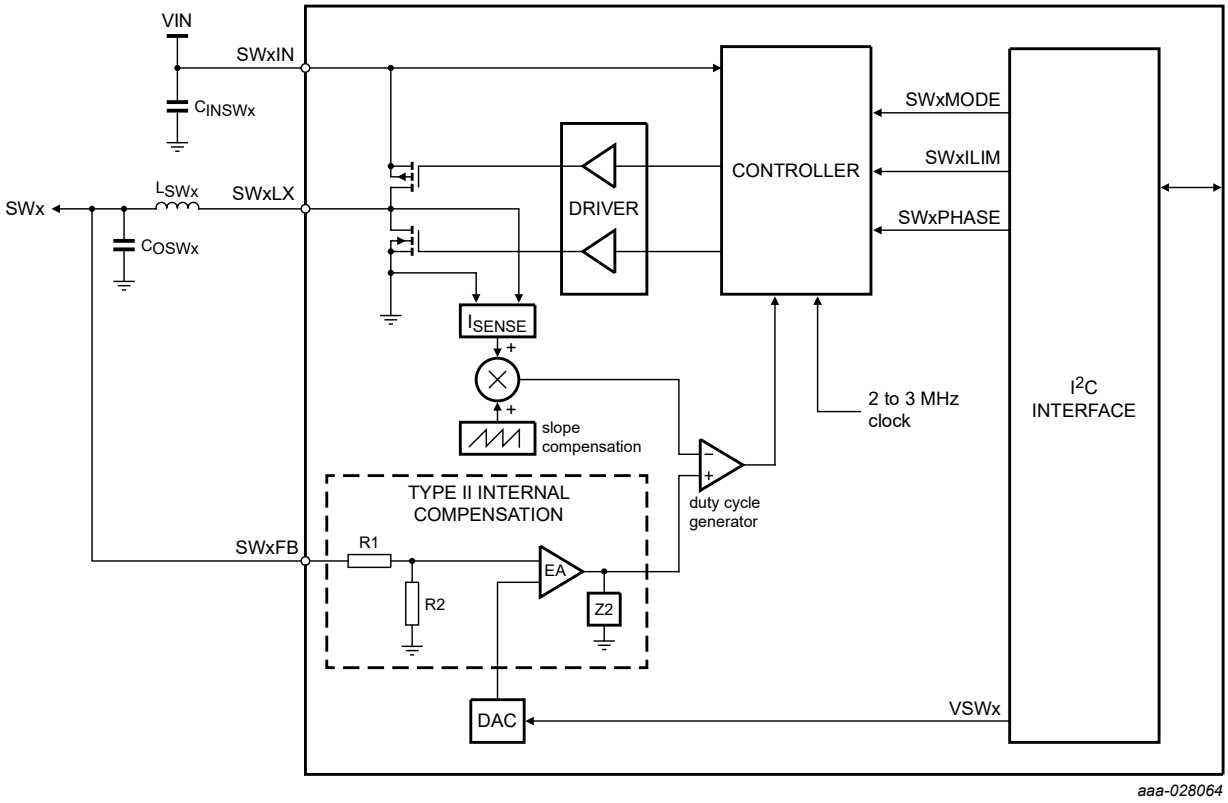

Figure 23. Buck regulator block diagram

The OTP_SWxDVS_RAMP bit sets the default step/time ratio for the power up ramp during the power up/down sequence as well as the DVS slope during the system On.

The power down ramp and DVS rate during the system On of SW1 to SW4 can be modified during the system On state by changing the SWxDVS_RAMP bit on the I^2C register map.

The DVS ramp rate between 0.4 V and 1.5 V output setting is based on the internal clock configuration as shown in Table 37.

The ramp rate at 1.8 V output setting is 20 % faster than the values in Table 37.

Table 37. SWx ramp rates

All ramp rates are typical values.
Clock frequency tolerance = ± 6 %.

CLK_ FREQ[3:0]	Switching regulators frequency (MHz)	DVS_RAMP = 00		DVS_RAMP = 01		DVS_RAMP = 10		DVS_RAMP = 11	
		Ramp up rate (mV/µs)	Ramp down rate (mV/µs)	Ramp up rate (mV/µs)	Ramp down rate (mV/µs)	Ramp up rate (mV/µs)	Ramp down rate (mV/µs)	Ramp up rate (mV/µs)	Ramp down rate (mV/µs)
0000	2.500	7.81	5.21	15.63	10.42	3.91	2.60	1.95	1.30
0001	2.625	8.20	5.47	16.41	10.94	4.10	2.73	2.05	1.37
0010	2.750	8.59	5.73	17.19	11.46	4.30	2.86	2.15	1.43
0011	2.875	8.98	5.99	17.97	11.98	4.49	2.99	2.25	1.50
0100	3.000	9.38	6.25	18.75	12.50	4.69	3.13	2.34	1.56
1001	2.000	6.25	4.17	12.50	8.33	3.13	2.08	1.56	1.04

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Table 37. SWx ramp rates*...continued*

All ramp rates are typical values.
Clock frequency tolerance = ± 6 %.

CLK_ FREQ[3:0]	Switching regulators frequency (MHz)	DVS_RAMP = 00		DVS_RAMP = 01		DVS_RAMP = 10		DVS_RAMP = 11	
		Ramp up rate (mV/µs)	Ramp down rate (mV/µs)	Ramp up rate (mV/µs)	Ramp down rate (mV/µs)	Ramp up rate (mV/µs)	Ramp down rate (mV/µs)	Ramp up rate (mV/µs)	Ramp down rate (mV/µs)
1010	2.125	6.64	4.43	13.28	8.85	3.32	2.21	1.66	1.11
1011	2.250	7.03	4.69	14.06	9.38	3.52	2.34	1.76	1.17
1100	2.375	7.42	4.95	14.84	9.90	3.71	2.47	1.86	1.24

Buck regulators SWx use 8 bits to set the output voltage.

- The VSWx_RUN[7:0] set the output voltage during Run mode.
- The VSWx_STBY[7:0] set the output voltage during Standby mode.

The default output voltage configuration for Run and Standby modes is loaded from the OTP_VSWx[7:0] registers upon power up.

Table 38. SWx output voltage configuration

Set point	VSWx_RUN[7:0] VSWx_STBY[7:0]	V_{SWxFB} (V)
0	00000000	0.40000
1	00000001	0.40625
2	00000010	0.41250
3	00000011	0.41875
. .	. .	. .
175	10101111	1.49375
176	10110000	1.50000
177	10110001	1.80000
178 to 255	10110010 to 11111111	Reserved

DVS operation is available for all voltage settings between 0.4 V to 1.5 V. However, the SWx regulator is not intended to perform DVS transitions to or from the 1.8 V configuration. In the event a voltage change is requested between any of the low voltage settings and 1.8 V, the switching regulator is automatically disabled first and then re-enabled at the selected voltage level to avoid an uncontrolled transition to the new voltage setting.

Each regulator is provided with two bits to set its mode of operation.

- The SWx_RUN_MODE[1:0] bits allow the user to change the mode of operation of the SWx regulators during the run state. If the regulator was programmed as part of the power up sequence, the SWx_RUN_MODE[1:0] bits are loaded with 0b11 (autoskip) by default. Otherwise it is loaded with 0b00 (disabled).
- The SWx_STBY_MODE[1:0] bits allow the user to change the mode of operation of the SWx regulators during the standby state. If the regulator was programmed as part of the power up sequence, the SWx_STBY_MODE[1:0] bits are loaded with 0b11 (autoskip) by default. Otherwise it is loaded with 0b00 (disabled).

Table 39. SWx regulator mode configuration

SWx_MODE[1:0]	Mode of operation
00	OFF
01	PWM mode
10	PFM mode

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Table 39. SWx regulator mode configuration*...continued*

SWx_MODE[1:0]	Mode of operation
11	Auto skip mode

The SWx_MODE_I interrupt asserts the INTB pin when any of the Type 1 regulators have changed the mode of operation, provided the corresponding interrupt is not masked.

To avoid potential detection of an OV/UV fault during SWx ramp up, it is recommended to power up the regulator in PWM or autoskip mode.

SWx regulators use 2 bits SWxILIM[1:0], to program the current limit detection.

Table 40. SWx current limit selection

SWxILIM[1:0]	Typical current limit
00	2.1 A
01	2.6 A
10	3.0 A
11	4.5 A

The current limit specification is given with respect to the inductor peak current. To calculate the DC current at which the buck regulator would enter into current limitation, it is necessary to calculate the inductor ripple current. An ideal approximation is enough to obtain the ripple current as follows:

$$\Delta iL = [(VIN-VOUT) \times (VOUT/VIN)]/(L \times FSW)$$

Where L is the inductance value and Fsw is the selected switching frequency.

The DC current limit is then calculated by

$$DC\ ILIM = ILIM - (\Delta iL / 2)$$

In order to account for component tolerances, use the minimum inductor value per the inductor specification.

During single phase operation, all buck regulators use 3 bits (SWxPHASE[2:0]) to control the phase shift of the switching frequency. Upon power up, the switching phase of all regulators is defaulted to 0 degrees and can be modified during the system On state.

Table 41. SWx phase configuration

SWx_PHASE[2:0]	Phase shift [degrees]
000	45
001	90
010	135
011	180
100	225
101	270
110	315
111	0 (default)

Each one of the buck regulator provides 2 OTP bits to configure the value of the inductor used in the corresponding block. The OTP_SWx_LSELECT[1:0] allows to choose the inductor as shown in Table 42.

Table 42. SWx inductor selection bits

OTP_SWx_LSELECT[1:0]	Inductor value
00	1.0 µH

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Table 42. SWx inductor selection bits*...continued*

OTP_SWx_LSELECT[1:0]	Inductor value
01	0.47 µH
10	1.5 µH
11	Reserved

15.2.1 SW2 VTT operation

SW2 features a selectable VTT mode to create VTT termination for DDR memories.

When SW2_VTTEN = 1, the VTT mode is enabled. In this mode, SW2 reference voltage is internally connected to SW1FB output through a divider by 2.

During the VTT mode, the DVS operation on SW2 is disabled and SW2 output is given by V_{SW1FB} / 2. In this mode, the minimum output voltage configuration for SW1 should be 800 mV to ensure the SW2 is still within the regulation range at its output.

During the power up sequence, the SW2 (VTT) may be turned on in the same or at a slot higher than SW1, as required by the system. When SW2 and SW1 are enabled in the same slot, SW2 will always track the VSW1/2. When SW2 is enabled after SW1, it will ramp up gradually to a predefined voltage and once this voltage is reached, it will start tracking VSW1/2. The user may adjust the value at which the SW2 should start tracking the voltage on the SW1 regulator by setting the OTP_VSW2 register accordingly.

During normal operation, if the SW1 is disabled via the I^2C command, SW2 tracks the output of SW1 and both regulators are discharged together and pulled down internally. When SW1 is enabled back via the I^2C commands, the SW1 output ramps up to the corresponding voltage while SW2 is always VSW1/2.

When only SW2 is disabled the PMIC uses the OTP_VTT_PDOWN bit to program whether the SW2 regulator is disabled with the output in high impedance or discharged internally.

- When OTP_VTT_PDOWN = 0, the output is disabled in high impedance mode.
- When OTP_VTT_PDOWN = 1, the output is disabled with the internal pull down enabled.

When SW2 is requested to enable back again, the SW2 ramps up to the voltage set on the VSW2_RUN or VSW2_STBY registers. Once it reaches the final DVS value, it will change its reference to start tracking SW1 output again. Note that VSW2_RUN(STBY) must be set to VSW1_RUN(STBY)/2 or the closest code by the MCU to ensure proper operation.

When operating in VTT mode, the minimum output voltage configuration for SW1 should be 800 mV to ensure the SW2 is still within the regulation range at its output.

15.2.2 Multiphase operation

Regulators SW1, SW2, SW3 and SW4 can be configured in dual, triple and quad phase mode. In this mode, SW1 registers control the output voltage and other configurations. Likewise, SW1FB pin becomes the main feedback node for the resulting voltage rail, however the two FB pins should be connected together.

The OTP_SW1CONFIG[1:0] bits are used to select the multiphase configuration for SW1/SW2/SW3/SW4.

Table 43. OTP_SW1CONFIG register description

OTP_SW1CONFIG[1:0]	Description
00	SW1 and SW2 operate in single phase mode
01	SW1/SW2 operate in dual phase mode
10	SW1/SW2/SW3/SW4 operate in quad phase mode
11	SW1/SW2/SW3 operate in triple phase mode

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The OTP_SW4CONFIG[1:0] bits are used to select the dual phase operation of SW3/SW4, if the OTP_SW1CONFIG[1:0] bits are set at 0b00 or 0b01.

Table 44. OTP_SW4CONFIG register description

OTP_SW4CONFIG[1:0]	Description
00	SW3 and SW4 operate in single phase mode
01	SW3/SW4 operate in dual phase mode
10	Reserved
11	Reserved

15.2.3 Electrical characteristics

Table 45. Type 1 buck regulator electrical characteristics

All parameters are specified at T_A = −40 to 125 °C, V_{SWxIN} = UVDET to 5.5 V, V_{SWxFB} = 1.0 V, I_{SWx} = 500 mA, typical external component values, f_{SW} = 2.25 MHz, unless otherwise noted. Typical values are characterized at V_{SWxIN} = 5.0 V, V_{SWxFB} = 1.0 V, I_{SWx} = 500 mA, and T_A = 25 °C, unless otherwise noted.

Symbol	Parameter [1][2]	Min	Typ	Max	Unit
V_{SWxIN}	Operating functional input voltage	UVDET	—	5.5	V
V_{SWxACC}	Output voltage accuracy PWM mode 0.4 V ≤ V_{SWxFB} ≤ 0.8 V 0 ≤ I_{SWx} ≤ 2.5 A	−10	—	10	mV
V_{SWxACC}	Output voltage accuracy PWM mode 0.8 V < V_{SWxFB} ≤ 1.0 V 0 ≤ I_{SWx} ≤ 2.5 A	−2.0	—	2.0	%
V_{SWxACC}	Output voltage accuracy PWM mode 1.0 V < V_{SWxFB} ≤ 1.5 V 0 ≤ I_{SWx} ≤ 2.5 A	−1.5	—	1.5	%
V_{SWxACC}	Output voltage accuracy PWM mode V_{SWxFB} = 1.8 V 0 ≤ I_{SWx} ≤ 2.5 A	−1.5	—	1.5	%
$V_{SWxACCPFM}$	Output voltage accuracy PFM mode 0.4 V ≤ V_{SWxFB} ≤ 1.5 V 0 ≤ I_{SWx} ≤ 100 mA	−36	—	36	mV
$V_{SWxACCPFM}$	Output voltage accuracy PFM mode V_{SWxFB} = 1.8 V 0 ≤ I_{SWx} ≤ 100 mA	−57	—	57	mV
$t_{PFMtoPWM}$	PFM to PWM transition time	30	—	—	µs
I_{SWx}	Max load current in single phase [3]	2500	—	—	mA
I_{SWx_DP}	Max load current in dual phase [3]	5000	—	—	mA
I_{SWx_TP}	Max load current in triple phase [3]	7500	—	—	mA
I_{SWx_QP}	Max load current in quad phase [3]	10000	—	—	mA
I_{SWxLIM}	Current limiter - inductor peak current detection SWxILIM[1:0] = 00	1.6	2.1	2.5	A
I_{SWxLIM}	Current limiter - inductor peak current detection SWxILIM[1:0] = 01	2.0	2.6	3.1	A
I_{SWxLIM}	Current limiter - inductor peak current detection SWxILIM[1:0] = 10	2.4	3.0	3.7	A
I_{SWxLIM}	Current limiter - inductor peak current detection SWxILIM[1:0] = 11	3.6	4.5	5.45	A

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Table 45. Type 1 buck regulator electrical characteristics*...continued*

All parameters are specified at T_A = −40 to 125 °C, V_{SWxIN} = UVDET to 5.5 V, V_{SWxFB} = 1.0 V, I_{SWx} = 500 mA, typical external component values, f_{SW} = 2.25 MHz, unless otherwise noted. Typical values are characterized at V_{SWxIN} = 5.0 V, V_{SWxFB} = 1.0 V, I_{SWx} = 500 mA, and T_A = 25 °C, unless otherwise noted.

Symbol	Parameter [1][2]	Min	Typ	Max	Unit
$I_{SWxNLIM}$	Negative current limit in single phase mode	0.6	1.0	1.4	A
$I_{SWxxLIM_DP}$	Current limit in dual phase operation SWxILIM = 00 (primary)	3.2	4.2	5.0	A
$I_{SWxxLIM_DP}$	Current limit in dual phase operation SWxILIM = 01 (primary)	4.0	5.2	6.2	A
$I_{SWxxLIM_DP}$	Current limit in dual phase operation SWxILIM = 10 (primary)	4.8	6.0	7.4	A
$I_{SWxxLIM_DP}$	Current limit in dual phase operation SWxILIM = 11 (primary)	7.2	9.0	10.9	A
$I_{SWxxLIM_TP}$	Current limit in triple phase operation SWxILIM = 00 (primary)	4.8	6.3	7.5	A
$I_{SWxxLIM_TP}$	Current limit in triple phase operation SWxILIM = 01 (primary)	6.0	7.8	9.3	A
$I_{SWxxLIM_TP}$	Current limit in triple phase operation SWxILIM = 10 (primary)	7.2	9.0	11.1	A
$I_{SWxxLIM_TP}$	Current limit in triple phase operation SWxILIM = 11 (primary)	10.8	13.5	16.35	A
$I_{SWxxLIM_QP}$	Current limit in quad phase operation SWxILIM = 00 (primary)	6.4	8.4	10.0	A
$I_{SWxxLIM_QP}$	Current limit in quad phase operation SWxILIM = 01 (primary)	8.0	10.4	12.4	A
$I_{SWxxLIM_QP}$	Current limit in quad phase operation SWxILIM = 10 (primary)	9.6	12.0	14.8	A
$I_{SWxxLIM_QP}$	Current limit in quad phase operation SWxILIM = 11 (primary)	14.4	18.0	21.8	A
V_{SWxOSH}	Startup overshoot SWxDVS RAMP = 6.25 mV/µs VSWxIN = 5.5 V, VSWxFB= 1.0 V	−25	25	50	mV
$t_{ONSWxMAX}$	Maximum turn on time From enable to 90 % of end value SWxDVS RAMP = 11 (1.56 mV/µs, 2 MHz) VSWxIN = 5.5 V, VSWxFB= 1.5 V	—	—	895	µs
t_{ONSWx_MIN}	Minimum turn on time From enable to 90 % of end value SWxDVS RAMP = 01 (18.75 mV/µs, 3 MHz) VSWxIN = 5.5 V, VSWxFB= 0.4 V	49.2	—	—	µs
η_{SWx}	Efficiency (PFM mode, 1.0 V, 1.0 mA)	—	80	—	%
η_{SWx}	Efficiency (PFM mode, 1.0 V, 50 mA)	—	81	—	%
η_{SWx}	Efficiency (PFM Mode, 1.0 V, 100 mA)	—	82	—	%
η_{SWx}	Efficiency (PWM mode, 1.0 V, 500 mA)	—	83	—	%
η_{SWx}	Efficiency (PWM mode, 1.0 V, 1000 mA)	—	82	—	%
η_{SWx}	Efficiency (PWM mode, 1.0 V, 2000 mA)	—	79	—	%
$V_{SWxLOTR}$	Transient load regulation (overshoot/undershoot) at 0.8 V < VSWxFB ≤ 1.2 V, COUT = 44 µF per phase ILOAD = 200 mA to 1.0 A, di/dt = 2.0 A/µs (Single phase) ILOAD = 400 mA to 2.0 A, di/dt = 4.0 A/µs (Dual phase) ILOAD = 600 mA to 3.0 A, di/dt = 6.0 A/µs (Triple phase) ILOAD = 800 mA to 4.0 A, di/dt = 8.0 A/µs (Quad phase)	−25	—	25	mV

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Table 45. Type 1 buck regulator electrical characteristics*...continued*

All parameters are specified at T_A = −40 to 125 °C, V_{SWxIN} = UVDET to 5.5 V, V_{SWxFB} = 1.0 V, I_{SWx} = 500 mA, typical external component values, f_{SW} = 2.25 MHz, unless otherwise noted. Typical values are characterized at V_{SWxIN} = 5.0 V, V_{SWxFB} = 1.0 V, I_{SWx} = 500 mA, and T_A = 25 °C, unless otherwise noted.

Symbol	Parameter [1][2]	Min	Typ	Max	Unit
$V_{SWxLOTR}$	Transient load regulation (overshoot/undershoot) at 1.25 V < VSWxFB ≤ 1.8 V, COUT = 44 µF per phase ILOAD = 200 mA to 1.0 A, di/dt = 2.0 A/µs (Single phase) ILOAD = 400 mA to 2.0 A, di/dt = 4.0 A/µs (Dual phase) ILOAD = 600 mA to 3.0 A, di/dt = 6.0 A/µs (Triple phase) ILOAD = 800 mA to 4.0 A, di/dt = 8.0 A/µs (Quad phase)	−3.0	—	3.0	%
F_{SWx}	PWM switching frequency range Frequency set by CLK_FREQ[3:0]	1.9	2.5	3.15	MHz
$T_{OFFminSWx}$	Minimum off time	—	27	—	ns
T_{DBSWx}	Deadband time	—	3.0	—	ns
T_{slew}	Slewing time (10 % to 90 %)	—	—	5.0	ns
D_{VSWx}	Output ripple in PWM mode at V_{SWxFB} = 1.0 V	—	—	1.0	%
I_{RCS}	DCM (skip mode) reverse current sense threshold Current flowing from PGND to SWxLX	−200	—	200	mA
I_{SWxQ}	Quiescent current PFM mode	—	14	—	µA
I_{SWxQ}	Quiescent current Auto skip mode	—	160	250	µA
I_{SWxQ_DP}	Quiescent current in dual phase PWM mode	—	200	320	µA
I_{SWxQ_QP}	Quiescent current in quad phase PWM mode	—	240	480	µA
$R_{ONSWxHS}$	SWx high-side P-MOSFET $R_{DS(on)}$ [4]	—	—	135	mΩ
$R_{ONSWxLS}$	SWx low-side N-MOSFET $R_{DS(on)}$ [4]	—	—	80	mΩ
R_{SWxDIS}	Discharge resistance Regulator disabled and ramp down completed	50	100	200	Ω

[1] For VSWx configurations greater than 1.35 V, full parametric operation is guaranteed for 2.7 V < SWxVIN < 5.5 V. Below 2.7 V, the SWx regulators are fully functional with degraded operation due to headroom limitation.

[2] For VSWx = 1.8 V, output capacitance should be kept at or below the maximum recommended value. Likewise, it is recommended to use the slow turn on/off ramp rate to ensure the output is discharged completely when it is disabled.

[3] The Type 1 buck regulator in single or multiphase configuration is capable of providing output current above the nominal max current specification as long as it does not reach the current limitation. However, if operating above the nominal maximum current, overall thermal considerations must be taken into account to prevent PMIC thermal shutdown during high ambient temperature conditions.

[4] Max $R_{DS(on)}$ does not include bondwire resistance. Consider +/- 50 % tolerance to account for bondwire and pin loss.

Table 46. Recommended external components

Symbol	Parameter	Min	Typ	Max	Unit
L	Output inductor [1] Maximum inductor DC resistance 50 mΩ Minimum saturation current at full load: 3.0 A	0.47	1.0	1.5	µH
C_{out}	Output capacitor Use 2 × 22 µF, 6.3 V X7T ceramic capacitor to reduce output capacitance ESR	35	44	53	µF
C_{in}	Input capacitor 4.7 µF, 10 V X7R ceramic capacitor	4.23	4.7	5.17	µF

[1] Keep inductor DCR as low as possible to improve regulator efficiency.

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15.3 Voltage monitoring

The PF5024 provides OV and UV monitoring capability for the following voltage regulators:

- SW1, SW2, SW3, SW4

A programmable UV threshold is selected via the OTP_SWxUV_TH[1:0]. UV threshold selection represents a percentage of the nominal voltage programmed on each regulator.

Table 47. UV threshold configuration register

OTP_SWxUV_TH[1:0]	UV threshold level
00	95 %
01	93 %
10	91 %
11	89 %

A programmable OV threshold is selected via the OTP_SWxOV_TH[1:0]. OV threshold selection represents a percentage of the nominal voltage programmed on each regulator.

Table 48. OV threshold configuration register

OTP_SWxOV_TH	OV threshold level
00	105 %
01	107 %
10	109 %
11	111 %

Two functional bits are provided to program the UV debounce time for the voltage regulators.

Table 49. UV debounce timer configuration

UV_DB[1:0]	UV debounce time
00	5 µs
01	15 µs
10	30 µs
11	40 µs

The default value of the UV_DB[1:0] upon a full register reset is 0b10.

Two functional bits to program the OV debounce time for all the voltage regulators.

Table 50. OV debounce timer configuration

OV_DB[1:0]	OV debounce time
00	30 µs
01	50 µs
10	80 µs
11	125 µs

The default value of the OV_DB[1:0] upon a full register reset is 0b00.

The VMON_EN bits enable or disable the OV/UV monitor for each one of the external regulators (SWxVMON_EN).

- When the VMON_EN bit of a specific regulator is 1, the voltage monitor for that specific regulator is enabled.

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- When the VMON_EN bit of a specific regulator is 0, the voltage monitor for that specific regulator is disabled.

By default, the VMON_EN bits are set to 1 on power up.

When the I2C_SECURE_EN = 1, a secure write must be performed to set or clear the VMON_EN bits to enable or disable the voltage monitoring for a specific regulator.

On enabling a regulator, the UV/OV monitor is masked until the corresponding regulator reaches the point of regulation. If a voltage monitor is disabled, the UV_S and OV_S indicators from that monitor are reset to 0.

Figure 24 shows the PF5024 voltage monitoring architecture.

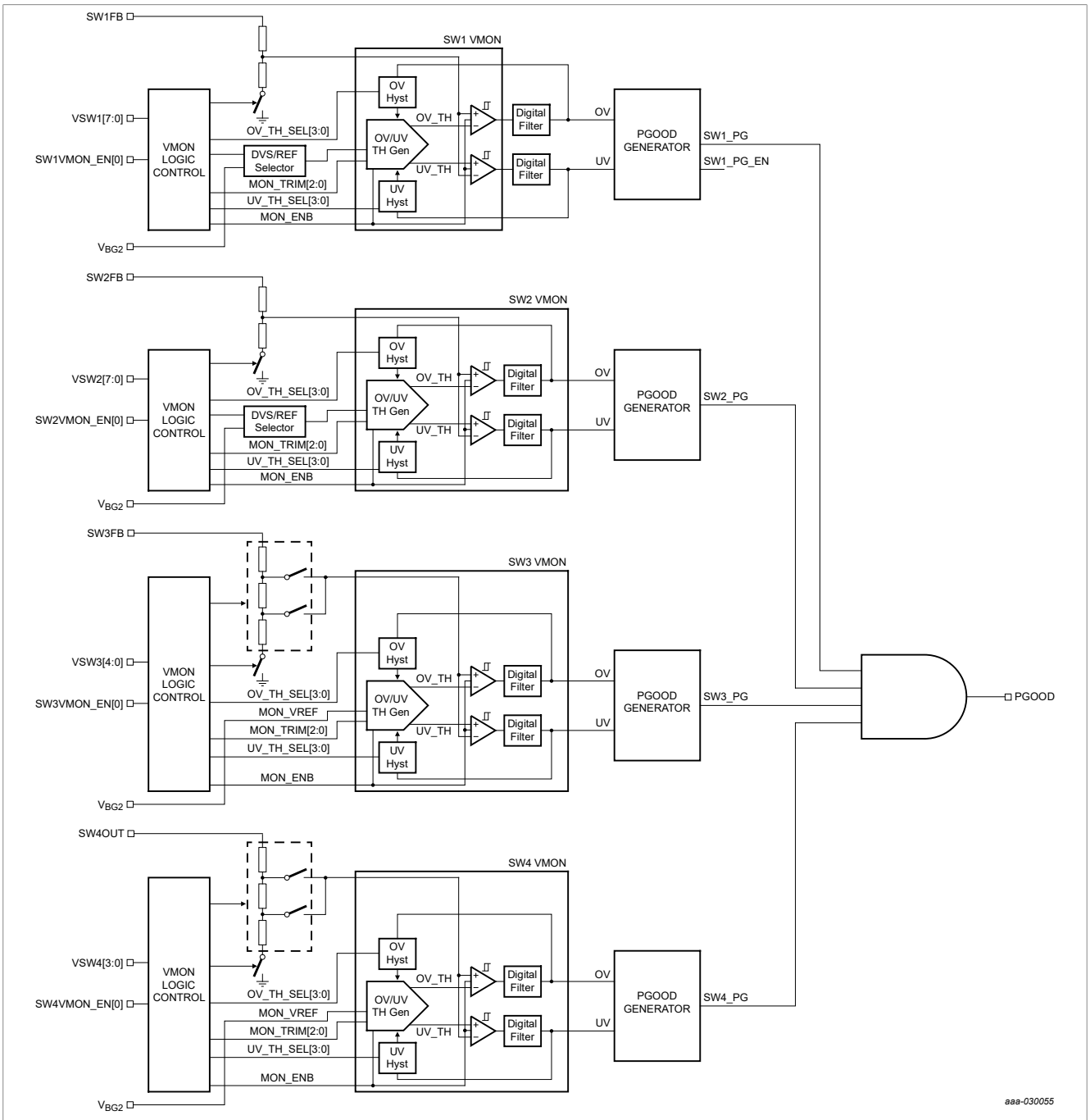

Figure 24. Voltage monitoring architecture

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15.3.1 Electrical characteristics

Table 51. VMON electrical characteristics

All parameters are specified at T_A = –40 °C to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5.0 V, V_{xFB} = 1.5 V (Type 1 Buck regulator), and T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
I_{QON}	Block quiescent current, when block is enabled one block per regulator one block per regulator	—	10	13	µA
I_{OFF}	Block leakage current when disabled	—	—	500	nA
t_{ON_MON}	Voltage monitor settling time after enabled	—	—	30	µs
$V_{xFBUVHysteresis}$	Power good (UV) hysteresis Voltage difference between UV rising and falling thresholds	—	0.5	—	%
V_{UV_Tol}	Undervoltage falling threshold accuracy With respect to target feedback voltage tolerance For type 1 switching regulator when V_{SWxFB} > 0.75 V	−2	—	2	%
V_{UV_Tol}	Under voltage falling threshold accuracy With respect to target feedback voltage For type 1 switching regulator when VSWxFB ≤ 0.75 V	−3	—	3	%
t_{UV_DB}	Power good (UV) debounce time UV_DV = 00	2.5	5.0	7.5	µs
	Power good (UV) debounce time UV_DV = 01	10	15	20	
	Power good (UV) debounce time UV_DV = 10	20	30	40	
	Power good (UV) debounce time UV_DV = 11	25	40	55	
V_{OV_Tol}	Overvoltage rising threshold accuracy With respect to target feedback voltage tolerance For type 1 switching regulator when V_{SWxFB} > 0.75 V	−2	—	2	%
V_{OV_Tol}	Overvoltage rising threshold With respect to target feedback voltage tolerance For type 1 switching regulator when V_{SWxFB} ≤ 0.75 V	−3	—	3	%
$V_{xFBOVHysteresis}$	Overvoltage (OV) hysteresis Voltage difference between OV rising and falling thresholds	—	0.5	—	%
t_{OV_DB}	Power good (OV) debounce time OV_DV = 00	20	30	40	µs
	Power good (OV) debounce time OV_DV = 01	35	50	65	
	Power good (OV) debounce time OV_DV = 10	55	80	105	
	Power good (OV) debounce time OV_DV = 11	90	135	160	

15.4 Clock management

The clock management provides a top-level management control scheme of internal clock and external synchronization intended to be primarily used for the switching regulators. The clock management incorporates various subblocks:

- Low power 100 kHz clock
- Internal high frequency clock with programmable frequency
- Phase Locked Loop (PLL)

A digital clock management interface is in charge of supporting interaction among these blocks.

The clock management provides clocking signals for the internal state machine, the switching frequencies for the buck converters as well as the multiples of those switching frequencies in order to enable phase shifting for multiple phase operation.

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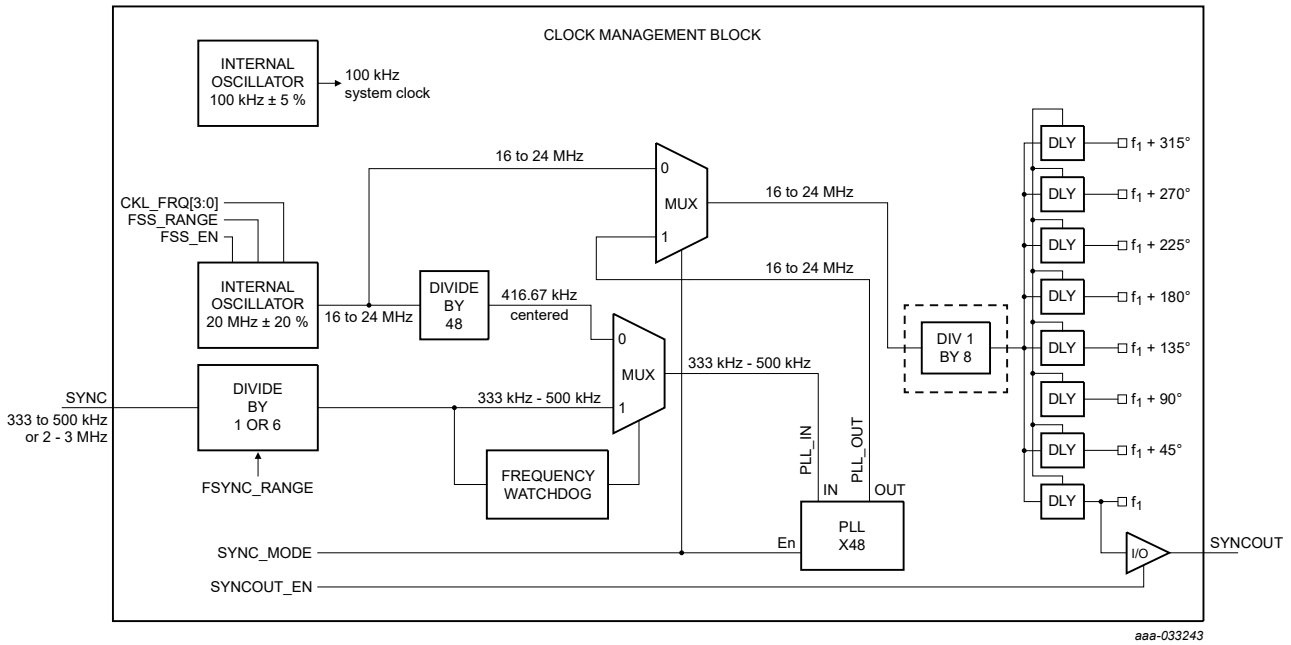

Figure 25. Clock management architecture

15.4.1 Low frequency clock

A low power 100 kHz clock is provided for overall logic and digital control. Internal logic and debounce timers are based on this 100 kHz clock.

15.4.2 High frequency clock

The PF5024 features a high frequency clock with nominal frequency of 20 MHz. Clock frequency is programmable over a range of ±20 % via the CLK_FREQ[3:0] control bits.

15.4.3 Manual frequency tuning

The PF5024 features a manual frequency tuning to set the switching frequency of the high frequency clock. The CLK_FREQ [3:0] bits allow a manual frequency tuning of the high frequency clock from 16 MHz to 24 MHz.

If a frequency change of two or more steps is requested by a single I^2C command, the device performs a gradual frequency change passing through all steps in between with a 5.2 µs time between each frequency step. When the frequency reaches the programmed value, The FREQ_RDY_I asserts the INTB pin, provided it is not masked.

When the internal clock is used as the main frequency for the power generation, an internal frequency divider by 8 is used to generate the switching frequency for all the buck regulators. Adjusting the frequency of the high frequency clock allows for manual tuning of the switching frequencies for the buck regulators from 2.0 MHz to 3.0 MHz.

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Table 52. Manual frequency tuning configuration

CLK_FREQ[3:0]	High speed clock frequency (MHz)	Switching regulators frequency (MHz)
0000	20	2.500
0001	21	2.625
0010	22	2.750
0011	23	2.875
0100	24	3.000
0101	Not used	Not used
0110	Not used	Not used
0111	Not used	Not used
1000	Not used	Not used
1001	16	2.000
1010	17	2.125
1011	18	2.250
1100	19	2.375
1101	Not used	Not used
1110	Not used	Not used
1111	Not used	Not used

The default switching frequency is set by the OTP_CLK_FREQ[3:0] bits.

Manual tuning cannot be applied when frequency spread-spectrum or external clock synchronization is used. However, during external clock synchronization, it is recommended to program the CLK_FREQ[3:0] bits to match the external frequency as close as possible.

15.4.4 Spread-spectrum

The internal clock provides a programmable frequency spread spectrum with two ranges for narrow spread and wide spread to help manage EMC in the automotive applications.

- When the FSS_EN = 1, the frequency spread-spectrum is enabled.
- When the FSS_EN = 0, the frequency spread-spectrum is disabled.

The default state of the FSS_EN bit upon a power up can be configured via the OTP_FSS_EN bit.

The FSS_RANGE bit is provided to select the clock frequency range.

- When FSS_RANGE = 0, the maximum clock frequency range is ±5 %.
- When FSS_RANGE = 1, the maximum clock frequency range is ±10 %.

The default value of the FSS_RANGE bit upon a power up can be configured via the OTP_FSS_RANGE bit.

The frequency spread-spectrum is performed at a 24 kHz modulation frequency when the internal high frequency clock is used to generate the switching frequency for the switching regulators. When the external clock synchronization is enabled, the spread-spectrum is disabled.

Figure 26 shows implementation of spread-spectrum for two settings.

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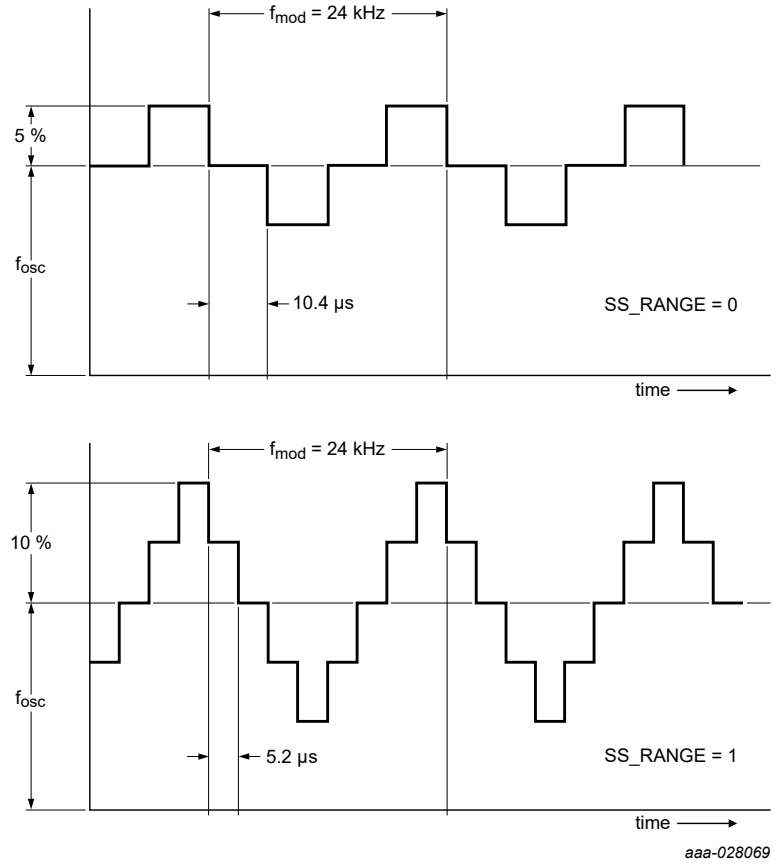

Figure 26. Spread-spectrum waveforms

If the frequency spread-spectrum is enabled, the switching regulators should be set in PWM mode to ensure clock synchronization at all time.

If the external clock synchronization is enabled, (SYNC_MODE = 1), the spread spectrum is disabled regardless of the value of the FSS_EN bit.

15.4.5 Clock synchronization

An external clock can be fed via the SYNC pin to synchronize the switching regulators to this external clock.

When the OTP_SYNC_MODE = 0, the external clock synchronization is disabled. In this case, the PLL is disabled, and the device always uses the internal high frequency clock to generate the main frequency for the switching regulators.

When the OTP_SYNC_MODE = 1, the external clock synchronization is enabled. In this case, the internal PLL is always enabled and it uses either the internal high frequency clock or the SYNC pin as the source to generate the main frequency for the switching regulators.

If the SYNCIN function is not used, the pin should be grounded. If the external clock is meant to start up after the PMIC has started, the SYNC pin must be maintained low until the external clock is applied.

The SYNC pin is prepared to detect clock signals with a 1.8 V or 3.3 V amplitude and within the frequency range set by the FSYNC_RANGE bit.

- When the FSYNC_RANGE = 0, the input frequency range at SYNC pin should be between 2000 kHz and 3000 kHz.

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- When the FSYNC_RANGE = 1, the input frequency range at SYNC pin should be between 333 kHz and 500 kHz.

The OTP_FSYNC_RANGE bit is used to select the default frequency range accepted in the SYNC pin.

The external clock duty cycle at the SYNC pin should be between 40 % and 60 %. An input frequency in the SYNC pin outside the range defined by the FSYNC_RANGE bit is detected as invalid. If the external clock is not present or invalid, the device automatically switches to the internal clock and sets the FSYNC_FLT_I interrupt, which in turn asserts the INTB pin provided it is not masked.

The FSYNC_FLT_S bit is set to 1 as long as the input frequency is not preset or invalid, and it is cleared to 0 when the SYNC has a valid input frequency.

The device switches back to the external switching frequency only when both, the FSYNC_FLT_I interrupt has been cleared and the SYNC pin sees a valid frequency.

When the external clock is selected, the switching regulators should be set in PWM mode to ensure clock synchronization at all time.

Upon an external clock failure, the MCU must ensure the integrity of the external clock by implementing a three step diagnostic strategy.

1. MCU shall acknowledge and find the source of the interrupt event.
2. After deciding the interrupt is generated by the FSYNC_FLT_I event, the MCU must read the FSYNC_FLT_S bit to verify if the fault condition is persistent or not.
3. a. If FSYNC_FLT_S bit is 0, the fault condition can be considered as a transient condition and the system is ready to switch over to the external clock by clearing the FSYNC_FLT_I flag.
   b. If the FSYNC_FLT_S bit is 1, the fault is considered a persistent fault and the MCU must take corrective action to send the system to safe operation.

It is responsibility of the system designer to define the tolerance time to allow the external frequency to be lost before taking a corrective action such as stopping the system or placing the system in safe state in safety related applications.

When the OTP_SYNC_MODE = 0 and OTP_SYNCOUT_EN = 1, the SYNC pin is used to synchronize an external device to the PF5024.

The SYNC pin outputs the main frequency used for the switching regulators in the range of 2.0 MHz to 3.0 MHz. The SYNCOUT_EN bit can be used to enable or disable the SYNCOUT feature via I^2C during the system On state.

- When SYNCOUT_EN = 0, the SYNCOUT feature is disabled and the pin is internally pulled to ground.
- When SYNCOUT_EN = 1, the SYNC pin toggles at the base frequency used by the switching regulators.

The SYNCOUT function can be enabled or disabled by default by using the OTP_SYNCOUT_EN bit.

Table 53. Clock management specifications

All parameters are specified at T_A = −40 to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5.0 V and T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
Low frequency clock					
$I_{Q100KHz}$	100 kHz clock quiescent current	—	—	3.0	µA
$f_{100KHzACC}$	100 kHz clock accuracy	−5.0	—	5.0	%
High frequency clock					
f_{20MHz}	High frequency clock nominal frequency via CLK_FREQ[3:0] = 0000	—	20	—	MHz
$f_{20MzACC}$	High frequency clock accuracy	−6.0	—	6.0	%
$t_{20MHzStep}$	Clock step transition time				µs

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Table 53. Clock management specifications*...continued*

All parameters are specified at T_A = −40 to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5.0 V and T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
	Minimum time to transition from one frequency step to the next in manual tuning mode	—	5.2	—	
FSS_{RANGE}	Spread-spectrum range FSS_RANGE= 0 via CLK_FREQ[3:0] Spread-spectrum is done around center frequency of 20 MHz	—	±5.0	—	%
FSS_{RANGE}	Spread-spectrum range FSS_RANGE= 1 via CLK_FREQ[3:0] Spread-spectrum is done around center frequency of 20 MHz	—	±10	—	%
FSS_{mod}	Spread spectrum frequency modulation	—	24	—	kHz
Clock synchronization					
f_{SYNCIN}	SYNC input frequency range FSYNC_RANGE = 0	2000	—	3000	kHz
f_{SYNCIN}	SYNC input frequency range FSYNC_RANGE = 1	333	—	500	kHz
$f_{SYNCOUT}$	SYNC output frequency range via CLK_FREQ[3:0]	2000	—	3000	kHz
$V_{SYNCINLO}$	Input frequency low voltage threshold	—	—	0.3*VDDIO	V
$V_{SYNCINHI}$	Input frequency high voltage threshold	0.7*VDDIO	—	—	V
R_{PD_SYNCIN}	SYNC internal pull down resistance	0.475	1.0	__	MΩ
$V_{SYNCOUTLO}$	Output frequency low voltage threshold	0	—	0.4	V
$V_{SYNCOUTHI}$	Output frequency high voltage threshold	VDDIO − 0.5	—	—	V

15.5 Thermal monitoring

The PF5024 features a temperature sensor at the center of the die which is used to generate the thermal interrupts and thermal shutdown.

Figure 27 shows a high level block diagram of the thermal monitoring architecture in PF5024.

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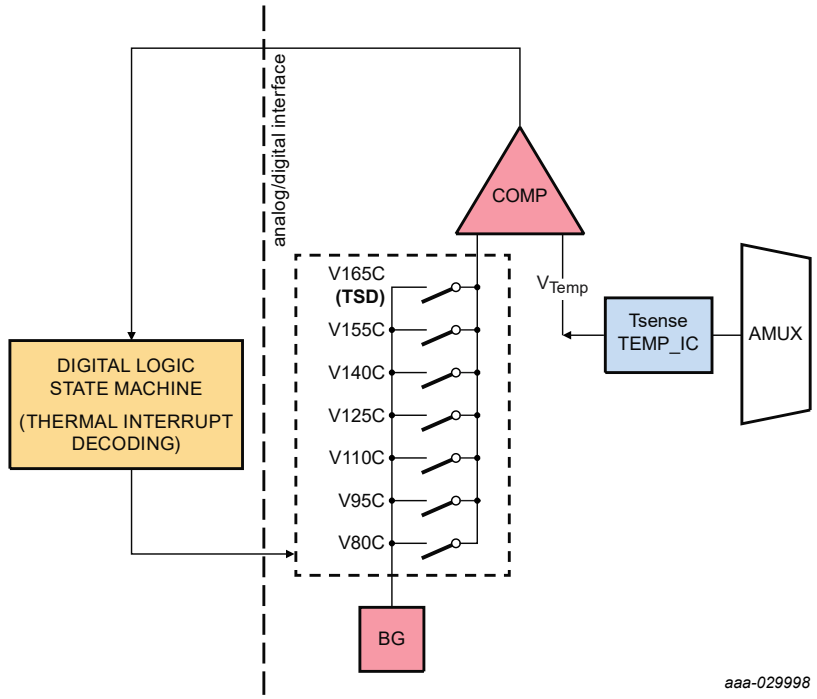

Figure 27. Thermal monitoring architecture

Table 54. Thermal monitor specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Operating voltage range of thermal circuit	UVDET	—	5.5	V
TCOF	Thermal sensor coefficient	—	−3.8	—	mV/ºC
V_{TSROMM}	Thermal sensor voltage 24 ºC	— 	1.414	— 	V
T_{SEN_RANGE}	Thermal sensor temperature range	–40	—	175	ºC
T_{80C}	80 ºC temperature threshold	70	80	90	ºC
T_{95C}	95 ºC temperature threshold	85	95	105	ºC
T_{110C}	110 ºC temperature threshold	100	110	120	ºC
T_{125C}	125 ºC temperature threshold	115	125	135	ºC
T_{140C}	140 ºC temperature threshold	130	140	150	ºC
$T1_{55C}$	155 ºC temperature threshold	145	155	165	ºC
T_{SD}	Thermal shutdown threshold	155	165	175	ºC
T_{WARN_HYS}	Thermal threshold hysteresis	—	5.0	—	ºC
T_{SD_HYS}	Thermal shutdown hysteresis	—	10	—	ºC
t_temp_db	Debounce timer for temperature thresholds (bidirectional)	—	10	—	µs
$t_{Sinterval}$	Sampling interval time When TMP_MON_AON = 1	— 	3.0	— 	ms
$t_{Swindow}$	Sampling window When TMP_MON_AON = 1	— 	450	— 	µs

As the temperature crosses the thermal thresholds, the corresponding interrupts are set to notify the system. The processor may take appropriate action to bring down the temperature (either by turning off external regulators, reducing load, or turning on a fan).

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A 5 ºC hysteresis is implemented on a falling temperature in order to release the corresponding THERM_x_S signal. When the shutdown threshold is crossed, the PF5024 initiates a thermal shutdown and it prevents from turning back on until the 15 ºC thermal shutdown hysteresis is crossed as the device cools down.

The temperature monitor can be enabled or disabled via I^2C with the TMP_MON_EN bit.

- When TMP_MON_EN = 0, the temperature monitor circuit is disabled.
- When TMP_MON_EN = 1, the temperature monitor circuit is enabled.

In the Run state, the temperature sensor can operate in always On or Sampling modes.

- When the TMP_MON_AON = 1, the device is always on during the Run mode.
- When the TMP_MON_AON = 0, the device operates in sampling mode to reduce current consumption in the system. In Sampling mode, the thermal monitor is turned on during 450 µs at a 3.0 ms sampling interval.

In the Standby mode, the thermal monitor operates only in sampling mode as long as the TMP_MON_EN = 1.

Table 55. Thermal monitor bit description

Bit(s)	Description
THERM_80_I, THERM_80_S, THERM_80_M	Interrupt, sense and mask bits for 80 ºC threshold
THERM_95_I, THERM_95_S, THERM_95_M	Interrupt, sense and mask bits for 95 ºC threshold
THERM_110_I, THERM_110_S, THERM_110_M	Interrupt, sense and mask bits for 110 ºC threshold
THERM_125_I, THERM_125_S, THERM_125_M	Interrupt, sense and mask bits for 125 ºC threshold
THERM_140_I, THERM_140_S, THERM_140_M	Interrupt, sense and mask bits for 140 ºC threshold
THERM_155_I, THERM_155_S, THERM_155_M	Interrupt, sense and mask bits for 155 ºC threshold
TMP_MON_EN	Disables temperature monitoring circuits when cleared
TMP_MON_AON	When set, the temperature monitoring circuit is always ON. When cleared, the temperature monitor operates in Sampling mode.

15.6 Analog multiplexer

An analog multiplexer (AMUX) is provided to allow access to internal temperature monitor. The selected voltage is buffered and made available on the PGOOD1 output pin.

When the AMUX_EN bit is 0, the AMUX block is disabled and the PGOOD1 block is enabled.

When the AMUX_EN bit is 1, the AMUX block is enabled and the PGOOD1 block is disabled. The system can select the channel to be read using the AMUX_SEL bits. The AMUX output is selected by the AMUX_SEL[4:0] bits.

Table 56. AMUX channel selection

AMUX_EN	AMUX_SEL[4:0]	AMUX selection
0	XXXXX	PGOOD mode
1	00000	Disabled - high impedance
1	00001 to 00110	Reserved
1	00111	TEMP_IC
1	01000 to 11111	Reserved

When the AMUX_EN = 1, and the AMUX_SEL = 00000, the AMUX output is set to a high impedance mode to allow an external signal to drive the AMUX node. The AMUX is enabled and accessible during the system On states.

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15.7 Watchdog event management

A watchdog event may be started in two ways:

- The WDI pin toggles low due to a watchdog failure on the MCU
- The internal watchdog expiration counter reaches the maximum value the WD timer is allowed to expire

A watchdog event initiated by the WDI pin may perform a hard WD reset or a soft WD reset as defined by the WDI_MODE bit. A watchdog event initiated by the internal watchdog always performs a hard WD reset.

15.7.1 Internal watchdog timer

The internal WD timer counts up and it expires when it reaches the value in the WD_DURATION[3:0] register. When the WD timer starts counting, the WD_CLEAR flag is set to 1. Clearing the WD_CLEAR flag within the valid window is interpreted as a successful watchdog refresh and the WD timer gets reset. The MCU must write a 1 to clear the WD_CLEAR flag.

The WD timer is reset when device goes into any of the Off modes and does not start counting until RESETBMCU is deasserted in the next power up sequence.

The OTP_WD_DURATION[3:0] selects the initial configuration for the watchdog window duration between 1.0 ms and 32768 ms (typical values).

The watchdog window duration can change during the system On state by modifying the WD_DURATION[3:0] bits in the functional register map. If the WD_DURATION[3:0] bits get changed during the system On state, the WD timer is reset.

Table 57. Watchdog duration register

WD_DURATION[3:0]	Watchdog timer duration (ms)
0000	1
0001	2
0010	4
0011	8
0100	16
0101	32
0110	64
0111	128
1000	256
1001	512
1010	1024
1011	2048
1100	4096
1101	8192
1110	16384
1111	32768

The WD_EXPIRE_CNT[2:0] counter is used to ensure no cyclic watchdog condition occurs. When the WD_CLEAR flag is cleared successfully before the WD timer expires, the WD_EXPIRE_CNT[2:0] is decreased by 1. Every time the WD timer is not successfully refreshed, it gets reset and starts a new count and the WD_EXPIRE_CNT[2:0] is increased by 2.

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If WD_EXPIRE_CNT[2:0] = WD_MAX_EXPIRE[2:0], a WD event is initiated. The default maximum amount of time the watchdog can expire before starting a WD reset, is set by the OTP_WD_MAX_EXPIRE[2:0]. Writing a value less than or equal to 0x02 on the OTP_WD_MAX_EXPIRE causes the watchdog event to be initiated, as soon as the WD timer expires for the first time.

The OTP_WDWINDOW bit selects whether the watchdog is single ended or window mode.

- When OTP_WDWINDOW = 0, the WD_CLEAR flag can be cleared within 100 % of the watchdog timer.
- When OTP_WDWINDOW = 1, the WD_CLEAR flag can only be cleared within the second half of the programmed watchdog timer. Clearing the WD_CLEAR flag within the first half of the watchdog window is interpreted as a failure to refresh the watchdog.

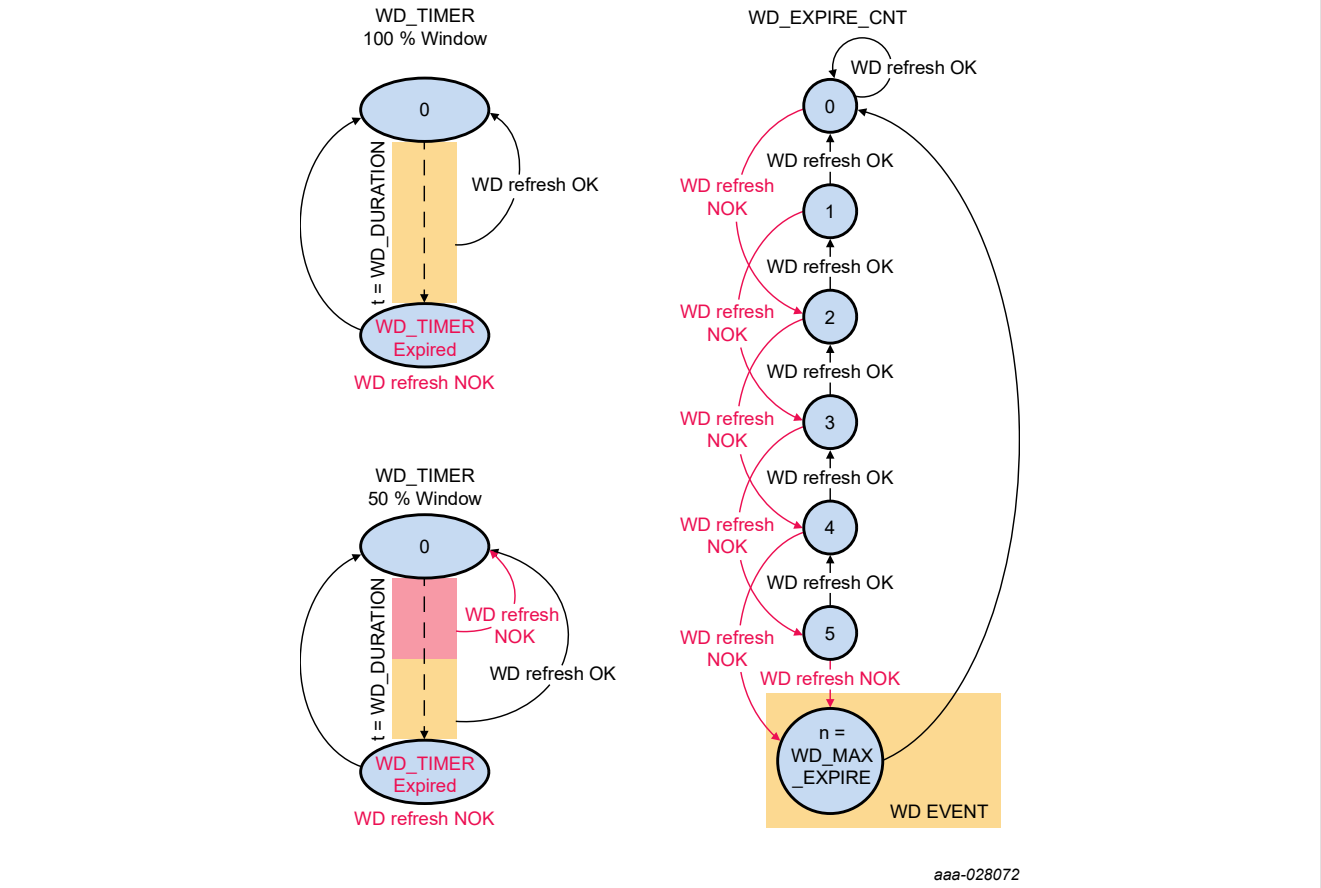

Figure 28. Watchdog timer operation

The watchdog function can be enabled or disabled by writing the WD_EN bit in the I^2C register map. When the I2C_SECURE_EN = 1, a secure write must be performed to change the WD_EN bit.

- When WD_EN = 0 the internal watchdog timer operation is disabled.
- When WD_EN = 1 the internal watchdog timer operation is enabled.

The OTP_WD_EN bit is used to select the default status of the watchdog counter upon power up.

The watchdog function can be programmed to be enabled or disabled during the Standby state by writing the WD_STBY_EN bit in the I^2C register map. When the I2C_SECURE_EN = 1, a secure write must be performed to modify the WD_STBY_EN bit.

- When WD_STBY_EN = 0 the internal watchdog timer operation during standby is disabled.
- When WD_STBY_EN = 1 the internal watchdog timer operation during standby is enabled.

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The OTP_WD_STBY_EN bit selects whether the watchdog is active in Standby mode by default or not.

15.7.2 Watchdog reset behaviors

When a watchdog event is started, a watchdog (WD) reset is performed. There are two types of watchdog reset:

- Soft WD reset
- Hard WD reset

A soft WD reset is used as a safe way for the MCU to force the PMIC to return to a known default configuration without forcing a POR reset on the MCU. During a soft WD reset, the RESETBMCU remains de-asserted all the time.

Upon a soft WD reset, a partial OTP register reload is performed on the registers as shown in Table 58.

Table 58. Soft WD register reset

Bit name	Register	Bits
Configuration registers		
STANDBYINV	CTRL2	2
RUN_PG_GPO	CTRL2	1
STBY_PG_GPO	CRTL2	0
RESETBMCU_SEQ[7:0]	RESETBMCU PWRUP	7:0
PGOOD_SEQ[7:0]	PGOOD PWRUP	7:0
WD_EN	CTRL1	3
WD_DURATION[3:0]	WD CONFIG	3:0
WD_STBY_EN	CTRL1	2
WDI_STBY_ACTIVE	CTRL1	1
SW registers		
SWx_WDBYPASS	SWx CONFIG1	1
SWx_PG_EN	SWx CONFIG1	0
SWxDVS_RAMP	SWx CONFIG2	5
SWxILIM[1:0]	SWx CONFIG2	4:3
SWxPHASE[2:0]	SWx CONFIG2	2:0
SWx_SEQ[7:0]	SWx PWRUP	7:0
SWx_PDGRP[1:0]	SWx MODE	5:4
SWx_STBY_MODE [1:0]	SWx MODE	3:2
SWx RUN_MODE [1:0]	SWx MODE	1:0
VSWx_RUN [7:0]	SWx RUN VOLT	7:0
VSWx_STBY [7:0]	SWx STBY VOLT	7:0
SW2_VTTEN	SW2_CONFIG2	6

A soft WD reset may require all or some regulators to be reset to their default OTP configuration. In the event a regulator is required to keep its current configuration during a soft WD reset, a watchdog bypass bit is provided for each regulator (SWx_WDBYPASS).

- When the WDBYPASS = 0, the watchdog bypass is disabled and the output of the corresponding regulator is returned to its default OTP value during the soft WD reset.
- When the WDBYPASS = 1, the watchdog bypass is enabled and the output of the corresponding regulator is not affected by the soft WD reset, keeping its current configuration.

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During a soft WD reset, only regulators that are activated in the power up sequence go back to their default voltage configuration if their corresponding WDBYPASS = 0.

Switching regulators returning to their default voltages configuration, will gradually reach the new output voltage using its DVS configuration. Regulators with WDBYPASS = 0 and which are not activated during the power up sequence will turn off immediately.

After all output voltages have transitioned to their corresponding default values, the device waits for at least 30 µs before returning to the Run state and announces it has finalized the soft WD reset by asserting the INTB pin, provided the WDI_I interrupt is not masked.

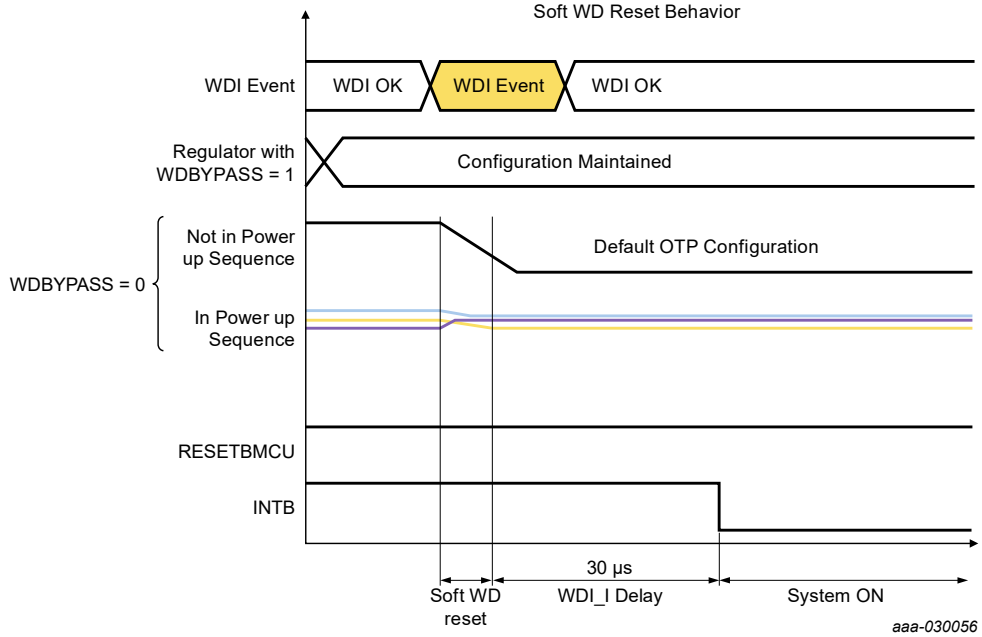

Figure 29. Soft WD reset behavior

A hard WD reset is used to force a system power-on reset when the MCU has become unresponsive. In this scenario, a full OTP register reset is performed.

During a hard WD reset, the device turns off all regulators and asserts RESETBMCU as indicated by the power down sequence. If PGOOD is programmed as a GPO and configured as part of the power up sequence, it will also be disabled accordingly.

After all regulator's outputs have gone through the power down sequence and the power down delay is finished , the device waits for 30 µs before reloading the default OTP configuration and get ready to start a power up sequence if the XFAILB pin is not held low externally.

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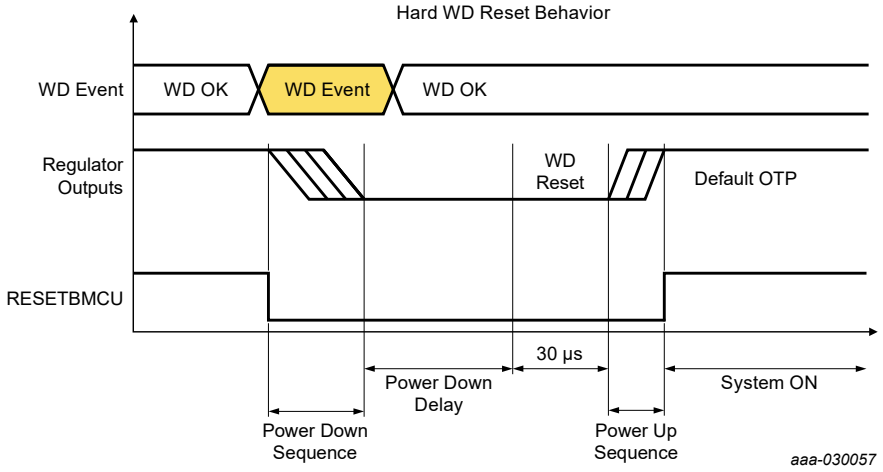

Figure 30. Hard WD reset behavior

After a WD reset, the PMIC may enter the Standby state depending on the status of STANDBY pin.

Every time a WD event occurs, the WD_EVENT_CNT[3:0] nibble is incremented. To prevent continuous failures, if the WD_EVENT_CNT[3:0] = WD_MAX_CNT[3:0] the state machine will proceed to the fail-safe transition. The MCU is expected to clear the WD_EVENT_CNT[3:0] when it is able to do so in order to keep proper operation. Upon power up, the WD_MAX_CNT[3:0] is loaded with the values on the OTP_WD_MAX_CNT[3:0] bits.

Every time the device passes through the off states, the WD_EVENT_CNT[3:0] is reset to 0x00, to ensure the counter has a fresh start after a device power down.

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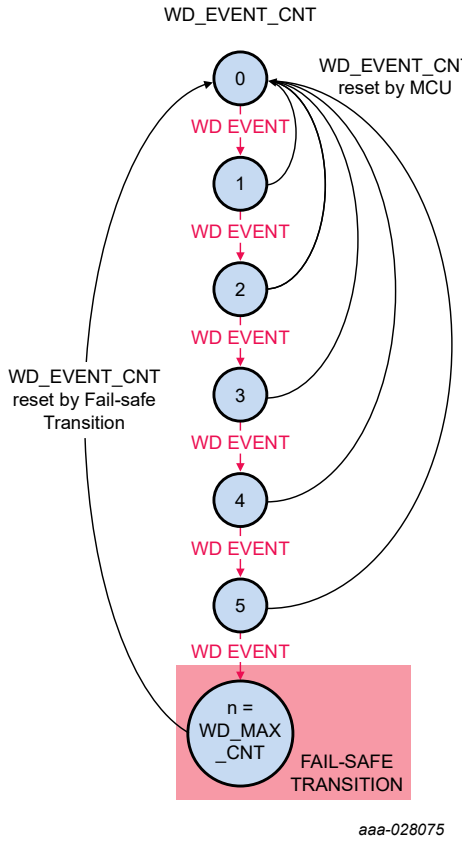

Figure 31. Watchdog event counter

16 I²C register map

The PF5024 provides a complete set of registers for control and diagnostics of the PMIC operation. The configuration of the device is done at two different levels.

At first level, the OTP mirror registers provide the default hardware and software configuration for the PMIC upon power up. These are one-time programmable and should be defined during the system development phase, and are not meant to be modified during the application. See Section 17 "OTP/TBB and hardwire default configurations" for the OTP configuration feature.

At a second level, the PF5024 provides a set of functional registers intended for system configuration and diagnostics during the system operation. These registers are accessible during the system On state and can be modified at any time by the system control unit.

The device ID register provides general information about the PMIC:

- DEVICE_FAM[3:0]: indicates the PF50x0 family of devices.
  0101 (fixed)
- DEVICE_ID[3:0]: provides the device type identifier
  0100 = PF5024 QM
  1100 = PF5024 ASIL B

Registers 0x02 and 0x03 provide a customizable program ID registers to identify the specific OTP configuration programmed in the part.

- EMREV (Address 0x02): contains the MSB bits PROG_ID[8:11]

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- PROG_ID (Address 0x03): contains the LSB bit PROG_ID[7:0]

16.1 PF5024 OTP mirror register map

Reset types	
OFF_OTP	Register loads the OTP mirror register values during power up
OTP	Register available in OTP bank only, Reset From fuses when VIN crosses UVDET threshold

MR ADDR	FUSE ADDR	Register name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
A0	0	OTP I2C	—	—	—	OTP_I2C_SECURE_EN	OTP_I2C_CRC_EN	OTP_I2C_ADD[2:0]		
A1	1	OTP CTRL1	—	—	OTP_EWARN_TIME[1:0]		OTP_FS_BYPASS	OTP_STANDBYINV	OTP_PG_ACTIVE	OTP_PG_CHECK
A2	2	OTP CTRL2	OTP_FSS_EN	OTP_FSS_RANGE	—	OTP_XFAILB_EN	OTP_VIN_OVLO_SDWN	OTP_VIN_OVLO_EN	OTP_VIN_OVLO_DBNC[1:0]	
A3	3	OTP CTRL3	OTP_VTT_PDOWN	OTP_SW2_VTTEN	—	—	OTP_SW4CONFIG[1:0]		OTP_SW1CONFIG[1:0]	
A4	4	OTP FREQ CTRL	OTP_SW_MODE	OTP_SYNC_MODE	OTP_SYNCOUT_EN	OTP_FSYNC_RANGE	OTP_CLK_FREQ[3:0]			
A5	5	OTP PWRON	—	—	OTP_PWRON_MODE	OTP_PWRON_DBNC[1:0]		OTP_PWRON_RST_EN	OTP_TRESET[1:0]	
A6	6	OTP WD CONFIG	—	—	OTP_WDI_MODE	OTP_WDI_INV	OTP_WD_EN	OTP_ WD_STBY_EN	OTP_WDI_STBY_ACTIVE	OTP_WDWINDOW
A7	7	OTP WD EXPIRE	—	—	—	—	—	OTP_WD_MAX_EXPIRE[2:0]		
A8	8	OTP WD COUNTER	OTP_WD_DURATION[3:0]				OTP_WD_MAX_CNT [3:0]			
A9	9	OTP FAULT COUNTERS	OTP_FS_MAX_CNT[3:0]				OTP_FAULT_MAX_CNT[3:0]			
AA	A	OTP FAULT TIMERS	—	OTP_FS_OK_TIMER[2:0]			OTP_TIMER_FAULT[3:0]			
AB	B	OTP PWRDN DLY1	OTP_GRP4_DLY[1:0]		OTP_GRP3_DLY[1:0]		OTP_GRP2_DLY[1:0]		OTP_GRP1_DLY[1:0]	
AC	C	OTP PWRDN DLY2	OTP_PD_SEQ_DLY[1:0]		—	—	—	—	OTP_RESETBMCU_DLY[1:0]	
AD	D	OTP PWRUP CTRL	—	OTP_PWRDWN_MODE	OTP_PGOOD_PDGRP[1:0]		OTP_RESETBMCU_PDGRP[1:0]		OTP_SEQ_TBASE[1:0]	
AE	E	OTP RESETBMCU PWRUP	OTP_RESETBMCU_SEQ[7:0]							
AF	F	OTP PGOOD PWRUP	OTP_PGOOD_SEQ[7:0]							
B0	10	OTP SW1 VOLT	OTP_VSW1[7:0]							
B1	11	OTP SW1 PWRUP	OTP_SW1_SEQ[7:0]							
B2	12	OTP SW1 CONFIG1	OTP_SW1UV_TH[1:0]		OTP_SW1OV_TH[1:0]		OTP_SW1_PDGRP[1:0]		OTP_SW1ILIM[1:0]	
B3	13	OTP SW1 CONFIG2	OTP_SW1_LSELECT[1:0]		OTP_SW1PHASE[2:0]			—	OTP_SW1_PG_EN	OTP_SW1_WDBYPASS
B4	14	OTP SW2 VOLT	OTP_VSW2[7:0]							
B5	15	OTP SW2 PWRUP	OTP_SW2_SEQ[7:0]							
B6	16	OTP SW2 CONFIG1	OTP_SW2UV_TH[1:0]		OTP_SW2OV_TH[1:0]		OTP_SW2_PDGRP[1:0]		OTP_SW2ILIM[1:0]	
B7	17	OTP SW2 CONFIG2	OTP_SW2_LSELECT[1:0]		OTP_SW2PHASE[2:0]			—	OTP_SW2_PG_EN	OTP_SW2_WDBYPASS
B8	18	OTP SW3_VOLT	OTP_VSW3[7:0]							
B9	19	OTP SW3 PWRUP	OTP_SW3_SEQ[7:0]							
BA	1A	OTP SW3 CONFIG1	OTP_SW3UV_TH[1:0]		OTP_SW3OV_TH[1:0]		OTP_SW3_PDGRP[1:0]		OTP_SW3ILIM[1:0]	
BB	1B	OTP SW3 CONFIG2	OTP_SW3_LSELECT[1:0]		OTP_SW3PHASE[2:0]			—	OTP_SW3_PG_EN	OTP_SW3_WDBYPASS
BC	1C	OTP SW4 VOLT	OTP_VSW4[7:0]							
BD	1D	OTP SW4 PWRUP	OTP_SW4_SEQ[7:0]							

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MR ADDR	FUSE ADDR	Register name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BE	1E	OTP SW4 CONFIG1	OTP_SW4UV_TH[1:0]		OTP_SW4OV_TH[1:0]		OTP_SW4_PDGRP[1:0]		OTP_SW4ILIM[1:0]	
BF	1F	OTP SW4 CONFIG2	OTP_SW4_LSELECT[1:0]		OTP_SW4PHASE[2:0]			—	OTP_SW4_PG_EN	OTP_SW4_ WDBYPASS
C8	28	OTP_OV_ BYPASS1	—	Reserved	—	—	OTP_SW4_ OVBYPASS	OTP_SW3_ OVBYPASS	OTP_SW2_ OVBYPASS	OTP_SW1_ OVBYPASS
CA	2A	OTP_UV_ BYPASS1	—	Reserved	—	—	OTP_SW4_ UVBYPASS	OTP_SW3_ UVBYPASS	OTP_SW2_ UVBYPASS	OTP_SW1_ UVBYPASS
CC	2C	OTP_ILIM_ BYPASS1	—	Reserved	—	—	OTP_SW4_ ILIMBYPASS	OTP_SW3_ ILIMBYPASS	OTP_SW2_ ILIMBYPASS	OTP_SW1_ ILIMBYPASS
CE	2E	OTP_PROG_ IDH	—	—	—	—	OTP_PROG_ID11	OTP_PROG_ID10	OTP_PROG_ID9	OTP_PROG_ID8
CF	2F	OTP_PROG_ IDL	OTP_PROG_ID7	OTP_PROG_ID6	OTP_PROG_ID5	OTP_PROG_ID4	OTP_PROG_ID3	OTP_PROG_ID2	OTP_PROG_ID1	OTP_PROG_ID0
D0	30	OTP DEBUG1	—	—	—	—	—	—	—	BGMON_BYPASS
D1	31	OTP SW COMP1	—	—	OTP_SW2_GM_COMP[2:0]			OTP_SW1_GM_COMP[2:0]		
D2	32	OTP SW COMP2	—	—	OTP_SW4_GM_COMP[2:0]			OTP_SW3_GM_COMP[2:0]		
D4	34	OTP SW RAMP	OTP_SW4DVS_RAMP[1:0]		OTP_SW3DVS_RAMP[1:0]		OTP_SW2DVS_RAMP[1:0]		OTP_SW1DVS_RAMP[1:0]	
D5	35	OTP_S0_CRC_ LSB	OTP_S0_CRC_LSB[7:0]							
D6	36	OTP_SO_ CRC_MSB	OTP_SO_CRC_MSB[7:0]							

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16.2 PF5024 functional register map

RESET signals	
UVDET	Reset when VIN crosses UVDET threshold
OFF_OTP	Bits are loaded with OTP values (mirror register)
OFF_TOGGLE	Reset when device goes to OFF mode
SC	Self-clear after write

R/W types	
R	Read only
R/W	Read and Write
RW1C	Read, Write a 1 to clear
R/SW	Read/Secure Write
R/TW	Read/Write on TBB only

Default values	
1	bit set on reset
0	bit cleared on reset
x	unknown state
F	loaded from OTP fuse
T	Hard coded

ADDR	Register name	R/W	Default	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00	DEVICE ID	R	0101_TTTT	DEVICE_FAM[3:0]				DEVICE_ID[3:0]			
01	REV ID	R	TTTT_TTTT	FULL_LAYER_REV[3:0]				METAL_LAYER_REV[3:0]			
02	EMREV	R	FFFF_TTTT	PROG_ID[11:8]				—	EMREV[2:0]		
03	PROG ID	R	FFFF_FFFF	PROG_ID[7:0]							
04	INT STATUS1	RW1C	0000_0000	SDWN_I	FREQ_RDY_I	CRC_I	PWRUP_I	PWRDN_I	—	PGOOD_I	VIN_OVLO_I
05	INT MASK1	R/W	1111_1011	SDWN_M	FREQ_RDY_M	CRC_M	PWRUP_M	PWRDN_M	—	PGOOD_M	VIN_OVLO_M
06	INT SENSE1	R	0000_00xx	—	—	—	—	—	—	PGOOD_S	VIN_OVLO_S
07	INT STATUS2	RW1C	0000_0000	WDI_I	FSYNC_FLT_I	THERM_155_I	THERM_140_I	THERM_125_I	THERM_110_I	THERM_95_I	THERM_80_I
08	INT MASK2	R/W	1111_1111	WDI_M	FSYNC_FLT_M	THERM_155_M	THERM_140_M	THERM_125_M	THERM_110_M	THERM_95_M	THERM_80_M
09	INT SENSE2	R	xxxx_xxxx	WDI_S	FSYNC_FLT_S	THERM_155_S	THERM_140_S	THERM_125_S	THERM_110_S	THERM_95_S	THERM_80_S
0A	SW MODE INT	RW1C	0000_0000	—	Reserved	—	—	SW4_MODE_I	SW3_MODE_I	SW2_MODE_I	SW1_MODE_I
0B	SW MODE MASK	R/W	0100_1111	—	Reserved	—	—	SW4_MODE_M	SW3_MODE_M	SW2_MODE_M	SW1_MODE_M
0C	SW ILIM INT	RW1C	0000_0000	—	Reserved	—	—	SW4_ILIM_I	SW3_ILIM_I	SW2_ILIM_I	SW1_ILIM_I
0D	SW ILIM MASK	R/W	0100_1111	—	Reserved	—	—	SW4_ILIM_M	SW3_ILIM_M	SW2_ILIM_M	SW1_ILIM_M
0E	SW ILIM SENSE	R	0x00_00xx	—	Reserved	—	—	SW4_ILIM_S	SW3_ILIM_S	SW2_ILIM_S	SW1_ILIM_S
12	SW UV INT	RW1C	0000_0000	—	Reserved	—	—	SW4_UV_I	SW3_UV_I	SW2_UV_I	SW1_UV_I
13	SW UV MASK	R/W	0100_1111	—	Reserved	—	—	SW4_UV_M	SW3_UV_M	SW2_UV_M	SW1_UV_M
14	SW UV SENSE	R	0x00_00xx	—	Reserved	—	—	SW4_UV_S	SW3_UV_S	SW2_UV_S	SW1_UV_S
15	SW OV INT	RW1C	0000_0000	—	Reserved	—	—	SW4_OV_I	SW3_OV_I	SW2_OV_I	SW1_OV_I
16	SW OV MASK	R/W	0100_1111	—	Reserved	—	—	SW4_OV_M	SW3_OV_M	SW2_OV_M	SW1_OV_M
17	SW OV SENSE	R	0x00_00xx	—	Reserved	—	—	SW4_OV_S	SW3_OV_S	SW2_OV_S	SW1_OV_S
1E	PWRON INT	RW1C	0000_0000	BGMON_I	PWRON_8S_I	PWRON_4S_I	PRON_3S_I	PWRON_2S_I	PWRON_1S_I	PWRON_REL_I	PWRON_PUSH_I
1F	PWRON MASK	R/W	1111_1111	BGMON_M	PWRON_8S_M	PWRON_4S_M	PRON_3S_M	PWRON_2S_M	PWRON_1S_M	PWRON_REL_M	PWRON_PUSH_M
20	PWRON SENSE	R	x000_000x	BGMON_S	—	—	—	—	—	—	PWRON_S
21	EN SENSE	R	0000_xxxx	—	—	—	—	EN4_S	EN3_S	EN2_S	EN1_S
22	SYS INT	R	0000_0000	EWARN_I	PWRON_I	OV_I	UV_I	ILIM_I	MODE_I	STATUS2_I	STATUS1_I
23	HARDFAULT FLAGS	RW1C	0000_0000	—	—	—	—	PU_FAIL	WD_FAIL	REG_FAIL	TSD_FAIL
24											
25	ABIST PGOOD MON	R/SW	0000_0000	—	—	—	—	—	—	—	AB_PGOOD_MON
26	ABIST OV1	R/SW	0000_0000	—	Reserved	—	—	AB_SW4_OV	AB_SW3_OV	AB_SW2_OV	AB_SW1_OV
28	ABIST UV1	R/SW	0000_0000	—	Reserved	—	—	AB_SW4_UV	AB_SW3_UV	AB_SW2_UV	AB_SW1_UV
2A	TEST FLAGS	R/TW	0000_0000	—	—	—	—	—	STEST_NOK	TRIM_NOK	OTP_NOK
2B	ABIST RUN	R/SW	0000_0000	—	—	—	—	—	—	—	AB_RUN
2C											
2D	RANDOM GEN	R	xxxx_xxxx	RANDOM_GEN[7:0]							
2E	RANDOM CHK	R/W	0000_0000	RANDOM_CHK[7:0]							
2F	VMONEN1	R/SW	0100_1111	—	Reserved	—	—	SW4VMON_EN	SW3VMON_EN	SW2VMON_EN	SW1VMON_EN
31	CTRL1	R/SW	FFF1_FFFF	VIN_OVLO_EN	VIN_OVLO_SDWN	WDI_MODE	TMP_MON_EN	WD_EN	WD_STBY_EN	WDI_STBY_ACTIVE	I2C_SECURE_EN
32	CTRL2	R/W	FF01_0FFF	VIN_OVLO_DBNC[1:0]		—	TMP_MON_AON	LPM_OFF	STANDBYINV	RUN_PG_GPO	STBY_PG_GPO
33	CTRL3	R/W	0010_0000	OV_DB[1:0]		UV_DB[1:0]		—	—	PMIC_OFF	INTB_TEST
34	PWRUP CTRL	R/W	0FFF_FFFF	—	PWRDWN_MODE	PGOOD_PDGRP[1:0]		RESETBMCU_PDGRP[1:0]		SEQ_TBASE[1:0]	
35											

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ADDR	Register name	R/W	Default	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
36	RESETBMCU PWRUP	R/W	FFFF_FFFF	RESETBMCU_SEQ[7:0]							
37	PGOOD PWRUP	R/W	FFFF_FFFF	PGOOD_SEQ[7:0]							
38	PWRDN DLY1	R/W	FFFF_FFFF	GRP4_DLY[1:0]		GRP3_DLY[1:0]		GRP2_DLY[1:0]		GRP1_DLY[1:0]	
39	PWRDN DLY2	R/W	0000_00FF	—	—	—	—	—	—	RESETBMCU_DLY[1:0]	
3A	FREQ CTRL	R/W	FFFF_FFFF	SYNCOUT_EN	FSYNC_RANGE	FSS_EN	FSS_RANGE	CLK_FREQ[3:0]			
3B											
3C	PWRON	R/W	000F_FFFF	—	—	—	PWRON_DBNC[1:0]		PWRON_RST_EN	TRESET[1:0]	
3D	WD CONFIG	R/W	0000_FFFF	—	—	—	—	WD_DURATION[3:0]			
3E	WD CLEAR	R/W1C	0000_0000	—	—	—	—	—	—	—	WD_CLEAR
3F	WD EXPIRE	R/W	0FFF_0000	—	WD_MAX_EXPIRE[2:0]			—	WD_EXPIRE_CNT[2:0]		
40	WD COUNTER	R/W	FFFF_0000	WD_MAX_CNT[3:0]				WD_EVENT_CNT[3:0]			
41	FAULT COUNTER	R/W	FFFF_0000	FAULT_MAX_CNT[3:0]				FAULT_CNT[3:0]			
42	FSAFE COUNTER	R/W	0000_0000	—	—	—	—	FS_CNT [3:0]			
43	FAULT TIMERS	R/W	0000_FFFF	—	—	—	—	TIMER_FAULT[3:0]			
44	AMUX	R/W	0000_0000	—	—	AMUX_EN	AMUX_SEL[4:0]				
45											
46	SW RAMP	R/W	FFFF_FFFF	SW4DVS_RAMP[1:0]		SW3DVS_RAMP[1:0]		SW2DVS_RAMP[1:0]		SW1DVS_RAMP[1:0]	
47	SW1 CONFIG1	R/W	FFF1_11FF	SW1_UV_BYPASS	SW1_OV_BYPASS	SW1_ILIM_BYPASS	SW1_UV_STATE	SW1_OV_STATE	SW1_ILIM_STATE	SW1_WDBYPASS	SW1_PG_EN
48	SW1 CONFIG2	R/W	10FF_FFFF	SW1_FLT_REN	—	—	SW1ILIM[1:0]		SW1PHASE[2:0]		
49	SW1 PWRUP	R/W	FFFF_FFFF	SW1_SEQ[7:0]							
4A	SW1 MODE	R/W	00FF_FFFF	—	—	SW1_PDGRP[1:0]		SW1_STBY_MODE[1:0]		SW1_RUN_MODE[1:0]	
4B	SW1 RUN VOLT	R/W	FFFF_FFFF	VSW1_RUN[7:0]							
4C	SW1 STBY VOLT	R/W	FFFF_FFFF	VSW1_STBY[7:0]							
4D											
4E											
4F	SW2 CONFIG1	R/W	FFF1_11FF	SW2_UV_BYPASS	SW2_OV_BYPASS	SW2_ILIM_BYPASS	SW2_UV_STATE	SW2_OV_STATE	SW2_ILIM_STATE	SW2_WDBYPASS	SW2_PG_EN
50	SW2 CONFIG2	R/W	1FFF_FFFF	SW2_FLT_REN	SW2_VTTEN	—	SW2ILIM[1:0]		SW2PHASE[2:0]		
51	SW2 PWRUP	R/W	FFFF_FFFF	SW2_SEQ[7:0]							
52	SW2 MODE1	R/W	00FF_FFFF	—	—	SW2_PDGRP[1:0]		SW2_STBY_MODE[1:0]		SW2_RUN_MODE[1:0]	
53	SW2 RUN VOLT	R/W	FFFF_FFFF	VSW2_RUN[7:0]							
54	SW2 STBY VOLT	R/W	FFFF_FFFF	VSW2_STBY[7:0]							
55											
56											
57	SW3 CONFIG1	R/W	FFF1_11FF	SW3_UV_BYPASS	SW3_OV_BYPASS	SW3_ILIM_BYPASS	SW3_UV_STATE	SW3_OV_STATE	SW3_ILIM_STATE	SW3_WDBYPASS	SW3_PG_EN
58	SW3 CONFIG2	R/W	10FF_FFFF	SW3_FLT_REN	—	—	SW3ILIM[1:0]		SW3PHASE[2:0]		
59	SW3 PWRUP	R/W	FFFF_FFFF	SW3_SEQ[7:0]							
5A	SW3 MODE	R/W	00FF_FFFF	—	—	SW3_PDGRP[1:0]		SW3_STBY_MODE[1:0]		SW3_RUN_MODE[1:0]	
5B	SW3 RUN VOLT	R/W	FFFF_FFFF	VSW3_RUN[7:0]							
5C	SW3 STBY VOLT	R/W	FFFF_FFFF	VSW3_STBY[7:0]							
5D											
5E											
5F	SW4 CONFIG1	R/W	FFF1_11FF	SW4_UV_BYPASS	SW4_OV_BYPASS	SW4_ILIM_BYPASS	SW4_UV_STATE	SW4_OV_STATE	SW4_ILIM_STATE	SW4_WDBYPASS	SW4_PG_EN
60	SW4 CONFIG2	R/W	10FF_FFFF	SW4_FLT_REN	—	—	SW4ILIM[1:0]		SW4PHASE[2:0]		
61	SW4 PWRUP	R/W	FFFF_FFFF	SW4_SEQ[7:0]							
62	SW4 MODE	R/W	00FF_FFFF	—	—	SW4_PDGRP[1:0]		SW4_STBY_MODE[1:0]		SW4_RUN_MODE[1:0]	
63	SW4 RUN VOLT	R/W	FFFF_FFFF	VSW4_RUN[7:0]							
64	SW4 STBY VOLT	R/W	FFFF_FFFF	VSW4_STBY[7:0]							
65											
66											
6C											

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ADDR	Register name	R/W	Default	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
6D											
73											
74											
76											
77	PAGE SELECT	R/TW	0000_0000	—	—	—	—	—	PAGE[2:0]		

17 OTP/TBB and hardwire default configurations

The PF5024 supports OTP fuse bank configuration and a predefined hardwire configuration to select the default power up configuration via the VDDOTP pin.

The default power up configuration is loaded into the functional I^2C registers based on the voltage on VDDOTP pin on register loading.

- If VDDOTP = GND, the device loads the configuration from the OTP mirror registers.
- If VDDOTP = V1P5D, the device loads the configuration from the default hardwire configuration.

When OTP configuration is selected, the register loading occurs in two stages:

- In the first stage, the fuses are loaded in the OTP mirror registers each time VIN crosses the UVDET threshold in the rising edge.
- At the second stage, the data from the mirror registers are loaded into the functional I^2C registers for device operation.

When VDDOTP = GND, the mirror registers hold the default configuration to be used on a power-on event. The mirror registers can be modified during the TBB mode in order to test a custom power up configuration and/or burn the configuration into the OTP fuses to generate a customized default power up configuration.

When VDDOTP = V1P5D, the I^2C functional register will always be loaded from the hardwire configuration each time a default loading is required. Therefore, no TBB operation is possible in this configuration.

In the event of a TRIM/OTP loading failure or a self-test failure, the corresponding fault flag is set and any PWRUP event is ignored until the flags are cleared by writing a 1 during the QPU_OFF state.

The TRIM_NOK, OTP_NOK and STEST_NOK flags can only be written when the TBBEN = V1P5D (in TBB mode). In normal operation, the TRIM_NOK, OTP_NOK and STEST_NOK flags can only be read, but not cleared.

17.1 TBB (Try Before Buy) operation

The PF5024 allows temporary configuration (TBB) to debug or test a customized power up configuration in the system. In order to access the TBB mode, the TBBEN pin should be pulled up to V1P5D.

In this mode of operation, the device ignores the default value of the LPM_OFF bit and moves into the QPU_Off state, regardless of the result of the self-test. However, the actual result of the self-test is notified by the STEST_NOK flag.

- When the self-test is successful the STEST_NOK flag is set to 0.
- When the self-test has failed, the STEST_NOK flag is set to 1.

In the TBB mode, the following conditions are valid:

- I^2C communication uses standard communication with no CRC and secure write disabled.
- Default I^2C address is 0x08 regardless of the address configured by OTP.
- Watchdog monitoring is disabled (including WDI and internal watchdog timer).
- The PF5024 can communicate through I^2C as long as V_{DDIO} is provided to the PMIC externally.

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The PAGE[2:0] bits are provided to grant access to the mirror registers and other OTP dedicated bits. When the device is in the TBB mode, it can access the mirror registers in the extended register Page 1. With the TBBEN pin pulled low, access to the extended register pages is not allowed.

The mirror registers are preloaded with the values from the OTP configuration. These may be modified to set the proper power up configuration during TBB operation.

If a power up event is present with the TBBEN pin pulled to V1P5D, the device will power up with the proper configuration but limited functionality.

Limited functionality includes:

- Default I^2C address = 0x08
- CRC and secure write disabled
- Watchdog operation/monitoring disable

In order to allow TBB operation with full functionality, the TBBEN pin must be low when the power up event occurs.

The PF5024 can operate normally using the TBB configuration, as long as VIN does not go below the UVDET threshold. If VIN is lost (VIN < UVDET) the mirror register will be reset and TBB configuration must be performed again.

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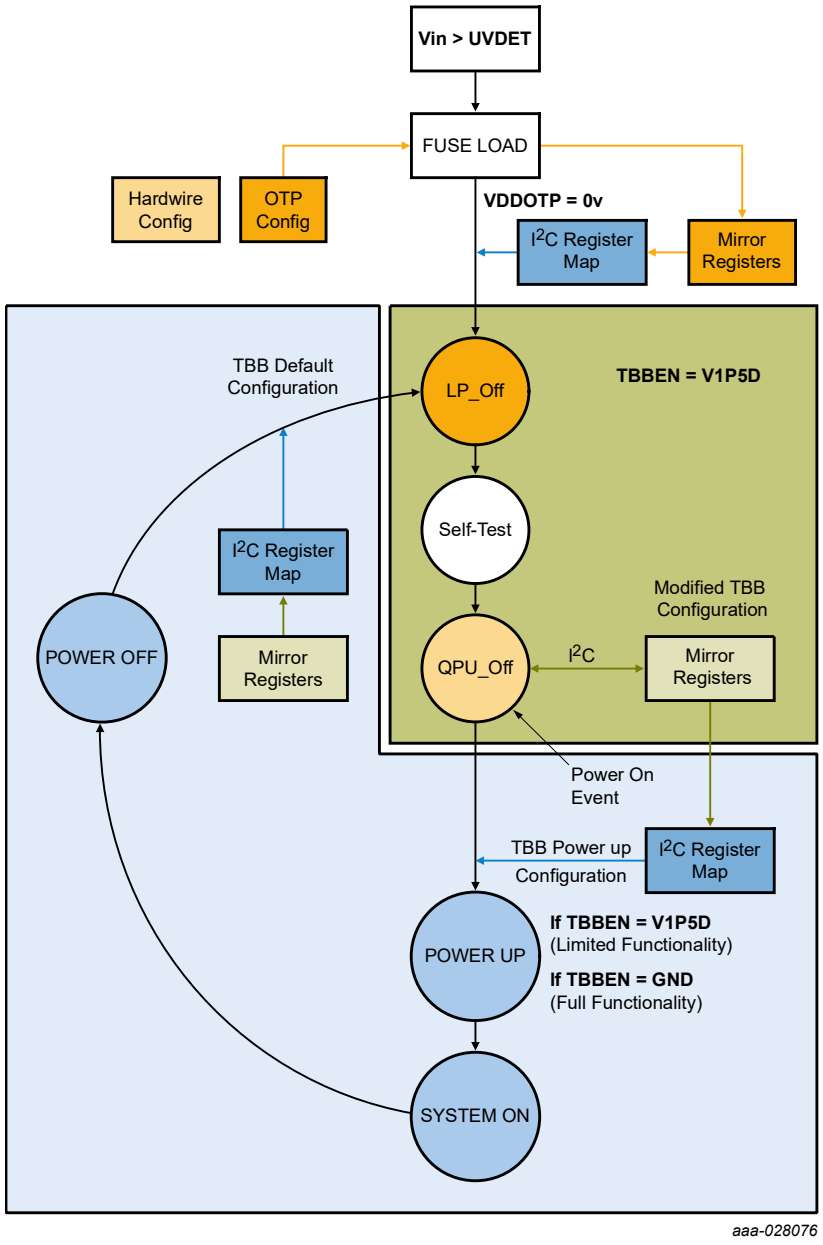

Figure 32. TBB operation diagram

17.2 OTP fuse programming

A permanent OTP configuration is possible by burning the OTP fuses. OTP fuse burning is performed in the TBBEN mode during the QPU_Off state. Contact your NXP representative for detailed information on OTP fuse programming.

17.3 Default hardwire configuration

If VDDOTP = V1P5D, the device loads the configuration from the default hardwire configuration directly into the corresponding I^2C functional registers each time the registers need to be reloaded.

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When using the hardwire configuration, the TRIM values are still loaded from the OTP fuses. In the event of a TRIM loading failure, the corresponding fault flag is set to 1.

When the hardwire configuration is used, the PF5024 does not allow TBB mode operation. When TBBEN = V1P5D, the device enters a debug mode. In this mode of operation, the device ignores the default value of the LPM_OFF bit and moves into the QPU_Off state, regardless of the result of the self-test. However, the actual result of the self-test is notified by the STEST_NOK flag.

- When the self-test is successful, the STEST_NOK flag is set to 0
- When the self-test has failed, the STEST_NOK flag is set to 1

During hardwire configuration, the OTP_NOK flag is always set to 0.

When any of the TRIM_NOK, OTP_NOK or STEST_NOK flags are set, any PWRUP event is ignored until the flags are cleared by writing a 0. These flags can only be written when the system is in the debug mode, (TBBEN = V1P5D). In normal operation, the TRIM_NOK, OTP_NOK and STEST_NOK flags are read only.

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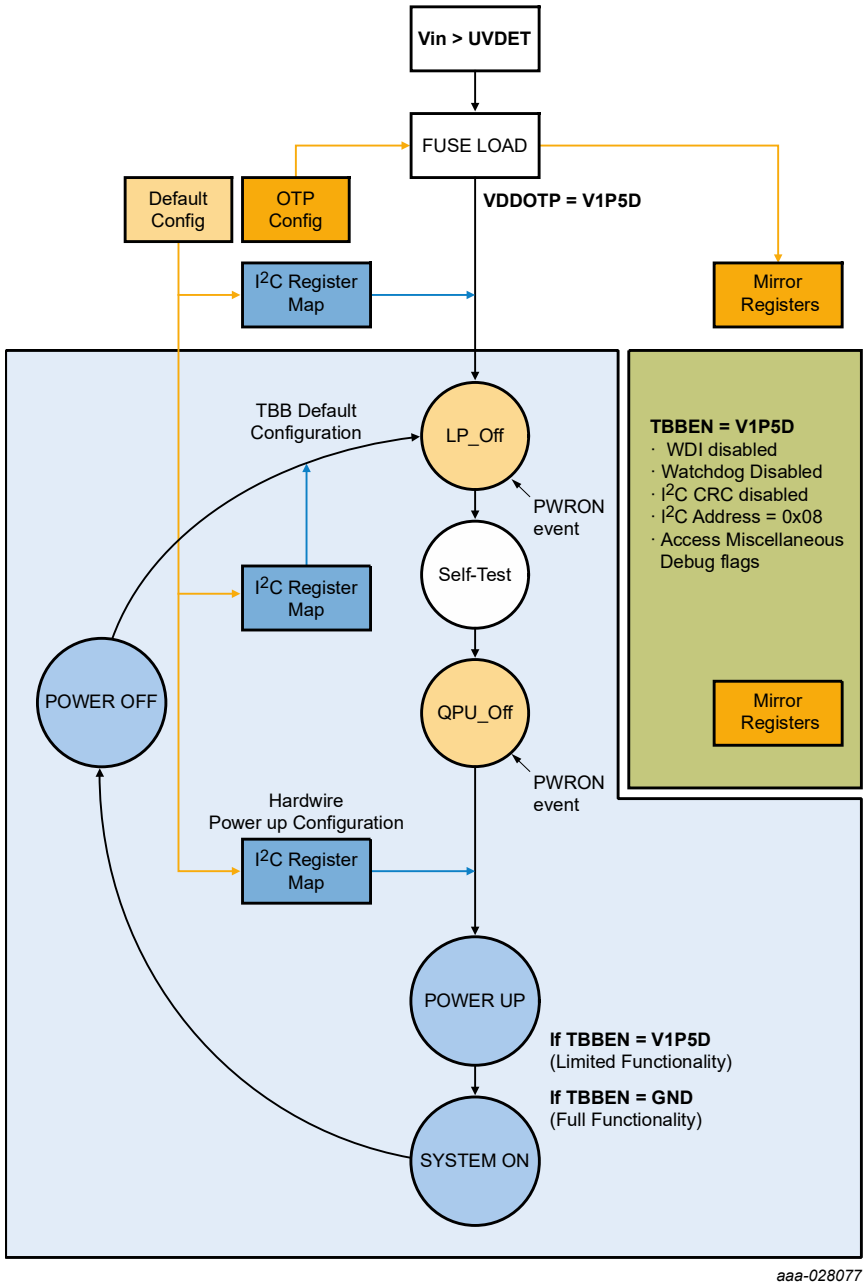

Figure 33. Hardwire operation diagram

For simplicity, the default hardwire configuration in PF5024 is organized based on the OTP register map as shown in Table 59.

Table 59. Default hardwire configuration

ADDR	Register Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Configuration
A0	OTP I2C	0	0	0	0	0	0	0	0	Secured I2C disabled | I2C CRC disabled | I2C address = 0x08
A1	OTP CTRL1	0	0	0	0	0	0	1	0	EWARN_TIME = 100 µs | Fail-safe state enabled | STANDBY active high | PGOOD indicator | RESETBMCU is not influenced by power-up
A2	OTP CTRL2	0	0	0	0	0	1	0	1	XFAIL = disabled | VIN_OVLO shutdown disabled | VIN_OVLO enabled | VIN_OVLO debounce = 100 µs

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Table 59. Default hardwire configuration*...continued*

ADDR	Register Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Configuration
A3	OTP CTRL3	0	0	0	0	0	0	0	1	VTT pull down enabled | Single phase: SW4, SW3 | Dual phase: SW1/SW2
A4	OTP FREQ CTRL	0	0	0	0	0	0	0	0	SYNCIN = Disabled | SYNCOUT disabled | SYNCIN range = 2 MHz to 3 MHz | CLK frequency = 2.5 MHz
A5	OTP PWRON	0	0	0	0	0	0	0	0	PWRON = Level sensitive
A6	OTP WD CONFIG	0	0	0	1	0	0	0	0	WDI generates soft WD reset | WDI detect on rising edge | WD timer disabled | WD timer in Standby disabled |WDI detect in Standby disabled | WD Windows = 100 %
A7	OTP WD EXPIRE	0	0	0	0	0	1	1	1	Max WD Expire count = 8
A8	OTP WD COUNTER	1	0	1	0	1	1	1	1	WD Duration = 1024 ms | Max WD count = 16
A9	OTP FAULT COU NTERS	1	1	1	1	1	1	1	1	Fail-safe MAX counter = 16 | Regulator Fault Max Counter = 16
AA	OTP FAULT TIMERS	0	0	0	0	1	1	1	1	Fail-safe OK timer = 1 minute | Regulator Fault timer = Disabled
AB	OTP PWRDN DLY1	0	0	0	0	0	0	0	0	GRP4 delay = 125 µs | GRP 3 delay = 125 µs | GRP 2 delay = 125 µs | GRP 1 delay = 125 µs
AC	OTP PWRDN DLY2	0	0	0	0	0	0	0	1	Power Down Delay = 0 | RESETBMCU delay = 10 µs
AD	OTP PWRUP CTRL	0	0	0	0	0	0	1	0	PD Mirror Sequence | RESETBMCU PD Group2 | TBASE = 250 µs
AE	OTP RESETBMCU PWRUP	0	0	0	0	0	1	1	1	RESETBMCU SEQ = Slot 6 (TBASE x 6 = 1500 µs)
AF	OTP PGOOD PWRUP	0	0	0	0	0	0	0	0	PGOOD SEQ = OFF
B0	OTP SW1 VOLT	0	1	1	0	0	0	0	0	Voltage = 1.0 V
B1	OTP SW1 PWRUP	0	0	0	0	0	0	0	1	SEQ = Slot 0
B2	OTP SW1 CONFIG1	0	1	0	1	0	0	1	1	UV mon = 7 % | OV mon = 7 % | SW PD Group4 | ILIM min 3.1 A
B3	OTP SW1 CONFIG2	0	0	1	1	1	1	1	0	L = 1 µH | Phase = 0º | DVS Ramp = 12.5 mV/µs | PG = EN | WDBYPASS = Disable
B4	OTP SW2 VOLT	0	1	1	0	0	0	0	0	Voltage = 1.0 V
B5	OTP SW2 PWRUP	0	0	0	0	0	0	0	1	SEQ = Slot 0
B6	OTP SW2 CONFIG1	0	1	0	1	0	0	1	1	UV mon = 7 % | OV mon = 7 % | SW PD Group4 | ILIM min 3.1 A
B7	OTP SW2 CONFIG2	0	0	0	1	1	1	1	0	L = 1 µH | Phase = 180º | DVS Ramp = 12.5 mV/µs | PG = EN | WDBYPASS = Disabled
B8	OTP SW3_VOLT	0	1	1	1	0	0	0	0	Voltage = 1.1 V
B9	OTP SW3 PWRUP	0	0	0	0	0	1	0	1	SEQ = Slot 4 (TBASE x 4 = 1000 µs)
BA	OTP SW3 CONFIG1	0	1	0	1	0	0	1	1	UV mon = 7 % | OV mon = 7 % | SW PD Group4 | ILIM min 3.1 A
BB	OTP SW3 CONFIG2	0	0	1	1	1	1	1	0	L = 1 µH | Phase = 0º | DVS Ramp = 12.5 mV/µs | PG = EN | WDBYPASS = Disable
BC	OTP SW4 VOLT	0	1	1	1	0	0	0	0	Voltage = 1.1 V
BD	OTP SW4 PWRUP	0	0	0	0	0	1	0	1	SEQ =Slot 4 (TBASE x 4 = 1000 µs)
BE	OTP SW4 CONFIG1	0	1	0	1	0	0	1	1	UV mon = 7 % | OV mon = 7 % | SW PD Group4 | ILIM min 3.1 A
BF	OTP SW4 CONFIG2	0	0	1	1	1	1	1	0	L = 1 µH | Phase = 0º | DVS Ramp = 12.5 mV/µs | PG = EN | WDBYPASS = Disable
C8	OTP_OV_BYPASS1	0	0	0	0	0	0	0	0	SWx OVBYPASS disabled
CA	OTP_UV_BYPASS1	0	0	0	0	0	0	0	0	SWx UVBYPASS disabled
CC	OTP_ILIM_ BYPASS1	1	1	1	1	1	1	1	1	SWx ILIMBYPASS enabled
CE	OTP_PROG_IDH	0	0	0	0	1	1	1	1	Default Program ID high Nibble = 0x0F

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Table 59. Default hardwire configuration*...continued*

ADDR	Register Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Configuration
CF	OTP_PROF_IDL	1	1	1	1	1	1	1	1	Default Program ID low Byte = 0xFF
D0	OTP DEBUG1	0	0	0	0	0	0	0	0	BG Monitor Disabled
D1	OTP SW COMP1	0	0	0	0	0	0	0	0	SW2 = 65GM | SW1 = 65GM
D2	OTP SW COMP2	0	0	0	0	0	0	0	0	SW4 = 65GM | SW3 = 65GM

18 Functional safety

18.1 System safety strategy

The PF5024 is defined in a context of safety and shall provide a set of features to achieve the safety goals on such context. It provides a flexible yet complete safety architecture to comply with ASIL B systems providing full programmability to enable or disable features to address the safety goal. This architecture includes protective mechanisms to avoid unwanted modification on the respective safety features, as required by the system.

The following are features considered to be critical for the functional safety strategy:

- Internal watchdog timer
- External watchdog monitoring input (WDI)
- Output voltage monitoring with dedicated bandgap reference
- Protected I^2C protocol with CRC verification
- Input overvoltage protection
- Analog built-in self-test (ABIST)

18.2 Output voltage monitoring with dedicated bandgap reference

For the type 1 buck regulators, the OV/UV monitor operate from the same reference as the regulator. To ensure the integrity of the type 1 buck regulators, a comparison between the regulator bandgap and the monitoring bandgap is performed. A 5 % to 12 % difference between the two bandgaps is an indicator of a potential regulation or monitoring fault and is considered as a critical issue. Therefore, the device prevents the switching regulators from powering up.

On the PF5024 ASIL B device, if a bandgap error is detected during a power up event, the self-test will fail and prevent the device from powering up regardless of the value of the OTP_BGMON_BYPASS bit.

During system On state, if a drift between two bandgaps is detected:

- When OTP_BGMON_BYPASS = 0, the power stage of the voltage regulators will be shutdown.
- When OTP_BGMON_BYPASS = 1, The bandgap monitor only sends an interrupt to the system to announce the bandgap failure.

The BGMON_I is asserted when a bandgap failure occurs, provided it is not masked.

The BGMON_S bit is set to 0 when the bandgaps are within range, and set to 1 when the bandgaps are out of range.

18.3 ABIST verification

The PF5024 ASIL B implements an ABIST verification of all output voltage monitors as well as PGOOD pin. The ABIST verification on the output voltage monitoring behaves as follows:

- Device tests the OV comparators for each individual SWx supply during the self-test routine
- Device tests the UV comparators for each individual SWx supply during the self-test routine

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- During the ABIST verification, it is required to ensure the corresponding OV/UV comparators are able to toggle, which in turn is a sign of the integrity of these functions
- If any of the comparators is not able to toggle, a warning bit is set on the I^2C register map.
  - The ABIST_OV1 register contains the AB_SWx_OV bits for all external regulators.
  - The ABIST_UV1 register contains the AB_SWx_UV bits for all external regulators.
- The ABIST registers are cleared or overwritten each time the ABIST check is performed.
- The ABIST registers are part of the secure registers and will require an I^2C secure write to be cleared if this feature is enabled.

Once ABIST check is performed, the PF5024 can proceed with the power up sequence and the MCU should be able to request the value of these registers and learn if ABIST failed for any of the voltage monitors.

The AB_RUN bit is provided to perform an ABIST verification on demand.

When the AB_RUN bit is set to 1, the control logic perform an ABIST verification on all OV/UV monitoring circuits. When the ABIST verification is finished, the AB_RUN bit self-clear to 0 and a new ABIST verification can be commanded as needed.

When the secure write feature is enabled, the system must perform a secure write sequence in order to start an ABIST verification on demand.

When the PF5024 performs an ABIST verification on demand, the OV/UV fault monitoring is blanked for a maximum period of 200 µs. During this time, the system must ensure it is in a safe state, or it is safe to perform this action without violating the safety goals of the system.

If a failure on the OV/UV monitor is detected during the ABIST on demand request, the PMIC will assert the corresponding ABIST flags. It is responsibility of the system to perform a diagnostic check after each ABIST verification to ensure it places the system in safe state if an ABIST fault is detected.

19 IC level quiescent current requirements

Table 60. Quiescent current requirements

All parameters are specified at T_A = −40 to 125 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5.0 V and T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
I_{LPOFF}	LP_Off state LPM_OFF = 0 VIN > UVDET	—	40	150	µA
I_{QPUOFF}	QPU_Off LPM_OFF = 1 System ready to power on	—	750	1000	µA
I_{SYSON}	System On core current Run or standby and all regulators disabled Coin cell charger disabled AMUX disabled	—	750	1000	µA
I_{FSAFE}	Fail-safe mode VIN > UVDET	—	40	150	µA

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20 Typical applications

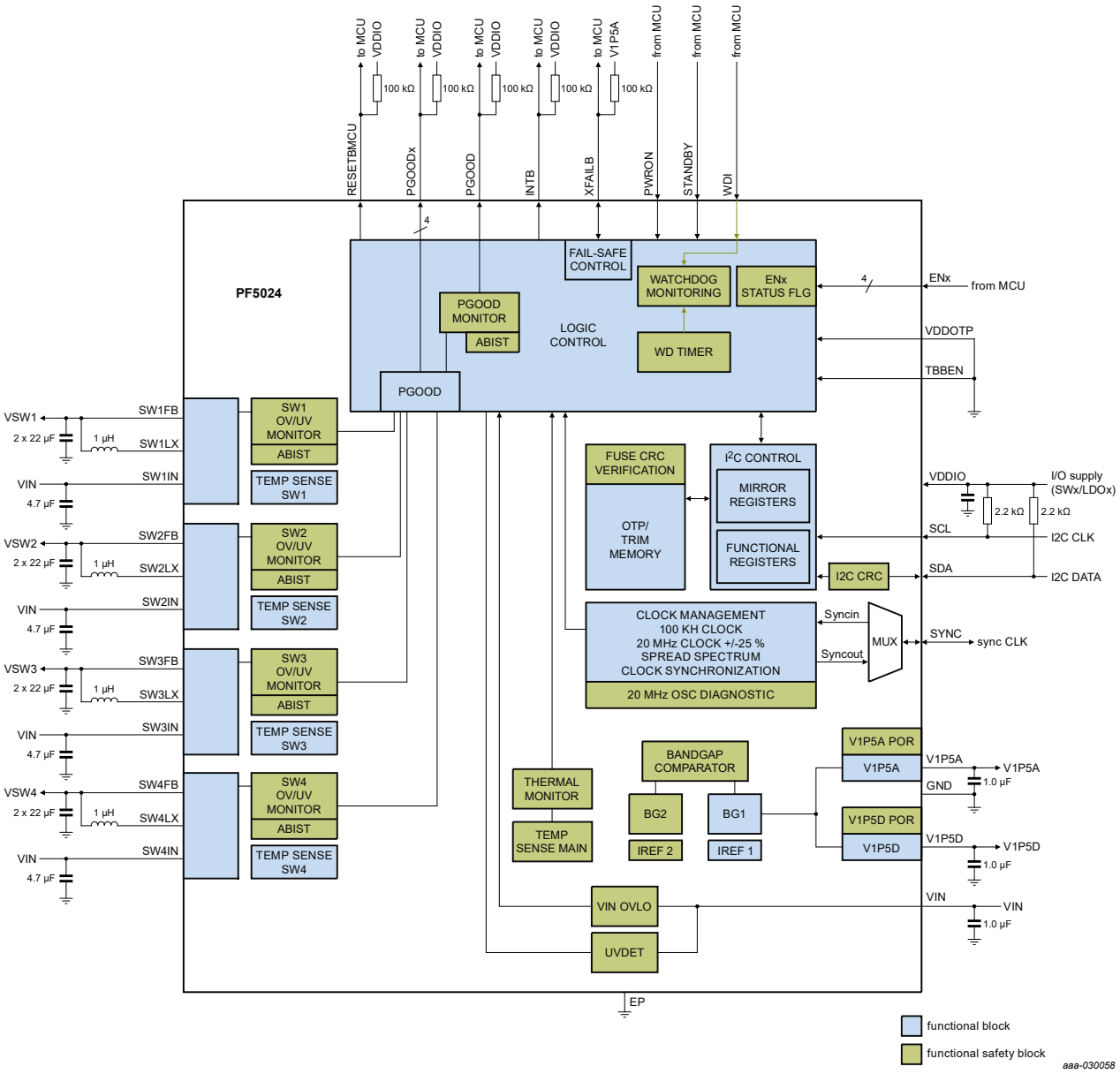

Figure 34. Typical application diagram

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21 Package outline

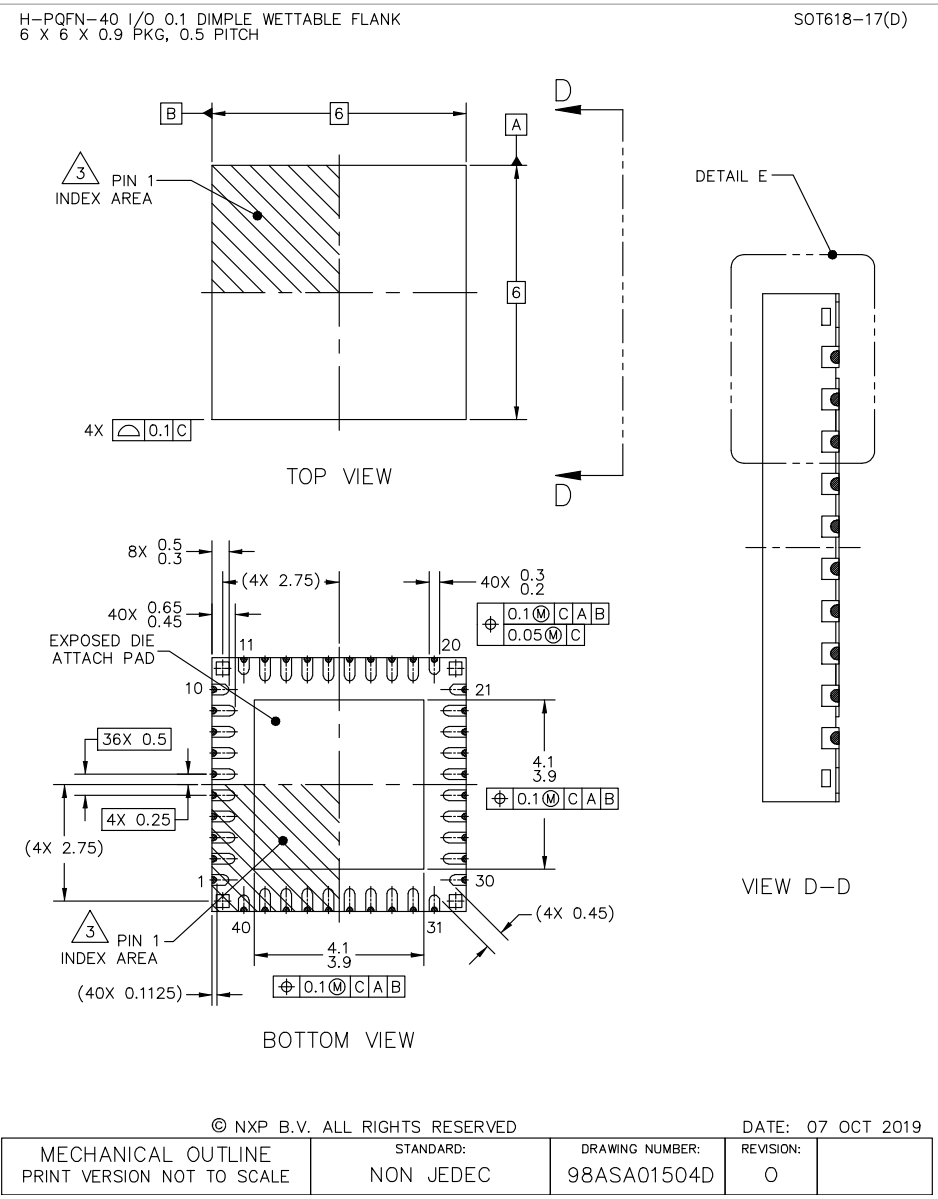

Figure 35. Package outline for HVQFN40 - SOT618-17(D)

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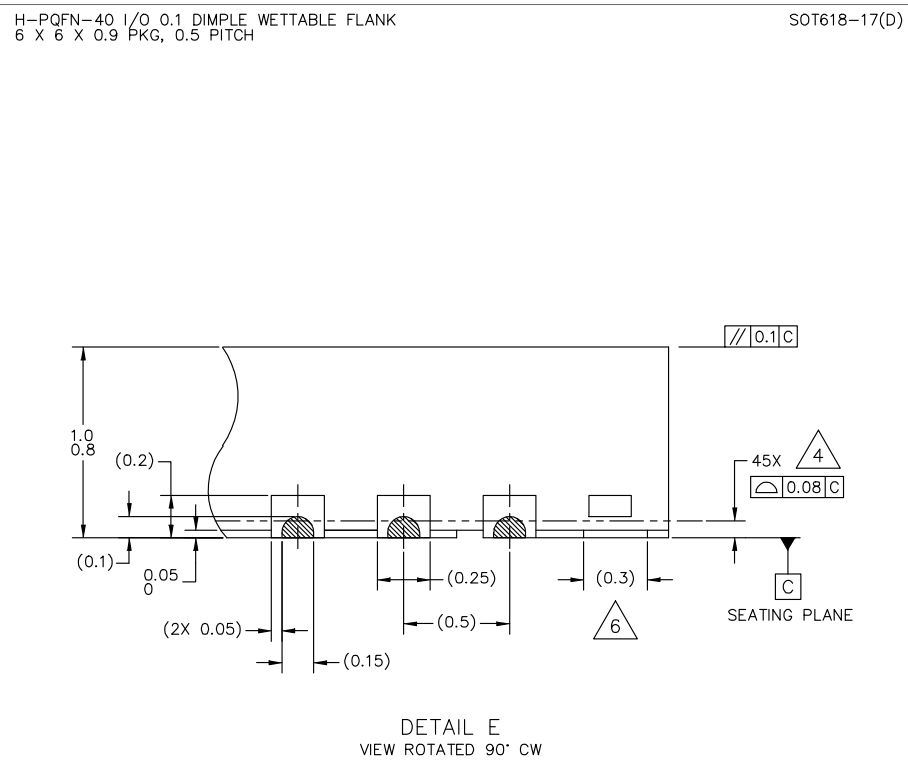

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Figure 36. Package outline detail for HVQFN40 - SOT618-17(D)

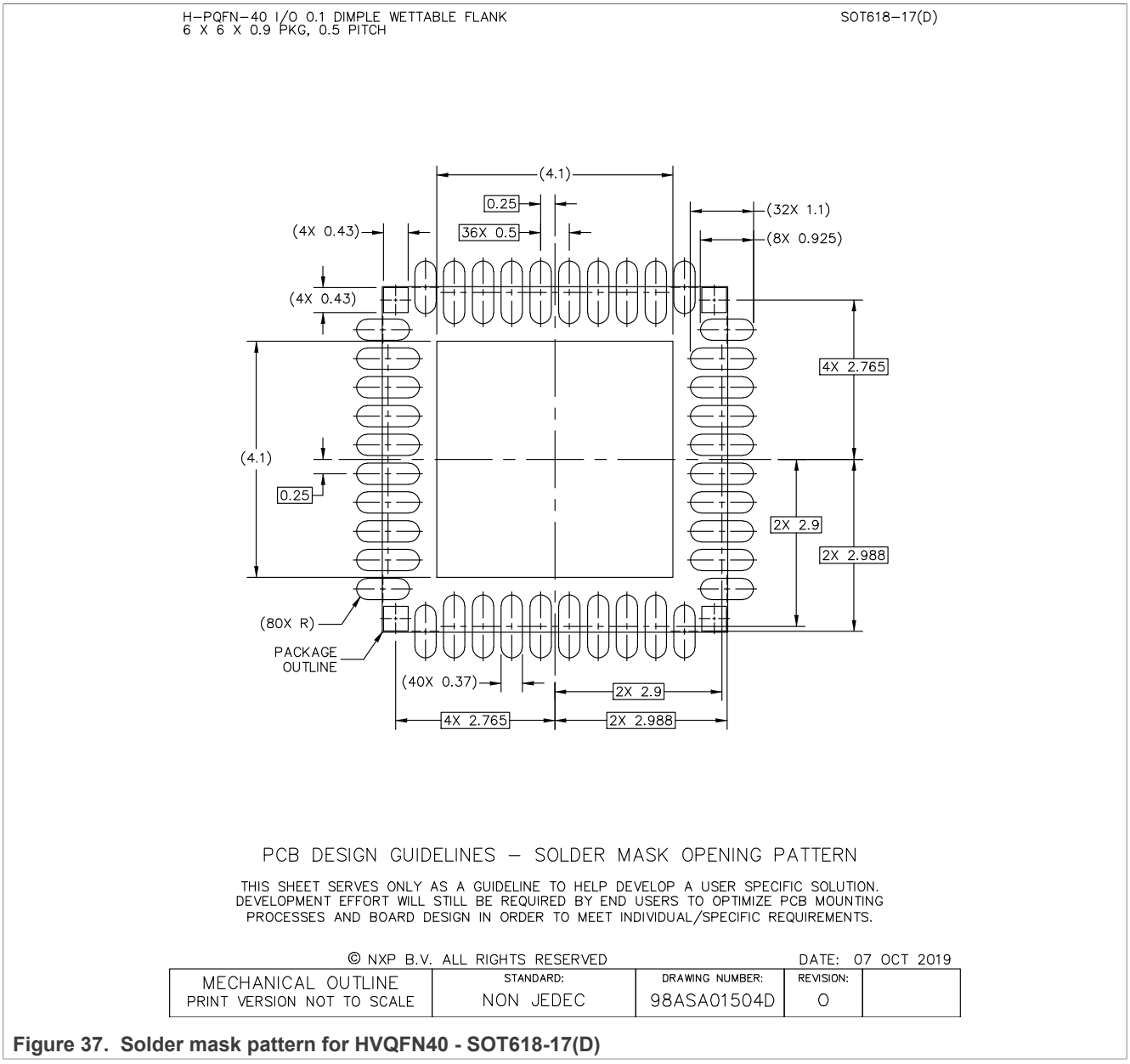

Figure 37. Solder mask pattern for HVQFN40 - SOT618-17(D)

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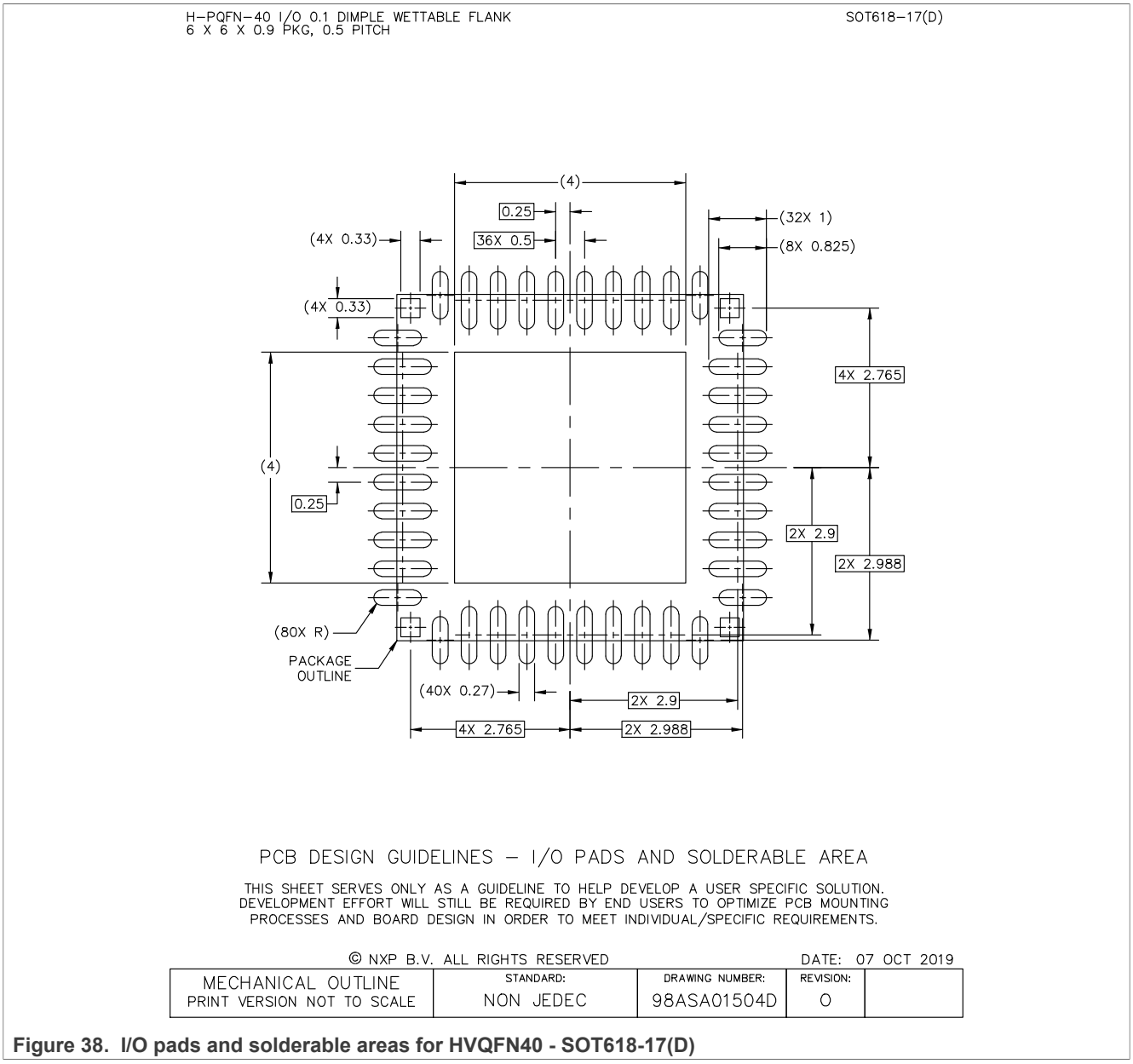

Figure 38. I/O pads and solderable areas for HVQFN40 - SOT618-17(D)

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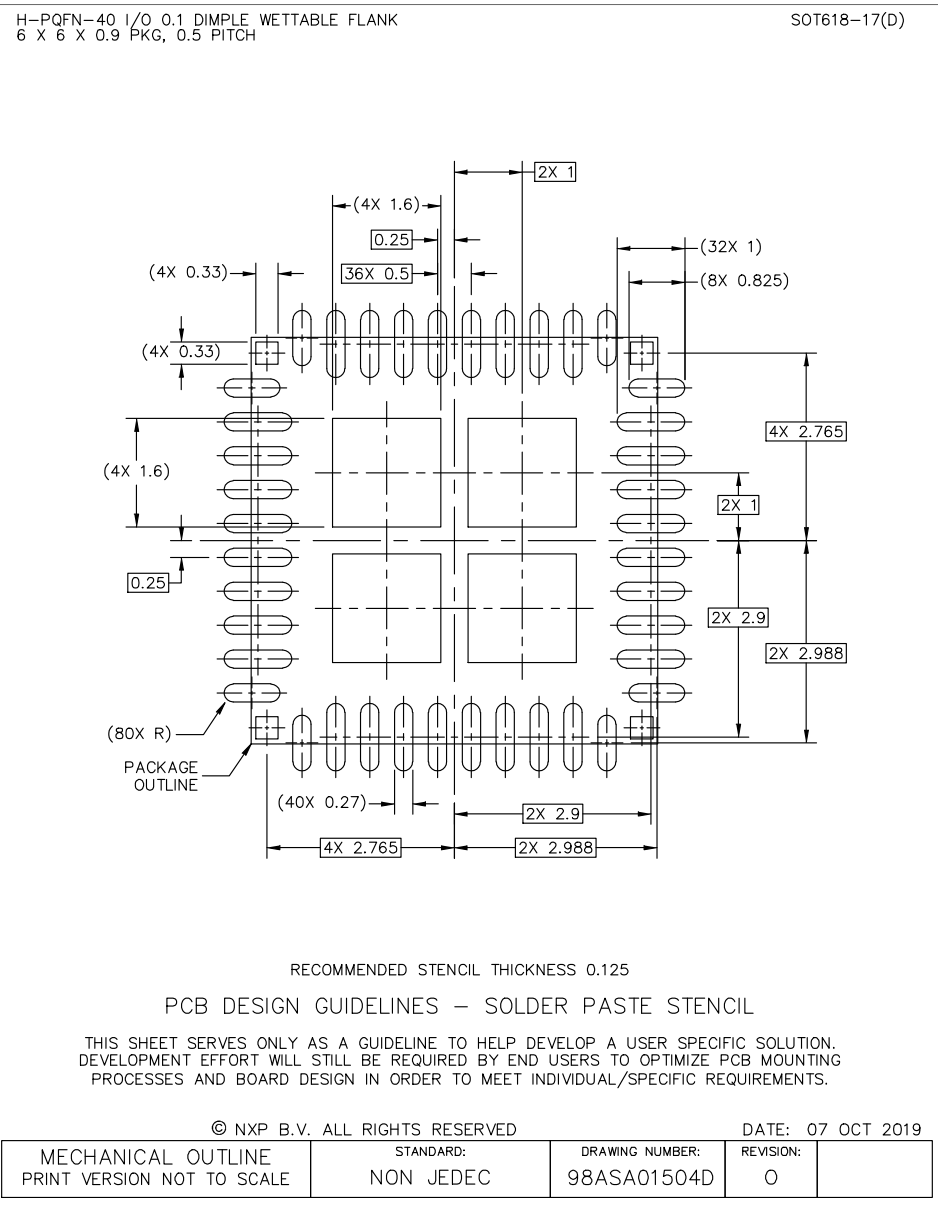

Figure 39. Solder paste stencil for HVQFN40 - SOT618-17(D)

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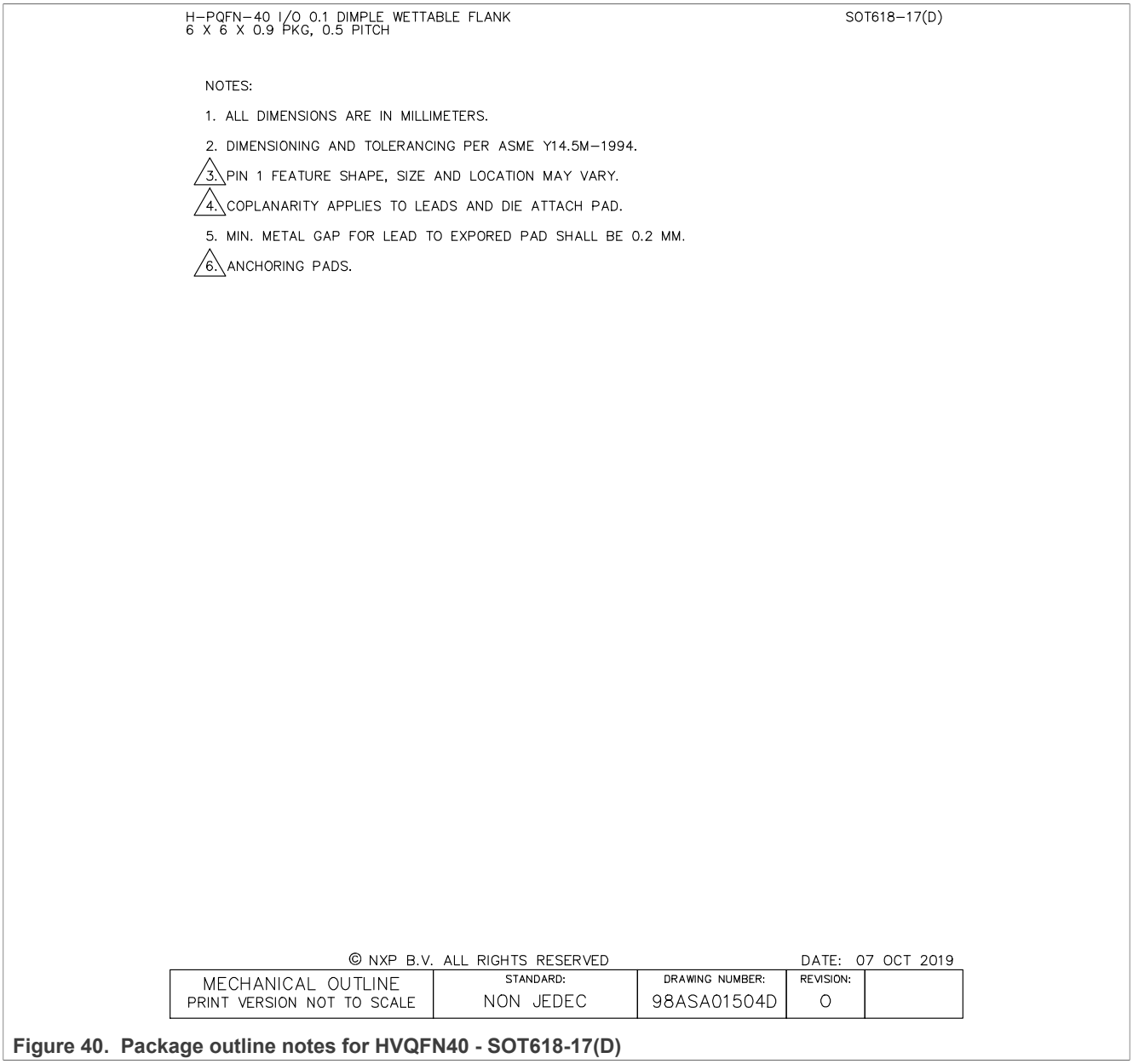

Figure 40. Package outline notes for HVQFN40 - SOT618-17(D)

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22 Revision history

Table 61. Revision history

Document ID	Release date	Description
PF5024 v.3.2	5 March 2024	• Updated per CIN number 202402005I • Added the CIN numbers back in for v.2.0 and v.3.0 that were inadvertently omitted during the v.3.1 revision history update
PF5024 v.3.1	22 February 2024	• Updated per CIN number 202402005I • Section 4: Added statement regarding OTP emulation and programming • Updated legal information
PF5024 v.3.0	20 September 2021	• Updated per CIN number 202107008I • Global: replaced "master" with "primary" and "slave" with "secondary" or "companion" • Section 4: updated the package version from SOT618-14 to SOT618-17(D). This update is due to the change in the assembly site for this product. • Section 4: updated all the orderable part numbers with new part number notation for the new assembly site • Section 10: updated min storage temp to -55 °C • Section 14.9.10: updated Figure 20 and Figure 21 • Table 6: added Junction to Board Thermal Parameters • Section 21: updated the package outline drawing for the new assembly site - NXP ATTJ and to change the package from step-cut QFN to dimple cut QFN
PF5024 v.2.0	14 December 2020	• Updated per CIN number 202012017I Section 12.1: updated Buck regulators features list (deleted "2 % accuracy") • Section 13: updated Figure 5 and added new transitions to the State machine transition definition table • Section 14.8: added Table 26 • Section 14.9.8: added new paragraph before Table 33 • Section 15.2: added a section for current limit specification (The current limit specification is given with respect to the inductor ……) • Table 45: updated V_{SWxACC} values and conditions • Table 45 (I_{SWx}, I_{SWx_DP}, I_{SWx_TP}, I_{SWx_QP}): added note "The Type 1 buck regulator in single or multi phase configuration is capable of providing output current above the nominal max current specification as long as it does not reach the current limitation. However, if operating above the nominal maximum current, overall thermal considerations must be taken into account to prevent PMIC thermal shutdown during high ambient temperature conditions." • Section 15.4.5: added a section to provide clarification on the system level implementation to handle an external clock failure (Upon an external clock failure, the MCU must proof…..)
PF5024 v.1.0	15 April 2020	Initial release of product data sheet.

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[1] Please consult the most recently issued document before initiating or completing a design.
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