PF5300; PF5301; PF5302

12 A / 8 A / 15 A core supply regulators with AVP and watchdog

Rev. 7.0 — 27 July 2026 Product data sheet

1 Overview

The PF5300, PF5301, and PF5302 integrate high-performance buck converters, 12 A, 8 A, and 15 A, respectively, to power high-end automotive and industrial processors.

With adaptive-voltage positioning and a high-bandwidth loop, they offer transient regulation to minimize capacitor requirements.

Clock synchronization and spread-spectrum features reduce EMC issues in the system. The PF5300/PF5301/PF5302 can operate as standalone point-of-load regulator ICs or as companion chips to a larger PMIC.

Built-in one-time programmable (OTP) memory stores key startup configurations, drastically reducing external components. Regulator parameters are adjustable through high-speed I^2C after startup, offering flexibility for different system states.

PF5300/PF5301/PF5302 have been developed to comply with the ISO 26262 automotive safety specification. They include configurable feature sets to fit in or support applications with safety levels up to ASIL D.

To simplify, PF5300 is used in this document to refer to PF5300, PF5301, and PF5302. Unless explicitly mentioned, references to PF5300 include PF5301 and PF5302.

2 Features

The PF5300/PF5301/PF5302 integrate a high-performance 12 A / 8 A /15 A buck converter to power high-end automotive and industrial processors.

- High-performance core buck regulator
  - 12 A, 5 V_{IN} buck regulator - internal FETs (PF5300)
  - 8 A, 5 V_{IN} buck regulator - internal FETs (PF5301)
  - 15 A, 5 V_{IN} buck regulator - internal FETs (PF5302)
  - 2.7 V to 5.5 V input range
  - 0.5 V to 1.2 V output range
  - High efficiency
  - ±1 % output accuracy
  - 2 MHz to 3 MHz switching frequency
  - Dynamic voltage scaling
  - Programmable adaptive-voltage positioning (AVP) (droop)
- 1.5 µA quiescent current in OFF mode
- PFM mode in STBY for **PF530xB version**
- Fast startup time (< 500 µs)
- OTP memory for device configuration
- Overtemperature protection
- Safety features
  - Available in ASIL D, ASIL B, and QM variations
  - Watchdog timer
  - 1 % OV/UV monitoring
  - PGOOD output
  - Analog built-in self-test
- Automotive AEC-Q100 qualified and extended industrial versions available
- Rated from -40 ℃ to 150 ℃ Tj
- 3.5 mm x 4.5 mm WF-QFN package

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

3 Simplified application diagram

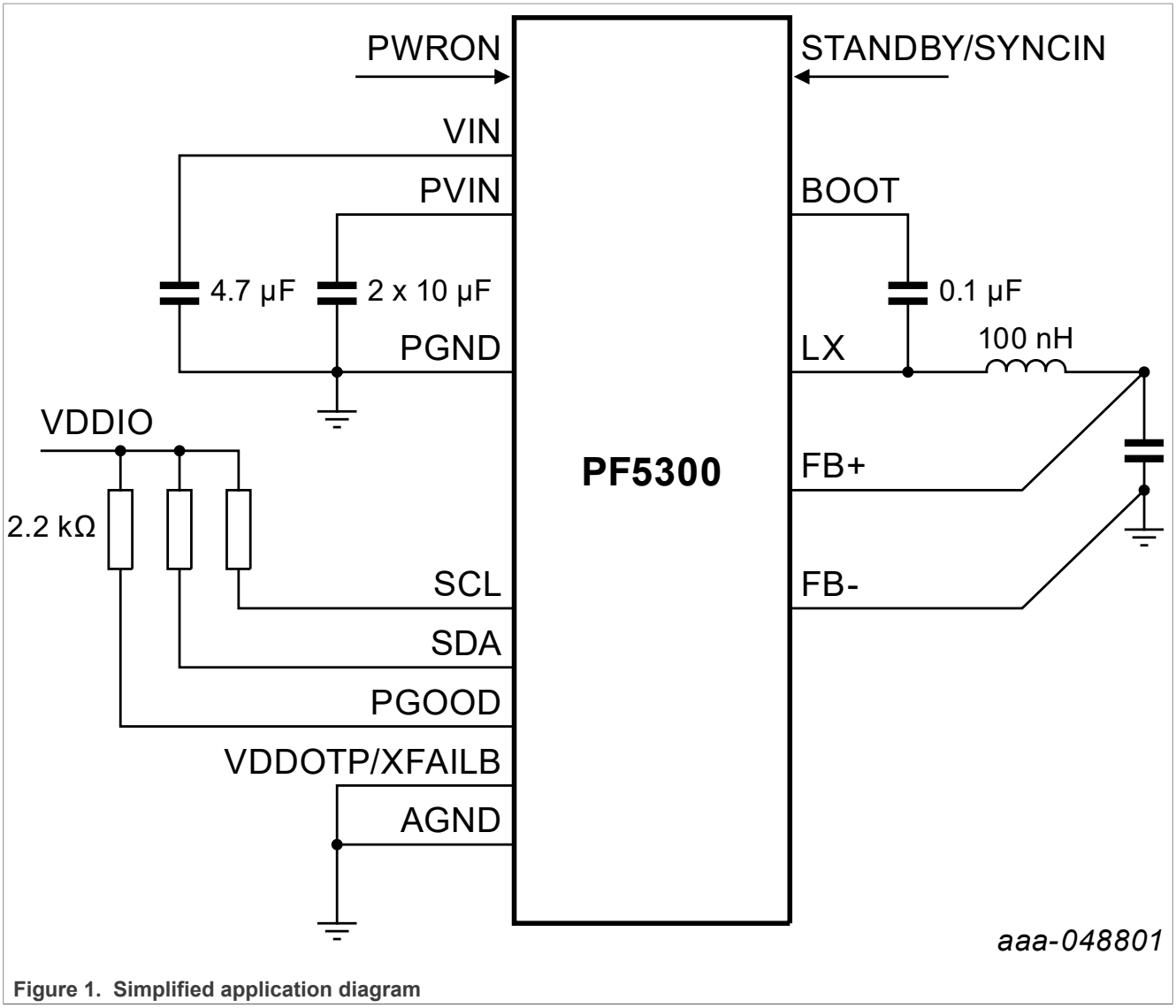


Figure 1. Simplified application diagram

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

4 Ordering information

Table 1. Ordering information

Part number[1][2]	Current Capability	ASIL	MCU	Application	Package Description	Package Version
MPF53BDAMMA1ES	12 A	QM	S32G3	Automotive	HWQFN24, thermal enhanced, very-very thin quad flat package, no leads, 24 terminals, step-cut wettable flank, 0.5 mm pitch, 3.5 mm x 4.5 mm x 0.68 mm body	SOT2090-1(SC)
MPF5300AMMALES	12 A	QM	S32N_VDD			
MPF5300AMMA0ES[3]	12 A	QM	—			
MPF5300AMMAMES	12 A	QM	S32N_VDD_RTU			
MPF5300AMBA0ES[3]	12 A	B	—			
MPF5300AMDA0ES[3]	12 A	D	—			
MPF5301AMMABES	8 A	QM	i.MX95 VDD_ARM			
MPF5301AMMA0ES[3]	8 A	QM	—			
MPF5301AMBA0ES[3]	8 A	B	—			
MPF5301AMDA0ES[3]	8 A	D	—			
MPF5302AMMAAES	15 A	QM	i.MX95 VDD_SOC			
MPF5302AMMA0ES[3]	15 A	QM	—			
MPF5302AMBA0ES[3]	15 A	B	—			
MPF5302AMDA0ES[3]	15 A	D	—			
MPF5300AVNA0EP[3]	12 A	QM	—	Industrial	H-FC-PQFN24, thermal enhanced - flip chip - plastic quad flat non-lead, 24 terminals, 0.5 mm pitch, 3.5 mm x 4.5 mm x 0.68 mm body	SOT2090-1
MPF5301AVNA0EP[3]	8 A	QM	—			
MPF5301AVNABEP	8 A	QM	i.MX95 VDD_ARM			
MPF5302AVNA0EP[3]	15 A	QM	—			
MPF5302AVNAAEP	15 A	QM	i.MX95 VDD_SOC			
MPF53BDBMMA1ES[4]	12 A	QM	S32G3	Automotive	HWQFN24, thermal enhanced, very-very thin quad flat package, no leads, 24 terminals, step-cut wettable flank, 0.5 mm pitch, 3.5 mm x 4.5 mm x 0.75mm body	SOT2283-1(SC)
MPF5300BMMALES[4]	12 A	QM	S32N_VDD			
MPF5300BMMA0ES[4][3][3]	12 A	QM	—			
MPF5300BMMAMES[4]	12 A	QM	S32N_VDD_RTU			
MPF5300BMBA0ES[4][3]	12 A	B	—			
MPF5300BMDA0ES[4][3]	12 A	D	—			
MPF5300BMMBRES[4]	12 A	QM	i.MX95, i.MX 952,i.MX 943			
MPF5301BMMABES[4]	8 A	QM	i.MX95 VDD_ARM			
MPF5301BMMA0ES[4][3]	8 A	QM	—			
MPF5301BMBA0ES[4][3]	8 A	B	—			
MPF5301BMDA0ES[4][3]	8 A	D	—			
MPF5302BMMAAES[4]	15 A	QM	i.MX95 VDD_SOC			
MPF5302BMMA0ES[4][3]	15 A	QM	—			
MPF5302BMBA0ES[4][3]	15 A	B	—			
MPF5302BMDA0ES[4][3]	15 A	D	—			

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 1. Ordering information*...continued*

Part number[1][2]	Current Capability	ASIL	MCU	Application	Package Description	Package Version
MPF5300BVNA0EP[4][3]	12 A	QM	—	Industrial	H-FC-PQFN24, thermal enhanced - flip chip - plastic, quad flat non-lead, 24 terminals, 0.5 mm pitch, 3.5 mm x 4.5 mm x 0.75 mm body	SOT2283-1
MPF5300BVNBREP[4]	12 A	QM	i.MX95, i.MX 952,i.MX 943			
MPF5301BVNA0EP[4][3]	8 A	QM	—			
MPF5301BVNABEP[4][3]	8 A	QM	—			
MPF5302BVNA0EP[4][3]	15 A	QM	—			
MPF5302BVNAAEP[4]	15 A	QM	i.MX95 VDD_SOC			

[1] PF530xB version is recommended for new designs.
[2] To order parts in tape and reel, add the R2 suffix to the part number.
[3] Non-programmed device.
[4] Recommended for new designs.

OTP emulation and programming performed by the customer is allowed during engineering development using NXP's latest graphical user interface and socketed evaluation board.

Customer is not allowed to perform OTP programming for production purposes. Only NXP or a recommended third party are allowed to program the device for production purposes.

Table 2. Feature comparison

Feature	QM version bundled with VR5510	QM version general	ASIL B version general	ASIL D version general
SW1 DC-DC converter	Yes	Yes	Yes	Yes
High accuracy voltage monitor	No	Yes	Yes	Yes
ABIST	No	No	Yes	Yes
On-demand ABIST	No	No	No	Yes
Simple watchdog timer	No	No	Yes	Yes
Challenger watchdog timer	No	No	No	Yes
PGOOD output	Yes	Yes	Yes	Yes
I2C bus for control/ diagnostics	Yes	Yes	Yes	Yes
I2C CRC	No	No	No	Yes
Secure write	No	No	No	Yes
Misc. internal safety mechanisms	No	No	Yes	Yes

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

5 Applications

- Automotive – infotainment, gateway, domain controllers
- High-end consumer and industrial

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

6 Internal block diagram

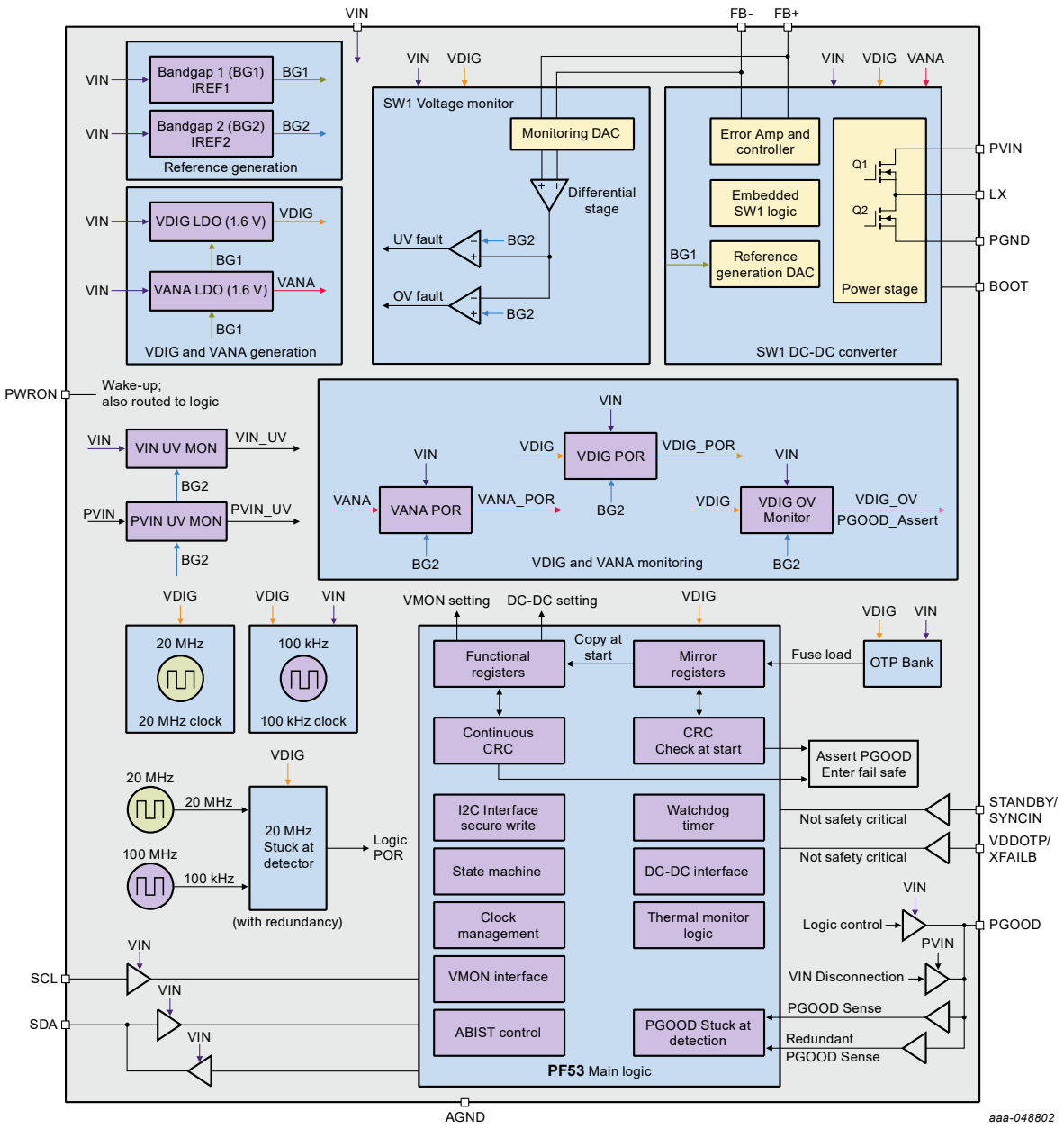


Figure 2. PF5300 internal block diagram

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

7 Pinning information

7.1 Pinout

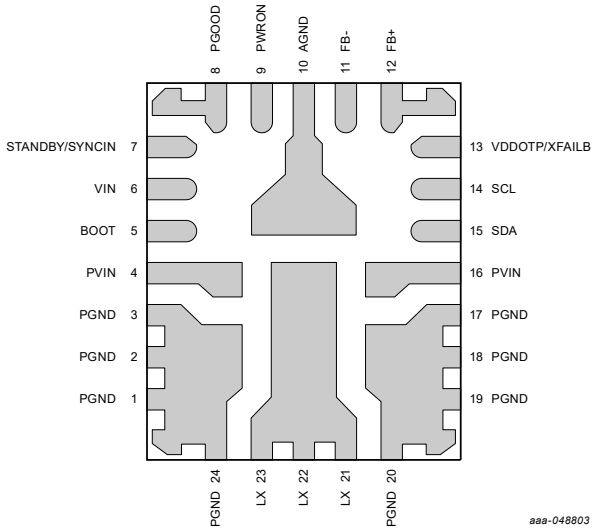


Figure 3. PF5300 pinout (bottom view)

7.2 Pin descriptions

Table 3. Pin descriptions

Pin number	Pin name	Description	Minimum operating voltage (V)	Maximum operating voltage (V)
1-3, 17-20, 24	PGND	Power ground of buck converter. Connect to ground plane including top layer.	-0.3	0.3
4, 16	PVIN	PVIN input to buck converter. Bypass with 0.1 µF and 10 µF on either side with the shortest possible loop distance between corresponding PGND pins.	-0.3	5.5
5	BOOT	Bootstrap pin for high-side gate drive. Connect 0.1 µF from BOOT to LX pin.	(LX - 0.3 V)	(LX + 5.5 V)
6	VIN	Gate drive input. Connect to gate drive supply (preferably 5.0 V). Bypass with 4.7 µF capacitor.	-0.3	5.5
7	STANDBY/ SYNCIN	External clock synchronization input. Connect to ground if not used. Optionally used as STANDBY input to enter Low-power mode at the system level.	-0.3	5.5
8	PGOOD	Open-drain PGOOD output. Pull up to external pullup voltage via 4.7 kΩ resistor.	-0.3	5.5
9	PWRON	Enable input. 1.8 V logic accepted. Also used to enter Debug mode when pulled up to 8 V prior to startup.	-0.3	9
10	AGND	Analog ground of IC. Connect to ground plane using a via.	-0.3	0.3
11	FB-	Differential amplifier negative input. Connect to negative (ground) end of output voltage.	-0.3	5.5

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 3. Pin descriptions*...continued*

Pin number	Pin name	Description	Minimum operating voltage (V)	Maximum operating voltage (V)
12	FB+	Differential amplifier positive input. Connect to positive end of output voltage. Route FB+ and FB- in parallel on the PCB to reduce differential noise.	-0.3	5.5
13	VDDOTP/ XFAILB	VDDOTP used to program OTP memory and enter Fuse Emulation mode. Optional use as XFAILB pin to communicate with other NXP PF PMICs. Connect to ground in application if XFAILB function is not used. Pull up to XFAILB bus voltage with a 4.7 kΩ resistor if the function is used.	-0.3	9
14	SCL	I^2C clock input. Pull up to external I/O voltage.	-0.3	5.5
15	SDA	I^2C data line. Pull up to external I/O voltage.	-0.3	5.5
21-23	LX	Output of buck converter.	-0.7	5.5

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

8 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
VIN, PVIN	Main input supply voltage [1]	−0.3	6.0	V
LX	Regulator switching voltage [1]	−0.7	6.0	V
BOOT	Bootstrap voltage [1]	(LX - 0.3 V)	(LX + 6 V)	V
FB+, FB-	Regulator feedback [1]	−0.3	6.0	V
PGOOD, STANDBY/ SYNCIN, SCL, SDA	I/O voltages [1]	−0.3	6.0	V
VDDOTP/XFAILB, PWRON	OTP programming input supply voltage (VDDOTP/XFAILB), Debug entry (PWRON)[1]	−0.3	10	V

[1] Pin reliability may be affected if system voltages are above the maximum operating range of 6.0 V for an extended period of time. To minimize system reliability impact, system must not operate above 6.0 V for more than 1800 seconds over the lifetime of the device.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

9 Characteristics

9.1 ESD ratings

All ESD specifications are compliant with AEC-Q100 specification.

Table 5. ESD ratings

Symbol	Parameter	Min	Typ	Max	Unit
VESD	Human body model [1]	—	—	2000	V
VESD	Charge device model [1]	—	—	500	V
ILATCHUP	Latch-up current	—	—	100	mA

[1] ESD testing is performed in accordance with the human body model (HBM) (CZAP = 100 pF, RZAP = 1500 Ω), and the charge device model (CDM), robotic (CZAP = 4.0 pF).

9.2 Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient operating temperature	−40	—	125	°C
T_A	Ambient operating temperature (industrial)	−40	—	105	°C
Tj	Junction temperature	−40	—	150	°C
TST	Storage temperature range	−55	—	150	°C
TPPRT	Peak package reflow temperature	—	—	260	°C

Table 7. QFN24 thermal resistance and package dissipation ratings

Rating	Board type[1]	Symbol	Value	Unit
Junction to Ambient Thermal Resistance[2]	JESD51-9, 2s2p	RθJA	41.3	°C/W
Junction-to-Top of Package Thermal Characterization Parameter [2]	JESD51-9, 2s2p	ΨJT	0.6	°C/W
Junction to Case Thermal Resistance[3]	JESD51-9	RθJC	8.4	°C/W
Junction to Ambient Thermal Resistance[4]	Customized, 2s6p	RθJA	24.8	°C/W

[1] Thermal test board meets JEDEC specification for this package (JESD51-9).
[2] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
[3] Junction-to-Case thermal resistance determined using an isothermal cold plate. Case is defined as the bottom of the packages (exposed pad).
[4] Simulation of PF53 on an eight-layer (2s6p = eight layers) application representative PCB. Actual performance on a given application should be simulated by the customer to optimize thermal design of the system. IcePAK, Flotherm, and 3D PF5300 simulation models are available on NXP.com.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

9.3 Recommended operating conditions

All parameters are specified at Ta = -40 °C to 125 °C, PVIN = V_{IN} = 3.3 V, PWRON = 1.8 V, no load on regulator, Fsw = 2.2 MHz, typical external component values, unless otherwise noted. Typical values are specified at 25 °C, unless otherwise noted.

Table 8. Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	V_{IN} operating range	VIN_{UVDET}	—	5.5	V
PVIN	PVIN operating range	$PVIN_{UVDET}$	—	5.5	V
VIN_UVDET_R	Rising V_{IN} UVDET	2.85	3.00	3.15	V
VIN_UVDET_F	Falling V_{IN} UVDET	2.80	2.90	3.00	V
PVIN_UVDET_R	Rising PVIN UVDET	2.6	2.75	2.9	V
PVIN_UVDET_F	Falling PVIN UVDET	2.5	2.6	2.7	V

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

10 General description

10.1 Functional block diagram

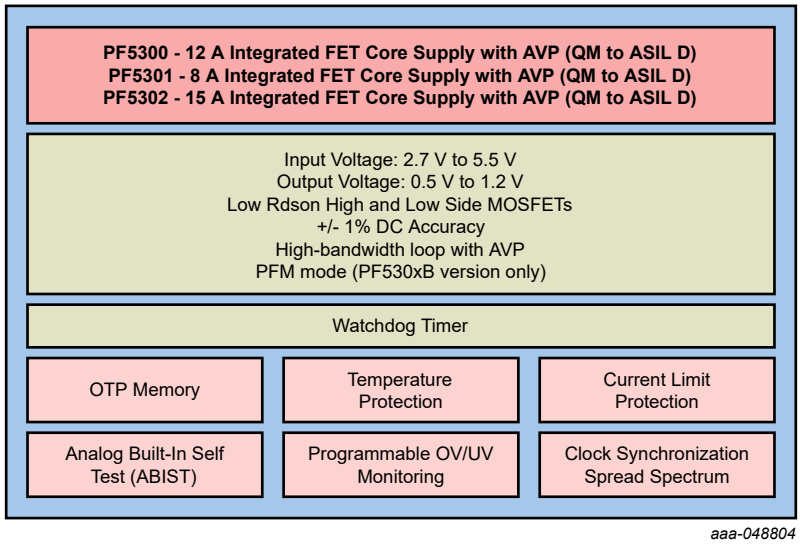


Figure 4. Functional block diagram

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

11 State machine

The PF5300 features a state-of-the-art state machine for a seamless processor interface. The state machine handles the IC startup, provides fault monitoring and reporting, and protects the IC and the system during fault conditions. The STATE[7:0] register provides information on the current state of the state machine. See Section 11.1 for descriptions of the states.

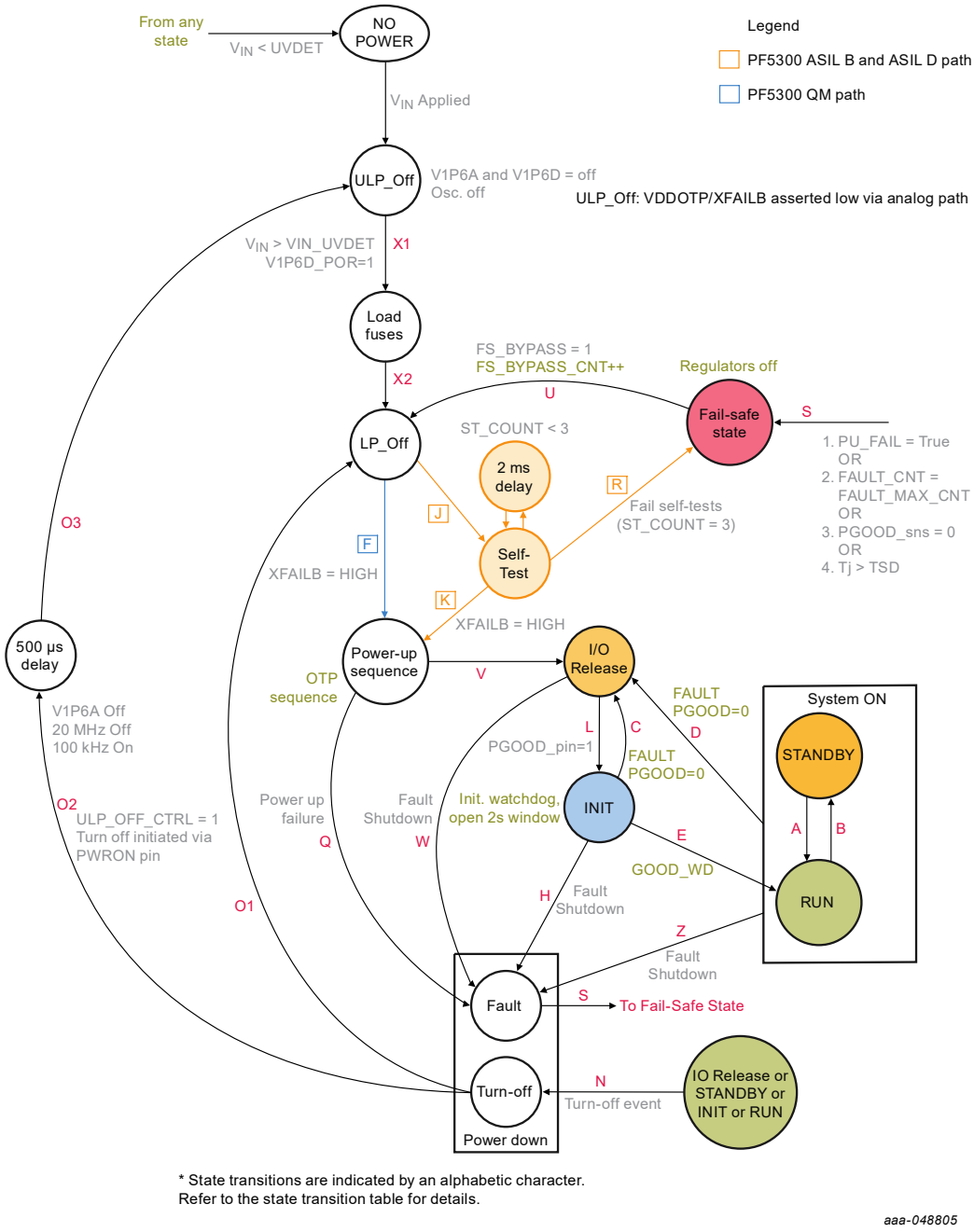


Figure 5. State machine diagram

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 9. State transition table

Transition	Conditions
Transition A Description: STANDBY to RUN	Condition 1: (STANDBY = 0 && STANDBYINV bit = 0 && (STBY_DELAY expiry if applicable))
Transition A Description: STANDBY to RUN	Condition 2: (STANDBY = 1 && STANDBYINV bit = 1 && (STBY_DELAY expiry if applicable))
Transition B Description: RUN to STANDBY	Condition 1: (STANDBY = 1 && STANDBYINV bit = 0 && (STBY_DELAY expiry if applicable))
Transition B Description: RUN to STANDBY	Condition 2: (STANDBY = 0 && STANDBYINV bit = 1 && (STBY_DELAY expiry if applicable))
Transition C Description: INIT to IO_Release	Condition 1: PGOOD assertion (low) because of SW1 OV Fault With OTP_PGOOD_SW1_OV = 1
Transition C Description: INIT to IO_Release	Condition 2: PGOOD assertion (low) because of SW1 UV Fault With OTP_PGOOD_SW1_UV = 1
Transition C Description: INIT to IO_Release	Condition 3: PGOOD assertion (low) because of band gap error with OTP_PGOOD_BG = 1
Transition C Description: INIT to IO_Release	Condition 4: PGOOD assertion (low) because of PGOOD stuck at 0
Transition C Description: INIT to IO_Release	Condition 5: PGOOD assertion (low) because of no good watchdog refresh (if enabled) for 2 s and FAULT_CNT < FAULT_MAX_CNT
Transition C Description: INIT to IO_Release	Condition 6: PGOOD assertion (low) because of PGOOD_RLS clear via I^2C (PGOOD_SEQ = 0x00)
Transition D Description: System ON to IO_Release	Condition 1: PGOOD assertion (low) because of SW1 OV fault with OTP_PGOOD_SW1_OV = 1
Transition D Description: System ON to IO_Release	Condition 2: PGOOD assertion (low) because of SW1 UV fault with OTP_PGOOD_SW1_UV = 1
Transition D Description: System ON to IO_Release	Condition 3: PGOOD assertion (low) because of band gap error with OTP_PGOOD_BG = 1
Transition D Description: System ON to IO_Release	Condition 4: PGOOD assertion (low) because of PGOOD stuck at 0
Transition D Description: System ON tol IO_Release	Condition 5: PGOOD assertion (low) because of WD_ERROR_CNT[3:0] >= WD_MAX_ERROR[1:0] and FAULT_CNT < FAULT_MAX_CNT
Transition D Description: System ON to IO_Release	Condition 6: PGOOD assertion (low) because of PGOOD_RLS clear via I^2C (PGOOD_SEQ = 0x00)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 9. State transition table*...continued*

Transition	Conditions
Transition E Description: INIT to RUN	Condition 1: 2 s watchdog window petted with good watchdog refresh
Transition E Description: INIT to RUN	Condition 2. Watchdog disabled
Transition F Description: LP_Off to power-up sequence (PF5300 QM Only)	Condition 1: PWRON = 1 (but less than debug threshold) && PVIN > PVIN_UVDET && Tj < TSD (If entered LP_Off via Transition U or O1. Bypass if entered LP_Off via Transition X2) && {[(VIN < VIN_OVLO) && VIN_OVLO_SDWN = 1] OR [VIN_OVLO_SDWN = 0]} && TRIM_NOK = 0 && OTP_NOK = 0 && VDDOTP < VDDOTP_threshold && (OTP_XFAILB_EN = 0)
Transition F Description: LP_Off to power-up sequence (PF5300 QM Only) .	Condition 2: PWRON = 1 (but less than debug threshold) && PVIN > PVIN_UVDET && Tj < TSD (If entered LP_Off via Transition U or O1. Bypass if entered LP_Off via Transition X2) && {[(VIN < VIN_OVLO) && VIN_OVLO_SDWN = 1] OR [VIN_OVLO_SDWN = 0]} && TRIM_NOK = 0 && OTP_NOK = 0 && VDDOTP < VDDOTP_threshold && (OTP_XFAILB_EN = 1 && XFAILB_pin = High)
Transition H Description: INIT to power down (Fault)	Condition 1: FAULT_CNT = FAULT_MAX_CNT
Transition H Description: INIT to power down (Fault)	Condition 2: Thermal shutdown Tj > TSD
Transition H Description: INIT to Power Down (Fault)	Condition 3: Register Map CRC Error
Transition J Description: LP_Off to Self-test (PF5300 ASIL B and ASIL D Only)	Condition: PWRON = 1 (but less than debug threshold) && PVIN > PVIN_UVDET && Tj < TSD (If entered LP_Off via Transition U or O1. Bypass if entered LP_Off via Transition X2) && {[(VIN < VIN_OVLO) && VIN_OVLO_SDWN = 1] OR [VIN_OVLO_SDWN = 0]} && TRIM_NOK = 0 && OTP_NOK = 0 && VDDOTP < VDDOTP_threshold

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 9. State transition table*...continued*

Transition	Conditions
Transition K Description: Self-test to Power Up sequence (PF5300 ASIL B and ASIL D Only)	Condition 1 (assumes non-debug mode): Pass all self-tests except ABIST (ABIST result don't care) && (OTP_XFAILB_EN = 0)
Transition K Description: Self-test to power-up sequence (PF5300 ASIL B and ASIL D Only)	Condition 2 (assumes non-Debug mode): Pass all self-tests except ABIST (ABIST result don't care) && (OTP_XFAILB_EN = 1 && XFAILB_pin = High)
Transition L Description: IO_Release to INIT	Condition 1: PGOOD internally released and PGOOD_sns = 1 (high)
Transition N Description: RUN/STANDBY/INIT/IO_Release to Power Down (Turn-Off)	Condition 1: PWRON = 0
Transition N Description: RUN/STANDBY/INIT/IO_Release to Power Down (Turn-Off)	Condition 2: PMIC_OFF = 1 && 500us_Shutdown_Timer_Expired
Transition N Description: RUN/STANDBY/INIT/IO_Release to Power Down (Turn-Off)	Condition 3: VIN_OVLO_SDWN = 1 && VIN_OVLO event
Transition N Description: RUN/STANDBYINIT/IO_Release to Power Down (Turn-Off)	Condition 4: XFAILB_pin = 0 (pulled low externally; OTP_XFAILB_EN = 1)
Transition O1 Description: Power Down (Turn-off) to LP_Off	Condition 1: Power Down sequence (including OTP_PD_SEQ_DLY) finished via PMIC_OFF I^2C path (ULP_OFF_CTRL = don't care)
Transition O1 Description: Power Down (Turn-off) to LP_Off	Condition 2: Power Down sequence (including OTP_PD_SEQ_DLY) finished via VIN_OVLO path (ULP_OFF_CTRL = don't care)
Transition O1 Description: Power Down (Turn-off) to LP_Off	Condition 3: Power Down sequence (including OTP_PD_SEQ_DLY) initiated via PWRON = 0 path && ULP_OFF_CTRL = 0
Transition O1 Description: Power Down (Turn-off) to LP_Off	Condition 4: Power Down sequence (including OTP_PD_SEQ_DLY) finished via XFAILB path (ULP_OFF_CTRL = don't care)
Transition O2/O3 Description: Power Down (Turn-off) to ULP_Off	Condition 1: Power Down sequence (including OTP_PD_SEQ_DLY) finished via PWRON = 0 path && ULP_OFF_CTRL = 1 Note: 500 µs delay between O2 and O3 to allow discharge of V1P6A output.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 9. State transition table*...continued*

Transition	Conditions
Transition Q Description: Power Up Sequence to Power Down (Fault)	Condition 1: SW1 failure (OV/UV) during power-up sequence (if OTP_SW1_PGOOD_OV/UV = 1)
Transition Q Description: Power Up Sequence to Power Down (Fault)	Condition 2: PGOOD internally asserted low and PGOOD_sns = 1 (high) for > 10 µs (to detect external stuck-at-high fault)
Transition Q Description: Power Up Sequence to Power Down (Fault)	Condition 3: Register Map CRC Error
Transition R Description: Self-Test to Fail-safe State	Conditions: ST_COUNT = 3 (Self-test fails 3 times)
Transition S Description: Power Down (Fault) to Fail-safe State	Condition 1: Power Down Sequencer (including OTP_PD_SEQ_DLY) is finished
Transition U Description: Fail-safe State to LP_Off	Condition 1: 1. OTP_FS_BYPASS=1 && OTP_FS_BYPASS_CNT=0 && FS_BYPASS_CNT<15
Transition U Description: Fail-safe State to LP_Off	Condition 2: OTP_FS_BYPASS=1 && OTP_FS_BYPASS_CNT=1
Transition V Description: Power Up Sequence to IO_Release	Condition 1: Completion of the power-up sequence according to OTP.
Transition W Description: IO_Release to Power Down (Fault)	Condition 1: FAULT_CNT = FAULT_MAX_CNT
Transition W Description: IO_Release to Power Down (Fault)	Condition 2: PGOOD internally released and PGOOD_sns = 0 (low) until 100 ms timer expires
Transition W Description: IO_Release to Power Down (Fault)	Condition 3: Thermal shutdown Tj > TSD
Transition W Description:IO_Release to Power Down (Fault)	Condition 4: Register Map CRC Error
Transition X1 Description: ULP_Off to LP_Off	Condition 1: PWRON = 1
Transition X2 Description: Fuse Load to LP_OFF	Condition: Fuse Load complete
Transition Z Description: System On to Power Down (Fault)	Condition 1: FAULT_CNT = FAULT_MAX_CNT
Transition Z Description: System On to Power Down (Fault)	Condition 2: Thermal shutdown Tj > TSD
Transition Z Description: System On to Power Down (Fault)	Condition 3: Register Map CRC Error

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

11.1 State descriptions

11.1.1 ULP_Off state

The ULP_Off state is an Ultra-low Power-off mode with very low quiescent current.

When V_{IN} is applied, the device moves to this state and waits for a power-on event. In this state, the internal bias circuits are off to maintain the low Iq requirement, and only the PWRON detection circuits are enabled.

During power down, the ULP_OFF_CTRL bit determines the transition to the ULP_Off state. If power down is because of PWRON going low, if the ULP_OFF_CTRL = 0, the state machine moves to LP_Off directly. If ULP_OFF_CTRL = 1, the state machine transitions to the ULP_Off state, where the internal regulators are off to reduce the supply current consumption.

While powering off into the ULP_Off state results in lower quiescent current, powering off into the LP_Off state results in faster power up.

The initial value of the ULP_OFF_CTRL bit is loaded from the OTP_ULP_OFF_CTRL bit.

11.1.2 Load fuses

During a power up from the ULP_Off state, the fuses (for trim and OTP) are loaded into the mirror registers and the functional I^2C registers.

The fuse circuits have a CRC error check routine, which reports and protects against register loading errors on the mirror registers. If a register loading error is detected, the corresponding TRIM_NOK or OTP_NOK flag is set and the device does not power up further.

11.1.3 LP_Off state

The LP_Off state is a Low Power-off mode with current consumption higher than the ULP_Off mode. All the internal circuits are ON in this state, and the device transitions to the power-up sequence state depending on the PWRON pin status.

During this state, if PWRON goes high, the device moves to start the power-up sequence as defined in the OTP settings. See Section 15.1 for details on Debug entry while in LP_Off.

When ULP_OFF_CTRL = 0, the device enters the LP_Off state from IO_Release, INIT, or System ON states when turned off.

11.1.4 Self-test routine (PF5300 ASIL B and ASIL D only)

When the device transitions from the LP_Off state, it moves into the self-test routine and performs tests to verify the integrity of the internal circuits.

During the self-test routine, the following blocks are verified:

1. The high-speed clock circuit operates within a maximum 15 % tolerance.
2. The outputs of both the voltage generation band gap and the monitoring band gap are not more than 120 mV apart from each other.
3. A CRC is performed on the OTP mirror registers to ensure the integrity of the registers before powering up.
4. ABIST of SW1 OV and UV monitors

The self-test routine takes about eleven 100 kHz clock cycles (approximately 110 µs).

To allow for varying settling times for the internal band gap and clocks, the self-test block is executed up to three times (with 2.0 ms between each test) in case of a failure. If a failure is encountered, the state machine

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

proceeds to the fail-safe state. Failure of 1, 2, or 3 above is considered a self-test failure. Failure of ABIST is not considered a self-test failure.

11.1.4.1 ABIST test on all voltage monitors

The SW1 OV and UV monitors are checked for functional operation during the self-test routine. This check of the voltage monitors is referred to as ABIST in this document. A failure in the ABIST test is not interpreted as a self-test failure; it only sets the corresponding ABIST flag for system information. The processor is responsible for reading the information and deciding whether it can continue with a safe operation.

Upon a successful self-test, the state machine proceeds to the power-up sequence state.

11.1.5 Power-up sequence

During the power-up sequence, the PF5300 starts up per OTP programmed power-up sequence/timing.

If SW1 has an OV or UV fault at the end of the power-up sequence (if OTP_PGOOD_SW1_OV or OTP_PGOOD_SW1_UV = 1), the PF5300 waits for up to 2 ms to allow the output voltage to settle and continue the boot up after OV and/or UV pass. If OV/UV persists after 2 ms, it is considered a power-up failure. After a power-up failure, the state machine proceeds to the Fail-safe state via Transition Q and increments the fault counter.

During the power-up sequence, PGOOD is checked for a stuck at high fault (internally asserted low, but externally high) and Transition Q is taken if PGOOD is stuck high for more than 10 µs. See Table 9 for full conditions. The PGOOD pin is checked for stuck-at faults continuously. See Section 12.7.3 for details.

The PGOOD pin can also be programmed, as part of the power-up sequence, to allow controls of its release timing. See Section 12.3.2 for details.

When PGOOD is internally released high, but externally pulled low, the FAULT_CNT[3:0] is incremented. If it is expected that the PGOOD is externally asserted low while the PF5300 may have released it, set OTP_FAULT_MAX_CNT[2:0] to > 3b'000. This is to ensure that FAULT_CNT does not reach its maximum limit because of a systematic event.

11.1.6 IO_Release state

If the Power Up state is successfully completed, the state machine transitions to the IO_Release state. PGOOD_sns = 1 is a condition to exit the IO_Release state. A 100 ms timer becomes active in the IO_Release state if PGOOD is internally released. This timer is to check whether the PGOOD pin is shorted to ground (internally released, but externally low). If a short to GND is detected for more than 100 ms, device fault shutdown is initiated. The 100 ms timer is disabled in Debug mode. Figure 6 and Figure 7 show some examples of the IO_Release behavior.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

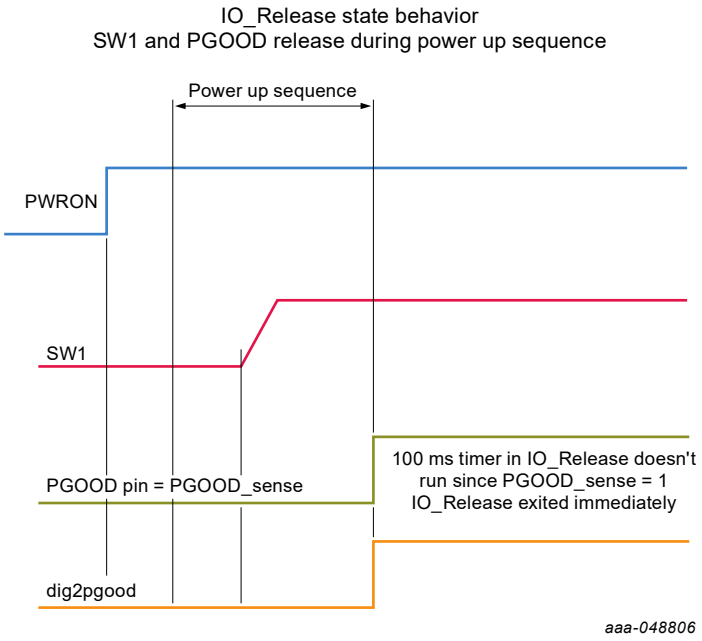


Figure 6. IO_Release state behavior - SW1 and PGOOD release during power-up sequence

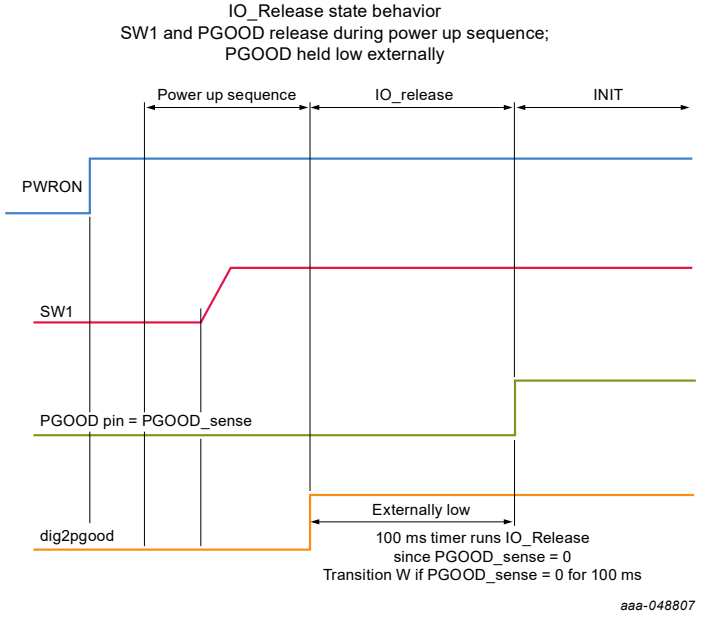


Figure 7. IO_Release state behavior - SW1 and PGOOD release during power-up sequence - PGOOD held low externally

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

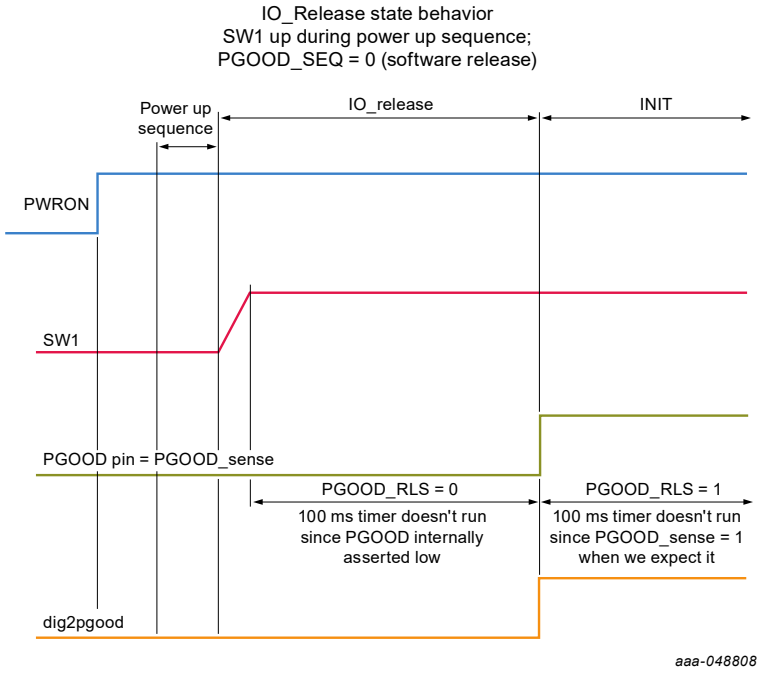


Figure 8. IO_Release state behavior - SW1 up during power-up sequence - PGOOD_SEQ = 0 (software release)

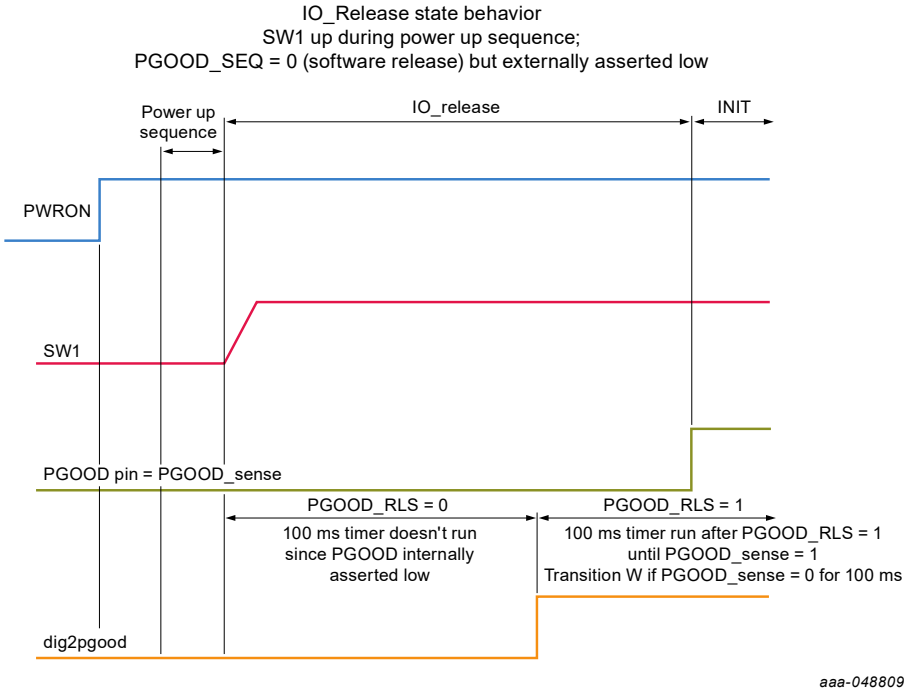


Figure 9. IO_Release state behavior - SW1 up during power-up sequence; PGOOD_SEQ = 0 (software release) but externally asserted low

11.1.7 INIT state

If the Power Up state is completed and PGOOD is released, the state machine transitions to the INIT state. In this state, the processor is expected to boot up and set up specific registers of the PMIC.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

The INIT window must be closed within 2 seconds of entering the INIT state with a good watchdog refresh. Expiration of this timer (absence of good watchdog refresh) is considered to be a watchdog event and the state machine will transition to the IO_Release state, assert PGOOD, and increment the fault counter.

If the watchdog is disabled, the INIT state is bypassed automatically without waiting for a refresh.

Upon state transition, the state machine exits into the System ON state.

11.1.8 System ON state

The System ON state is a virtual state composed of two modes of operations: the RUN state and the STANDBY state.

RUN state

In this state, regulator-specific registers to control SW1's output voltage, operation mode and/or enable/disable state can be modified.

By default, the SW1_VOLT[7:0] registers are loaded with the data stored in the OTP_SW1_VOLT[7:0] register. In the RUN state, SW1 regulates to the voltage set by SW1_VOLT[7:0] register. The user can change the SW1 voltage dynamically by changing the SW1_VOLT[7:0] register value.

STANDBY state

SW1 regulates the voltage set by SW1_STBY_VOLT[7:0] register. If the STANDBY/SYNCIN pin is configured as STANDBY pin by setting OTP_SYNCIN_EN = 0, the STANDBY pin can be toggled to change SW1's regulation voltage. This presents a way to dynamically change SW1's voltage that is faster than using I^2C to change SW1_VOLT[7:0] while in the RUN state.

OTP_SW1_DVS_MAX[7:0] and OTP_SW1_DVS_MIN[7:0] set the maximum and minimum values of the SW1_VOLT[7:0] and SW1_STBY_VOLT[7:0] registers that are accepted. This is useful to prevent unintended values at the regulator output that may potentially cause harm. If the user attempts to write a value to SW1_VOLT[7:0] or SW1_STBY_VOLT[7:0] beyond the OTP_SW1_DVS_MAX[7:0] and OTP_SW1_DVS_MIN[7:0] values, the PF5300 rejects the write attempt, and the DVS_ERR_I flag is set.

Once a STANDBY exit or entry event is recognized and initiated, the STANDBY pin is masked until the transition is complete. OTP_STBY_DLY[5:0] bits can be used to add a delay at the start of the transition when entering or exiting the STANDBY state. The delay value is (OTP_STBY_DELAY[5:0] * SEQ_TBASE[1:0]). If OTP_STBY_DELAY[5:0] = 0x00, no delay is added.

11.1.9 Power-down state

During the Power-down state, SW1 is disabled and PGOOD is asserted low per the configured power-down sequence. The power-down sequence is programmable as defined in Section 12.4.2.

Two types of events may lead to the power-down sequence:

1. Non-faulty turn-off events: Depending on the ULP_OFF_CTRL bit, move directly into LP_Off state or ULP_OFF state as soon as the power-down sequence is finalized.
2. Turn-off events because of a PMIC fault: move to the Fail-safe transition as soon as the power-down sequence is finalized.

11.1.10 Fail-safe state

The Fail-safe state is a fault state where the PMIC turns off the regulator and either remains in the Fail-safe state or can be programmed to restart the power-up sequence. The transition to this state is because of any of the following PMIC faults being TRUE:

1. Power-up fault (PU_FAIL)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

2. PGOOD sense fault (PG_FAIL)
3. PGOOD short to high
4. FAULT_CNT = FAULT_MAX_CNT (REG_FAIL)
5. Junction temperature > the thermal shutdown threshold (TSD_FAIL)
6. Register CRC error

The Fail-safe state provides the following status bits:

- PU_FAIL will be set to 1 when the state machine powered down because of a power-up failure.
- PG_FAIL will be set to 1 when the state machine powered down because of PGOOD failure.
- REG_FAIL will be set to 1 when the state machine powered down because of a regulator failure (fault counter maxed out).
- TSD_FAIL will be set to 1 when the state machine powered down because of a thermal shutdown.

The xxx_FAIL bits will be reset to 0 when V_{IN} crosses the UVDET threshold. The processor can read the FAIL bits during the System ON states (RUN and STANDBY) or the INIT state, in order to obtain information about the previous failure, provided the state machine is able to power up successfully after such failure. The processor should clear the FAIL bits by writing a 1 to them during the System ON states (RUN and STANDBY) and INIT state, provided the state machine is able to power up successfully after such failure.

The Fail-safe state works as a safety transition during a fault or as a lock-down upon a critical device/system failure. Upon entering the Fail-safe state, the OTP_FS_BYPASS bit configures whether the state machine will be able to exit the state back in to the System ON states through LP_Off, or stay in the Fail-safe state. When the OTP_FS_BYPASS bit = 0, the fail-safe bypass feature is disabled, and the state machine will remain in the Fail-safe state indefinitely until a power cycle takes place. When the OTP_FS_BYPASS bit = 1, the fail-safe bypass feature is enabled, and the state machine will be allowed to transition from the Fail-safe state to the LP_Off state, depending on the OTP_FS_BYPASS_CNT bit. The state machine will provide a fail-safe bypass counter configured by OTP_FS_BYPASS_CNT bit to count the number of bypass transitions. The fail-safe bypass counter is incremented every time the transition from the Fail-safe state to the LP_Off state happens.

When OTP_FS_BYPASS_CNT bit = 0, the number of transitions allowed will be configured to 15. When OTP_FS_BYPASS_CNT bit = 1, the number of transitions allowed will be infinite. When OTP_FS_BYPASS_CNT bit = 0, and if the fail-safe bypass counter reaches the maximum count value of 15, the state machine will stay in the Fail-safe state.

In the Fail-safe state, the SW_1 regulator will be disabled.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

12 General device operation

12.1 UVDET

V_{IN} and PVIN need to be above their respective UVDET thresholds for powering up the PF5300. V_{IN} falling below the $V_{IN_UVDET_F}$ threshold causes the PF5300 to shut down immediately (no power down sequence) whereas PVIN falling below $P_{VIN_UVDET_F}$ does not cause a shutdown.

All parameters are specified at Ta = -40 °C to 125 °C, PVIN = V_{IN} = 3.3 V, PWRON = 1.8 V, no load on regulator, Fsw = 2.2 MHz, typical external component values, unless otherwise noted. Typical values are specified at 25 °C, unless otherwise noted.

Table 10. UVDET thresholds

Symbol	Parameter	Min	Typ	Max	Unit
VIN_UVDET_R	Rising V_{IN} UVDET	2.85	3.00	3.15	V
VIN_UVDET_F	Falling V_{IN} UVDET	2.80	2.90	3.00	V
PVIN_UVDET_R	Rising PVIN UVDET	2.6	2.75	2.9	V
PVIN_UVDET_F	Falling PVIN UVDET	2.5	2.6	2.7	V

12.2 VIN OVLO condition

The VIN_OVLO circuit monitors the VIN pin for an overvoltage. VIN_OVLO_EN = 1 enables this monitoring.

PF5300 can be programmed to react to an overvoltage in two ways:

- When the VIN_OVLO_SDWN = 0, the VIN_OVLO event triggers an VIN_OVLO_I interrupt, but does not turn off the device
- When the VIN_OVLO_SDWN = 1, the VIN_OVLO event initiates a power-down sequence

The default configuration of the VIN_OVLO_EN bit is set by the OTP_VIN_OVLO_EN bit in OTP. Likewise, the default value of the VIN_OVLO_SDWN bit is set by the OTP_VIN_OVLO_SDWN upon power up.

Debounce on the VIN_OVLO comparator is programmable to 10 µs, 100 µs, or 1.0 ms, by the VIN_OVLO_DBNC[1:0] bits. The default value for the VIN_OVLO debounce is set by the OTP_VIN_OVLO_DBNC[1:0] bits upon power up.

All parameters are specified at Ta = -40 °C to 125 °C, PVIN = V_{IN} = 3.3 V, PWRON = 1.8 V, no load on regulator, Fsw = 2.2 MHz, typical external component values, unless otherwise noted. Typical values are specified at 25 °C, unless otherwise noted.

Table 11. VIN_OVLO debounce configuration

VIN_OVLO_DBNC[1:0]	V_{IN} OVLO debounce value (µs)
00	10
01	100
10	1000
11	Reserved

All parameters are specified at Ta = -40 °C to 125 °C, PVIN = V_{IN} = 3.3 V, PWRON = 1.8 V, no load on regulator, Fsw = 2.2 MHz, typical external component values, unless otherwise noted. Typical values are specified at 25 °C, unless otherwise noted.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 12. VIN_OVLO specifications

Symbol	Parameter	Min	Typ	Max	Unit
VIN_OVLO	V_{IN} overvoltage lockout rising[1]	5.6	5.8	6.0	V
VIN_OVLO_HYS	V_{IN} overvoltage lockout hysteresis[1]	100	120	140	mV

[1] Operating the device above the maximum V_{IN} = 5.5 V for an extended period of time may degrade and cause permanent damage to the device.

12.3 Power up

12.3.1 Power-up events

Upon a power cycle (VIN_UVDET_R), the device moves to the ULP_Off state by default. PWRON = 1 is a necessary condition for further power up to load fuses and to enter the LP_Off state. From LP_Off, the PF5300 proceeds to Power-up based on the conditions listed in Table 9.

12.3.2 Power-up sequencing

Although it has only one regulator, the PF5300 uses a power-up sequencer similar to other PF PMICs from NXP. This is useful in a multi-PMIC system where the user is trying to control power-up timing across different devices.

The power-up sequencer controls the time and order in which PGOOD and SW1 are enabled when going from the LP_Off to the RUN state.

The OTP_SEQ_TBASE[1:0] bits set the default timebase for the power-up and power-down sequencer.

The SEQ_TBASE[1:0] bits can be modified via I^2C during the IO_Release, INIT, and System ON states (RUN and STANDBY) in order to change the sequencer timing during RUN/STANDBY transitions, as well as the power-down sequence.

Table 13. Power-up timebase register

OTP bits OTP_SEQ_TBASE[1:0]	Functional bits SEQ_TBASE[1:0]	Sequencer timebase (µs)
00	00	100
01	01	250
10	10	500
11	11	1000

The DC-DC powers up based on the OTP_SW1_SEQ[5:0] setting. PGOOD is released high based on the OTP_PGOOD_SEQ[5:0] setting (in combination with passing PGOOD conditions as applicable). Sequence code 0x00 indicates that SW1/PGOOD are not part of the startup sequence and remain off. This is useful when the PF5300 is expected to power up via full software control. SW1_MODE[1:0] and PGOOD_RLS bits can be used to enable and release PGOOD, respectively. If SW1_SEQ[5:0] is 0x00 (off) and a power-on event is present, the device waits in the IO_Release state for software instructions to turn on SW1 and release PGOOD.

Note: *There is no TBASE time prior to SLOT0. SLOT0 occurs immediately upon entering a power-up sequence. There is a TBASE time between SLOT0 and SLOT1, and so on.*

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 14. Power-up sequence registers

OTP bits OTP_SW1_SEQ[5:0]/ OTP_PGOOD_SEQ[5:0]	Functional bits SW1_SEQ[5:0]/ PGOOD_SEQ[5:0]	Sequence slot	Startup time (µs)
000000	000000	Off	Off
000001	000001	0	SLOT0 (right after PWRON event is valid)
000010	000010	1	SEQ_TBASE x SLOT1
. . .	. . .	. . .	. . .
111111	111111	62	SEQ_TBASE x SLOT62

If OTP_PGOOD_SEQ[5:0] = 0x00, the default value of the PGOOD_RLS = 0. The processor can decide to release this bit after turning on any one or all of the regulators.

When the processor sets PGOOD_RLS = 1, then the device will release PGOOD after verifying all the signals assigned to the PGOOD monitor block.

12.4 Power down

12.4.1 Turn-off events

Turn-off events may be requested by the processor (non-PMIC Fault related) or because of a critical failure of the PMIC (Hard Fault condition).

Non-PF5300 failure turn-off events:

1. Hardware turn off: PWRON pin is pulled low
2. Software turn off:
   - When bit PMIC_OFF bit is set to 1, the 500 µs shutdown timer is started and the SDWN_I bit is set
   - If the 500 µs timer expires, the state machine starts a turn off event.
   - If the SDWN_I bit is cleared before the 500 µs shutdown timer is expired, the shutdown request is cleared and the shutdown event is canceled. The PMIC_OFF bit self-clears if the SDWN_I flag is cleared.
3. XFAILB event
4. VIN goes below VIN_UVDET_F (no power down sequence)

For fault conditions resulting in a turn off, see Table 9. The device shuts down immediately (no power-down sequence) when Tj crosses the thermal shutdown threshold rising.

After a power-down sequence is started, the PWRON pin is masked until the sequence is finished and transition to the Off/Fail-safe states is completed.

12.4.2 Power-down sequencing

A post power-down delay can be programmed on OTP with the OTP_PD_SEQ_DLY[2:0] bits to delay entering the Off mode after completion of Power Down. This is useful when synchronizing power-down of multiple devices in the system, or to allow sufficient time for output capacitors to discharge.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 15. OTP_PD_SEQ_DLY[2:0] configuration

OTP_PD_SEQ_DLY[2:0]	Post power-down delay (ms)
0b000	0
0b001	1
0b010	10
0b011	50
0b100	100
0b101	250
0b110	500
0b111	1000

A delay determined by the OTP_TURN_OFF_DELAY[5:0] bits can be executed before turning off SW1 and PGOOD assertion (low). The delay value is (OTP_TURN_OFF_DELAY[5:0] * OTP_SEQ_TBASE[1:0]).

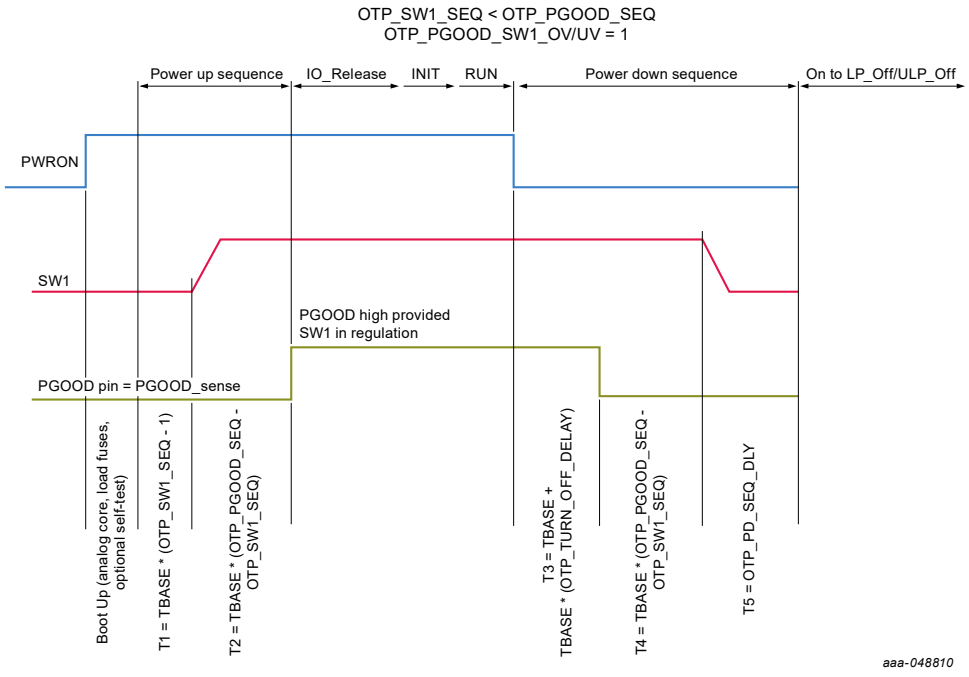


Figure 10. SW1/PGOOD sequence example 1

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

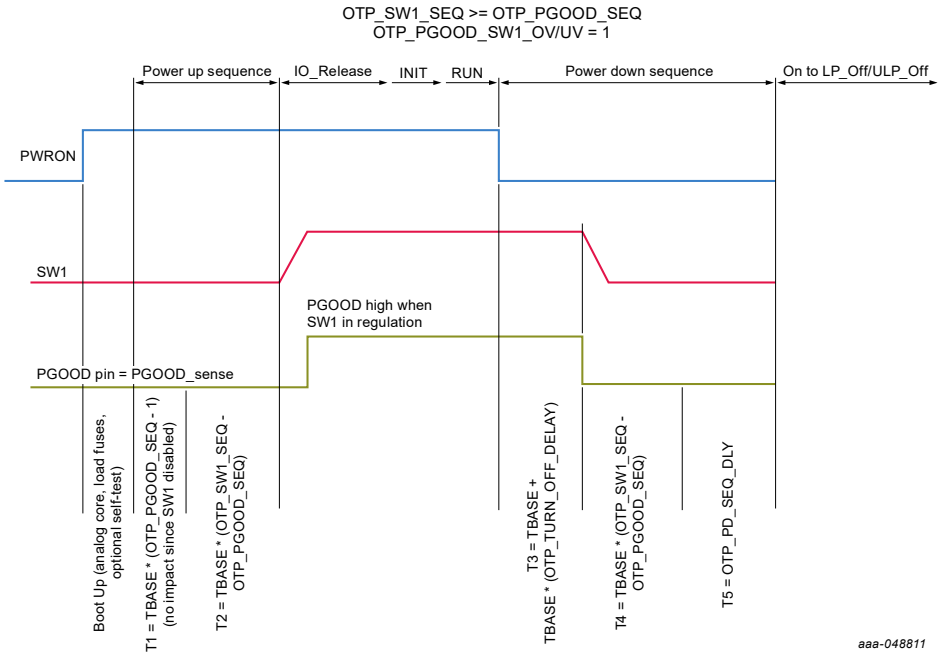


Figure 11. SW1/PGOOD sequence example 2

12.5 Fault management

Three types of faults are monitored per regulator: UV, OV, and ILIM. Faults are monitored during the power-up sequence (after soft-start complete), IO_Release, INIT, and System ON state (RUN and STANDBY) states.

OV/UV faults are debounced for a programmable filter time before they are detected as a fault condition.

ILIM faults are debounced for 40 µs before they can be detected as a fault condition.

A global fault counter is provided in FAULT_CNT [3:0] bits. The decimal value stored in FAULT_CNT[3:0] represents the value of the fault counter. The FAULT_CNT[3:0] can be programmed to increment for different types of faults, with the state machine taking action if the counter value exceeds a maximum value programmed using the OTP_FAULT_MAX_CNT[2:0] bits.

If the FAULT_MAX_CNT[2:0] is changed during System ON states, the FAULT_CNT[3:0] is reset to 0x00.

For each type of fault on SW1, an option is available to increment the FAULT_CNT[3:0] value.

SW1_ILIM_BYPASS (initial value from OTP_SW1_ILIM_BYPASS), SW1_OV_BYPASS (initial value from OTP_SW1_OV_BYPASS), or SW1_UV_BYPASS (initial value from OTP_SW1_UV_BYPASS) control whether the FAULT_CNT[3:0] is incremented (0) or bypassed (1) for a current limit, an overvoltage, or an undervoltage fault, respectively.

Table 16. Fault counter limit configuration

OTP bits OTP_FAULT_MAX_CNT [2:0]	Functional bits FAULT_MAX_CNT [2:0]	Value
000	000	1
001	001	2
010	010	4
011	011	6
100	100	8

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 16. Fault counter limit configuration*...continued*

OTP bits OTP_FAULT_MAX_CNT [2:0]	Functional bits FAULT_MAX_CNT [2:0]	Value
101	101	10
110	110	12
111	111	15

If the FAULT_CNT[3:0] = FAULT_MAX_CNT[2:0], the PF5300 powers down into the Fail-safe state. See Table 9 for details. For ASIL B and ASIL D devices, the FAULT_CNT[3:0] bits can be decremented by doing a good watchdog refresh via an I^2C command. The FAULT_CNT[3:0] can also be cleared by setting the FLT_CNT_CLR bit.

The FAULT_CNT[3:0] is reset to 0 when the state machine enters the LP_off state. Once regulators are turned off after a FAULT_CNT[3:0] is maxed out, the device moves to the LP_off transition if FS_BYPASS = 1.

Note: *Fault count could be incremented more than once for the same type of fault (regx OV, UV) if the fault persists after the voltage setpoint changes. This could be either a voltage change in the same state or voltage change during a state change between RUN and STANDBY.*

Even if a specific fault is bypassed, the corresponding interrupt bit is still set.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 17. Fault types and the corresponding PGOOD pin responses

Safety mechanism	Monitored state	Error flag	Fault counter	WD_ERROR_CNT	PGOOD low assertion	FSM state transition from INIT and System ON	Comments
SW1 UV	Power Up Sequence, IO_Release, INIT, and System ON states	VMON_UV_I	+1 if SW1_UV_BYPASS bit = 0	—	Yes, if OTP_PGOOD_SW1_UV = 1	IO_Release	Fault shutdown from power-up sequence
SW1 OV		VMON_OV_I	+1 if SW1_OV_BYPASS bit = 0	—	Yes, if OTP_PGOOD_SW1_OV = 1	IO_Release	Fault shutdown from power-up sequence
PGOOD short to high		PGOOD_STUCK_AT_1	+1	—	—	—	Fault shutdown from power-up sequence and IO_Release; No transition from INIT and System ON
BG1 and BG2 Drift apart		BG_ERR_I	—	—	Yes, if OTP_PGOOD_BG = 1	IO_Release	Self-test fail
Reg map CRC error (OTP and functional bits)		REGMAP_CRC_I	—	—	Yes[1]	—	Fault shutdown
CLOCK stuck monitoring		—	Cleared	—	Yes	—	FSM reset/ shutdown
Bad watchdog refresh	INIT, System ON states	—	—	+2 if WD_EN = 1	—	—	—

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 17. Fault types and the corresponding PGOOD pin responses*...continued*

Safety mechanism	Monitored state	Error flag	Fault counter	WD_ ERROR_CNT	PGOOD low assertion	FSM state transition from INIT and System ON	Comments
Watchdog event	INIT, System ON states	—	+1 if WD_EN = 1	—	Yes, if WD_EN = 1	IO_Release	Fault shutdown if FAULT_CNT ≥ FAULT_ MAX_CNT
VIN_OV (OVLO monitor)	IO_Release, INIT, and System ON states	VIN_OVLO_I	+1	—	Yes, if VIN_ OVLO_ SDWN = 1[2]	—	Power down
ABIST OV/ UV error (Startup and AB_RUN)	Self-test state, IO_ Release, INIT, and System ON states	AB_SW1_OV, AB_SW1_UV	—	—	—	—	—
VIN pin disconnection	INIT, IO_ Release, System ON states	—	Cleared	—	Yes (analog safety path)	—	FSM reset/ shutdown
OTP / TRIM corrupted	Self-test state	OTP_NOK TRIM_NOK	—	—	Yes [2]	—	—
BG1 and BG2 drift apart	Self-test state	BG_ERR_I	—	—	Yes[2]	—	—
CLK drift error 20 MHz and 100 kHz	Self-test state	OSC_ERR	—	—	Yes [2]	—	—
CLOCK sync error	INIT, System ON states	FSYNC_FLT_ I	—	—	—	—	Switch to internal CLK

[1] Power-down/shutdown event. PGOOD doesn't get asserted low immediately upon fault. PGOOD assertion will be handled by the state machine and the sequencer.

[2] Startup fault. PGOOD is asserted by default as device doesn't progress to Power-up state. Not valid during Debug mode.

12.6 Interrupt management

The processor is notified of any interrupt through various interrupt registers. There is no explicit INTB pin in the PF5300.

The interrupt registers are composed of two types of bits to help manage all the interrupt requests in the PF5300:

- The interrupt latch XXXX_I: This bit is set when the corresponding interrupt event occurs. It can be read at any time, and is cleared by writing a 1 to the bit.
- The sense bit XXXX_S: If available, the sense bit provides the actual status of the signal triggering the interrupt.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 18. Interrupt Registers

Register name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
INT STATUS1	SDWN_I	BG_ERR_I	CRC_I	SW1_DVS_ DONE	SW1_ILIM_I	VMON_UV_ I	VMON_ OV_I	VIN_ OVLO_I
INT_ SENSE1	—	BG_ERR_S	—	—	SW1_ILIM_ S	VMON_UV_ S	VMON_ OV_S	VIN_ OVLO_S
INT STATUS2	PGOOD_ STUCK_ AT_0	PGOOD_ STUCK_ AT_1	DVS_ ERR_I	FSYNC_I	THERM_ 155_I	THERM_ 140_I	THERM_ 125_I	THERM_ 110_I
INT_ SENSE2	—	PGOOD_S	—	FSYNC_S	THERM_ 155_S	THERM_ 140_S	THERM_ 125_S	THERM_ 110_S

12.7 I/O interface pins

The PF5300 is fully programmable via the I^2C interface. Additional communication between the processor, PF5300, and other companion PMICs is provided by direct logic interfacing, including PGOOD, among other pins.

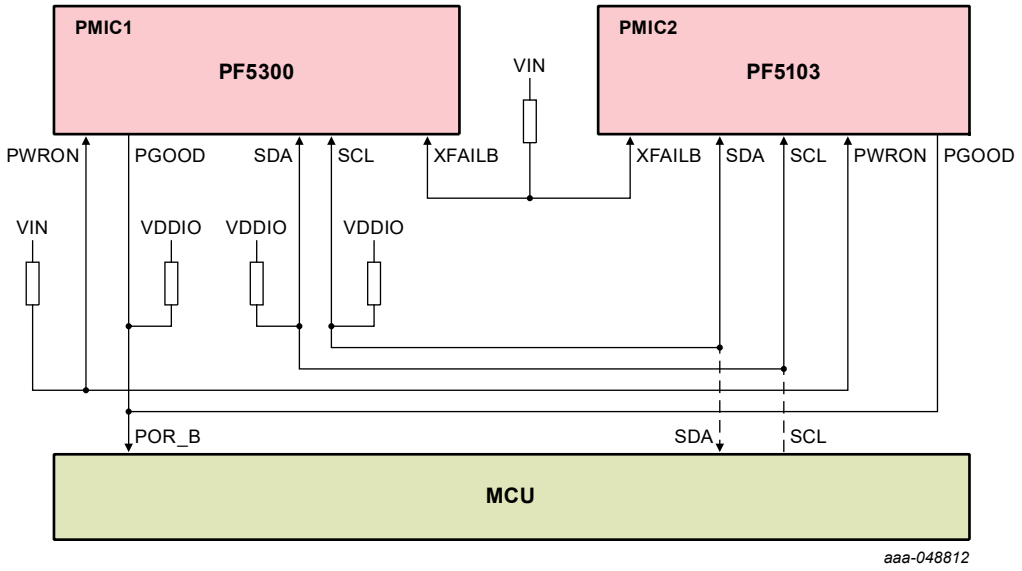


Figure 12. Multi-PMIC interface diagram

All parameters are specified at Ta = -40 °C to 125 °C, PVIN = V_{IN} = 3.3 V, PWRON = 1.8 V, no load on regulator, Fsw = 2.2 MHz, typical external component values, unless otherwise noted. Typical values are specified at 25 °C, unless otherwise noted.

Table 19. I/O Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
PWRON_V_{IL}	PWRON low input voltage	—	—	0.4	V
PWRON_V_{IH}	PWRON high input voltage	1.4	—	5.5	V
STANDBY/SYNCIN_ V_{IL}	STANDBY low input voltage	—	—	0.4	V
STANDBY/SYNCIN _V_{IH}	STANDBY high input voltage	1.4	—	5.5	V

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 19. I/O Electrical Characteristics*...continued*

Symbol	Parameter	Min	Typ	Max	Unit
PGOOD_V_{OL}	PGOOD low output voltage −2.0 mA load current	0	—	0.4	V
XFAILB_V_{IL}	XFAILB low input voltage	0	—	0.4	V
XFAILB_V_{IH}	XFAILB high input voltage	1.4	—	5.5	V
XFAILB_V_{OH}	XFAILB high output voltage Pulled-up to V_{IN}	V_{IN} − 0.5	—	—	V
XFAILB_V_{OL}	XFAILB low output voltage −2.0 mA load current	0	—	0.4	V
SCL_V_{IL}	SCL low input voltage	0	—	0.4	V
SCL_V_{IH}	SCL high input voltage	1.4	—	5.5	V
SDA_V_{IL}	SDA low input voltage	0	—	0.4	V
SDA_V_{IH}	SDA high input voltage	1.4	—	5.5	V
SDA_V_{OH}	SDA high output voltage	1.4	—	5.5	V
SDA_V_{OL}	SDA low output voltage −20 mA load current	0	—	0.4	V

12.7.1 PWRON

PWRON is an input signal to the IC that acts as a power-up event signal in the PF5300.

The PWRON pin operates in Level-sensitive mode. In this mode, the device is in one of the off modes when the PWRON pin is pulled low. Pulling the PWRON pin high is a necessary condition to generate a power-on event. The PWRON pin has a 10 µs debounce timer on the falling edge.

PWRON may be pulled up to V_{IN} with an external 10 kΩ resistor if the device is intended to come up automatically with application of V_{IN}.

12.7.2 STANDBY/SYNCIN

The STANDBY/SYNCIN pin has dual functions. It is used either as the clock synchronization input (SYNCIN) or STANDBY state selection (STANDBY). The STANDBY function can be enabled when the SYNC function is disabled (OTP_SYNCIN_EN = 0). If not used as SYNC, this pin can be selected in OTP to be used as the STANDBY input (OTP_SYNCIN_EN = 1).

Table 20. STANDBY/Syncin Configuration

OTP_SYNCIN_EN	Description
0	STANDBY/SYNCIN pin configured as STANDBY
1	STANDBY/SYNCIN pin configured as Syncin

STANDBY can be configured as active high or active low using the STANDBYINV bit, with default value set by the OTP_STANDBYINV bit.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 21. STANDBY pin polarity control

STANDBY (pin)	STANDBYINV (I^2C bit)	STANDBY control
0	0	Not in STANDBY state
0	1	In STANDBY state
1	0	In STANDBY state
1	1	Not in STANDBY state

12.7.3 PGOOD

PGOOD is an open-drain output used as a PGOOD indicator pin. PGOOD can be assigned a slot in the power-up sequence (to behave like a GPO), or it can be released after SW1 is on and in regulation. PGOOD should be pulled up to 1.8 V, 3.3 V, or V_{IN} with a pullup resistor.

The PGOOD pin is driven low or asserted when the PF5300 is out of the RUN state and enters the Fail-safe state. The PGOOD pin is asserted low in the Fail-safe, ULP_Off, and LP_Off states.

When V_{IN} is applied, the PGOOD pin is driven low as soon as the logic is able to control, to ensure no floating condition is present on the load being controlled by this pin. PGOOD is also asserted low through an analog path if PVIN is present, but VIN is not.

When OTP_PGOOD_SW1_OV = 1, PGOOD is asserted low if an overvoltage is detected by the voltage monitor monitoring SW1. When OTP_PGOOD_SW1_UV = 1, PGOOD is asserted low if an undervoltage is detected by the voltage monitor monitoring SW1. See Section 13.2 for thresholds and debounce values. The PGOOD pin is asserted low for at least 1 ms when being asserted low for a fault. For example, even if the fault is cleared immediately upon PGOOD assertion (low), PGOOD remains asserted low for 1 ms from there on.

The PGOOD pin is continually monitored digitally to detect "stuck-at" faults, by comparing the internal command to the output in real time. During the self-test routine, the PGOOD pin is checked to ensure it is not stuck high. If a PGOOD stuck at fault is detected, the state machine increments the fault counter FAULT_CNT.

PGOOD_STUCK_AT_1 = 1 indicates that PGOOD pin is stuck at 1 (internally asserted low, but externally measures high).

PGOOD_STUCK_AT_0 = 1 indicates that PGOOD pin is stuck at 0 (internally released high, but externally measures low).

PGOOD_S bit can be used to read the real-time status of the pin.

When PGOOD is ready to be released at the IO_Release state, but PGOOD_S = 0 for more than 100 ms (PGOOD stuck at 0 fault), the device initiates a power-down sequence and transition to the Fail-safe state. See the States and State machine for transition conditions.

To improve latent failure metric of the PF53, two instances of the PGOOD pin monitors operate in parallel. The outputs from the two monitors are ANDed and the resulting output is used for decisions. The two instances have a difference in the thresholds to add "diversity" in the safety path.

All parameters are specified at Ta = -40 °C to 125 °C, PVIN = V_{IN} = 3.3 V, PWRON = 1.8 V, no load on regulator, Fsw = 2.2 MHz, typical external component values, unless otherwise noted. Typical values are specified at 25 °C, unless otherwise noted.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 22. PGOOD monitoring electrical parameters

Parameter	Symbol	Min	Typ	Max	Unit
PGOOD Monitor1 VIH	PGOOD_Mon1_VIH	0.6	0.95	1.2	V
PGOOD Monitor1 VIL	PGOOD_mon1_VIL	0.4		0.65	V
PGOOD Monitor1 hysteresis	PGOOD_Mon1_hyst	150	370	600	mV
PGOOD Monitor2 VIH	PGOOD_Mon2_VIH	0.6	0.95	1.2	V
PGOOD Monitor2 VIL	PGOOD_mon2_VIL	0.45		0.7	V
PGOOD Monitor2 hysteresis	PGOOD_Mon2_hyst	100	350	550	mV
PGOOD Monitor debounce filter time	PGOOD_Mon_db	20	30	40	µs

12.7.4 XFAILB

XFAILB is a bidirectional pin with an open-drain output used to synchronize the power-up and power-down sequences of two or more PMICs. The XFAILB pin is available on several NXP PMICs, such as PF8100, PF7100, and PF5020, among others. By connecting the XFAILB pin of these devices together in the system, power up and power down of the devices (during normal operation, as well as fault situations) can be synchronized.

OTP_XFAILB_EN = 1 enables the XFAILB functionality in the VDDOTP/XFAILB pin. When OTP_XFAILB_EN = 0, the XFAILB feature is disabled. References to XFAILB in the document assume that OTP_XFAILB_EN = 1.

During LP_OFF mode, the XFAILB pin is asserted low internally, unless LP_OFF is entered in debug mode. See Section 15.1 for details.

The XFAILB pin is released just before the Power-up sequence state. The power-up sequence starts only when the XFAILB pin is released by all PMICs connecting to the bus (that is, XFAILB is pulled high). This ensures that all the PMICs start their respective power-up sequences at the same time, allowing the user to program the power-up sequence across multiple devices. See Table 9 for transition conditions involving XFAILB.

When the PF5300 has a turn-off event generated by transitions Q, W, Z, and H in the state machine, the PF5300 asserts XFAILB pin low, and 20 µs after asserting it low, the state machine progresses to Power down (Fault).

In IO_Release, INIT, RUN, and STANDBY states, if the XFAILB pin is externally pulled low, the PF53 detects an XFAILB event as soon as the pin is synchronized. When an external XFAILB event is detected, the XFAILB pin is asserted low internally, and the device starts a power-down sequence. See Table 9 conditions.

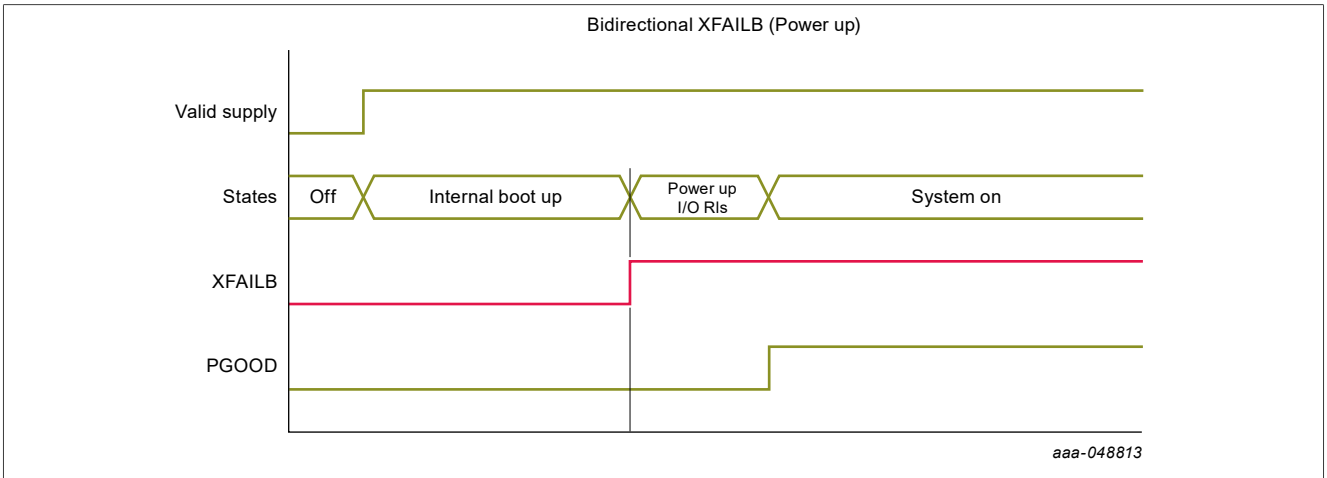


Figure 13. XFAILB during power up

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

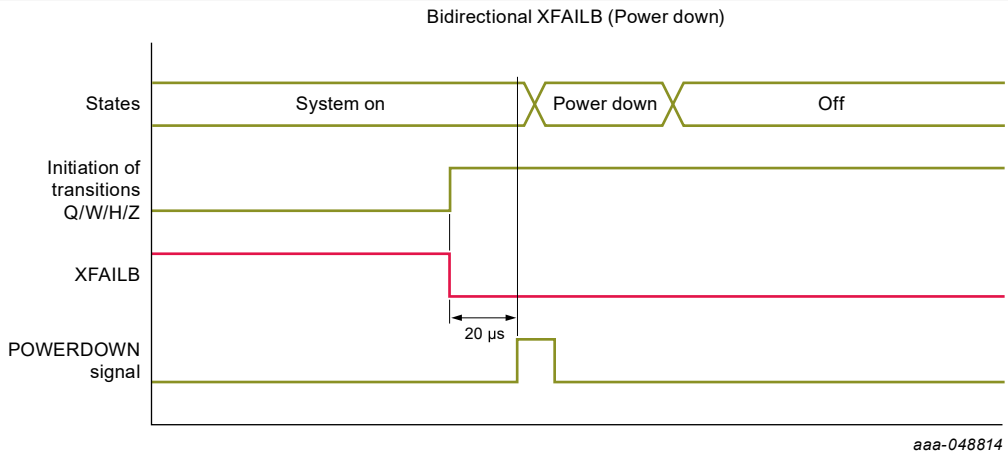


Figure 14. XFAILB during power down

12.7.5 SDA and SCL (I²C bus)

Communication with the PF5300 is done through I^2C, which supports High-speed Operation mode with up to 3.4 MHz operation. SDA and SCL are pulled up externally to 1.8 V or 3.3 V with 1.5 k Ω resistors to support operation up to the fast mode.

To use the High-speed Operation mode, a suitable pullup resistor must be used in the range of 500 Ω to 1 kΩ.

The PF5300 is designed to operate as a companion device during I^2C communication. The default I^2C device address is set by the OTP_I2C_ADD[2:0].

Table 23. I^2C address configuration

OTP_I2C_ADD[2:0]	Device address
000	0x28
001	0x29
010	0x2A
011	0x2B
100	0x2C
101	0x2D
110	0x2E
111	0x2F

Refer to UM10204 on nxp.com for detailed information on the digital I^2C communication protocol implementation.

During an I^2C transaction, the communication will latch after the eighth bit sent. If the data sent is not a multiple of 8 bits, any word with less than 8 bits is ignored. If only 7 bits are sent, no data is written and the logic will not provide an ACK bit to the MCU.

From an IC level, a wrong I^2C command can create a system-level safety issue. For example, though the processor may have intended to set the output of a given regulator to 1.0 V, it may be erroneously registered as 1.1 V because of noise in the bus.

To prevent a wrong I^2C configuration, various protective mechanisms are implemented.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

12.7.5.1 I²C CRC verification

When this feature is enabled, a selectable CRC verification is performed on each I^2C transaction.

- When OTP_I2C_CRC_EN = 0, the CRC verification mechanism is disabled.
- When OTP_I2C_CRC_EN = 1, the CRC verification mechanism is enabled.

After each I^2C transaction, the device calculates the corresponding CRC byte to ensure the configuration command has not been corrupted.

When a CRC fault is detected, the PF5300 ignores the erroneous configuration command and sets the CRC_I bit.

The PF5300 implements a CRC-8-SAE, per the SAE J1850 specification.

- Polynomial = 0x1D
- Initial value = 0xFF

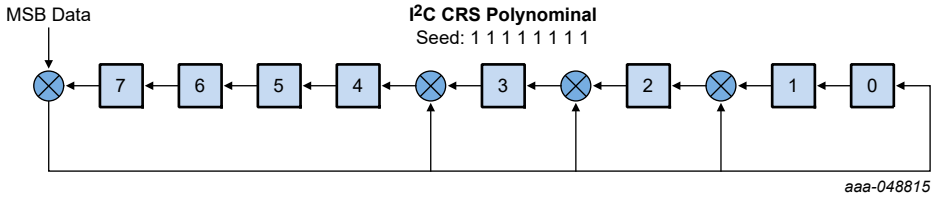


Figure 15. 8 bit SAE J1850 CRC polynomial

12.7.5.2 I²C secure write

A secure write mechanism is implemented for specific registers critical to the functional safety of the device.

- When OTP_I2C_SECURE_EN = 0, the secure write is disabled.
- When OTP_I2C_SECURE_EN = 1, the secure write is enabled.

When the secure write is enabled, a specific sequence must be followed in order to grant writing access on the corresponding secure register.

The secure write sequence is as follows:

- Processor sends command to modify the secure registers
- PMIC generates a random code in the RANDOM_GEN register
- Processor reads the random code from the RANDOM_GEN register and writes it back on the RANDOM_CHK register

The PMIC compares the RANDOM_CHK against the RANDOM_GEN register:

- If RANDOM_CHK [7:0] = RANDOM_GEN[7:0], the device applies the configuration on the corresponding secure register and self-clears both the RANDOM_GEN and RANDOM_CHK registers.
- If RANDOM_CHK[7:0] is different from RANDOM_GEN[7:0], the device ignores the configuration command and self-clears both the RANDOM_GEN and RANDOM_CHK registers.

In the event the processor sends any other command instead of providing a value for the RANDOM_CHK register, the state machine cancels the ongoing secure write transaction and performs the new I^2C command.

In the event the processor does not provide a value for the RANDOM_CHK register, the I^2C transaction will time out 10 ms after the RANDOM_GEN code is generated, and the device is then ready for a new transaction.

The following bits are protected by secure write if enabled: AB_RUN, VIN_OVLO_EN, VIN_OVLO_SDWN, FAULT_MAX_CNT, WD_EN, WD_STBY_EN, WD_ERROR_CNT, WD_DURATION, WD_MAX_ERROR, FLT_CNT_CLR, SW1_VOLT, SW1_STBY_VOLT, PGOOD_RLS, ULP_OFF_CTRL, TMP_MON_EN,

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

TMP_MON_AON, SW1_RUN_MODE, SW1_STBY_MODE, SW1_DVS, SW1_FLT_REN, SW1_ILIM_BYPASS, SW1_OV_BYPASS, SW1_UV_BYPASS.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

13 Functional blocks

13.1 SW1: DC-DC regulator

SW1 is a high-performance DC-DC regulator with integrated high- and low-side N-MOSFETs. SW1 offers a large number of programmable options to optimize the regulator for a wide range of applications.

With highly configurable compensation and adaptive-voltage positioning (AVP), loop bandwidths of up to 400 kHz can be achieved across a wide range of output capacitance. This allows meeting of stringent transient requirements of modern processors with a very low amount of capacitance. For instance, a 150 µF capacitor can maintain an AC tolerance of < 2 % for a 7.5 A load step.

13.1.1 SW1 architecture

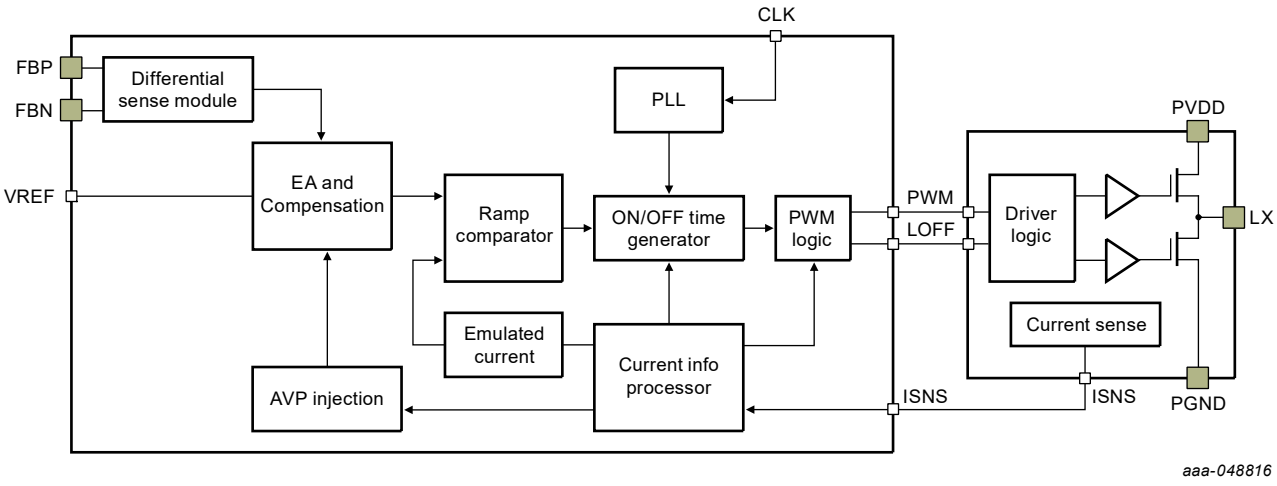


Figure 16. SW1 DC-DC Architecture

Figure 16 shows a high-level block diagram of the SW1 regulator. The reference for the regulator is set using a DAC that is controlled by the SW1_VOLT[7:0]/SW1_STBY_VOLT[7:0] registers. This reference is compared to the feedback voltage. The feedback is also injected with a signal that creates a droop on the output voltage proportional to the load current. Current sensed from the power stage is multiplied by the AVP slope gain set by the OTP_SW1_AVP[3:0] bits to create an offset on the output voltage proportional to the AVP gain and the sensed current.

The output of the error amplified is compared to an emulated current ramp signal to generate T_{ON} pulses that are sent to the power stage. The DC-DC is a constant on-time (T_{ON}) regulator with a current mode control. The T_{ON} is itself modulated with an outer loop PLL. Under steady state operation, the T_{ON} is modulated by the PLL to generate a fixed PWM frequency. A combination of these techniques strikes a balance between transient response (from a fast T_{ON} controller) and fixed frequency operation at steady state.

13.1.2 SW1 output voltage selection

The output voltage of SW1 is set using the OTP_SW1_VOLT[7:0] bits in the RUN state and using the OTP_SW1_STBY_VOLT[7:0] in the STANDBY state. The output voltage can also be changed on-the-fly by changing SW1_VOLT[7:0] in the I^2C space. SW1_VOLT[7:0]'s initial value is loaded from OTP. SW1_STBY_VOLT[7:0] can be changed before entering the STANDBY state to change from the default value loaded from OTP.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 24. SW1 voltage selection (Also applicable to SW1_STBY_VOLT[7:0])

SW1_VOLT[7:0]	Output voltage (V)	SW1_VOLT[7:0]	Output voltage (V)	SW1_VOLT[7:0]	Output voltage (V)	SW1_VOLT[7:0]	Output voltage (V)
0b00000000	0.500	0b00100100	0.680	0b01001000	0.860	0b01101100	1.040
0b00000001	0.505	0b00100101	0.685	0b01001001	0.865	0b01101101	1.045
0b00000010	0.510	0b00100110	0.690	0b01001010	0.870	0b01101110	1.050
0b00000011	0.515	0b00100111	0.695	0b01001011	0.875	0b01101111	1.055
0b00000100	0.520	0b00101000	0.700	0b01001100	0.880	0b01110000	1.060
0b00000101	0.525	0b00101001	0.705	0b01001101	0.885	0b01110001	1.065
0b00000110	0.530	0b00101010	0.710	0b01001110	0.890	0b01110010	1.070
0b00000111	0.535	0b00101011	0.715	0b01001111	0.895	0b01110011	1.075
0b00001000	0.540	0b00101100	0.720	0b01010000	0.900	0b01110100	1.080
0b00001001	0.545	0b00101101	0.725	0b01010001	0.905	0b01110101	1.085
0b00001010	0.550	0b00101110	0.730	0b01010010	0.910	0b01110110	1.090
0b00001011	0.555	0b00101111	0.735	0b01010011	0.915	0b01110111	1.095
0b00001100	0.560	0b00110000	0.740	0b01010100	0.920	0b01111000	1.100
0b00001101	0.565	0b00110001	0.745	0b01010101	0.925	0b01111001	1.105
0b00001110	0.570	0b00110010	0.750	0b01010110	0.930	0b01111010	1.110
0b00001111	0.575	0b00110011	0.755	0b01010111	0.935	0b01111011	1.115
0b00010000	0.580	0b00110100	0.760	0b01011000	0.940	0b01111100	1.120
0b00010001	0.585	0b00110101	0.765	0b01011001	0.945	0b01111101	1.125
0b00010010	0.590	0b00110110	0.770	0b01011010	0.950	0b01111110	1.130
0b00010011	0.595	0b00110111	0.775	0b01011011	0.955	0b01111111	1.135
0b00010100	0.600	0b00111000	0.780	0b01011100	0.960	0b10000000	1.140
0b00010101	0.605	0b00111001	0.785	0b01011101	0.965	0b10000001	1.145
0b00010110	0.610	0b00111010	0.790	0b01011110	0.970	0b10000010	1.150
0b00010111	0.615	0b00111011	0.795	0b01011111	0.975	0b10000011	1.155
0b00011000	0.620	0b00111100	0.800	0b01100000	0.980	0b10000100	1.160
0b00011001	0.625	0b00111101	0.805	0b01100001	0.985	0b10000101	1.165
0b00011010	0.630	0b00111110	0.810	0b01100010	0.990	0b10000110	1.170
0b00011011	0.635	0b00111111	0.815	0b01100011	0.995	0b10000111	1.175
0b00011100	0.640	0b01000000	0.820	0b01100100	1.000	0b10001000	1.180
0b00011101	0.645	0b01000001	0.825	0b01100101	1.005	0b10001001	1.185
0b00011110	0.650	0b01000010	0.830	0b01100110	1.010	0b10001010	1.190
0b00011111	0.655	0b01000011	0.835	0b01100111	1.015	0b10001011	1.195

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 24. SW1 voltage selection (Also applicable to SW1_STBY_VOLT[7:0])*...continued*

SW1_VOLT[7:0]	Output voltage (V)	SW1_VOLT[7:0]	Output voltage (V)	SW1_VOLT[7:0]	Output voltage (V)	SW1_VOLT[7:0]	Output voltage (V)
0b00100000	0.660	0b01000100	0.840	0b01101000	1.020	0b10001100	1.200
0b00100001	0.665	0b01000101	0.845	0b01101001	1.025	0b10001101 To 0b11111111	Reserved

13.1.3 SW1 adaptive-voltage positioning (AVP)

While the output voltage stays constant with respect to low without AVP, the output voltage droops linearly with load when AVP is enabled. This increases the headroom available for transient under and over shoots, thereby resulting in a reduced output capacitor requirement.

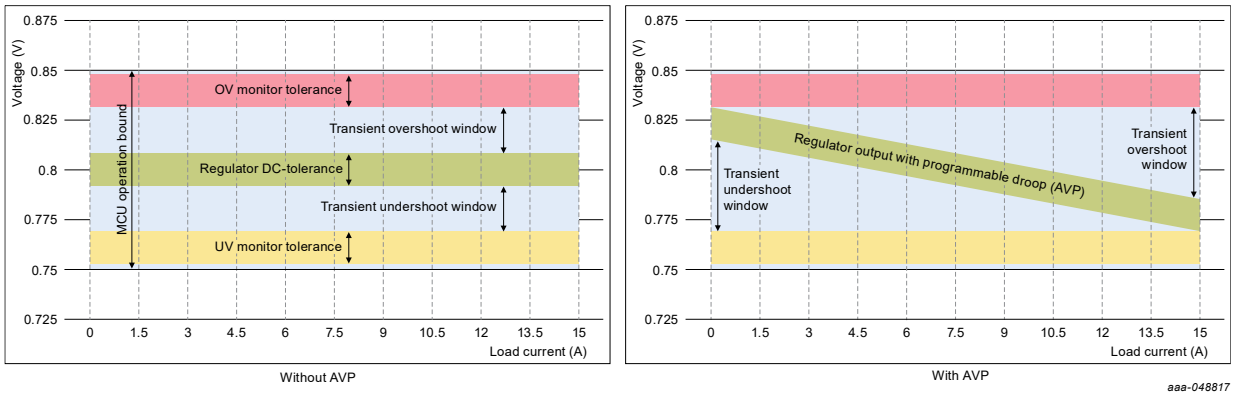


Figure 17. Adaptive-voltage positioning illustration

The AVP slope is programmable via OTP using the OTP_SW1_AVP[3:0] bits. Based on the available regulation window, the maximum expected load current, the AVP value can be chosen to provide the maximum use of the regulation window.

Table 25. AVP settings

OTP_SW1_AVP[3:0]	AVP value (mV/A)
0b0000	0 (disabled)
0b0001	0.25
0b0010	0.5
0b0011	0.75
0b0100	1
0b0101	1.5
0b0110	2
0b0111	2.5
0b1000	3
0b1001	3.5
0b1010	4
0b1011	4.5

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 25. AVP settings...*continued*

OTP_SW1_AVP[3:0]	AVP value (mV/A)
0b1100	5
0b1101	6
0b1110	7
0b1111	8

13.1.4 Calculating output accuracy with AVP

There are multiple factors to be taken into account when determining the output accuracy in an application when AVP is used. The AVP feature is dependent on the accuracy of the AVP loop and the accuracy of the current sense information.

13.1.4.1 Accuracy of the current sense circuit and the AVP loop

The current sense circuit and the AVP loop in the PF5300 have an accuracy shown in Table 26.

All parameters are specified at Ta = -40 °C to 125 °C, PVIN = 3.3 V, V_{IN} = 3.3 V, PWRON = 1.8 V, no load on regulator, Fsw = 2.25 MHz, and typical external component values, unless otherwise noted. Typical values are specified at 25 °C, unless otherwise noted.

Table 26. SW1 Current Sense and AVP Accuracy

Parameter	Symbol	Min	Typ	Max	Unit
Current Sense Accuracy	ISENSE	-7	-	7	%
AVP Setting Accuracy	AVP_0001	0.2	0.25	0.3	mV/A
AVP Setting Accuracy	AVP_0010	0.45	0.5	0.55	mV/A
AVP Setting Accuracy	AVP_0011	0.7125	0.75	0.7875	mV/A
AVP Setting Accuracy	AVP_0100	0.95	1	1.05	mV/A
AVP Setting Accuracy	AVP_0101	1.425	1.5	1.575	mV/A
AVP Setting Accuracy	AVP_0110	1.9	2	2.1	mV/A
AVP Setting Accuracy	AVP_0111	2.375	2.5	2.625	mV/A
AVP Setting Accuracy	AVP_1000	2.85	3	3.15	mV/A
AVP Setting Accuracy	AVP_1001	3.325	3.5	3.675	mV/A
AVP Setting Accuracy	AVP_1010	3.8	4	4.2	mV/A
AVP Setting Accuracy	AVP_1011	4.275	4.5	4.725	mV/A
AVP Setting Accuracy	AVP_1100	4.75	5	5.25	mV/A
AVP Setting Accuracy	AVP_1101	5.7	6	6.3	mV/A
AVP Setting Accuracy	AVP_1110	6.65	7	7.35	mV/A
AVP Setting Accuracy	AVP_1111	7.2	8	8.8	mV/A

13.1.4.2 Calculating total output voltage tolerance with AVP

Note: *The below calculations assume worst-case tolerance for all the parameters at the same time. This is improbable in a real system. A better assumption would be 50 % of the tolerance band for individual*

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

parameters. The below calculations are conservatively performed to show the theoretical worst-case tolerance band of the regulator.

Inductor tolerance also plays a factor in the overall AVP performance. Taking all of these factors into account, we can calculate the minimum and maximum voltages across load currents. The calculations result in an output voltage spread described in Figure 18 where the curve formed by points A, B, and C give the maximum regulation voltage, and the curve formed by points F and G give the minimum regulation voltage.

This section describes the procedure to calculate this spread for a given set of operating conditions.

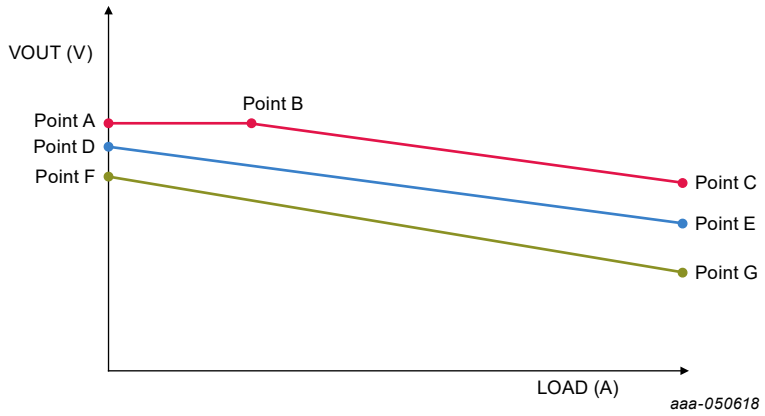


Figure 18. Vout tolerance calculation

Assuming Lmin and Lmax are the minimum and maximum values of inductance (based on the vendor's data sheet), and f is the switching frequency, the minimum and maximum single-ended ripple current are calculated as:

$$\Delta I_{L/2_Min} = \frac{0.5 V_{OUT}}{f L_{max}} [1 - \frac{V_{OUT}}{V_{IN}}]$$

$$\Delta I_{L/2_Max} = \frac{0.5 V_{OUT}}{f L_{\min}} [1 - \frac{V_{OUT}}{V_{IN}}]$$

Using the minimum and maximum ripple currents, we can calculate the minimum and maximum sensed current. These need to be calculated at 0 A and the maximum load current in the system (assumed to be X amperes). The tolerance and offset of the current sense circuit also needs to be taken into account. The tolerance of the current sense circuit is ± 7 %. The maximum offset of the current sense circuit is ± 1.62 A.

The lowest sensed current at 0 A load current is given by:

$$I_{sense_0A_lowest} = -\left(1.62 + 1.07 * \Delta I_{L/2_Min}\right)$$

The highest sensed current at 0 A load current is given by:

$$I_{sense_0A_highest} = +\left(1.62 + 1.07 * \Delta I_{L/2_Max}\right)$$

In other words, when there is 0 A load current, the current sense circuit can detect it as a current anywhere between $I_{sense_0A_lowest}$ and $I_{sense_0A_highest}$. This current value is sent to the AVP gain block that creates an offset in the output voltage.

Similarly, at a load current of X A, the lowest and highest sensed currents are given by:

$$I_{sense_XA_lowest} = I_{sense_XA_lowest} + X$$

$$I_{sense_XA_highest} = I_{sense_XA_highest} + X$$

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Now, the AVP gain works only for positive currents. Therefore, there is no AVP injection when the sensed current is lower than 0 A. This information allows us to plot the different points on the curves shown in Figure 18.

Point A:

$V_{pointA} = V_{OUT_{Nom}} * 1.01$

$I_{pointA} = 0\ A$

Point B:

$V_{pointB} = V_{OUT_{Nom}} * 1.01$

$I_{pointB} = |I_{sense_0A_lowest}|$

Point C:

$V_{pointC} = V_{OUT_{Nom}} * 1.01 - AVP_{Gain_{Min}} * I_{sense_XA_lowest}$

$I_{pointC} = X\ A$

Point D:

$V_{pointD} = V_{OUT_{Nom}} - AVP_{Gain_{Nom}} * X$

$I_{pointD} = X\ A$

Point E:

$V_{pointE} = V_{OUT_{Nom}} * 0.99 - AVP_{Gain_{Max}} * I_{sense_0A_highest}$

$I_{pointE} = 0\ A$

Point F:

$V_{pointF} = V_{OUT_{Nom}} * 0.99 - AVP_{Gain_{Max}} * \left(X + I_{sense0A_{highest}}\right)$

$I_{pointF} = X\ A$

Where,

V_{OUTNom} is the nominal output voltage as set using the SW1_VOLT[7:0]/ SW1_STBY_VOLT[7:0] register.

AVP_{Gain_Min} is the minimum AVP for the chosen setting as given in Table 26.

$AVPGainmax$ is the maximum AVP for the chosen setting as given in Table 26.

For example, for an output voltage of 0.76 V set using the SW1_VOLT[7:0] register and a nominal AVP of 1.5 mV/A set using the OTP_SW1_AVP[3:0] register:

$V_{OUT_Nom_0A}$ = 0.76 V

AVP_min = 1.425 mV/A

AVP_max = 1.575 mV/A

13.1.5 Compensating the SW1 loop

There are a number of programmable options in the SW1 regulator that can be used to adjust the loop performance.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

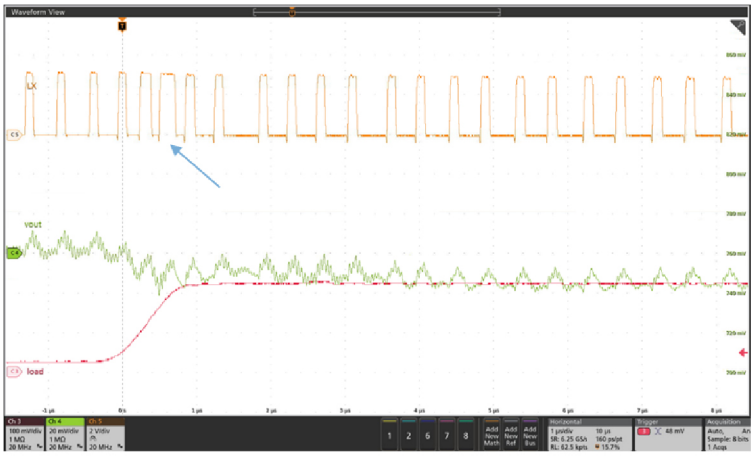
13.1.5.1 SW1 PLL

A phase-locked loop (PLL) within the SW1 block is used to adjust the T_{ON} duration such that the switching frequency is at the selected clock frequency. This PLL is enabled by setting the bit OTP_SW1_PLL_EN = 1. If OTP_SW1_PLL_EN = 0, the steady state switching frequency will increase as the load current is increased.

NXP recommends setting OTP_SW1_PLL_EN = 1, as there is no performance benefit in keeping the PLL disabled.

13.1.5.2 SW1 T_{ON} dominant operation

A feature in the PF5300 DC-DC can allow extension of the T_{ON} on a per cycle basis in the event of a large transient event. This allows for a faster response to a load step. Figure 19 shows this behavior where the T_{ON} pulse indicated by the arrow is longer compared to the other pulses. This feature can be disabled by setting the bit OTP_SW1_TON_DOM = 1. NXP recommends setting OTP_SW1_TON_DOM = 1, as there is no performance benefit in disabling this feature.



aaa-048820

Figure 19. T_{ON} extension for faster response

13.1.5.3 SW1 GM, RCOMP, and CCOMP

OTP_SW1_ GM[3:0], OTP_SW1_ RCOMP[3:0] and OTP_SW1_COMP_C[2:0] are used to select the error amplifier gain and the RC filter at the output of the error amplifier as shown in Table 27, Table 28, and Table 29. It is a good practice to use the PF5300 simulation model available in secure files on NXP.com to optimize these selections based on the use case. Given the complexity of the loop, it is not possible to develop an analytical model considering all the parameters.

Table 27. OTP_SW1_GM[3:0] selection

OTP_SW1_ GM[3:0]	Error amplifier transconductance (µS)
0b0000	68
0b0001	75
0b0010	82
0b0011	89
0b0100	95
0b0101	101

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 27. OTP_SW1_GM[3:0] selection*...continued*

OTP_SW1_ GM[3:0]	Error amplifier transconductance (µS)
0b0110	107
0b0111	113
0b1000	12
0b1001	19
0b1010	25
0b1011	32
0b1100	39
0b1101	46
0b1110	54
0b1111	61

Table 28. OTP_SW1_ RCOMP[3:0] selection

OTP_SW1_ RCOMP[3:0]	RCOMP selection (kΩ)
0b0000	90
0b0001	174
0b0010	257
0b0011	340
0b0100	415
0b0101	496
0b0110	577
0b0111	657
0b1000	725
0b1001	804
0b1010	884
0b1011	963
0b1100	1040
0b1101	1120
0b1110	1200
0b1111	1280

Table 29. OTP_SW1_ COMP_C[3:0] selection

OTP_SW1_COMP_C[2:0]	CCOMP Selection (pF)
0b000	5
0b001	10
0b010	15

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 29. OTP_SW1_ COMP_C[3:0] selection*...continued*

OTP_SW1_COMP_C[2:0]	CCOMP Selection (pF)
0b011	20
0b100	25
0b101	30
0b110	35
0b111	40

13.1.5.4 OTP_SW1_AVP_FILT[1:0] and OTP_SW1_LSEL[1:0]

OTP_SW1_AVP_FILT[1:0] controls the speed of response of the AVP loop. Set it to 0b11.

OTP_SW1_LSEL[1:0] should be set to 0x00.

13.1.6 SW1 operation mode selection

SW1_RUN_MODE[1:0] and SW1_STBY_MODE[1:0] set the switching mode of the DC-DC converter in the RUN and STANDBY states respectively, with initial values loaded from OTP_SW1_RUN_MODE[1:0] and OTP_SW1_STBY_MODE[1:0].

Table 30. SW1 Mode Selection

SW1_RUN/STBY_MODE[1:0]	Operating Mode
0b00	Off
0b01[1]	PFM, 100 kHz clock only
0b10	Reserved
0b11	PWM

[1] Only applies to PF530xB

The switching mode can be changed only on the fly via I^2C if required. Wait for at least 100 µs after the command for the new mode to take effect.

If PFM mode is used, VMON OV/UV should be set to the following range, depending on the SW1_DVS value:

Table 31. VMON OV/UV settings

SW1_DVS	DVS rate [mV/us]	Allowed OV threshold	Allowed UV threshold
00	1	104 % or more	96 % or less
01	2	105 % or more	96 % or less
10	4	106 % or more	96 % or less
11	8	108 % or more	96 % or less

13.1.7 SW1 soft-start and DVS selection

Soft-start, DVS, and power-down ramp rate can be programmed individually to provide maximum flexibility during operation.

OTP_SW1_SS[1:0] sets the soft-start slew rate. The value of OTP_SW1_SS[1:0] is loaded into SW1_DVS[1:0] in the I^2C space, which can be changed to control the ramp rate for on-the-fly changes on SW1 output voltage. OTP_SW1_DIS[1:0] sets the ramp down rate during power off of SW1. For systems with a large amount of

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

output capacitance, NXP recommends a lower rate during power down to control the amount of energy that is pumped back into the input.

Table 32. SW1 slew rate selection

OTP_SW1_SS[1:0] SW1_DVS[1:0] OTP_SW1_DIS[1:0]	Slew rate
0b00	1 mV/µs
0b01	2 mV/µs
0b10	4 mV/µs
0b11	8 mV/µs

Note: *DVS is supported only when operating in PWM mode. If a change in voltage is required in PFM mode:*

1. *Change the mode to PWM*
2. *Change the voltage*
3. *Change the mode back to PFM*

When OTP_SW1_RDIS = 1, an internal pulldown resistor of 20 ohms is added to help discharge the output capacitors. When OTP_SW1_HIZ_OFF = 1, there is no DVS ramp down during power down and the regulator relies on the external load and/or the internal RDIS discharge resistor.

All parameters are specified at Ta = -40 °C to 125 °C, PVIN = V_{IN} = 3.3 V, PWRON = 1.8 V, no load on regulator, Fsw = 2.2 MHz, typical external component values, unless otherwise noted. Typical values are specified at 25 °C, unless otherwise noted.

Table 33. SW1 electrical parameters

Parameter	Symbol	Min	Typ	Max	Unit
PVIN operating range	$PVIN_{Range}$	$PVIN_{UVDET}$	—	5.5	V
Load current capability (PF5300 only)	Iload	12	—	—	A
Load current capability (PF5301 only)	Iload	8	—	—	A
Load current capability (PF5302 only)	Iload	15	—	—	A
Nominal output voltage	Vout	—	See Table 24	—	V
SW frequency range under steady state	Fsw	2	—	3	MHz
High side FET Rds(on)	Rds(on)_HS	—	6	—	mΩ
Low side FET Rds(on)	Rds(on)_LS	—	3	—	mΩ
Output voltage accuracy (0.75 V <= Vout <= 1.2 V, Load 0 A to 15 A, AVP = 0 mΩ, PWM mode)	Acc	-1	—	1	%
Output Voltage Accuracy (0.5 V <= Vout < 0.75 V, Load 0 A to 15 A, AVP = 0 mΩ, PWM mode)	Acc	7.5	—	7.5	mV
Output voltage accuracy • PFM mode • 0.5 V ≤ VSWxFB ≤ 1.2 V • Load 0 A to 200 mA • AVP = 0 mΩ	Acc_PFM	-3	—	3	%

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 33. SW1 electrical parameters*...continued*

Parameter	Symbol	Min	Typ	Max	Unit
Peak current limit (PF5300)	ILIM	17.6	22	27	A
Peak current limit (PF5301)	ILIM	14	19	24	A
Peak current limit (PF5302)	ILIM	20	25	30	A
Current sense circuit offset (used for AVP)	I_sense_ Offset	-1.62	0	1.62	A
Discharge resistance	RDIS	—	20	—	Ω
Effective output capacitance range supported	Cout	70	—	650	µF
Output inductance range supported	Lout	70	—	130	nH
Rising-edge dead time	Tdead_r		3.6		ns
Falling-edge dead time	Tdead_f		4.5		ns
Negative current limit	Ilim_rev	-13	-10	-7	A
FB+ and FB- input current	I_fb	—	—	5	µA

13.2 Voltage monitoring

The PF5300 provides OV and UV monitoring capability for the SW1 regulator.

OTP_VMON_OV[3:0] sets the threshold for the overvoltage monitor and OTP_VMON_UV[3:0] sets the threshold for the undervoltage monitor. The thresholds are specified with respect to the voltage set by the SW1_VOLT[7:0] register. It is the user's responsibility to ensure the monitoring thresholds are set with AVP behavior taken into account, to avoid false tripping of the monitor.

OTP_VMON_OV_DB[1:0] sets the debounce time on the overvoltage monitor. OTP_VMON_UV_DB[1:0] sets the debounce time on the undervoltage monitor.

The debounce timer is derived from the high frequency clock. Values specified assume a clock frequency of 20 MHz. The value will vary depending on the CLK_FREQ[3:0] settings being selected.

The VMON_OV_I, VMON_UV_I, and SW1_ILIM_I interrupt bits are set internally if OV, UV, and ILIM faults are detected, respectively. These are latch bits and can be cleared by writing a 1 to each bit that needs to be cleared. VMON_OV_S, VMON_UV_S, and SW1_ILIM_S can be used to read the real-time status of the faults. The interrupts are for notification only and do not directly take an action to enable/disable the regulator. Enabling/disabling of the regulators under fault conditions is handled by the state machine.

Table 34. SW1 UV threshold selection

All parameters are specified at Ta = -40 °C to 125 °C, PVIN = VIN = 3.3 V, PWRON = 1.8 V, no load on regulator, Fsw = 2.2 MHz, typical external component values, unless otherwise noted. Typical values are specified at 25 °C, unless otherwise noted.

OTP_VMON_UV[3:0]	Undervoltage monitoring threshold (% of nominal)		
	Minimum	Typical	Maximum
0b0000	97.5	98.5	99.5
0b0001	97	98	99
0b0010	96.5	97.5	98.5
0b0011	96	97	98
0b0100	95.5	96.5	97.5

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 34. SW1 UV threshold selection*...continued*

All parameters are specified at Ta = -40 °C to 125 °C, PVIN = VIN = 3.3 V, PWRON = 1.8 V, no load on regulator, Fsw = 2.2 MHz, typical external component values, unless otherwise noted. Typical values are specified at 25 °C, unless otherwise noted.

OTP_VMON_UV[3:0]	Undervoltage monitoring threshold (% of nominal)		
	Minimum	Typical	Maximum
0b0101	95	96	97
0b0110	94.5	95.5	96.5
0b0111	94	95	96
0b1000	93.5	94.5	95.5
0b1001	93	94	95
0b1010	92.5	93.5	94.5
0b1011	92	93	94
0b1100	91.5	92.5	93.5
0b1101	91	92	93
0b1110	90.5	91.5	92.5
0b1111	90	91	92

Table 35. SW1 OV threshold selection

All parameters are specified at Ta = -40 °C to 125 °C, PVIN = VIN = 3.3 V, PWRON = 1.8 V, no load on regulator, Fsw = 2.2 MHz, typical external component values, unless otherwise noted. Typical values are specified at 25 °C, unless otherwise noted.

OTP_VMON_OV[3:0]	Overvoltage monitoring threshold (% of nominal)		
	Minimum	Typical	Maximum
0b0000	100.5	101.5	102.5
0b0001	101	102	103
0b0010	101.5	102.5	103.5
0b0011	102	103	104
0b0100	102.5	103.5	104.5
0b0101	103	104	105
0b0110	103.5	104.5	105.5
0b0111	104	105	106
0b1000	104.5	105.5	106.5
0b1001	105	106	107
0b1010	105.5	106.5	107.5
0b1011	106	107	108
0b1100	106.5	107.5	108.5
0b1101	107	108	109
0b1110	107.5	108.5	109.5

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 35. SW1 OV threshold selection*...continued*

All parameters are specified at Ta = -40 °C to 125 °C, PVIN = VIN = 3.3 V, PWRON = 1.8 V, no load on regulator, Fsw = 2.2 MHz, typical external component values, unless otherwise noted. Typical values are specified at 25 °C, unless otherwise noted.

OTP_VMON_OV[3:0]	Overvoltage monitoring threshold (% of nominal)		
	Minimum	Typical	Maximum
0b1111	108	109	110

Table 36. SW1 UV monitor debounce selection

All parameters are specified at Ta = -40 °C to 125 °C, PVIN = VIN = 3.3 V, PWRON = 1.8 V, no load on regulator, Fsw = 2.2 MHz, typical external component values, unless otherwise noted. Typical values are specified at 25 °C, unless otherwise noted.

OTP_VMON_UV_DB[1:0]	Undervoltage monitor debounce (µs)
0b00	5
0b01	15
0b10	40
0b11	90

Table 37. SW1 OV monitor debounce selection

All parameters are specified at Ta = -40 °C to 125 °C, PVIN = VIN = 3.3 V, PWRON = 1.8 V, no load on regulator, Fsw = 2.2 MHz, typical external component values, unless otherwise noted. Typical values are specified at 25 °C, unless otherwise noted.

OTP_VMON_OV_DB[1:0]	Overvoltage monitor debounce (µs)
0b00	5
0b01	15
0b10	25
0b11	90

13.3 ABIST verification

PF5300 implements ABIST verification of all output voltage monitors. The PF5300 tests the OV and UV monitors during the self-test routine and on-demand ABIST (AB_RUN) sequence.

AB_SW1_OV = 1 indicates that the VMON's overvoltage monitor is not operating correctly.

AB_SW1_UV = 1 indicates that the VMON's undervoltage monitor is not operating correctly.

AB_SW1_OV and AB_SW1_UV bits are overwritten every time the ABIST check is performed.

A bit AB_RUN is provided to perform ABIST on demand, which is available in the RUN state.

When the AB_RUN bit is set to 1, the control logic performs an ABIST verification on the voltage monitors. When the ABIST verification is finished, the AB_RUN bit self-clears to 0.

The PGOOD pin retains its previous state during the AB_RUN and resumes normal PGOOD operation after completion of the on-demand ABIST operation. The ABIST registers are cleared or overwritten each time the ABIST check is performed. The ABIST registers are part of the secure registers and will require an I^2C secure write to be cleared if this feature is enabled.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

When the PF5300 performs an ABIST verification on demand, the OV/UV fault monitoring is blanked for a maximum period of 200 µs. During this time, the system must ensure it is in a safe state, or it is safe to perform this action without violating the safety goals of the system. If a failure on the OV/UV monitor is detected during the ABIST on-demand request, the PMIC will assert the corresponding ABIST flags. It is the responsibility of the system to perform a diagnostic check after each ABIST verification and take action at the system level.

13.4 Clock management

Clock management provides a top-level management control scheme of internal clock and external synchronization, intended to be primarily used for the switching regulators. Clock management incorporates various subblocks:

- Low power 100 kHz clock
- Internal high-frequency clock with programmable frequency
- Phase-locked loop (PLL)

A digital clock management interface is in charge of supporting interaction among these blocks.

Clock management provides clocking signals for the internal state machine, the switching frequencies for the buck converters, as well as the multiples of those switching frequencies in order to enable phase shifting for multiple-phase operation.

13.4.1 Low-frequency clock

A low-power 100 kHz clock is provided for overall logic and digital control. Internal logic and debounce timers are based on this 100 kHz clock.

13.4.2 High-frequency clock and SW1 switching frequency

The PF5300 features a high frequency clock with nominal frequency of 20 MHz. Clock frequency is programmable over a range of ±20 % via the CLK_FREQ[3:0] control bits. The initial value of CLK_FREQ[3:0] is loaded from the OTP_CLK_FREQ[3:0] bits.

SW1 uses the high-frequency clock divided by 8 as its frequency. For example, when CLK_FREQ[3:0] = 0b0000, the high-frequency oscillator runs at 20 MHz and SW1 runs at 2.5 MHz.

Since SW1 is a constant on-time regulator with the outer loop PLL that modulates the T_{ON} to maintain the switching frequency, the resulting SW1 frequency will be maintained only under steady state load conditions. Under transient load conditions, the switching frequency will vary (since the switcher PLL is much lower than the DC-DC bandwidth) as the switcher loop responds to the transient load.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

13.4.3 Manual frequency tuning

PF5300 provides manual frequency tuning of the high-speed oscillator to modulate the switching frequency. The CLK_FREQ [3:0] bits select manual frequency tuning of the high-speed oscillator from 18 MHz to 22 MHz. If a frequency change of two or more steps is requested by a single I^2C command, the device performs a gradual frequency change, passing through all steps in between.

Manual tuning is not supported when frequency spread spectrum or external clock synchronization are used.

Table 38. Manual frequency tuning configuration

CLK_FREQ[3:0]	High-speed clock frequency (MHz)
0000	20
0001	21
0010	22
0011	Not used
0100	Not used
0101	Not used
0110	Not used
0111	Not used
1000	Not used
1001	Not used
1010	Not used
1011	18
1100	19
1101	Not used
1110	Not used
1111	Not used

13.4.4 Spread spectrum

The internal clock provides a programmable frequency spread spectrum with two ranges for narrow spread and wide spread to help manage EMC in sensitive applications.

- When the FSS_EN = 1, the frequency spread-spectrum is enabled.
- When the FSS_EN = 0, the frequency spread-spectrum is disabled.

The default state of the FSS_EN bit upon a power up can be configured via the OTP_FSS_EN bit.

The OTP_FSS_SEL bit is used to select the spread spectrum type.

Table 39. Spread spectrum configuration

OTP_FSS_SEL FSS_SEL	Description
0	Triangular modulation
1	Pseudo-random modulation

When the triangular modulation type is selected, with FSS_SEL = 0, there will be an absolute frequency deviation of ±10 % with a step of 0.5 % around the CLK_FREQ frequency setting.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

When the external clock synchronization is enabled, spread-spectrum is to be disabled.

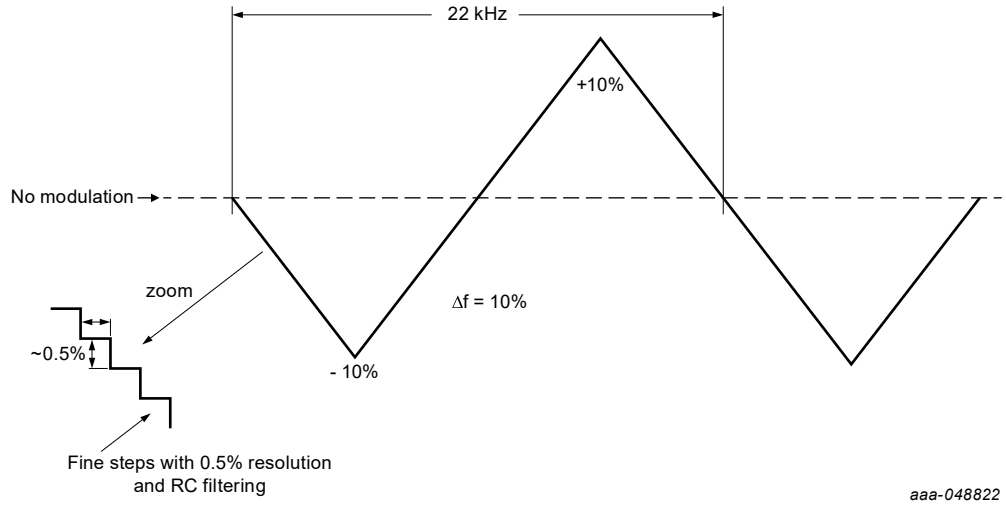


Figure 20. Triangular spread-spectrum modulation

When the pseudo-random modulation type is selected, with FSS_SEL = 1, the frequency will transition from 0 % to -10 %, through three random steps in between, and 0 % to +10 % through three random steps in between.

If the frequency spread-spectrum is enabled, the switching regulators should be set in PWM mode to ensure clock synchronization at all times.

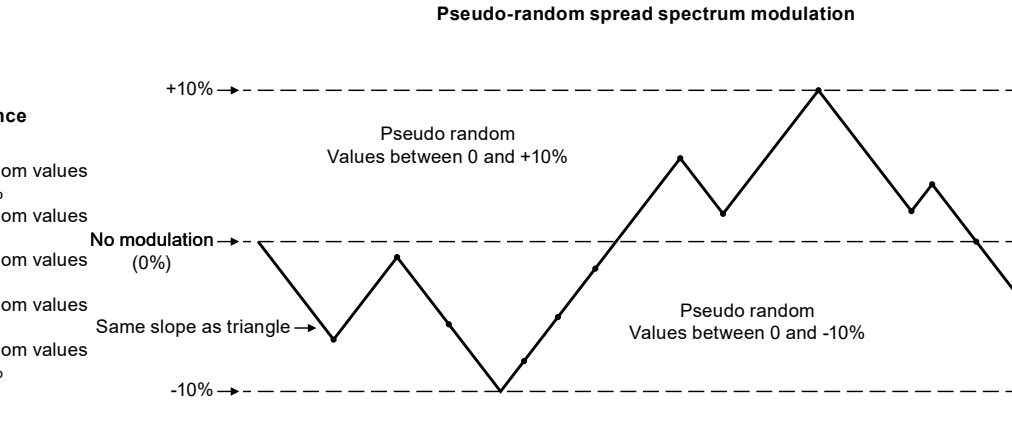


Figure 21. Pseudo-random spread-spectrum modulation

13.4.5 Clock synchronization

The SYNCIN pin can be used to synchronize the PF5300 to an external clock signal. The SYNCIN pin can accept two ranges of frequency, as defined by the OTP_FSYNC_RANGE bit. When OTP_FSYNC_RANGE = 0, the input frequency range at SYNCIN is valid between 2000 kHz and 3000 kHz. When the OTP_FSYNC_RANGE = 1 the input frequency range at SYNCIN pin is valid between 333 kHz and 500 kHz. When used as a SYNCIN input, it is not possible to enter the STANDBY state in the PF5300.

Transition from internal to external clock and vice versa happens automatically based on the validity of the external clock. FSYNC_I is set when switching from internal to external or external to internal clock sources. FSYNC_S indicates the real-time source of the clock. FSYNC_S = 1 indicates that the external clock is being used. FSYNC_S = 0 indicates that the internal clock is being used.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

The SYNCIN pin is compatible with 1.8 V or 3.3 V input signals. If the SYNCIN function is not used, the pin should be grounded. If the external clock is meant to start up after the PMIC has started, the SYNC pin must be maintained low until the external clock is applied.

The external clock duty cycle at the SYNCIN pin should be between 40 % and 60 %. An input frequency in the SYNC pin outside the range defined by the FSYNC_RANGE bit is detected as invalid.

Table 40. Clock management specifications

Symbol	Parameter	Min	Typ	Max	Unit
Low frequency clock					
f100KHzACC	100 kHz clock accuracy	−5.0	—	5.0	%
High frequency clock					
f20MHz	High-frequency clock nominal frequency	—	Table 38	—	MHz
f20MzACC	High -requency clock accuracy	−5.0	—	5.0	%
t20MHzStep	Clock step transition time minimum time to transition from one frequency step to the next in manual tuning mode	—	5.2	—	µs
FSSRANGE	Spread-spectrum range Spread-spectrum is done around center frequency of CLK_FREQ[3:0]	—	±10.0	—	%
Clock synchronization					
fSYNCIN	SYNC input frequency range FSYNC_RANGE = 0	2000	—	3000	kHz
fSYNCIN	SYNC input frequency range FSYNC_RANGE = 1	333	—	500	kHz

13.5 Thermal monitoring

The PF5300 features a temperature sensor at the center of the die which is used to generate the thermal interrupts and thermal shutdown to the Fail-safe state. Figure 22 shows a high-level block diagram of the thermal monitoring architecture in PF5300.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

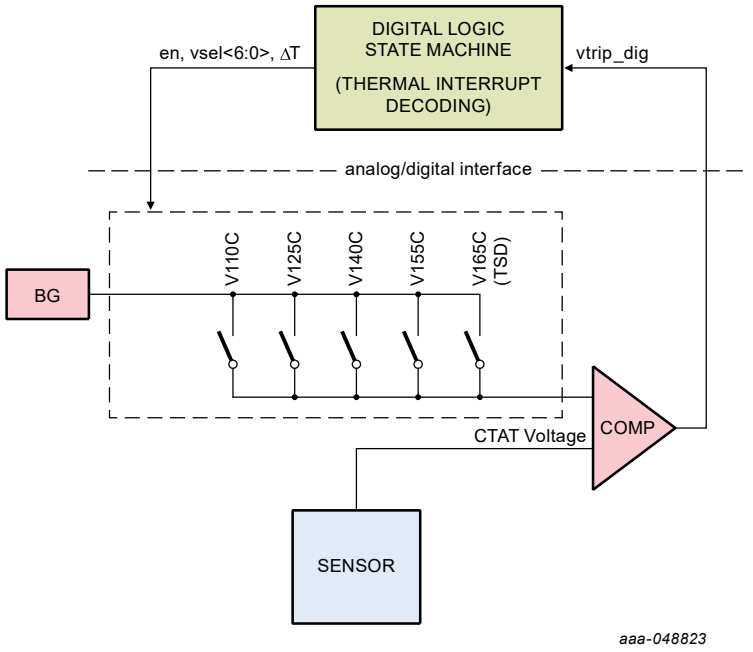


Figure 22. Thermal monitoring architecture

Table 41. Thermal monitor specifications

Symbol	Parameter	Min	Typ	Max	Unit
TSEN_RANGE	Thermal sensor temperature range	–40	—	175	ºC
T110C	110 ºC temperature threshold	100	110	120	ºC
T125C	125 ºC temperature threshold	115	125	135	ºC
T140C	140 ºC temperature threshold	130	140	150	ºC
T155C	155 ºC temperature threshold	145	155	165	ºC
TSD	Thermal shutdown threshold	155	165	175	ºC
TWARN_HYS	Thermal threshold hysteresis	—	5.0	—	ºC
TSD_HYS	Thermal shutdown hysteresis	—	15.0	—	ºC
TSD_DB	Thermal shutdown debounce timer		1		ms

As the temperature crosses the thermal thresholds, the corresponding interrupts are set to notify the system. The processor may take appropriate action to bring down the temperature (either by turning off, reducing load, or turning on a fan).

A 5 ºC hysteresis is implemented on a falling temperature in order to release the corresponding THERM_x_S signal. When the shutdown threshold is crossed, the PF5300 initiates a thermal shutdown and it prolongs shutdown until the 15 ºC thermal shutdown hysteresis is crossed as the device cools down.

The temperature monitor can be enabled or disabled via I^2C with the TMP_MON_EN bit.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

- When TMP_MON_EN = 0, the temperature monitor circuit is disabled.
- When TMP_MON_EN = 1, the temperature monitor circuit is enabled.

Table 42. Thermal monitor bit description

Bit or bits	Description
THERM_110_I, THERM_110_S	Interrupt and sense bits for 110 ºC threshold
THERM_125_I, THERM_125_S	Interrupt and sense bits for 125 ºC threshold
THERM_140_I, THERM_140_S	Interrupt and sense bits for 140 ºC threshold
THERM_155_I, THERM_155_S	Interrupt and sense bits for 155 ºC threshold
TMP_MON_EN	Disables temperature monitoring circuits when cleared

13.6 Watchdog timer

The PF5300 features a programmable watchdog timer that can be enabled using OTP_WD_EN = 1. The watchdog can also be enabled/disabled using the I^2C bit WD_EN. The WD_STBY_EN bit selects whether the watchdog is active in STANDBY state, with initial value loaded from OTP_WD_STBY_EN.

The period of the watchdog is based on the WD_DURATION[3:0] bits, with initial value loaded from OTP_WD_DURATION[3:0].

To allow for software boot up time, there is an INIT state where a 2 second window becomes active, during which a good watchdog refresh is expected from the processor. A good watchdog refresh from the processor during the INIT state closes the 2 second period, and the state machine proceeds to the RUN state. After the first refresh in the INIT state, the period of the watchdog is based on WD_DURATION[3:0].

Table 43. Watchdog window duration configuration

WD_DURATION[3:0]	Watchdog period (ms)
0b0000	1
0b0001	2
0b0010	4
0b0011	8
0b0100	16
0b0101	32
0b0110	64
0b0111	128
0b1000	256
0b1001	512
0b1010	1024
0b1011	2048
0b1100	4096
0b1101	8192
0b1110	16384
0b1111	32768

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Failure to pet the watchdog in the INIT state is considered a watchdog event, and the following occurs:

1. Increment FAULT_CNT
2. Assert PGOOD low
3. Move to IO_Release
4. Deassert PGOOD (high) after 8 ms (provided other faults controlling PGOOD do not exist)
5. Move to INIT (Transition L) to try again
6. If FAULT_CNT reaches max value, Transition H occurs to power down and enter the Fail-safe state

The watchdog timer can be programmed to be a fully open type or a windowed type. When OTP_WDWINDOW = 0, the watchdog can be petted anytime during the period (no window) to be considered a valid refresh. When OTP_WDWINDOW = 1, the watchdog can be petted only in the second half of the programmed watchdog timer duration to be considered a valid refresh. If the OTP_WDWINDOW =1, an attempt to pet the watchdog in the first half of the watchdog window is interpreted as a bad watchdog refresh. Petting the watchdog in the valid window with the right WD_ANSWER is interpreted as a successful watchdog refresh, and the next period starts immediately (without waiting for the period to be completed).

The watchdog window duration can be changed during the INIT and System ON states by modifying the WD_DURATION[3:0] bits on the functional register map. If the WD_DURATION[3:0] bits get changed during the System On states, the watchdog timer is reset (terminate on-going period without flagging an error and start a new one with updated WD_DURATION[3:0]).

A watchdog error counter is provided to keep track of erroneous refreshes of the watchdog. WD_ERROR_CNT[3:0] indicates the value of the error counter. For example, if WD_ERROR_CNT[3:0] = 0b0101, the counter value is 5. When the watchdog is petted correctly, the WD_ERROR_CNT[3:0] is decreased by 1 (floored at 0). An incorrect watchdog refresh (either data and/or temporal) is considered a watchdog error. The WD_ERROR_CNT[3:0] counter is then incremented by 2, and the next period started.

The WD_ERROR_CNT[3:0] is compared to a maximum value set by WD_MAX_ERROR[1:0]. Initial value of WD_MAX_ERROR[1:0] is loaded from OTP_ WD_MAX_ERROR[1:0].

Table 44. Watchdog error count configuration

WD_MAX_ERROR[1:0]	Maximum Error Count
0b00	8
0b01	6
0b10	4
0b11	2

If WD_ERROR_CNT[3:0] ≥ WD_MAX_ERROR[1:0], a WD event is considered to have occurred when the following takes place:

1. Increment FAULT_CNT
2. If FAULT_CNT >= FAULT_MAX_CNT, proceed via Transition Z
3. If FAULT_CNT < FAULT_MAX_CNT:
   a. Assert PGOOD low
   b. Goto IO_Release (Transition D)
   c. Deassert PGOOD (high) after 8 ms (provided other faults controlling PGOOD don’t exist) and take Transition L

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

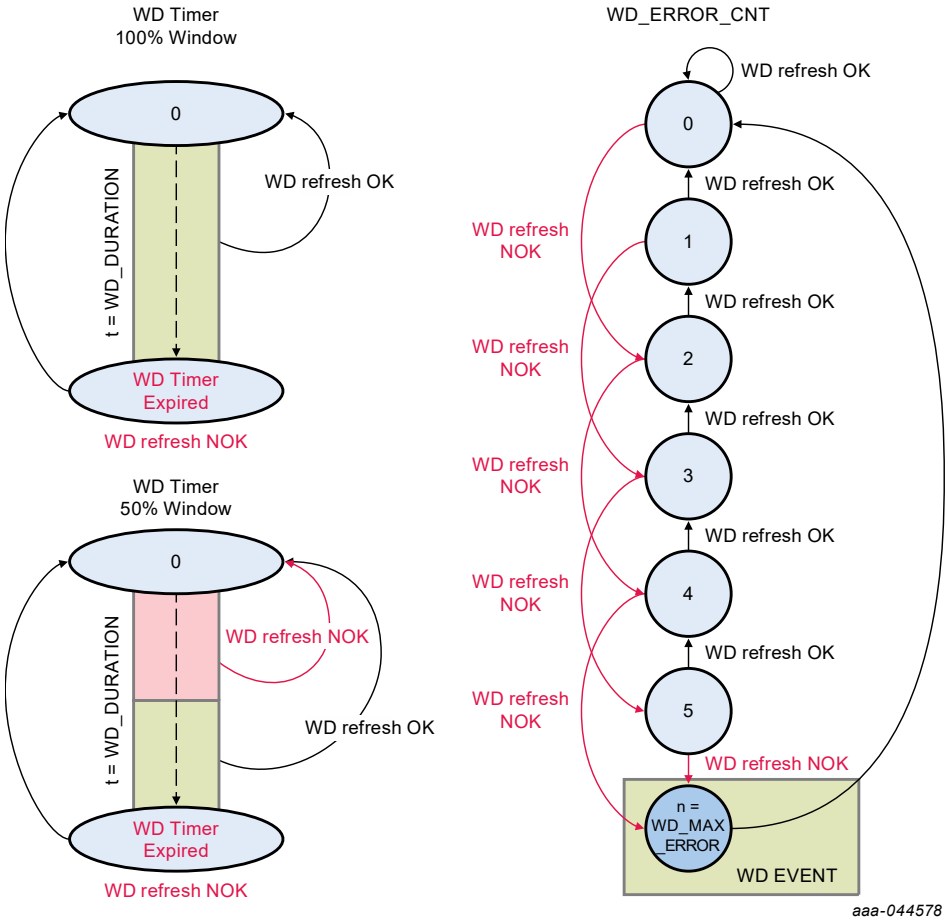


Figure 23. Watchdog timer and error counter

13.6.1 Simple watchdog (OTP_WD_SEL = 0)

When the simple watchdog type is selected with OTP_WD_SEL = 0, the WD_SEED register defaults to the seed value of 0x5B. A good watchdog refresh with the simple watchdog type consists of writing the WD_SEED 0x5B to the WD_ANSWER register within the correct window duration.

13.6.2 Challenger watchdog (OTP_WD_SEL = 1)

When the challenger watchdog type is selected with OTP_WD_SEL = 1, the WD_SEED register is updated based on an 8-bit LFSR. The starting seed for the challenger type watchdog is 0x5B. The processor is expected to read the WD_SEED (question), compute the watchdog answer, and write the value in the WD_ANSWER (answer) register within the window time. The processor can implement any type of algorithm on its side to compute the bitwise inversion of the current WD_SEED value and write that to the WD_ANSWER register. The WD_SEED value is updated to the next value in the LFSR sequence after receiving a good WD refresh from the processor.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

14 I²C register map

The PF5300 provides a complete set of registers for control and diagnostics of the PMIC operation. The configuration of the device is done at two different levels.

At the first level, the OTP mirror registers provide the default hardware and software configuration for the PMIC upon power up.

At the second level, the PF5300 provides a set of functional registers intended for system configuration and diagnostics during the system operation. These registers are accessible after power up and can be modified at any time by the system control unit.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

14.1 PF5300 OTP mirror register map

Table 45 shows the OTP register map for PF5300. All the registers default to a value of 0x00 in an unprogrammed device. The cells highlighted in yellow are monitoring using continuous CRC. The mirror registers can be read and written by the user when in Debug mode.

Table 45. PF5300 OTP map

ADDR	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
20	—	—	—	OTP_I2C_ SECURE_EN	OTP_I2C_CRC_EN	OTP_I2C_ADD[2:0]		
21	—	—	—	—	—	OTP_STANDBYINV	—	—
22	OTP_SW1_RDIS	—	—	OTP_XFAILB_EN	OTP_VIN_ OVLO_SDWN	OTP_VIN_ OVLO_EN	OTP_VIN_OVLO_DBNC[1:0]	
23	—	OTP_PD_SEQ_DLY[2:0]			—	—	—	—
24		OTP_SYNCIN_EN	OTP_SW1_PLL_EN	OTP_FSYNC_ RANGE	OTP_CLK_FREQ[3:0]			
25	OTP_FSS_EN	—	OTP_FSS_SEL	—	OTP_SW1_ TON_DOM	OTP_SW1_COMP_C[2:0]		
26	OTP_WD_DURATION[3:0]				OTP_WD_EN	OTP_WD_ STBY_EN	OTP_WD_SEL	OTP_WDWINDOW
27	—	OTP_FAULT_MAX_CNT[2:0]			OTP_SW1_AVP_FILT[1:0]		OTP_WD_MAX_ERROR[1:0]	
28	OTP_PGOOD_SEQ[5:0]						OTP_SEQ_TBASE[1:0]	
29	OTP_SW1_SEQ[5:0]						OTP_SW1_SS[1:0]	
2A	OTP_SW1_DVS_MAX[7:0]							
2B	OTP_SW1_DVS_MIN[7:0]							
2C	OTP_SW1_VOLT[7:0]							
2D	OTP_SW1_STBY_VOLT[7:0]							
2E	OTP_SW1_AVP[3:0]				OTP_SW1_GM[3:0]			
2F	OTP_SW1_RCOMP[3:0]				OTP_SW1_STBY_MODE[1:0]		OTP_SW1_RUN_MODE[1:0]	
30	RESERVED				—	OTP_SW1_ HIZ_OFF	OTP_SW1_DIS[1:0]	
31	Feature not supported. Set to 0b1	Feature not supported. Set to 0b1	Feature not supported. Set to 0b1	OTP_SW1_ ILIM_BYPASS	OTP_SW1_ UV_BYPASS	OTP_SW1_ OV_BYPASS	OTP_SW1_LSEL[1:0] Set to 0x00 always.	
32	OTP_STBY_DELAY[5:0]						RESERVED	OTP_ULP_ OFF_CTRL
33	OTP_TURN_OFF_DELAY[5:0]						OTP_FS_ BYPASS_CNT	OTP_FS_BYPASS
34	OTP_VMON_UV[3:0]				OTP_VMON_OV[3:0]			

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 45. PF5300 OTP map...*continued*

ADDR	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
35	—	OTP_PGOOD_BG	OTP_PGOOD_SW1_UV	OTP_PGOOD_SW1_OV	OTP_VMON_UV_DB[1:0]		OTP_VMON_OV_DB[1:0]	
36	—	—	—	—	OTP_PROG_ID2[3:0]			
37	OTP_PROG_ID1[7:0]							
38	OTP_S2_CRC_LSB[7:0]							
39	OTP_S2_CRC_MSB[7:0]							

14.1.1 OTP address 0x2A

Table 46. OTP address 0x2A bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OTP_SW1_DVS_MAX[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	RW							

Table 47. OTP address 0x2A bit description

Bit	Symbol	Description	
7 to 0	OTP_SW1_DVS_MAX[7:0]	Maximum SW1 voltage setting allowed.	
		All settings	See Table 24
		Reset condition	0000 0000

14.1.2 OTP address 0x2B

Table 48.

Bit	7	6	5	4	3	2	1	0
Symbol	OTP_SW1_DVS_MIN[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	RW							

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 49. OTP address 0x2B bit description

Bit	Symbol	Description	
7 to 0	OTP_SW1_DVS_MIN[7:0]	Minimum SW1 voltage setting allowed.	
		All settings	See Table 24
		Reset condition	0000 0000

14.1.3 OTP address 0x2C

Table 50. OTP address 0x2C bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OTP_SW1_VOLT[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	RW							

Table 51. OTP address 0x2C bit description

Bit	Symbol	Description	
7 to 0	OTP_SW1_VOLT[7:0]	SW1 output voltage in RUN state	
		All settings	See Table 24
		Reset condition	0000 0000

14.1.4 OTP address 0x2D

Table 52. OTP address 0x2D bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OTP_SW1_STBY_VOLT[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	RW							

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 53. OTP address 0x2D bit description

Bit	Symbol	Description	
7 to 0	OTP_SW1_STBY_VOLT[7:0]	SW1 output voltage in STANDBY state	
		All settings	See Table 24
		Reset condition	0000 0000

14.1.5 OTP address 0x2E

Table 54. OTP address 0x2E bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OTP_SW1_AVP[3:0]				OTP_SW1_GM[3:0]			
Reset	0	0	0	0	0	0	0	0
Access	RW				RW			

Table 55. OTP address 0x2E bit description

Bit	Symbol	Description	
7 to 4	OTP_SW1_AVP[3:0]	Automatic voltage positioning	
		All settings	See Table 26
		Reset condition	0000
3 to 0	OTP_SW1_GM[3:0]	Error amplifier transconductance setting.	
		All settings	See Table 27
		Reset condition	0000

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

14.1.6 OTP address 0x2F

Table 56. OTP address 0x2F bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OTP_SW1_RCOMP[3:0]				OTP_SW1_STBY_MODE[1:0]		OTP_SW1_RUN_MODE[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	RW				RW		RW	

Table 57. OTP address 0x2F bit description

Bit	Symbol	Description	
7 to 4	OTP_SW1_RCOMP[3:0]	Resistor selection for Compensator circuit	
		All settings	See Table 28
		Reset condition	0000
3 to 2	OTP_SW1_STBY_MODE[1:0]	Default operating mode in STANDBY	
		2b'00	Off
		2b'01	Reserved
		2b'10	Reserved
		2b'11	PWM Mode
		Reset condition	00
1 to 0	OTP_SW1_RUN_MODE[1:0]	Default operating mode in RUN	
		2b'00	Off
		2b'01	Reserved
		2b'10	Reserved
		2b'11	PWM Mode
		Reset condition	00

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

14.1.7 OTP address 0x20

Table 58. OTP address 0x20 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RESERVED	RESERVED	RESERVED	OTP_I2C_SECURE_EN	OTP_I2C_CRC_EN	OTP_I2C_ADD[2:0]		
Reset	0	0	0	0	0	0	0	0
Access	—	—	—	RW	RW	RW	RW	

Table 59. OTP address 0x20 bit description

Bit	Symbol	Description	
4	OTP_I2C_SECURE_EN	I^2C secure write configuration	
		1b'0	Disable
		1b'1	Enable
		Reset condition	0
3	OTP_I2C_CRC_EN	I^2C CRC verification configuration	
		1b'0	Disable
		1b'1	Enable
		Reset condition	0
2 to 0	OTP_I2C_ADD[2:0]	Default I^2C device address	
		3b'000	0x28
		3b'001	0x29
		3b'010	0x2A
		3b'011	0x2B
		3b'100	0x2C
		3b'101	0x2D
		3b'110	0x2E
		3b'111	0x2F
		Reset condition	000

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

14.1.8 OTP address 0x21

Table 60. OTP address 0x21 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	OTP_STANDBYINV	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0
Access	—	—	—	—	—	RW	—	—

Table 61. OTP address 0x21 bit description

Bit	Symbol	Description	
2	OTP_STANDBYINV	STANDBY pin polarity settings	
		1b'0	Active HIGH
		1b'1	Active LOW
		Reset condition	0000 0000

14.1.9 OTP address 0x22

Table 62. OTP address 0x22 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OTP_SW1_RDIS	RESERVED	RESERVED	OTP_XFAILB_EN	OTP_VIN_ OVLO_SDWN	OTP_VIN_ OVLO_EN	OTP_VIN_OVLO_DBNC[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	RW	—	—	RW	RW	RW	RW	RW

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 63. OTP address 0x22 bit description

Bit	Symbol	Description	
7	OTP_SW1_RDIS	SW1 internal pulldown resistor default configuration to quick discharge output capacitor	
		1b'0	Pulldown disabled
		1b'1	Pulldown enabled
		Reset condition	0
4	OTP_XFAILB_EN	Default VDDOTP/XFAILB pin configuration	
		1b'0	XFAILB functionality disabled
		1b'1	XFAILB functionality enabled
		Reset condition	0
3	OTP_VIN_OVLO_SDWN	Default shutdown configuration when VIN_OVLO event is detected	
		1b'0	Doesn’t shut down
		1b'1	Device initiates a shutdown
		Reset condition	0
2	OTP_VIN_OVLO_EN	V_{IN} OVLO monitoring default setting	
		1b'0	Disable
		1b'1	Enable
		Reset condition	0
1 to 0	OTP_VIN_OVLO_DBNC[1:0]	V_{IN} overvoltage default debounce time µS	
		2b'00	10
		2b'01	100
		2b'10	1000
		2b'11	Reserved
		Reset condition	00

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

14.1.10 OTP address 0x23

Table 64. OTP address 0x23 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RESERVED	OTP_PD_SEQ_DLY[2:0]			RESERVED	RESERVED	RESERVED	
Reset	0	0	0	0	0	0	0	0
Access	—	RW	RW	RW	—	—	—	—

Table 65. OTP address 0x23 bit description

Bit	Symbol	Description	
6 to 4	OTP_PD_SEQ_DLY[2:0]	Default delay to enter OFF mode after completion of Power Down in ms	
		3b'000	0
		3b'001	1
		3b'010	10
		3b'011	50
		3b'100	100
		3b'101	250
		3b'110	500
		3b'111	1000
		Reset condition	000

14.1.11 OTP address 0x24

Table 66. OTP address 0x24 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RESERVED	OTP_SYNCIN_EN	OTP_SW1_PLL_EN	OTP_FSYNC_RANGE	OTP_CLK_FREQ[3:0]			
Reset	0	0	0	0	0	0	0	0
Access	-	RW	RW	RW	RW			

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 67. OTP address 0x24 bit description

Bit	Symbol	Description	
6	OTP_SYNCIN_EN	STANDBY/SYNCIN pin configuration	
		1b'0	Act as STANDBY
		1b'1	Act as SYNCIN
		Reset condition	0
5	OTP_SW1_PLL_EN	PLL configuration	
		1b'0	PLL Enabled
		1b'1	PLL Disabled
		Reset condition	0
4	OTP_FSYNC_RANGE	Default valid frequency range setting for SYNCIN pin	
		1b'0	2000 kHz and 3000 kHz
		1b'1	333 kHz and 500 kHz
		Reset condition	0

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 67. OTP address 0x24 bit description...*continued*

Bit	Symbol	Description	
3 to 0	OTP_CLK_FREQ[3:0]	Default frequency for high-speed oscillator	
		4b'0000	20 MHz
		4b'0001	21 MHz
		4b'0010	22 MHz
		4b'0011	Not used
		4b'0100	Not used
		4b'0101	Not used
		4b'0110	Not used
		4b'0111	Not used
		4b'1000	Not used
		4b'1001	Not used
		4b'1010	Not used
		4b'1011	18 MHz
		4b'1100	19 MHz
		4b'1101	Not used
		4b'1110	Not used
		4b'1111	Not used
		Reset condition	0000

14.1.12 OTP address 0x25

Table 68. OTP address 0x25 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OTP_FSS_EN	RESERVED	OTP_FSS_SEL	RESERVED	OTP_SW1_TON_DOM	OTP_SW1_COMP_C[2:0]		
Reset	0	0	0	0	0	0	0	0
Access	RW	RO	RW	RO	RW	RW		

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 69. OTP address 0x25 bit description

Bit	Symbol	Description	
7	OTP_FSS_EN	Spread spectrum configuration	
		1b'0	Disable
		1b'1	Enable
		Reset condition	0
5	OTP_FSS_SEL	Spread spectrum type	
		1b'0	Triangular Modulation
		1b'1	Pseudo-random modulation
		Reset condition	0
3	OTP_SW1_TON_DOM	Extended T_{ON} configuration for SW1.	
		1b'0	Disable
		1b'1	Enable
		Reset condition	0
2 to 0	OTP_SW1_COMP_C[2:0]	Compensator capacitor selection in pF	
		3b'000	5
		3b'001	10
		3b'010	15
		3b'011	20
		3b'100	25
		3b'101	30
		3b'110	35
		3b'111	40
		Reset condition	000

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

14.1.13 OTP address 0x26

Table 70. OTP address 0x26 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OTP_WD_DURATION[3:0]				OTP_WD_EN	OTP_WD_STBY_EN	OTP_WD_SEL	OTP_WDWINDOW
Reset	0	0	0	0	0	0	0	0
Access	RW				RW	RW	RW	RW

Table 71. OTP address 0x26 bit description

Bit	Symbol	Description	
7 to 4	OTP_WD_DURATION[3:0]	Watchdog period configuration	
		All settings	Refer to Table 43
		Reset condition	0000
3	OTP_WD_EN	Watchdog feature availability in RUN state	
		1b'0	Watchdog disable
		1b'1	Watchdog enable
		Reset condition	0
2	OTP_WD_STBY_EN	Watchdog feature availability in STANDBY state	
		1b'0	Watchdog disable
		1b'1	Watchdog enable
		Reset condition	0
1	OTP_WD_SEL	Watchdog type configuration	
		1b'0	Simple watchdog with 0x5B seed
		1b'1	Challenger watchdog with seed based on 8-bit LFSR
		Reset condition	0

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 71. OTP address 0x26 bit description...*continued*

Bit	Symbol	Description	
0	OTP_WDWINDOW	Window watchdog configuration	
		1b'0	Non-windowed watchdog
		1b'1	Windowed watchdog
		Reset condition	0

14.1.14 OTP address 0x27

Table 72. OTP address 0x27 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RESERVED	OTP_FAULT_MAX_CNT[2:0]			OTP_SW1_AVP_FILT[1:0]		OTP_WD_MAX_ERROR[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	RO	RW			RW		RW	

Table 73. OTP address 0x27 bit description

Bit	Symbol	Description	
6 to 4	OTP_FAULT_MAX_CNT[2:0]	Maximum fault allowed	
		3b'000	1
		3b'001	2
		3b'010	4
		3b'011	6
		3b'100	8
		3b'101	10
		3b'110	12
		3b'111	15
		Reset condition	000

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 73. OTP address 0x27 bit description...*continued*

Bit	Symbol	Description	
3 to 2	OTP_SW1_AVP_FILT[1:0]	AVP filtering bandwidth selection	
		2b'00	2010 kHz
		2b'01	431 kHz
		2b'10	238 kHz
		2b'11	169 kHz
		Reset condition	00
1 to 0	OTP_WD_MAX_ERROR[1:0]	Maximum watchdog error configuration	
		2b'00	8
		2b'01	6
		2b'10	4
		2b'11	2
		Reset condition	00

14.1.15 OTP address 0x28

Table 74. OTP address 0x28 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OTP_PGOOD_SEQ[5:0]						OTP_SEQ_TBASE[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	RW						RW	

Table 75. OTP address 0x28 bit description

Bit	Symbol	Description	
7 to 2	OTP_PGOOD_SEQ[5:0]	Default power up sequence allocation for PGOOD pin	
		All settings	See Table 14
		Reset condition	000000

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 75. OTP address 0x28 bit description...*continued*

Bit	Symbol	Description	
1 to 0	OTP_SEQ_TBASE[1:0]	Default timebase for power up and power down in µs	
		2b'00	100
		2b'01	250
		2b'10	500
		2b'11	1000
		Reset condition	00

14.1.16 OTP address 0x29

Table 76. OTP address 0x29 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OTP_SW1_SEQ[5:0]						OTP_SW1_SS[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	RW						RW	

Table 77. OTP address 0x29 bit description

Bit	Symbol	Description	
7 to 2	OTP_SW1_SEQ[5:0]	Default power-up sequence allocation for SW	
		All settings	See Table 14.
		Reset condition	000000
1 to 0	OTP_SW1_SS[1:0]	Default soft-start slew rate in mV/µs	
		2b'00	1
		2b'01	2
		2b'10	4
		2b'11	8
		Reset condition	00

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

14.1.17 OTP address 0x30

Table 78. OTP address 0x30 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RESERVED				RESERVED	OTP_SW1_HIZ_OFF	OTP_SW1_DIS[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	RW				RO	RW	RW	

Table 79. OTP address 0x30 bit description

Bit	Symbol	Description	
2	OTP_SW1_HIZ_OFF	DVS ramp down selection	
		1b'0	DVS ramp down during power down
		1b'1	DVS ramp down feature is not available
		Reset condition	0
1 to 0	OTP_SW1_DIS[1:0]	Default ramp down rate for SW1 in mV/ µs	
		2b'00	1
		2b'01	2
		2b'10	4
		2b'11	8
		Reset condition	00

14.1.18 OTP address 0x31

Table 80. OTP address 0x31 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	Feature not supported. Set to 0b1	Feature not supported. Set to 0b1	Feature not supported. Set to 0b1	OTP_SW1_ILIM_BYPASS	OTP_SW1_UV_BYPASS	OTP_SW1_OV_BYPASS	OTP_SW1_LSEL[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 81. OTP address 0x31 bit description

Bit	Symbol	Description	
4	OTP_SW1_ILIM_BYPASS	Configures if respective fault increments the fault counter.	
		1b'0	Fault increment counter
		1b'1	Fault bypassed, counter not incremented
		Reset condition	0
2	OTP_SW1_OV_BYPASS	Configures if respective fault increments the fault counter	
		1b'0	Fault increment counter
		1b'1	Fault bypassed, counter not incremented
		Reset condition	0
3	OTP_SW1_OV_BYPASS	Configures if respective fault increments the fault counter	
		1b'0	Fault increment counter
		1b'1	Fault bypassed, counter not incremented
		Reset condition	0
1 to 0	OTP_SW1_LSEL[1:0]	Inductor selection	
		2b'00	Recommended for PF5300.
		2b'01	Not supported
		2b'10	Not supported
		2b'11	Not supported
		Reset condition	00

14.1.19 OTP address 0x32

Table 82. OTP address 0x32 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OTP_STBY_DELAY[5:0]						RESERVED	OTP_ULP_OFF_CTRL
Reset	0	0	0	0	0	0	0	0
Access	RW						RW	RW

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 83. OTP address 0x32 bit description

Bit	Symbol	Description	
7 to 2	OTP_STBY_DELAY[5:0]	Delay configuration entering and exiting STANDBY state	
		All settings	OTP_STBY_DELAY[5:0] * SEQ_TBASE[1:0]
		Reset condition	000000
0	OTP_ULP_OFF_CTRL	Power down system response	
		1b'0	State machine moves to LP_OFF state if Turn Off is initiated
		1b'1	State machine moves to ULP_OFF state if Turn Off is initiated
		Reset condition	0

14.1.20 OTP address 0x33

Table 84. OTP address 0x33 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OTP_TURN_OFF_DELAY[5:0]						OTP_FS_BYPASS_CNT	OTP_FS_BYPASS
Reset	0	0	0	0	0	0	0	0
Access	RW						RW	RW

Table 85. OTP address 0x33 bit description

Bit	Symbol	Description	
7 to 2	OTP_TURN_OFF_DELAY[5:0]	Delay before turning off SW1 and PGOOD assertion.	
		All settings	See Section 14.5.2
		Reset condition	000000
1	OTP_FS_BYPASS_CNT	Configure maximum number of Fail-safe bypass events allowed	
		1b'0	15
		1b'1	Infinite
		Reset condition	0

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 85. OTP address 0x33 bit description...*continued*

Bit	Symbol	Description	
0	OTP_FS_BYPASS	Configures exit from Fail-safe state. See Section 13.1.10	
		1b'0	Fail-safe bypass disabled
		1b'1	Fail-safe bypass feature enabled
		Reset condition	0

14.1.21 OTP address 0x34

Table 86. OTP address 0x34 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OTP_VMON_UV[3:0]				OTP_VMON_OV[3:0]			
Reset	0	0	0	0	0	0	0	0
Access	RW				RW			

Table 87. OTP address 0x34 bit description

Bit	Symbol	Description	
7 to 4	OTP_VMON_UV[3:0]	VMON pin undervoltage threshold selection	
		All settings	See Table 35
		Reset condition	0000
3 to 0	OTP_VMON_OV[3:0]	VMON pin overvoltage threshold selection	
		All settings	See Table 36
		Reset condition	0000

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

14.1.22 OTP address 0x35

Table 88. OTP address 0x35 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RESERVED	OTP_PGOOD_BG	OTP_PGOOD_SW1_UV	OTP_PGOOD_SW1_OV	OTP_VMON_UV_DB[1:0]		OTP_VMON_OV_DB[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	—	RW	RW	RW	RW		RW	

Table 89. OTP address 0x35 bit description

Bit	Symbol	Description	
6	OTP_PGOOD_BG	PGOOD response when respective fault is detected	
		1b'0	PGOOD not affected.
		1b'1	PGOOD pulled LOW.
		Reset condition	0
5	OTP_PGOOD_SW1_UV	PGOOD response when respective fault is detected	
		1b'0	PGOOD not affected.
		1b'1	PGOOD pulled LOW.
		Reset condition	0
4	OTP_PGOOD_SW1_OV	PGOOD response when respective fault is detected	
		1b'0	PGOOD not affected.
		1b'1	PGOOD pulled LOW.
		Reset condition	0
3 to 2	OTP_VMON_UV_DB[1:0]	Default debounce time for respective fault in µs	
		2b'00	5
		2b'01	15
		2b'10	25
		2b'11	90
		Reset condition	00

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 89. OTP address 0x35 bit description*...continued*

Bit	Symbol	Description	
1 to 0	OTP_VMON_OV_DB[1:0]	Default debounce time for respective fault in µs	
		2b'00	5
		2b'01	15
		2b'10	25
		2b'11	90
		Reset condition	0

14.1.23 OTP address 0x36

Table 90. OTP address 0x36 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RESERVED	RESERVED	RESERVED	OTP_PROG_ID2[3:0]				
Reset	0	0	0	0	0	0	0	0
Access	—	—	—	RW				

Table 91. OTP address 0x36 bit description

Bit	Symbol	Description	
3 to 0	OTP_PROG_ID2[3:0]	Mark OTP programming ID	
		All settings	Incremented per assigned OTP ID
		Reset condition	0000

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

14.1.24 OTP address 0x37

Table 92. OTP address 0x37 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OTP_PROG_ID1[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	RW							

Table 93. OTP address 0x37 bit description

Bit	Symbol	Description	
7 to 0	OTP_PROG_ID1[7:0]	Mark OTP programming ID	
		All settings	Incremented per assigned OTP ID
		Reset condition	0000 0000

14.2 PF5300 functional register map

Table 94 shows the I^2C register map for PF5300. The cells highlighted in yellow are monitoring using continuous CRC.

Table 94. PF5300 functional register map

0x00	DEVICE_ID	0101_0011	DEVICE_FAM[3:0]				DEVICE_ID[3:0]			
0x01	REV	0001_0000	FULL_LAYER_REV[3:0]				METAL_LAYER_REV[3:0]			
0x02	EMREV	0000_0000	PROG_ID[3:0]				—	EMREV[2:0]		
0x03	PROG_ID	0000_0000	PROG_ID[7:0]							
0x04	CONFIG1	0000_0011	—	—	—	DBG_TMR	PGOOD_RLS	ULP_OFF_CTRL	TMP_MON_AON	TMP_MON_EN
0x05	INT_STATUS1	0000_0000	SDWN_I	BG_ERR_I	CRC_I	SW1_DVS_DONE	SW1_ILIM_I	VMON_UV_I	VMON_OV_I	VIN_OVLO_I
0x06	INT_SENSE1	0000_0000	—	BG_ERR_S	—	—	SW1_ILIM_S	VMON_UV_S	VMON_OV_S	VIN_OVLO_S
0x07	INT_STATUS2	0000_0000	PGOOD_STUCK_AT_0	PGOOD_STUCK_AT_1	DVS_ERR_I	FSYNC_I	THERM_155_I	THERM_140_I	THERM_125_I	THERM_110_I
0x08	INT_SENSE2	0000_0000	—	PGOOD_S	—	FSYNC_S	THERM_155_S	THERM_140_S	THERM_125_S	THERM_110_S
0x09	BIST_STAT1	0000_0000	STEST_NOK	OTP_NOK	TRIM_NOK	REGMAP_CRC_I	—	AB_SW1_UV	AB_SW1_OV	OSC_ERR

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 94. PF5300 functional register map*...continued*

0x0A	BIST_CTRL	0000_0000	—	—	—	—	—	—	—	AB_RUN	
0x0B	STATE	0000_0000	—	—	DBG_EXIT	IN_DBG_MODE	STATE[3:0]				
0x0C	STATE_CTRL	0000_0000	PMIC_OFF	TSD_FAIL	REG_FAIL	PG_FAIL	PU_FAIL	—	-	STANDBYINV	
0x0D	SW1_VOLT	0000_0000	SW1_VOLT[7:0]								
0x0E	SW1_STBY_VOLT	0000_0000	SW1_STBY_VOLT[7:0]								
0x0F	SW1_CTRL1	0000_0000	—	—	SW1_STBY_MODE[1:0]		SW1_RUN_MODE[1:0]		SW1_DVS[1:0]		
0x10	SW1_CTRL2	0000_0000	SW1_FLT_REN	—	SW1_ILIM_STATE	SW1_UV_STATE	SW1_OV_STATE	SW1_ILIM_BYPASS	SW1_UV_BYPASS	SW1_OV_BYPASS	
0x11	CLK_CTRL	0000_0000	—	FSS_SEL	—	FSS_EN	CLK_FREQ[3:0]				
0x12	SEQ_CTRL1	0000_0000	SEQ_TBASE[1:0]		SW1_SEQ[5:0]						
0x13	SEQ_CTRL2	0000_0000	—	—	PGOOD_SEQ[5:0]						
0x14	RANDOM_CHK	0000_0000	RANDOM_CHK[7:0]								
0x15	RANDOM_GEN	0000_0000	RANDOM_GEN[7:0]								
0x16	WD_CTRL1	0000_0000	WD_MAX_ERROR[1:0]		WD_DURATION[3:0]				WD_STBY_EN	WD_EN	
0x17	WD_SEED	0000_0000	WD_SEED[7:0]								
0x18	WD_ANSWER	0000_0000	WD_ANSWER[7:0]								
0x19	FLT_CNT1	0000_0000	FAULT_CNT[3:0]				WD_ERROR_CNT[3:0]				
0x1A	FLT_CNT2	0000_0000	FLT_CNT_CLR	VIN_OVLO_DBNC[1:0]		VIN_OVLO_SDWN	VIN_OVLO_EN	FAULT_MAX_CNT[2:0]			

The following bit types are used in the PF5300 register map.

- RWOTP: Read/write bit with default value loaded from OTP
- RO: Read-only
- RW: Read/write capable
- FLGWC: Write 1 to clear flag bit
- FLGWC_CLR: Write 1 to clear flag bit with ability to be cleared via external signal
- EXTRW: Read/write bit with self-set/reset capability

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

14.2.1 DEVICE_ID register

Table 95. DEVICE_ID register, address 0x00 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	DEVICE_FAM[3:0]				DEVICE_ID[3:0]			
Reset	0	1	0	1	0	0	1	1
Access	RO				RO			

Table 96. DEVICE_ID register bit description

Bit	Symbol	Description	
4 to 7	DEVICE_FAM[3:0]	Device family	
		4b'0101	PF5300
		All other settings	NA
		Reset condition	POR
3 to 0	DEVICE_ID[3:0]	Device ID within the family	
		4b'0011	PF5300
		4b'0100	PF5301
		4b'0101	PF5302
		All other settings	NA
		Reset Condition	POR

14.2.2 REV register

Table 97. REV register, address 0x01 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	FULL_LAYER_REV[3:0]				METAL_LAYER_REV[3:0]			
Reset	0	0	1	0	0	x	x	1
Access	RO				RO			

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 98. REV register bit description

Bit	Symbol	Description	
7 to 4	FULL_LAYER_REV[3:0]	Full layer ID	
		4b'0000	0
		4b'0001	A
		4b'0010	B
		4b'0011	C
		4b'0100	D
		4b'0101	E
		4b'0110	F
		4b'0111	G
		4b'1000	H
		4b'1001	I
		4b'1010	J
		4b'1011	K
		4b'1100	L
		4b'1101	M
		4b'1110	N
		4b'1111	O
		Reset condition	POR

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 98. REV register bit description*...continued*

Bit	Symbol	Description	
3 to 0	METAL_LAYER_REV[3:0]	Metal layer ID	
		4b'0000	0
		4b'0001	1
		4b'0010	2
		4b'0011	3 (PF530xA version)
		4b'0100	4
		4b'0101	5 (PF530xB version)
		4b'0110	6
		4b'0111	7
		4b'1000	8
		4b'1001	9
		4b'1010	10
		4b'1011	11
		4b'1100	12
		4b'1101	13
		4b'1110	14
		4b'1111	15
		Reset condition	POR

14.2.3 CONFIG1 register

Table 99. CONFIG1 register, address 0x04 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RESERVED	RESERVED	RESERVED	DBG_TMR	PGOOD_RLS	ULP_OFF_CTRL	TMP_MON_AON	TMP_MON_EN
Reset	0	0	0	0	0	0	1	1
Access	—	—	—	RW	RWOTP	RWOTP	RW	RW

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 100. CONFIG1 register bit description

Bit	Symbol	Description	
4	DBG_TMR	Debug mode exit timer. Only useful in Debug mode.	
		1b'0	Exit LP_Off request
		1b'1	Remain in LP_Off until this bit is cleared
		Reset condition	POR
3	PGOOD_RLS	Software PGOOD control.	
		1b'0	Assert PGOOD (low) SW request
		1b'1	Deassert PGOOD SW request
		Reset condition	POR
2	ULP_OFF_CTRL	Turn offf transition configuration	
		1b'0	Turn off brings IC to LP_Off (transition O1)
		1b'1	Turn off brings IC to ULP_Off (transition O2)
		Reset condition	POR
1	TMP_MON_AON	Thermal monitor mode selection	
		1b'0	Thermal monitor in sampling mode (~3 ms per sample)
		1b'1	Thermal monitor always on
		Reset condition	POR
0	TMP_MON_EN	Temperature monitor enable	
		1b'0	Disable thermal monitoring
		1b'1	Enable thermal monitoring
		Reset condition	POR

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

14.2.4 INT_STATUS1 register

Table 101. INT_STATUS1 register, address 0x05 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SDWN_I	BG_ERR_I	CRC_I	SW1_DVS_DONE	SW1_ILIM_I	VMON_UV_I	VMON_OV_I	VIN_OVLO_I
Reset	0	0	0	0	0	0	0	
Access	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	FLGWC

Table 102. INT_STATUS1 register bit description

Bit	Symbol	Description	
7	SDWN_I	Software shutdown initiation	
		1b’0	Shut down request not present or cleared if present
		1b'1	Shut down requested.
		Reset condition	POR, LPOFF entry
6	BG_ERR_I	BG1-BG2 drift detection	
		1b'0	No fault/fault cleared
		1b'1	Fault detected (latch). Write a 1 to this bit to clear it
		Reset condition	POR, LPOFF entry
5	CRC_I	I^2C CRC error flag	
		1b'0	No fault/fault cleared
		1b'1	Fault detected (latch). Write a 1 to this bit to clear it
		Reset condition	POR, LPOFF entry
4	SW1_DVS_DONE	SW1 DVS complete flag	
		1b'0	DVS not completed/not used
		1b'1	DVS completed
		Reset condition	POR, LPOFF entry

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 102. INT_STATUS1 register bit description...*continued*

Bit	Symbol	Description	
3	SW1_ILIM_I	SW1 current limit fault flag	
		1b'0	No fault/fault cleared
		1b'1	Fault detected (latch). Write a 1 to this bit to clear it
		Reset condition	POR, LPOFF entry
2	VMON_UV_I	SW1 undervoltage fault flag	
		1b'0	No fault/fault cleared
		1b'1	Fault detected (latch). Write a 1 to this bit to clear it
		Reset condition	POR, LPOFF entry
1	VMON_OV_I	SW1 overvoltage fault flag	
		1b'0	No fault/fault cleared
		1b'1	Fault detected (latch). Write a 1 to this bit to clear it
		Reset condition	POR, LPOFF entry
0	VIN_OVLO_I	V_{IN} overvoltage Interrupt flag	
		1b'0	No fault/fault cleared
		1b'1	Fault detected (latch). Write a 1 to this bit to clear it
		Reset condition	POR

14.2.5 INT_SENSE1 register

Table 103. INT_SENSE1 register, Address 0x06 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RESERVED	BG_ERR_S	RESERVED	RESERVED	SW1_ILIM_S	VMON_UV_S	VMON_OV_S	VIN_OVLO_S
Reset	0	0	0	0	0	0	0	0
Access	—	RO	—	—	RO	RO	RO	RO

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 104. INT_SENSE1 register bit description

Bit	Symbol	Description	
6	BG_ERR_S	Band gap error real-time status bit	
		1b'0	Fault does not exist
		1b'1	Fault exists
		Reset condition	POR
3	SW1_ILIM_S	SW1 ILIM real-time status bit	
		1b'0	Fault does not exist
		1b'1	Fault exists
		Reset condition	POR
2	VMON_UV_S	SW1 UV real-time status bit	
		1b'0	Fault does not exist
		1b'1	Fault exists
		Reset condition	POR
1	VMON_OV_S	SW1 OV real-time status bit	
		1b'0	Fault does not exist
		1b'1	Fault exists
		Reset condition	POR
0	VIN_OVLO_S	V_{IN} OVLO real-time status bit	
		1b'0	Fault does not exist
		1b'1	Fault exists
		Reset condition	POR

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

14.2.6 INT_STATUS2 register

Table 105. INT_STATUS2 register, address 0x07 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	PGOOD_STUCK_AT_0	PGOOD_STUCK_AT_1	DVS_ERR_I	FSYNC_I	THERM_155_I	THERM_140_I	THERM_125_I	THERM_110_I
Reset	0	0	0	0	0	0	0	0
Access	FLGWC	FLGWC	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR

Table 106. INT_STATUS2 register bit description

Bit	Symbol	Description	
7	PGOOD_STUCK_AT_0	PGOOD stuck at low interrupt	
		1b'0	PGOOD stuck At 0 not detected when internally pin is released
		1b'1	PGOOD stuck at 0 detected when internally pin is released
		Reset condition	POR
6	PGOOD_STUCK_AT_1	PGOOD stuck at high interrupt	
		1b'0	PGOOD stuck At 1 not detected when internally pulled LOW
		1b'1	PGOOD stuck at 1 detected when internally pulled LOW
		Reset condition	POR
5	DVS_ERR_I	SW1 voltage range violation	
		1b'0	No violation detected
		1b'1	SW1 voltage set above/below max/min setting (OTP_SW1_DVS_MAXMIN[7:0], OTP_SW1_DVS_MIN[7:0])
		Reset condition	POR, LPOFF entry
4	FSYNC_I	Indicates transition from external to internal clock and vice versa	
		1b'0	No clock switchover
		1b'1	Clock source switchover (bidirectional)
		Reset condition	POR, LPOFF entry

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 106. INT_STATUS2 register bit description*...continued*

Bit	Symbol	Description	
3	THERM_155_I	155C threshold Interrupt (bi-directional)	
		1b'0	Interrupt not detected
		1b'1	Interrupt detected
		Reset condition	POR, LPOFF entry
2	THERM_140_I	140C threshold interrupt (bidirectional)	
		1b'0	Interrupt not detected
		1b'1	Interrupt detected
		Reset condition	POR, LPOFF entry
1	THERM_125_I	125C Threshold Interrupt (bidirectional)	
		1b'0	Interrupt not detected
		1b'1	Interrupt detected
		Reset condition	POR, LPOFF entry
0	THERM_110_I	110C Threshold Interrupt (bidirectional)	
		1b'0	Interrupt not detected
		1b'1	Interrupt detected
		Reset condition	POR, LPOFF entry

14.2.7 EMREV and PROGID registers

Reserved for NXP Internal Use

Table 107. EMREV register, address 0x02 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	PROG_IDH[3]	PROG_IDH[2]	PROG_IDH[1]	PROG_IDH[0]	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0
Access	RO							

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 108. EMREV register bit description

Bit	Symbol	Description	
7 to 4	PROG_IDH[3:0]	OTP ID first letter[1]	
		0000	A
		0001	B
		0010	C
		0011	D
		0100	E
		0101	F
		0110	G
		0111	H
		1000	J
		1001	K
		1010	L
		1011	M
		1100	N
		1101	P
		1110	Q
		1111	R
		10000 - 11111	Not assigned
		Reset condition	POR

[1] *I* and *O* are not used.

Table 109. PROGID register, address 0x03 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	PROG_IDL[7]	PROG_IDL[6]	PROG_IDL[5]	PROG_IDL[4]	PROG_IDL[3]	PROG_IDL[2]	PROG_IDL[1]	PROG_IDL[0]
Reset	0	0	0	0	0	0	0	0
Access	RO							

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 110. PROGID register bit description

Bit	Symbol	Description	
7 to 0	PROG_IDL[7:0]	OTP ID second letter[1]	
		8b'00000000	0
		8b'00000001	1
		8b'00000010	2
		8b'00000011	3
		8b'00000100	4
		8b'00000101	5
		8b'00000110	6
		8b'00000111	7
		8b'00001000	8
		8b'00001001	9
		8b'00001010	A
		8b'00001011	B
		8b'00001100	C
		8b'00001101	D
		8b'00001110	E
		8b'00001111	F
		8b'00010000	G
		8b'00010001	H
		8b'00010010	J
		8b'00010011	K
		8b'00010100	L
		8b'00010101	M
		8b'00010110	N
		8b'00010111	P
		8b'00011000	Q
		8b'00011001	R
		8b'00011010	S
		8b'00011011	T

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 110. PROGID register bit description*...continued*

Bit	Symbol	Description	
		8b'00011100	U
		8b'00011101	V
		8b'00011110	W
		8b'00011111	X
		8b'00100000	Y
		8b'00100001	Z
		8b'00100010	Not assigned
		Reset condition	POR

[1] *I* and *O* are not used.

14.2.8 INT_SENSE2 register

Table 111. INT_SENSE2 register, address 0x08 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RESERVED	PGOOD_S	RESERVED	FSYNC_S	THERM_155_S	THERM_140_S	THERM_125_S	THERM_110_S
Reset	0	0	0	0	0	0	0	0
Access	—	RO	—	RO	RO	RO	RO	RO

Table 112. INT_SENSE2 register bit description

Bit	Symbol	Description	
6	PGOOD_S	PGOOD real-time status bit	
		1b'0	PGOOD detected at logic low
		1b'1	PGOOD detected at logic high
		Reset condition	POR

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 112. INT_SENSE2 register bit description*...continued*

Bit	Symbol	Description	
4	FSYNC_S	Clock synchronization real-time status bit	
		1b'0	Internal oscillator used as clock source
		1b'1	Clock source is from external synchronized clock
		Reset condition	POR
3	THERM_155_S	Thermal sensor real-time status bit	
		1b'0	Temperature below 155 ℃
		1b'1	Temperature above 155 ℃
		Reset condition	POR
2	THERM_140_S	Thermal sensor real-time status bit	
		1b'0	Temperature below 140 ℃
		1b'1	Temperature above 140 ℃
		Reset condition	POR
1	THERM_125_S	Thermal sensor real-time status bit	
		1b'0	Temperature below 125C
		1b'1	Temperature above 125C
		Reset condition	POR
0	THERM_110_S	Thermal sensor real-time status bit	
		1b'0	Temperature below 110 ℃
		1b'1	Temperature above 110 ℃
		Reset condition	POR

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

14.2.9 BIST_STAT1 register

Table 113. BIST_STAT1 register bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	STEST_NOK	OTP_NOK	TRIM_NOK	REGMAP_CRC_I	Reserved	AB_SW1_UV	AB_SW1_OV	OSC_ERR
Reset	0	0	0	0	0	0	0	
Access	RO	RO	RO	FLGWC	RO	FLGWC_CLR	FLGWC_CLR	FLGWC_CLR

Table 114. BIST_STAT1 register bit description

Bit	Symbol	Description	
7	STEST_NOK	Self-test status	
		1b'0	Self-test pass
		1b'1	Self-test failure
		Reset condition	POR
6	OTP_NOK	OTP bit flip detection	
		1b'0	No bit flip detected
		1b'1	Bit flip detected
		Reset condition	POR
5	TRIM_NOK	Trim bit flip detection	
		1b'0	No bit flip detected
		1b'1	Bit flip detected
		Reset condition	POR
4	REGMAP_CRC_I	Register map continuous CRC status	
		1b'0	No fault
		1b'1	Register map CRC failure
		Reset condition	POR

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 114. BIST_STAT1 register bit description...*continued*

Bit	Symbol	Description	
2	AB_SW1_UV	SW1 undervoltage monitor failure status	
		1b'0	No fault
		1b'1	SW1 UV monitor fault
		Reset condition	POR, LPOFF Entry
1	AB_SW1_OV	SW1 overvoltage monitor failure status	
		1b'0	No fault
		1b'1	SW1 OV monitor fault
		Reset condition	POR, LPOFF Entry
0	OSC_ERR	100 kHz and 20 MHz comparison status	
		1b'0	No clock error
		1b'1	One of the clocks has drifted by at least 15 %
		Reset condition	POR, LPOFF Entry

14.2.10 BIST_CTRL register

Table 115. BIST_CTRL register, address 0x0A bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	AB_RUN
Reset	0	0	0	0	0	0	0	0
Access	—	—	—	—	—	—	—	RWCLR

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 116. BIST_CTRL register bit description

Bit	Symbol	Description	
0	AB_RUN	Start on-demand ABIST	
		1b'0	On-demand ABIST not started/completed
		1b'1	Set to initiate on-demand ABIST
		Reset condition	POR, LPOFF entry

14.2.11 STATE register

Table 117. STATE register, address 0x0B bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RESERVED	RESERVED	DBG_EXIT	IN_DBG_MODE	STATE[3:0]			
Reset	0	0	0	0	0	0	0	0
Access	—	—	WP	RO				

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 118. STATE register bit description

Bit	Symbol	Description	
5	DBG_EXIT	Exit Debug mode	
		1b'0	No change
		1b'1	Exit debug mode
		Reset condition	POR
4	IN_DBG_MODE	Indicates whether in Debug mode	
		1b'0	Not in Debug mode
		1b'1	In Debug mode
		Reset condition	POR
3 to 0	STATE[3:0]	Indicates current state machine state	
		4b'0000	POR
		4b'0001	Fuse load
		4b'0010	LP_Off
		4b'0011	Self-test
		4b'0100	Power up
		4b'0101	INIT
		4b'0110	IO_Release
		4b'0111	RUN
		4b'1000	STANDBY
		4b'1001	Fault (power-down)
		4b'1010	Fail-safe
		4b'1011	Turn off power down
		4b'1100	2 ms self-test retry
		4b'1101	Off_DLY
		4b'1110	Reserved
		4b'1111	Reserved
		Reset condition	POR

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

14.2.12 STATE_CTRL register

Table 119. STATE_CTRL register, address 0x0C bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	PMIC_OFF	TSD_FAIL	REG_FAIL	PG_FAIL	PU_FAIL	RESERVED	RESERVED	STANDBYINV
Reset	0	0	0	0	0	0	0	0
Access	RWCLR	FLGWC	FLGWC	FLGWC	FLGWC	—	—	RWOTP

Table 120. STATE_CTRL register bit description

Bit	Symbol	Description	
7	PMIC_OFF	Description	Software turn-off request
		1b'0	Turn off not requested
		1b'1	Software turn off initiated
		Reset condition	POR
6	TSD_FAIL	Description	Thermal failure status
		1b'0	Thermal shutdown fault not detected
		1b'1	Indicates that the state machine entered Fail-safe state because of thermal shutdown
		Reset condition	POR
5	REG_FAIL	Description	Fault counter failure status
		1b'0	Fault counter did not reach configured max count
		1b'1	Indicates that the state machine entered Fail-safe state because of fault counter reaching its maximum value
		Reset condition	POR
4	PG_FAIL	Description	PGOOD stuck at fail status
		1b'0	PGOOD stuck failure not detected
		1b'1	Indicates that the state machine entered Fail-safe state because of PGOOD stuck at 0 or 1.
		Reset condition	POR

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 120. STATE_CTRL register bit description*...continued*

Bit	Symbol	Description	
3	PU_FAIL	Description	Power up fail status
		1b'0	Power up failure not detected
		1b'1	Indicates that the state machine entered Fail-safe state because of a power-up failure. (Transition Q)
		Reset condition	POR
0	STANDBYINV	Description	STANDBY polarity control
		1b'0	STANDBY pin is logic high
		1b'1	STANDBY pin is logic low
		Reset condition	POR

14.2.13 SW1_VOLT register

Table 121. SW1_VOLT register, address 0x0D bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SW1_VOLT[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	RWOTP							

Table 122. SW1_VOLT register bit description

Bit	Symbol	Description	
7 to 0	SW1_VOLT[7:0]	SW1 voltage setting in RUN state	
		SW1_VOLT[7:0]	See Table 24
		Reset condition	POR

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

14.2.14 SW1_STBY_VOLT register

Table 123. SW1_STBY_VOLT register, address 0x0E bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SW1_STBY_VOLT[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	RWOTP							

Table 124. SW1_STBY_VOLT register bit description

Bit	Symbol	Description	
7 to 0	SW1_STBY_VOLT[7:0]	SW1 voltage setting in STANDBY state	
		SW1_STBY_VOLT[7:0]	See Table 24
		Reset condition	POR

14.2.15 SW1_CTRL1 register

Table 125. SW1_CTRL1 register bit allocation table

Bit	7	6	5	4	3	2	1	0
Symbol	RESERVED	RESERVED	SW1_STBY_MODE[1:0]		SW1_RUN_MODE[1:0]		SW1_DVS[1:0]	
Reset	0	0	0	0	0	0	0	0
Access	RO	RO	RWOTP		RWOTP		RWOTP	

Table 126. SW1_CTRL1 register bit description

Bit	Symbol	Description	
5 to 4	SW1_STBY_MODE[1:0]	SW1 Operating mode in STANDBY state	
		SW1_STBY_MODE[1:0]	See Table 30
		Reset condition	POR

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 126. SW1_CTRL1 register bit description...*continued*

Bit	Symbol	Description	
3 to 2	SW1_RUN_MODE[1:0]	SW1 Operating Mode in RUN state	
		SW1_RUN_MODE[1:0]	See Table 30
		Reset condition	POR
1 to 0	SW1_DVS[1:0]	SW1 DVS slew rate control	
		SW1_DVS[1:0]	See Table 32
		Reset condition	POR

14.2.16 SW1_CTRL2 register

Table 127. SW1_CTRL2 register, address 0x10 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SW1_FLT_REN	RESERVED	SW1_ILIM_STATE	SW1_UV_STATE	SW1_OV_STATE	SW1_ILIM_ BYPASS	SW1_UV_ BYPASS	SW1_OV_ BYPASS
Reset	0	0	0	0	0	0	0	0
Access	RW	-	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP

Table 128. SW1_CTRL2 register bit description

Bit	Symbol	Description	
7	SW1_FLT_REN	Not supported	
		Reset condition	POR
5	SW1_ILIM_STATE	Not supported. Automatically set to 1 via OTP.	
		Reset condition	POR
4	SW1_UV_STATE	Not supported. Automatically set to 1 via OTP.	
		Reset condition	POR
3	SW1_OV_STATE	Not supported. Automatically set to 1 via OTP.	
		Reset condition	POR

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 128. SW1_CTRL2 register bit description...*continued*

Bit	Symbol	Description	
2	SW1_ILIM_BYPASS	SW1 ILIM fault bypass reaction	
		1b'0	SW1 ILIM causes fault counter Increment
		1b'1	No impact because of SW1 ILIM on fault counter
		Reset condition	POR
1	SW1_UV_BYPASS	SW1 undervoltage fault bypass reaction	
		1b'0	SW1 UV causes fault counter Increment
		1b'1	No impact because of SW1 UV on fault counter
		Reset condition	POR
0	SW1_OV_BYPASS	SW1 overvoltage fault bypass reaction	
		1b'0	SW1 OV causes fault counter Increment
		1b'1	No impact because of SW1 OV on fault counter
		Reset condition	POR

14.2.17 CLK_CTRL register

Bit	7	6	5	4	3	2	1	0
Symbol	RESERVED	FSS_SEL	RESERVED	FSS_EN	CLK_FREQ[3:0]			
Reset	0	0	0	0	0	0	0	0
Access	RO	RWOTP	RO	RWOTP	RWOTP			

Bit	Symbol	Description	
6	FSS_SEL	Spread spectrum mode selection	
		1b'0	Triangular modulation
		1b'1	Pseudo-random modulation
		Reset condition	POR

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Bit	Symbol	Description	
4	FSS_EN	Spread spectrum enable	
		1b'0	Spread spectrum disabled
		1b'1	Spread spectrum enabled
		Reset condition	POR
3 to 0	CLK_FREQ[3:0]	20 MHz oscillator frequency selection	
		CLK_FREQ[3:0]	See Table 38
		Reset condition	POR

14.2.18 SEQ_CTRL1 register

Table 129. SEQ_CTRL1 register, address 0x12 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SEQ_TBASE[1:0]		SW1_SEQ[5:0]					
Reset	0	0	0	0	0	0	0	0
Access	RWOTP		RWOTP					

Table 130. SEQ_CTRL1 register bit description

Bit	Symbol	Description	
7 to 6	SEQ_TBASE[1:0]	Slot width selection	
		All settings	See Table 13
		Reset condition	POR
5 to 0	SW1_SEQ[5:0]	SW1 sequence control	
		All settings	See Table 14
		Reset condition	POR

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

14.2.19 SEQ_CTRL2 register

Table 131. SEQ_CTRL2 register, address 0x13 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RESERVED	RESERVED	PGOOD_SEQ[5:0]					
Reset	0	0	0	0	0	0	0	0
Access	—	—	RWOTP					

Table 132. SEQ_CTRL2 register bit description

Bit	Symbol	Description	
7 to 0	PGOOD_SEQ[5:0]	PGOOD sequence control	
		All settings	See Table 14
		Reset condition	POR

14.2.20 RANDOM_CHK register

Table 133. RANDOM_CHK register, address 0x14 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RANDOM_CHK[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	EXTRW							

Table 134. RANDOM_CHK register bit description

Bit	Symbol	Description	
7 to 0	RANDOM_CHK[7:0]	Secure Write Register	
		All settings	See Section 12.7.5.2
		Reset condition	POR

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

14.2.21 RANDOM_GEN register

Table 135. RANDOM_GEN register, address 0x15 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RANDOM_GEN[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	RO							

Table 136. RANDOM_GEN register bit description

Bit	Symbol	Description	
7 to 0	RANDOM_GEN[7:0]	Secure write register	
		All settings	See Section 12.7.5.2
		Reset condition	POR

14.2.22 WD_CTRL1 register

Table 137. WD_CTRL1 register, address 0x16 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	WD_MAX_ERROR[1:0]		WD_DURATION[3:0]				WD_STBY_EN	WD_EN
Reset	0	0	0	0	0	0	0	0
Access	RWOTP		RWOTP				RWOTP	RWOTP

Table 138. WD_CTRL1 register bit description

Bit	Symbol	Description	
6 to 7	WD_MAX_ERROR[1:0]	Watchdog maximum error count	
		All settings	See Table 44
		Reset condition	POR

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 138. WD_CTRL1 register bit description...*continued*

Bit	Symbol	Description	
5 to 2	WD_DURATION[3:0]	Watchdog window duration selection	
		All settings	See Table 43
		Reset condition	POR
1	WD_STBY_EN	Watchdog timer STANDBY enable control	
		1b'0	Watchdog timer disabled in STANDBY
		1b'1	Watchdog timer enabled in STANDBY
		Reset condition	POR
0	WD_EN	Watchdog timer enable control	
		1b'0	Watchdog timer disabled
		1b'1	Watchdog timer enabled
		Reset condition	POR

14.2.23 WD_SEED register

Table 139. WD_SEED register, address 0x17 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	WD_SEED[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	RO							

Table 140. WD_SEED register bit description

Bit	Symbol	Description	
7 to 0	WD_SEED[7:0]	Watchdog timer seed value	
		WD_SEED[7:0]	WD_ANSWER[7:0]
		Reset condition	POR

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

14.2.24 WD_ANSWER register

Table 141. WD_ANSWER register, address 0x18 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	WD_ANSWER[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	EXTRW							

Table 142. WD_ANSWER register bit description

Bit	Symbol	Description	
7 to 0	WD_ANSWER[7:0]	Watchdog answer register	
		WD_ANSWER[7:0]	Refer to Section 13.6
		Reset condition	POR

14.2.25 FLT_CNT1 register

Table 143. FLT_CNT1 register, address 0x19 bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	FAULT_CNT[3:0]				WD_ERROR_CNT[3:0]			
Reset	0	0	0	0	0	0	0	0
Access	RO				RO			

Table 144. FLT_CNT1 register bit description

Bit	Symbol	Description	
7 to 4	FAULT_CNT[3:0]	Fault counter value	
		FAULT_CNT[3:0]	Numerical count of the fault counter. See Section 12.5
		Reset condition	POR, Change FAULT_MAX_CNT[2:0], Write 1 to FLT_CNT_CLR

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 144. FLT_CNT1 register bit description...*continued*

Bit	Symbol	Description	
3 to 0	WD_ERROR_CNT[3:0]	Watchdog error count value	
		WD_ERROR_CNT[3:0]	See Section 15.6
		Reset condition	POR

14.2.26 FLT_CNT2 register

Table 145. FLT_CNT2 register, address 0x1A bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	FLT_CNT_CLR	VIN_OVLO_DBNC[1:0]		VIN_OVLO_SDWN	VIN_OVLO_EN	FAULT_MAX_CNT[2:0]		
Reset	0	0	0	0	0	0	0	0
Access	WP	RWOTP	RWOTP	RWOTP	RWOTP	RWOTP		

Table 146. FLT_CNT2 register bit description

Bit	Symbol	Description	
7	FLT_CNT_CLR	Clear fault counter	
		1b'0	No action
		1b'1	Clear FAULT_CNT[3:0]
		Reset condition	POR; Self-clear
6 to 5	VIN_OVLO_DBNC[1:0]	V_{IN} OV monitor debounce selection	
		All settings	See Table 11
		Reset condition	POR
4	VIN_OVLO_SDWN	V_{IN} OV failure reaction	
		1b'0	No shutdown because of V_{IN} OV
		1b'1	Shutdown because of V_{IN} OV
		Reset condition	POR

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Table 146. FLT_CNT2 register bit description...*continued*

Bit	Symbol	Description	
3	VIN_OVLO_EN	V_{IN} overvoltage monitor enable	
		1b'0	V_{IN} OV monitor disabled
		1b'1	V_{IN} OV monitor enabled
		Reset condition	POR
2 to 0	FAULT_MAX_CNT[2:0]	Fault counter maximum setting	
		All settings	See Table 16
		Reset condition	POR

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

15 OTP programming Debug mode

The PF5300 supports OTP fuse bank configuration and debug mode through the VDDOTP/XFAILB pin. Debug mode allows the user to modify OTP mirror registers before and after powering up. This facilitates exercising different features of the PF5300 while deciding on the best configuration for a given application. This is especially useful when optimizing the SW1 compensation for the desired transient response.

When powered up in Debug mode, the following restrictions are in place:

- The PF5300 ignores TRIM_NOK and OTP_NOK flags and proceeds with power up even if they are set.
- I^2C uses standard communication with no CRC
- I^2C address is set to 0x28
- Secure write is disabled
- Watchdog timer set to Infinite period if enabled
- 100 ms stuck-at-low timer in IO_Releaseis disabled (infinite time for PGOOD release)

If the DBG_EXIT bit is set in IO_Release, INIT, RUN or STANDBY states, Debug mode is exited and restrictions arising from debug operation are removed.

15.1 Debug operation

Follow the procedure below to power up the PF5300 in Debug mode.

1. In the ULP_OFF Mode, Connect PWRON > 7.5 V. This signal is used to deactivate the XFAILB pulldown device and move the PF5300 into the LP_Off State.
2. Apply 8 V at VDDOTP pin. This step sets the I^2C address to 0x28 and disables I^2C CRC (irrespective of OTP setting).
3. Submit I^2C keys 0xAB, 0xCD, 0xEF to the TM_ENTRY[7:0] register.
4. Configure mirror registers as needed. Optionally set DBG_TMR = 1.
5. Remove 8 V supply from VDDOTP pin (connect to XFAILB pullup source).
6. Bring PWRON to between 1.4 V and 5 V and clear DBG_TMR = 0 (if set) to exit LP_Off and power up in Debug mode.

Steps 1-2 and 5-6 can occur simultaneously to enable using a single high-voltage supply for debug entry.

Note: *The user can set the DBG_TMR bit to stay in the LP_Off state to allow time for system reconfiguration from Debug-->Normal operation. This is useful if the system has analog switches to isolate XFAILB and VDDOTP nets and the switches need time to change position. The user should clear the DBG_TMR bit as described in Step 6 to exit LP_Off.*

15.2 OTP fuse programming

A permanent OTP configuration is possible by burning the OTP fuses. OTP fuse burning is performed in the LP_Off state. Contact an NXP representative for detailed information on OTP fuse programming.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

16 Functional safety

16.1 System safety strategy

The PF5300 is defined in a context of safety, and provides a set of features to achieve the safety goals in this context.

It provides a flexible yet complete safety architecture to comply with safety classifications up to ASIL D, providing full programmability to enable or disable features to address the safety goals. This architecture includes protective mechanisms to avoid unwanted modification on the respective safety features, as required by the system.

The following features are considered to be critical for the functional safety strategy:

- Internal watchdog timer and watchdog monitor (simple and challenger type)
- Output voltage monitoring with dedicated band gap reference
- CRC protection for I^2C protocol and select I^2C, OTP registers
- Input voltage monitoring with dedicated band gap reference
- Clock monitoring at startup and during normal operation
- Analog built-in self-test (ABIST) on voltage monitors

Refer to the PF5300 safety manual for complete details of the safety operation.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

17 IC level current and timing specifications

All parameters are specified at Ta = -40 °C to 125 °C, PVIN = V_{IN} = 3.3 V, PWRON = 1.8 V, no load on regulator, Fsw = 2.2 MHz, typical external component values, unless otherwise noted. Typical values are specified at 25 °C, unless otherwise noted.

Table 147. Iq and timing specifications

Symbol	Parameter	Min	Typ	Max	Unit
IULPOFF	Quiescent Current, PWRON = 0 (ULP_OFF Mode)	—	1.5	25	µA
IRUN	Quiescent Current, PWRON = 1, (RUN state, PWM Mode)	—	—	60	mA
ISTANDBY	Quiescent Current, PWRON = 1, (Standby state, PFM mode, STBY_MODE = 0b01, 100 kHz clock only, -40 ℃ to 85℃)[1]	—	250	350	µA
TSTART	Startup time (PWRON = 1 to PGOOD = 1) MPF53BDAMMA1ES OTP Configuration	—	—	500	µs

[1] Guaranteed by design.

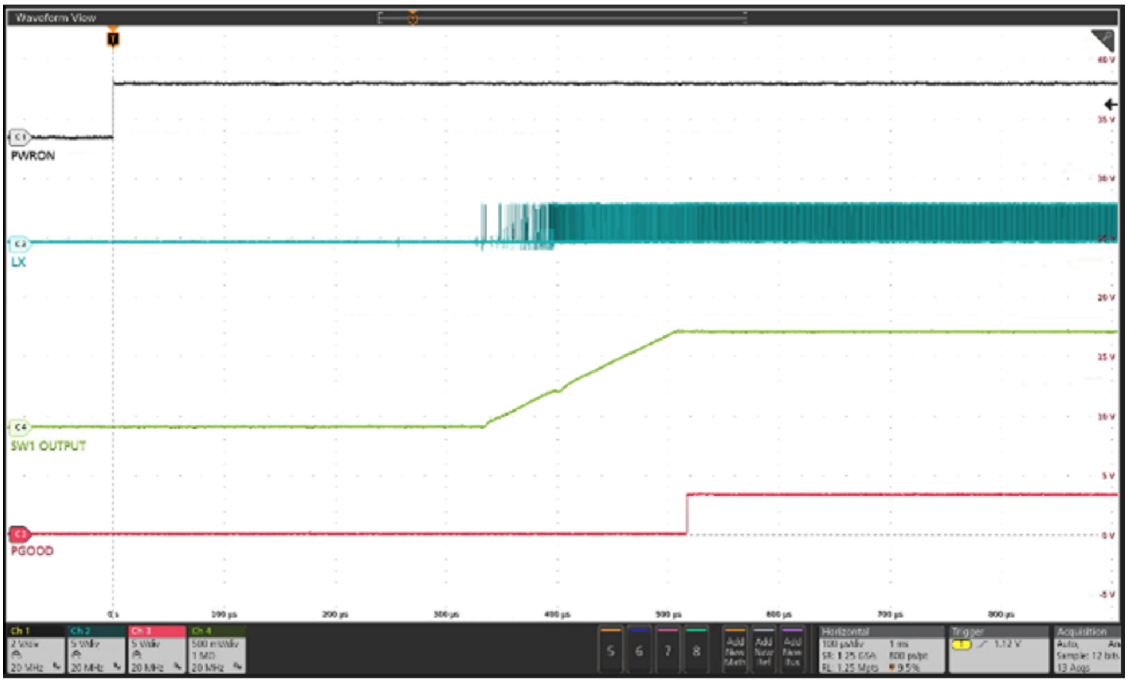
All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

18 Typical performance curves

These parameters and hardware were used to obtain graphical data for typical performance curves, unless otherwise noted:

- V_{IN} = PVIN = 3.3 V
- V_{OUT} = 0.8 V
- Switching frequency = 2200 kHz
- Hardware: KITPF5300FRDMEVM
- Temperature = 25 ℃
- Inductor =100 nH HPL505028FR10MRD3P
- Output capacitor = 8 x 22 µF



aaa-050535

Figure 24. SW1 soft-start (MPF53BDAMMA1ES); 100 µs/DIV

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

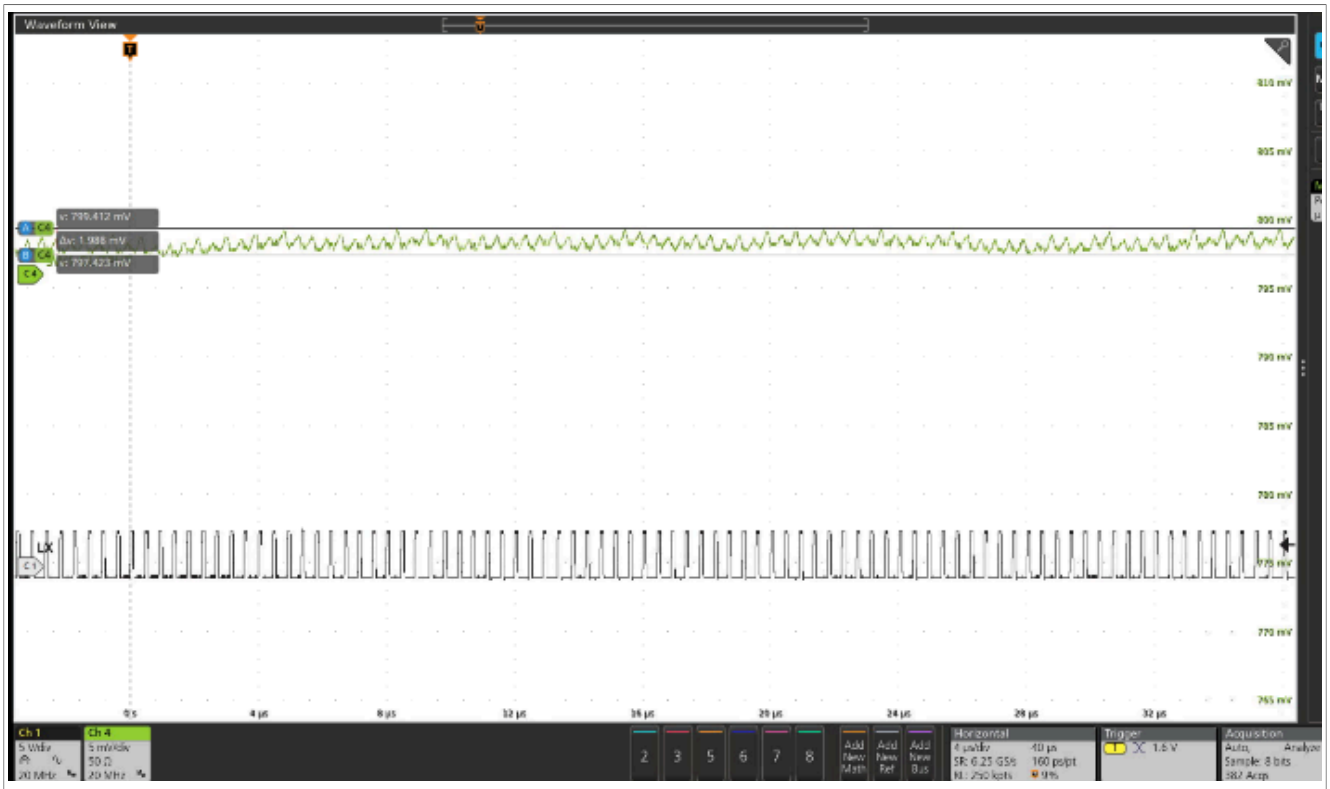


Figure 25. SW1 output ripple (MPF53BDAMMA1ES) ~ 3 mV

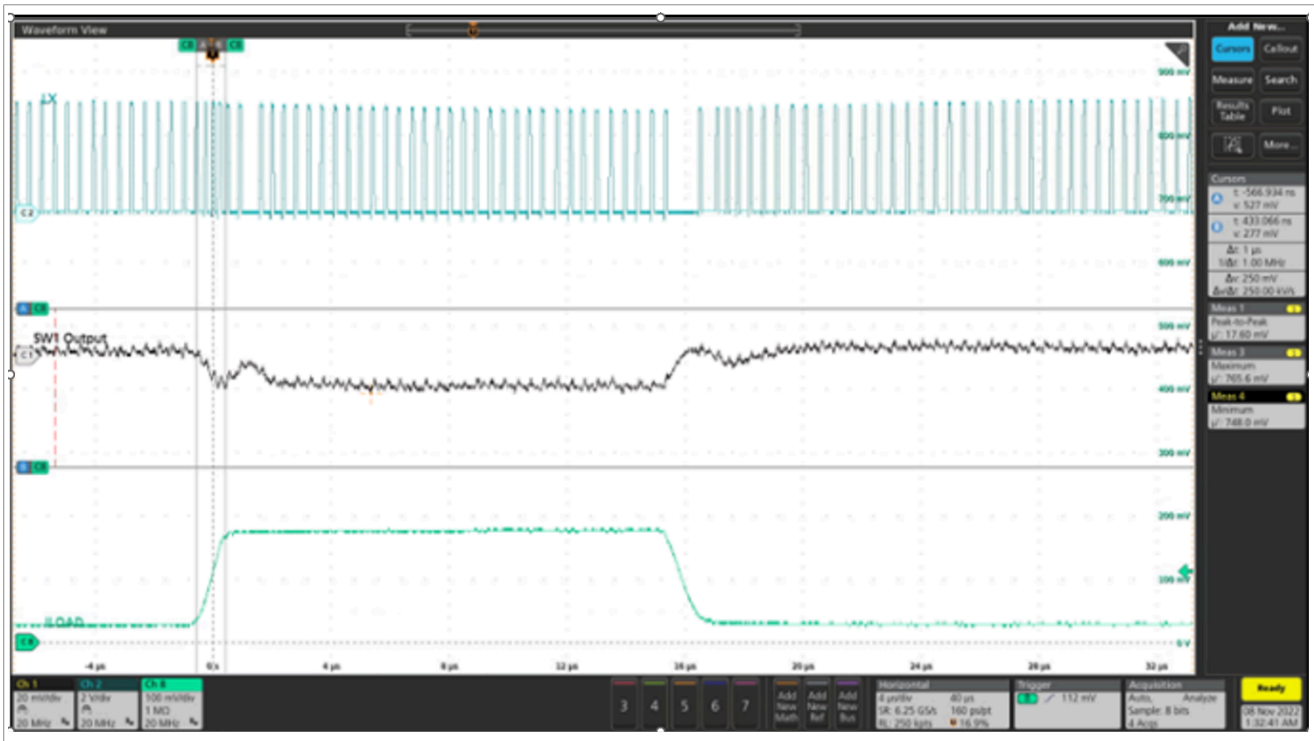


Figure 26. SW1 load transient response with AVP

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

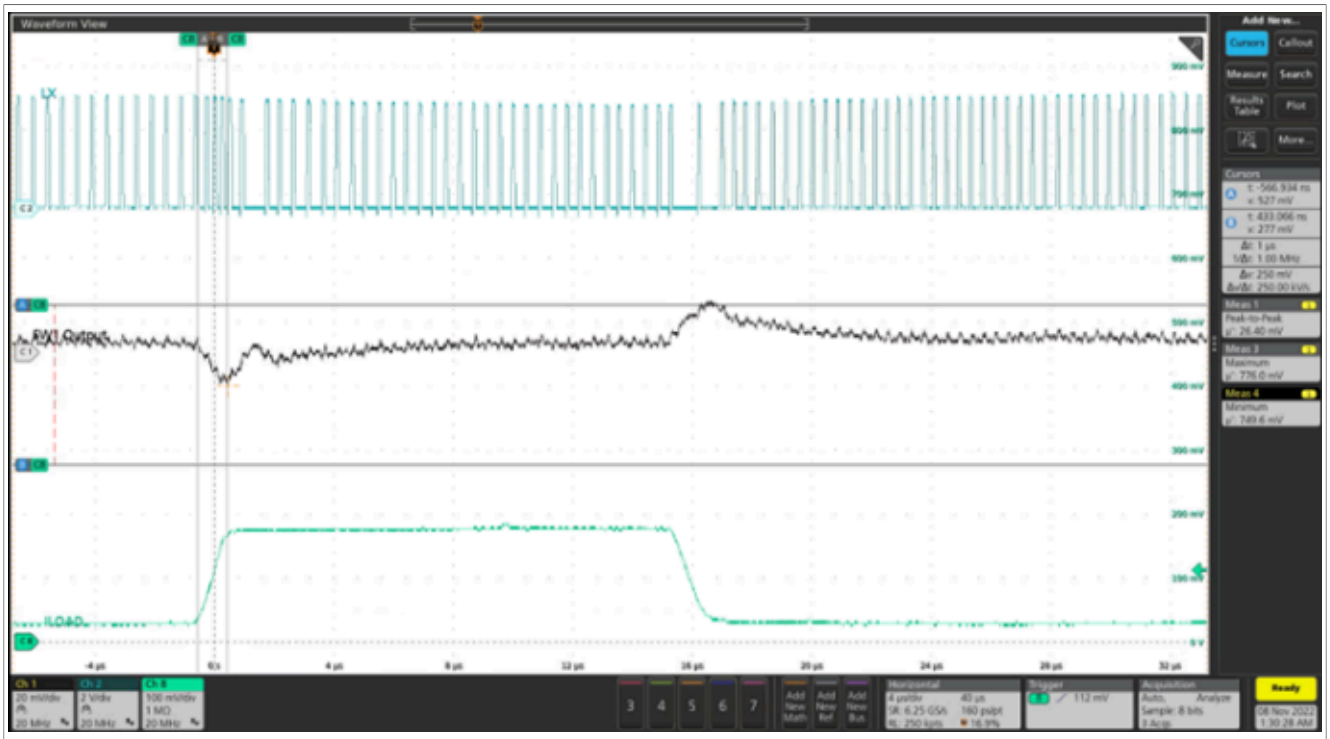


Figure 27. SW1 load transient response without AVP

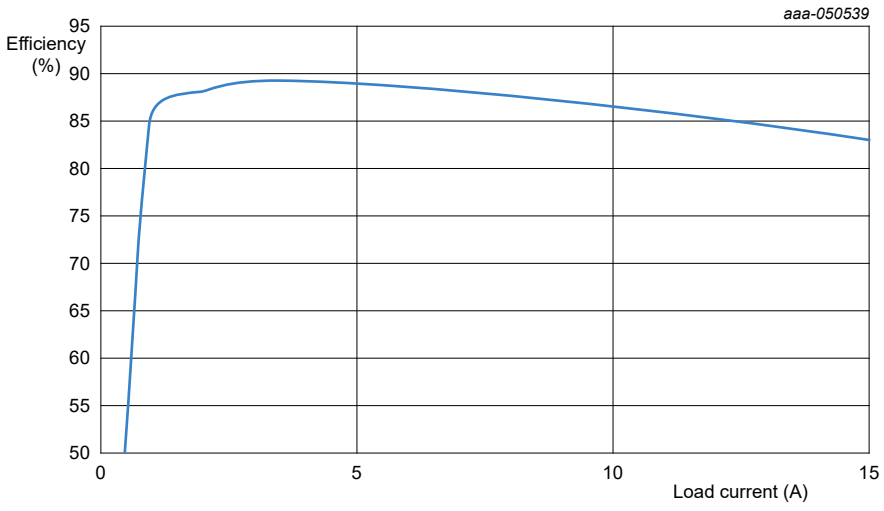


Figure 28. PWM efficiency, V_{out} = 1.0 V

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

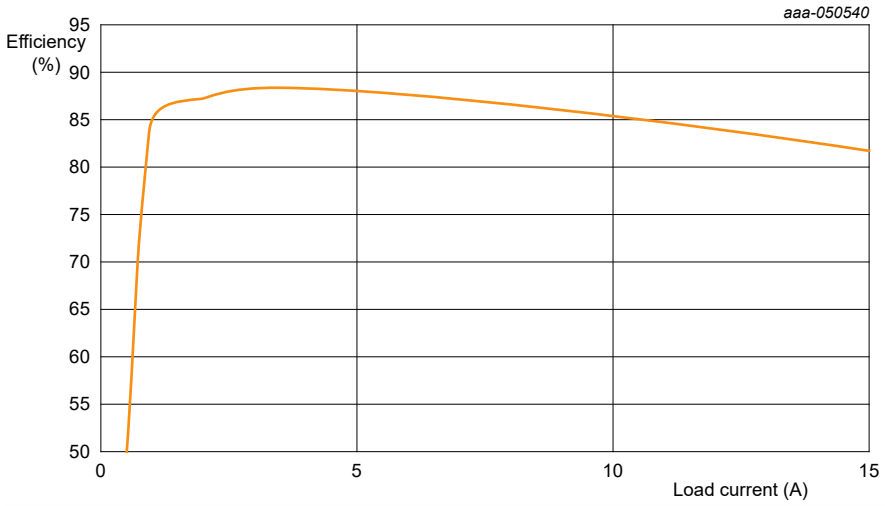


Figure 29. PWM efficiency, V_{out} = 0.9 V

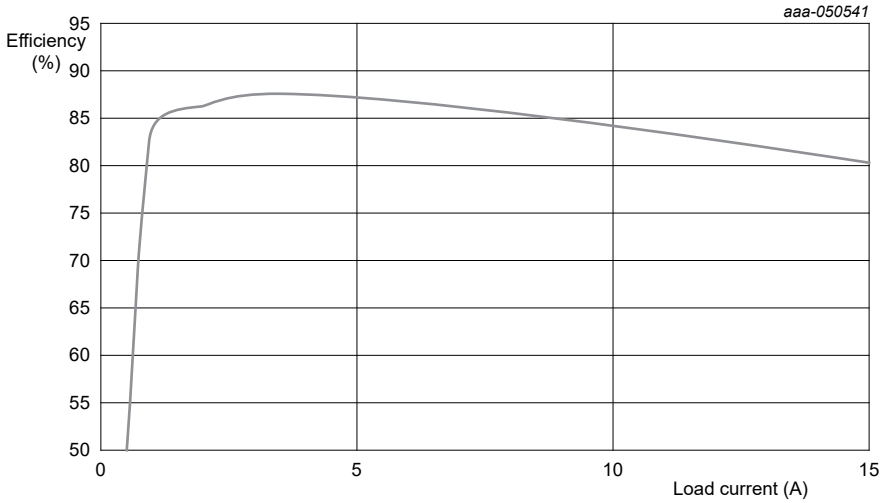


Figure 30. PWM efficiency, V_{out} = 0.8 V

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

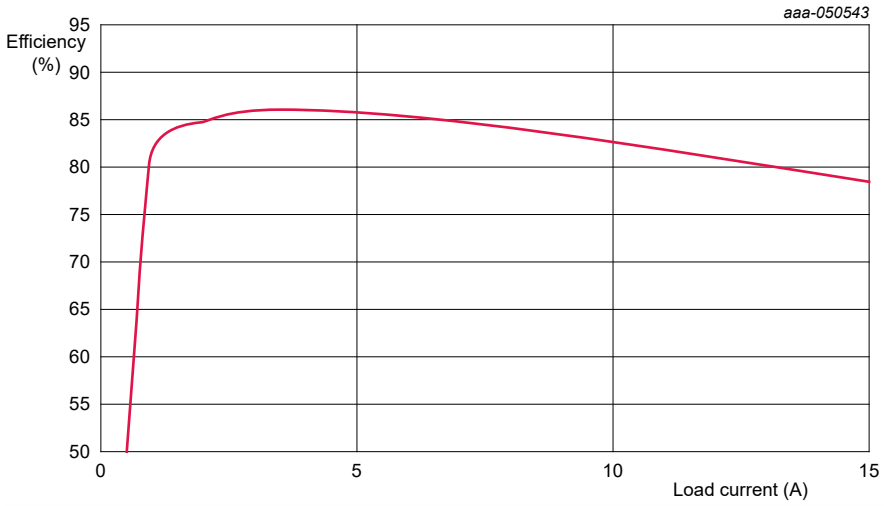


Figure 31. PWM efficiency, V_{out} = 0.7 V

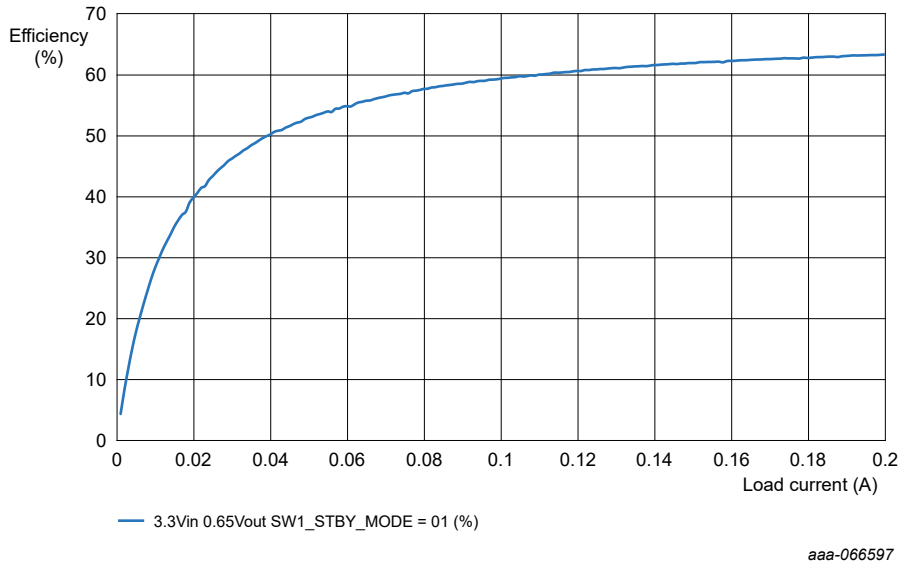


Figure 32. PFM Mode 3.3 Vin 0.65 Vout

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

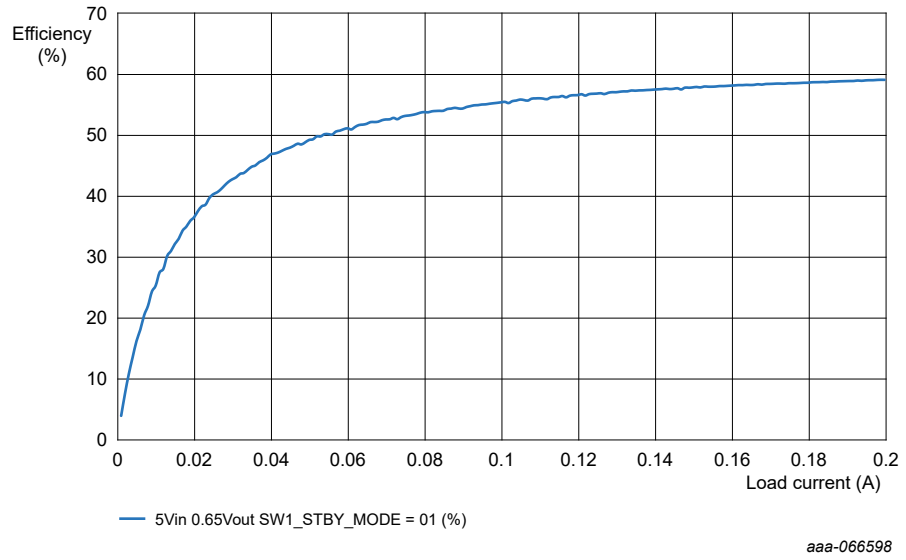


Figure 33. PFM Mode 5 Vin 0.65 Vout

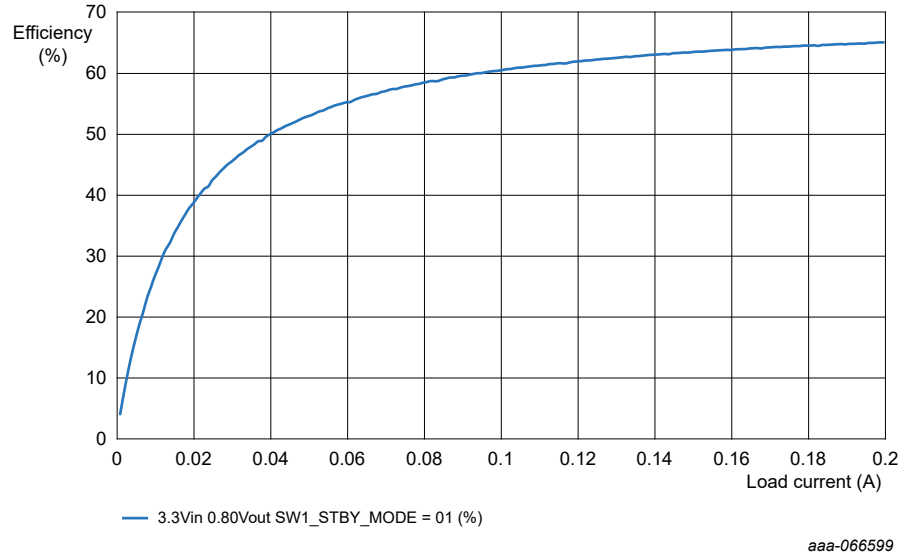


Figure 34. PFM Mode 3.3 Vin 0.80 Vout

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

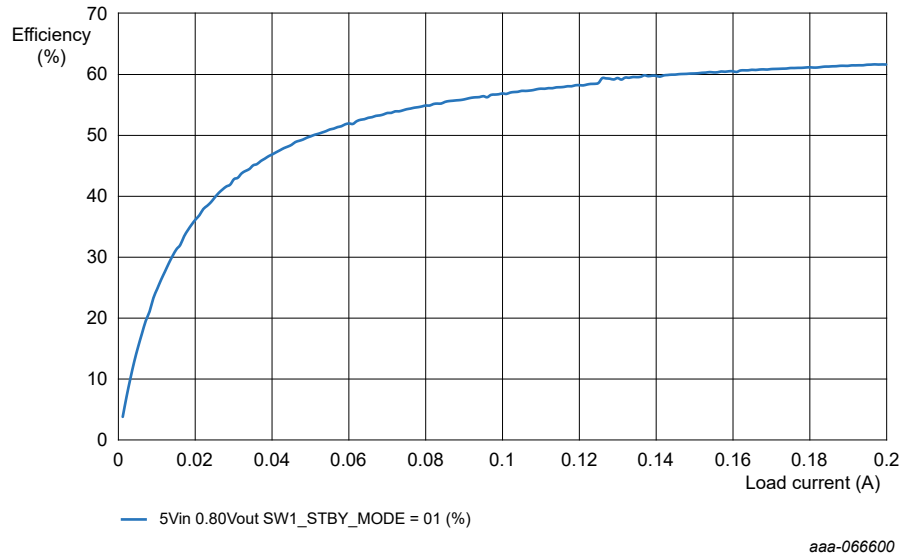


Figure 35. PFM Mode 5 Vin 0.80 Vout

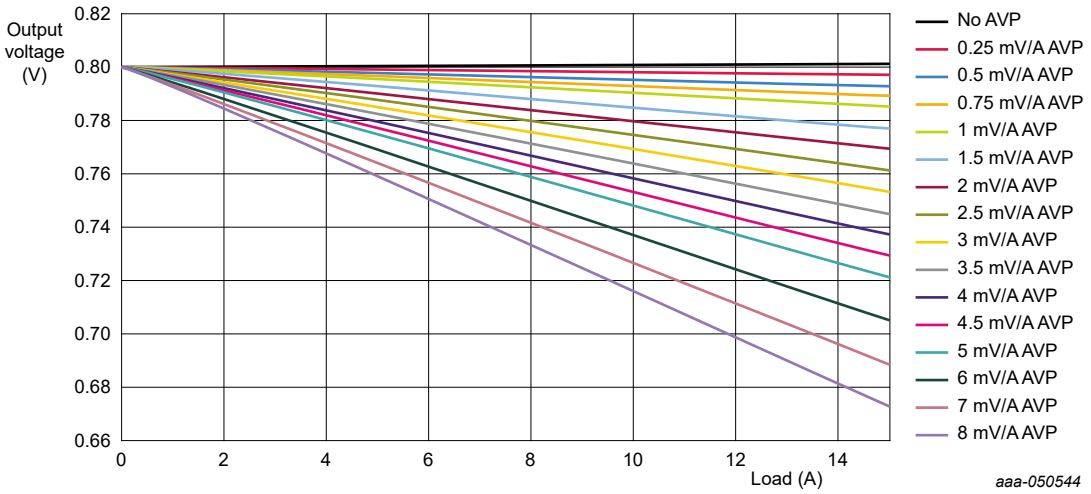
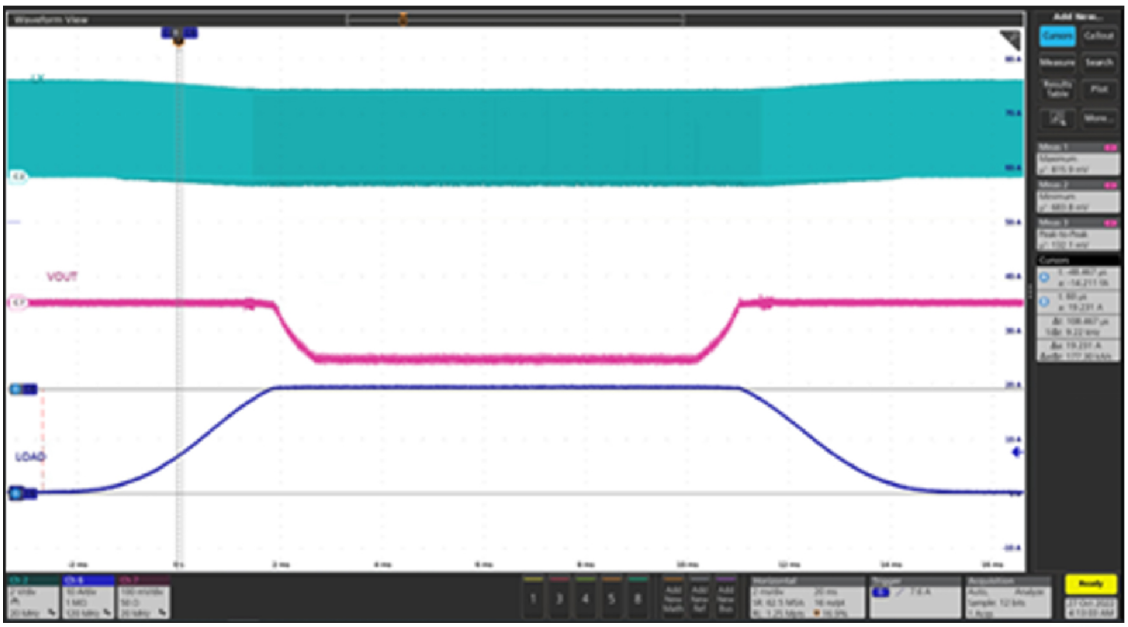


Figure 36. SW1 load regulation at different AVP settings

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.



aaa-050545

Figure 37. SW1 current limit entry and exit: V_{out} drops and recovers smoothly

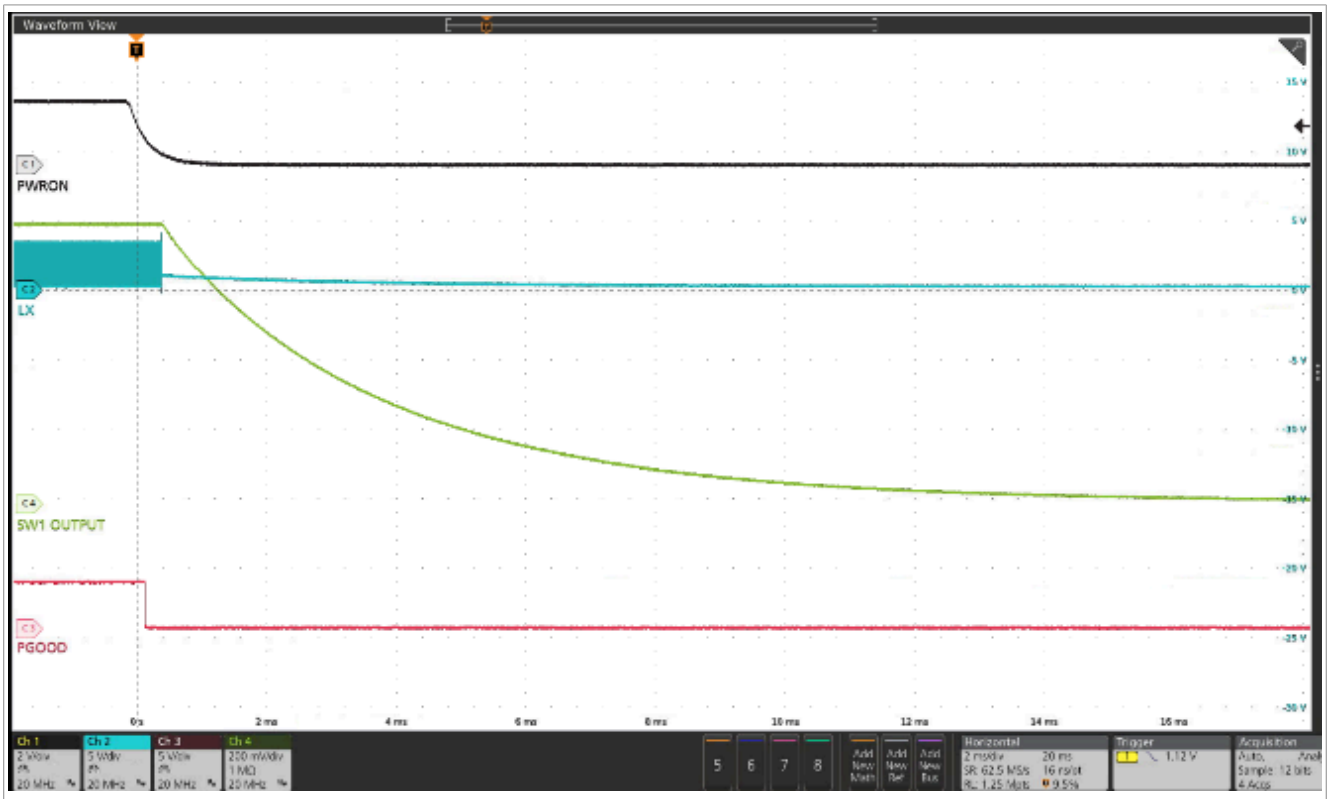


Figure 38. SW1 turn-off with OTP_SW1_RDIS = 1 and OTP_SW1_HIZOFF = 1

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

19 Schematic and layout guidelines

19.1 Schematic example

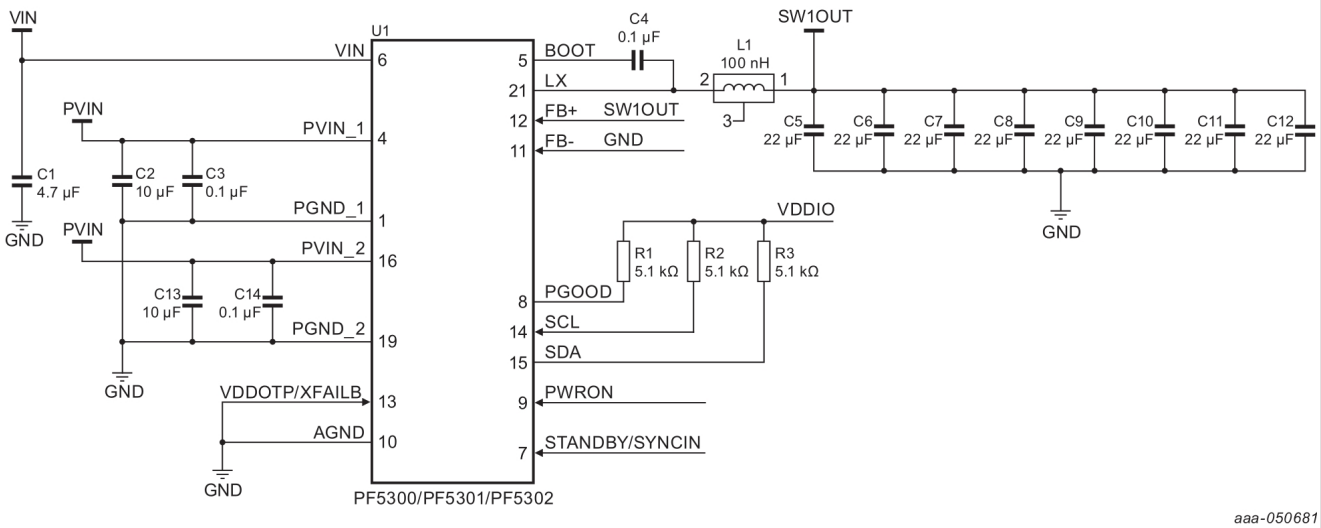


Figure 39. Typical application schematic

Figure 39 shows a typical application schematic using the PF5300/PF5301/PF5302. The VDDOTP/XFAILB pin should be grounded if the XFAILB function is not used. If the XFAILB function is used, pull it up to the XFAILB pullup supply, typically the VDIG bus of other PF PMICs in the system.

NXP recommends bypassing the PVIN pins by 0.1 µF capacitors, followed by at least 10 µF. Three terminal 0.1 µF capacitors are recommended, but not mandatory, for PVIN bypass, as they offer lower impedance compared to their two-terminal equivalent.

The FB+ and FB- nets can be routed from near the processor to compensate for voltage drop in the PCB.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

19.2 Layout guidelines

The KITPF5300FRDMEVM may be used as a guide for optimized component placement and layout. Figure 40 shows the top layout of KITPF5300FRDMEVM.

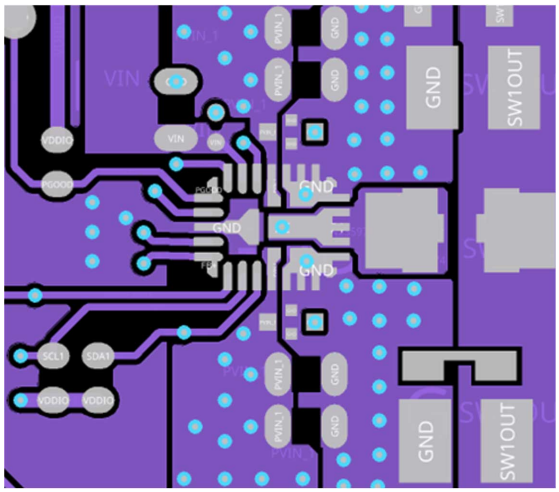


Figure 40. KITPF5300FRDMEVM top layout

PVIN bypass capacitors should be placed on either side, as close as possible to the PF5300, as shown. The loop between the PVIN-PGND pins and the bypass capacitors must be as short as possible.

NXP recommends placing the VIN bypass capacitor as the next priority, as shown. An optional additional 0.1 µF capacitor is used in KITPF5300FRDMEVM.

PVIN and VIN should not be shorted close to or directly at the pin, even though both are being supplied by a common voltage rail. They should routed separately from a common power island/plane located left of the respective decoupling capacitors. Keeping the routing separate for high-current devices prevents any PVIN noise from affecting the VIN rail, which supplies critical internal reference circuits.

The boot capacitor must be placed on the bottom layer as shown in Figure 41. The boot capacitor must be placed to minimize parasitic capacitance and coupling. Parasitic capacitance, if significant, can increase the switching time and switching losses, reducing efficiency. If alternate routing is used, it doesn't affect basic functionality. The LX node trace should be kept as small as possible.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

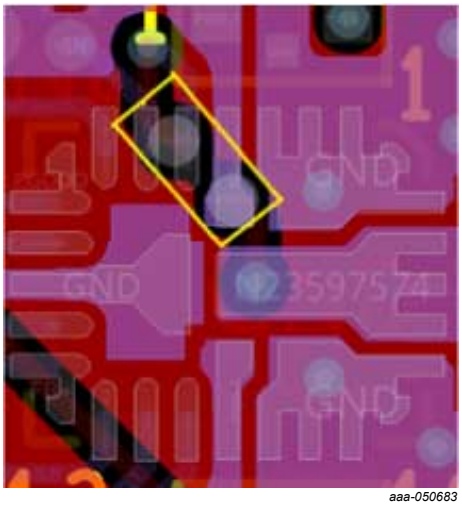


Figure 41. Boot capacitor placed at the bottom layer

The FB+ and FB- must be routed parallel to each other to minimize differential noise coupling in the feedback path. An optional 10 pF capacitor may be placed close to the pins if desired.

The AGND pin must be connected to the ground place using a via as shown in Figure 40.

The inductor must be placed close to the LX pins, and a large copper shape must be used to connect the two, to minimize conduction losses. The output capacitor placement must be optimized to achieve the desired PDN performance of the output plane. This is critical for 16 nm or lower processor nodes, to achieve the tight tolerance requirements.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

20 Package drawing

20.1 Automotive package, A

20.1.1 Package outline, A

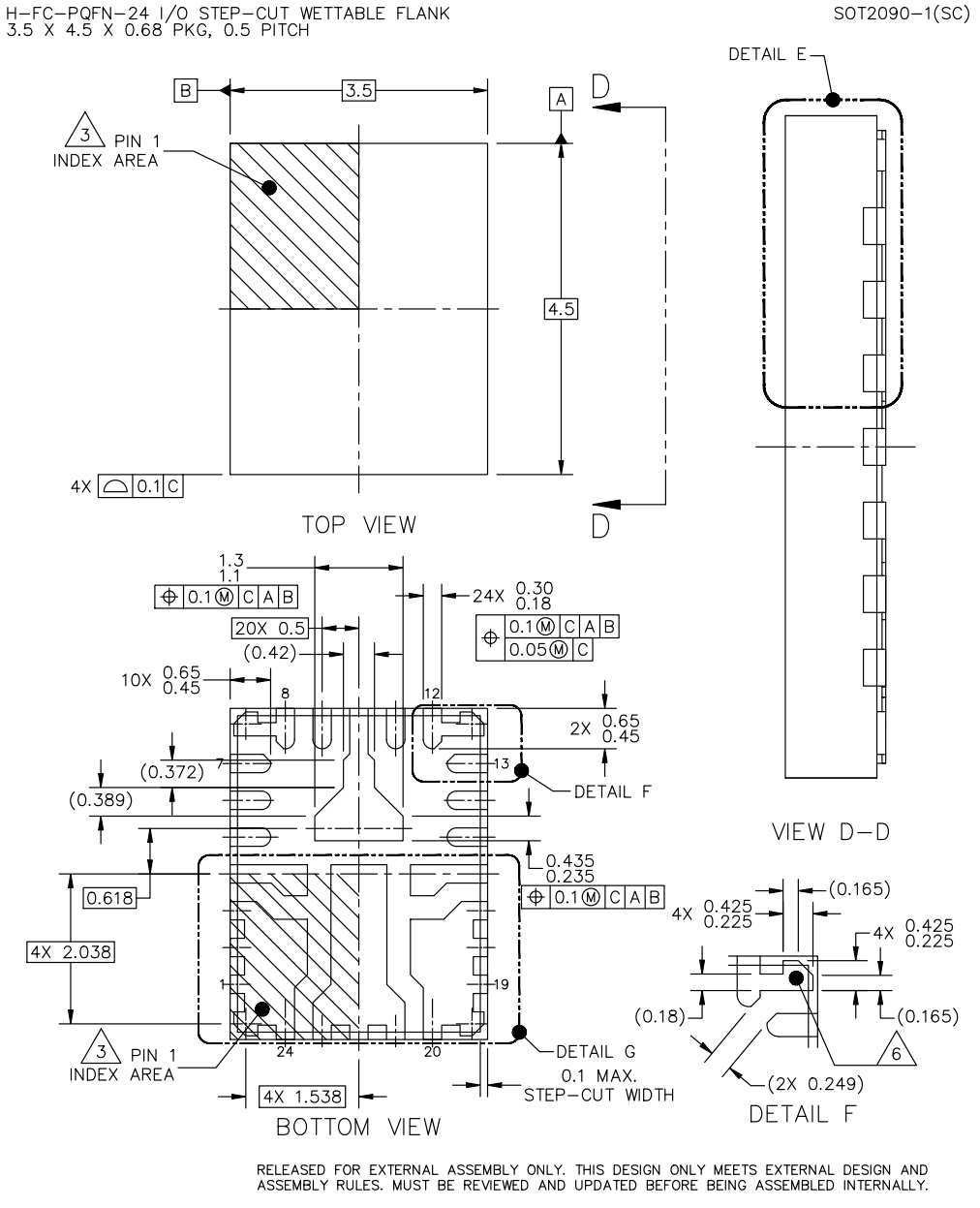


Figure 42. Package outline

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

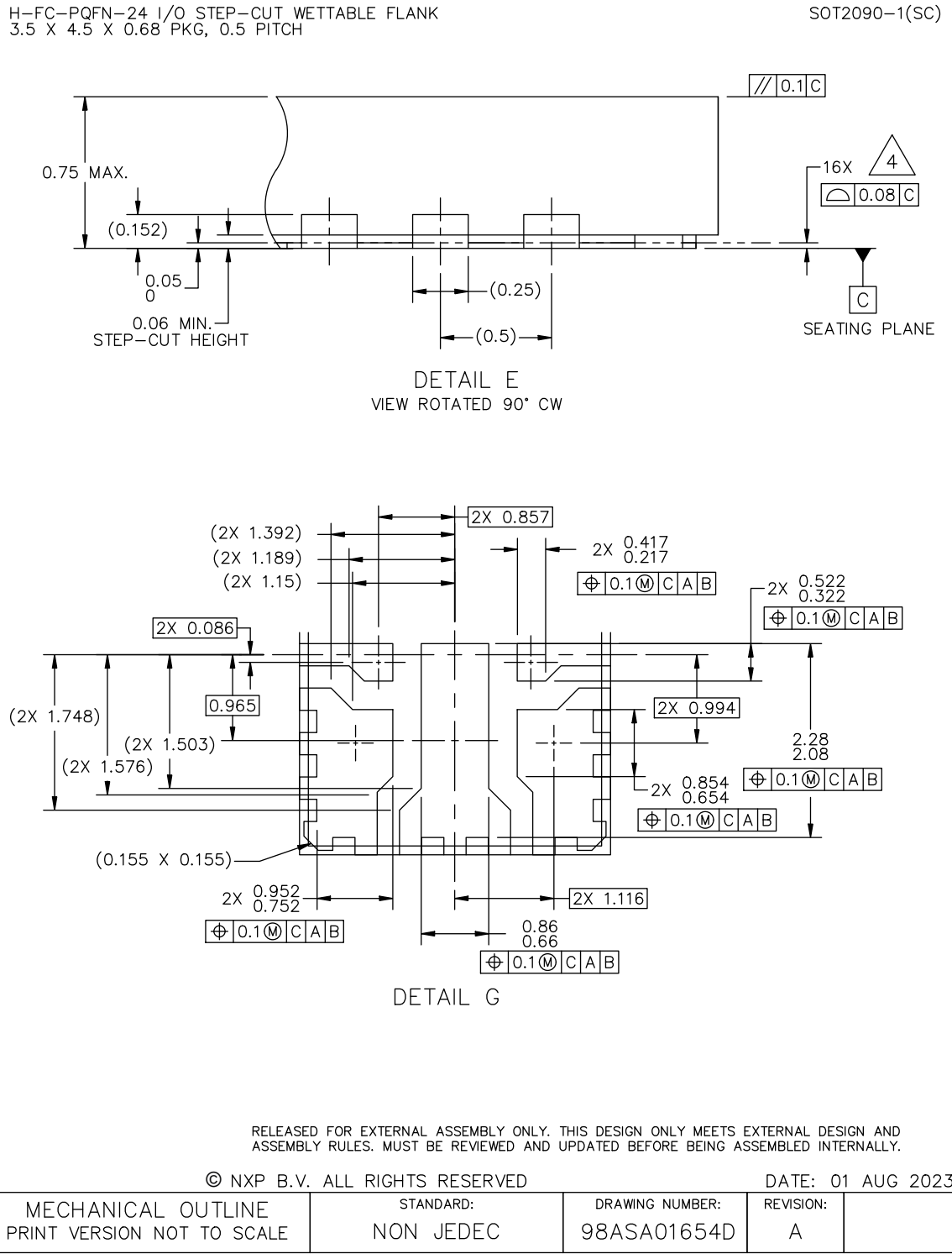


Figure 43. Package outline details

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

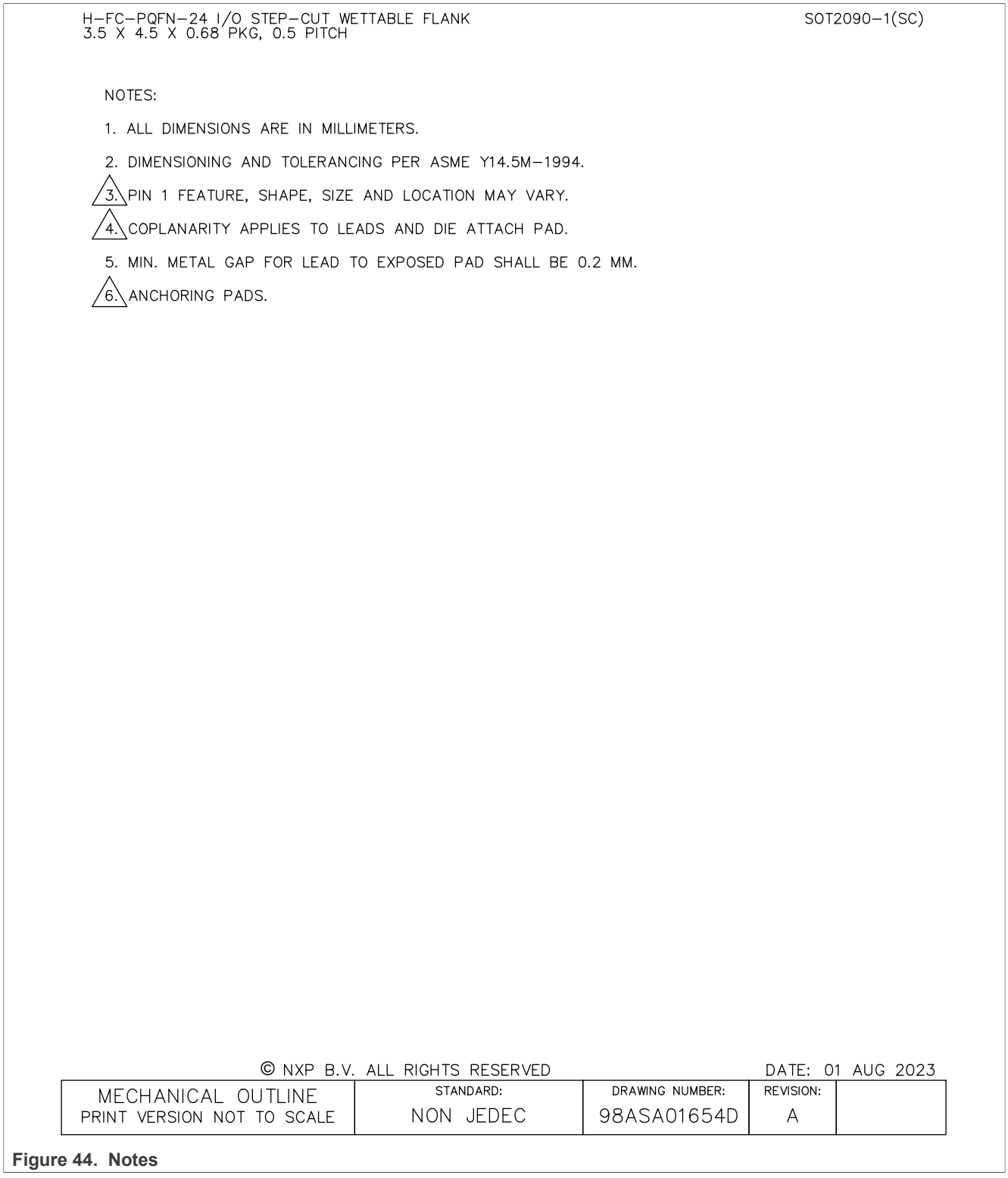


Figure 44. Notes

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

20.1.2 Soldering, A

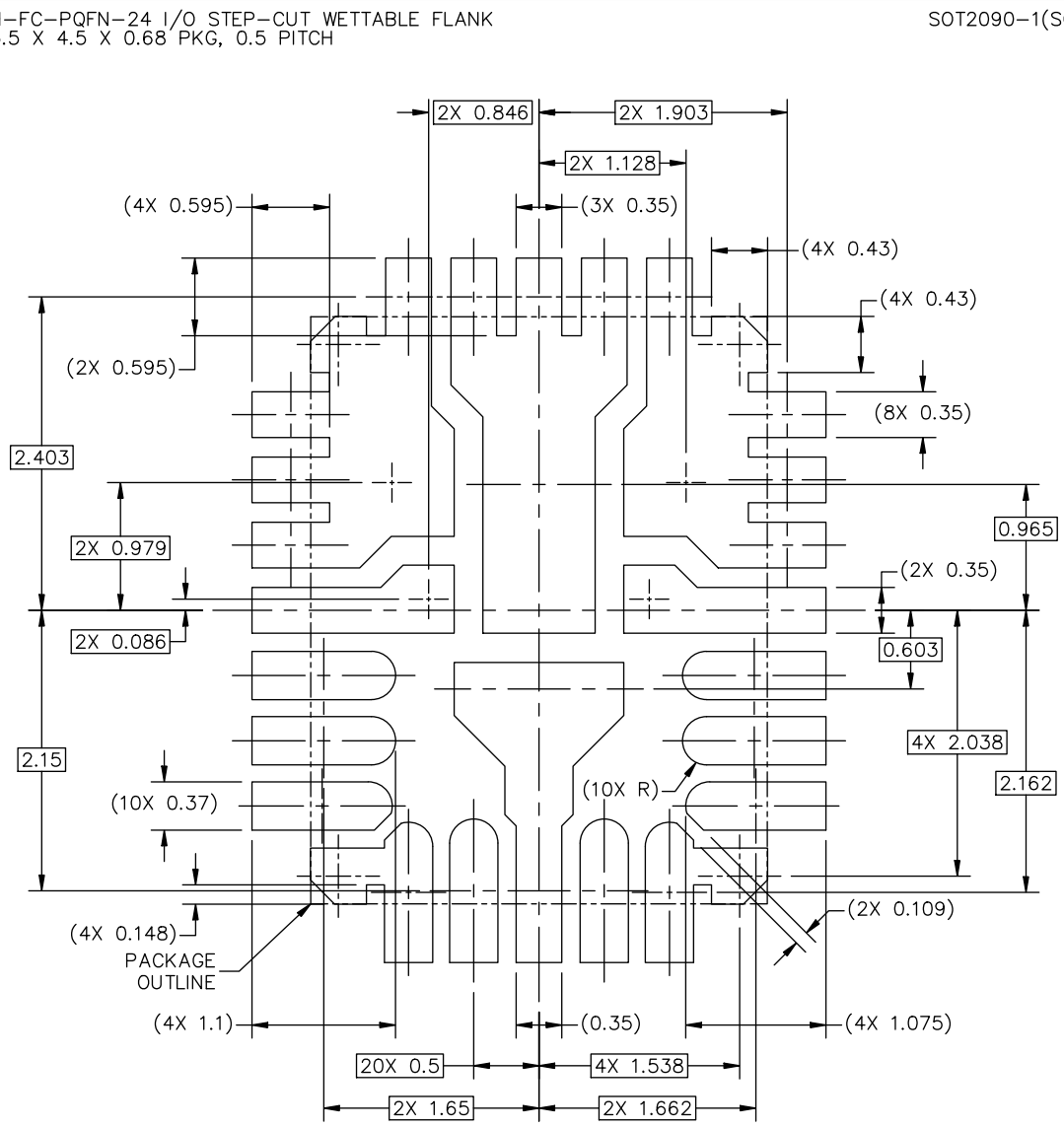
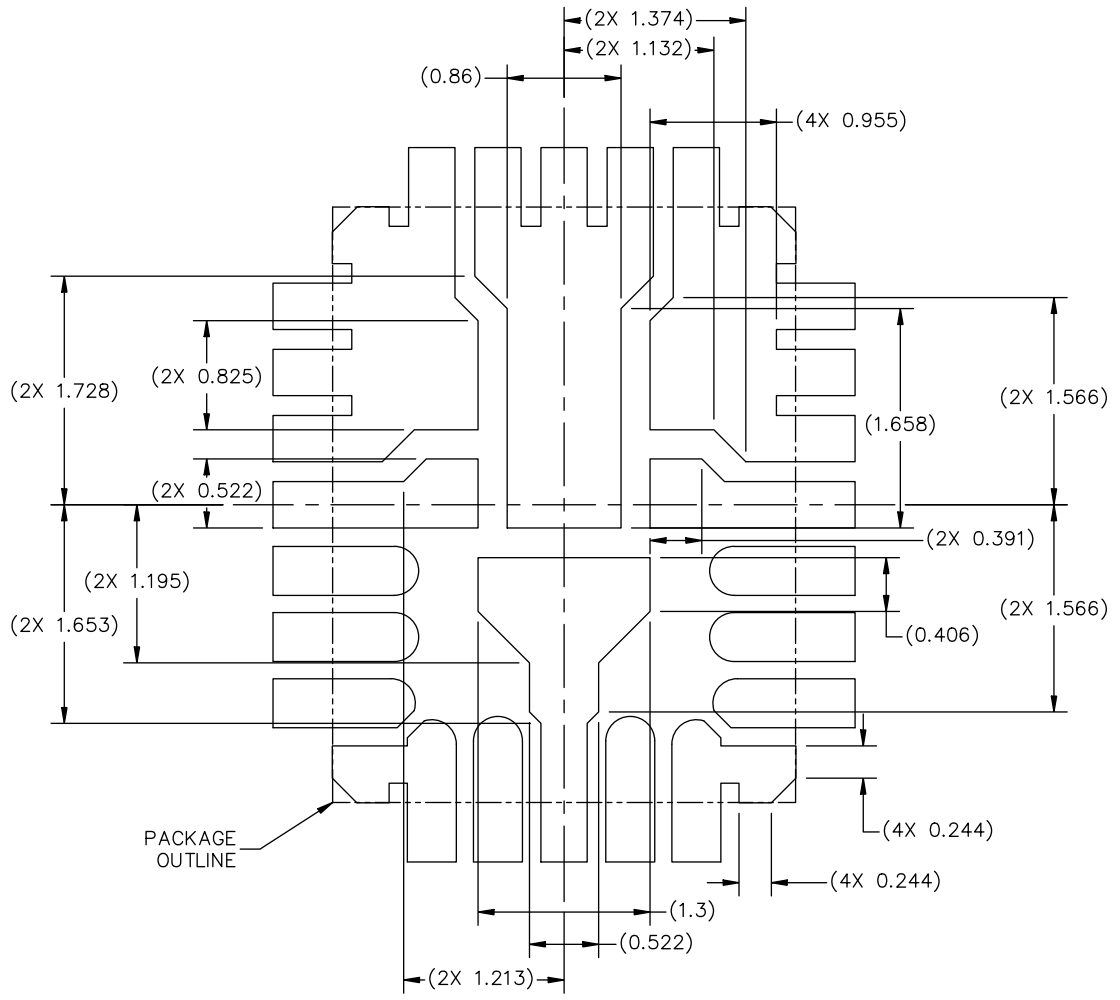


Figure 45. Reflow soldering footprint part1 for HVQFN24 (SOT2090-1(SC))

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 01 AUG 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01654D	REVISION: A	

Figure 46. Reflow soldering footprint part2 for HVQFN24 (SOT2090-1(SC))

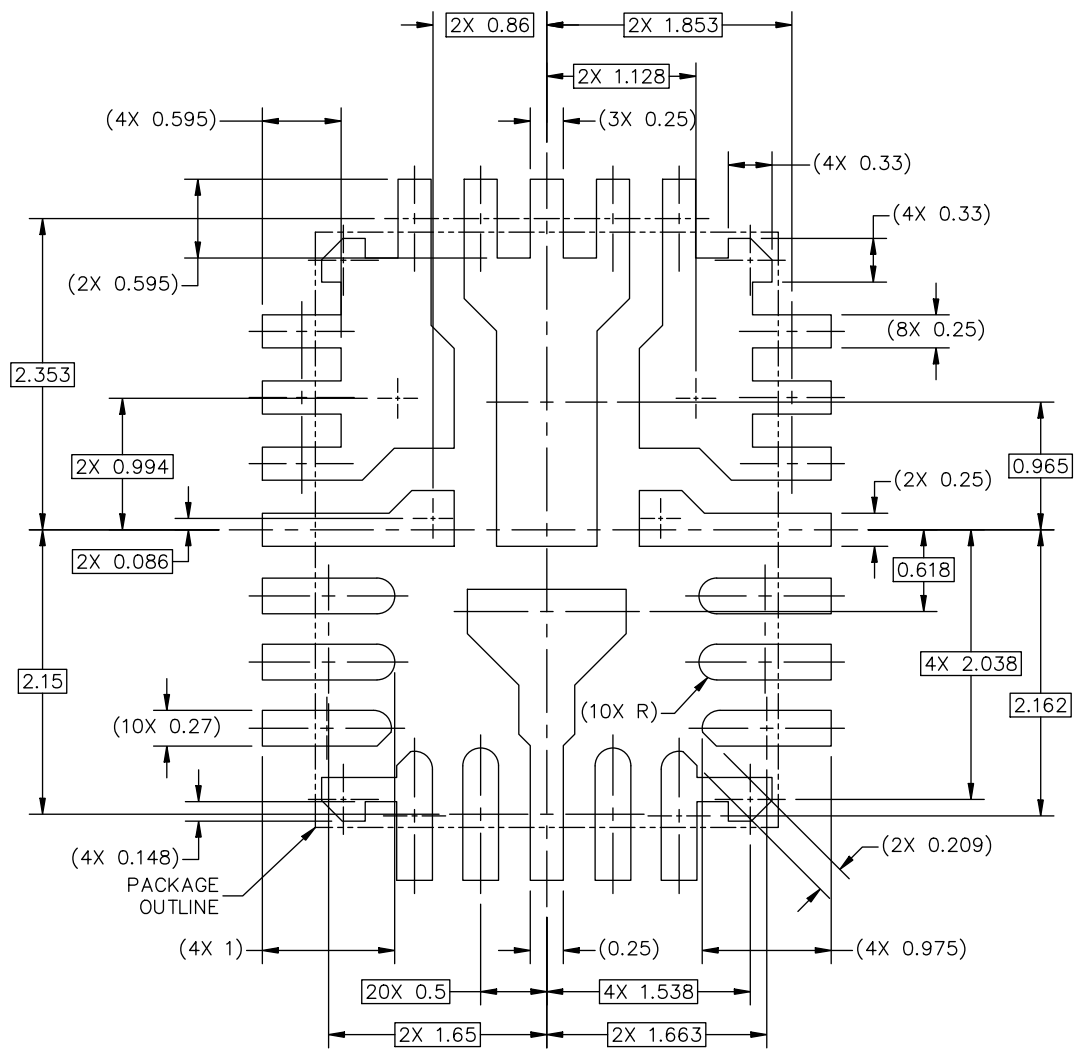
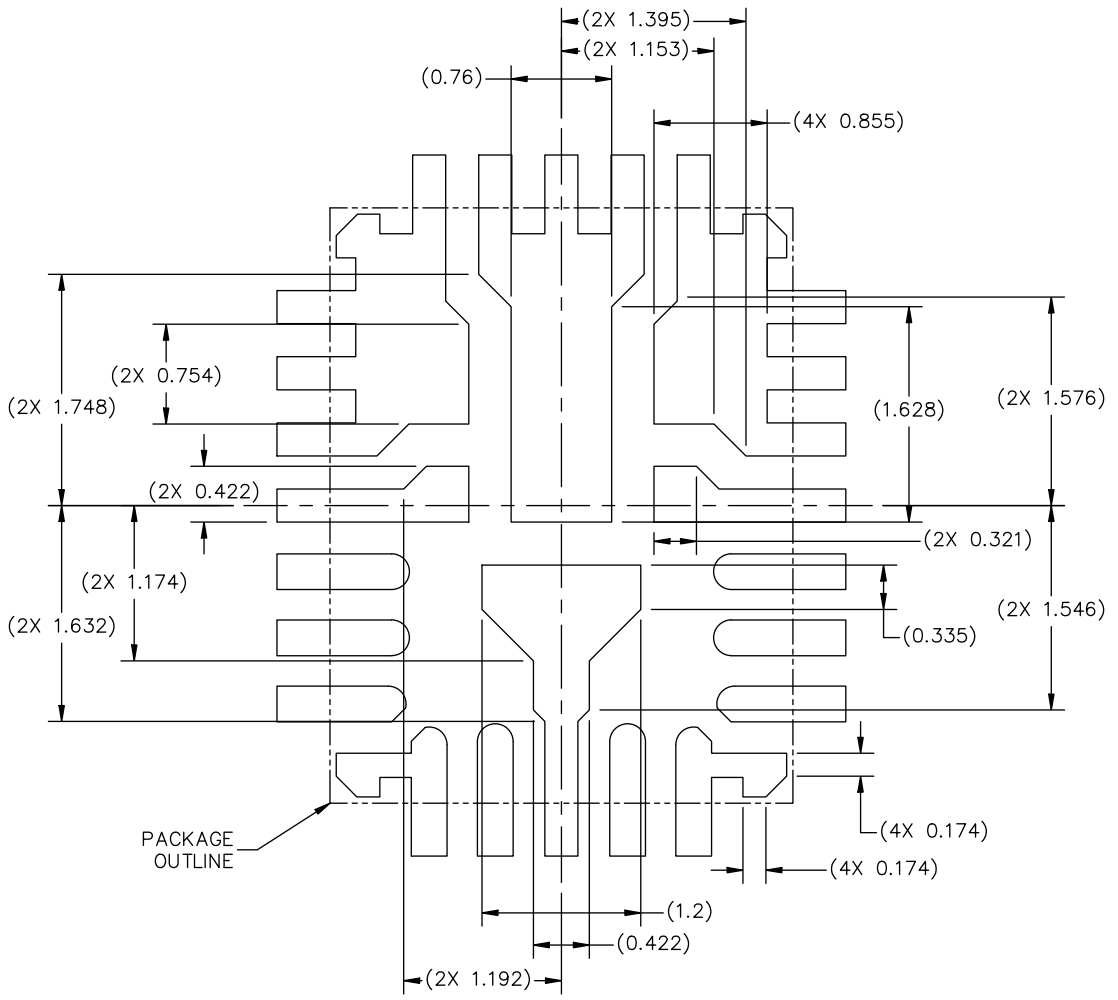


Figure 47. Reflow soldering footprint part3 for HVQFN24 (SOT2090-1(SC))

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 01 AUG 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01654D	REVISION: A	

Figure 48. Reflow soldering footprint part4 for HVQFN24 (SOT2090-1(SC))

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

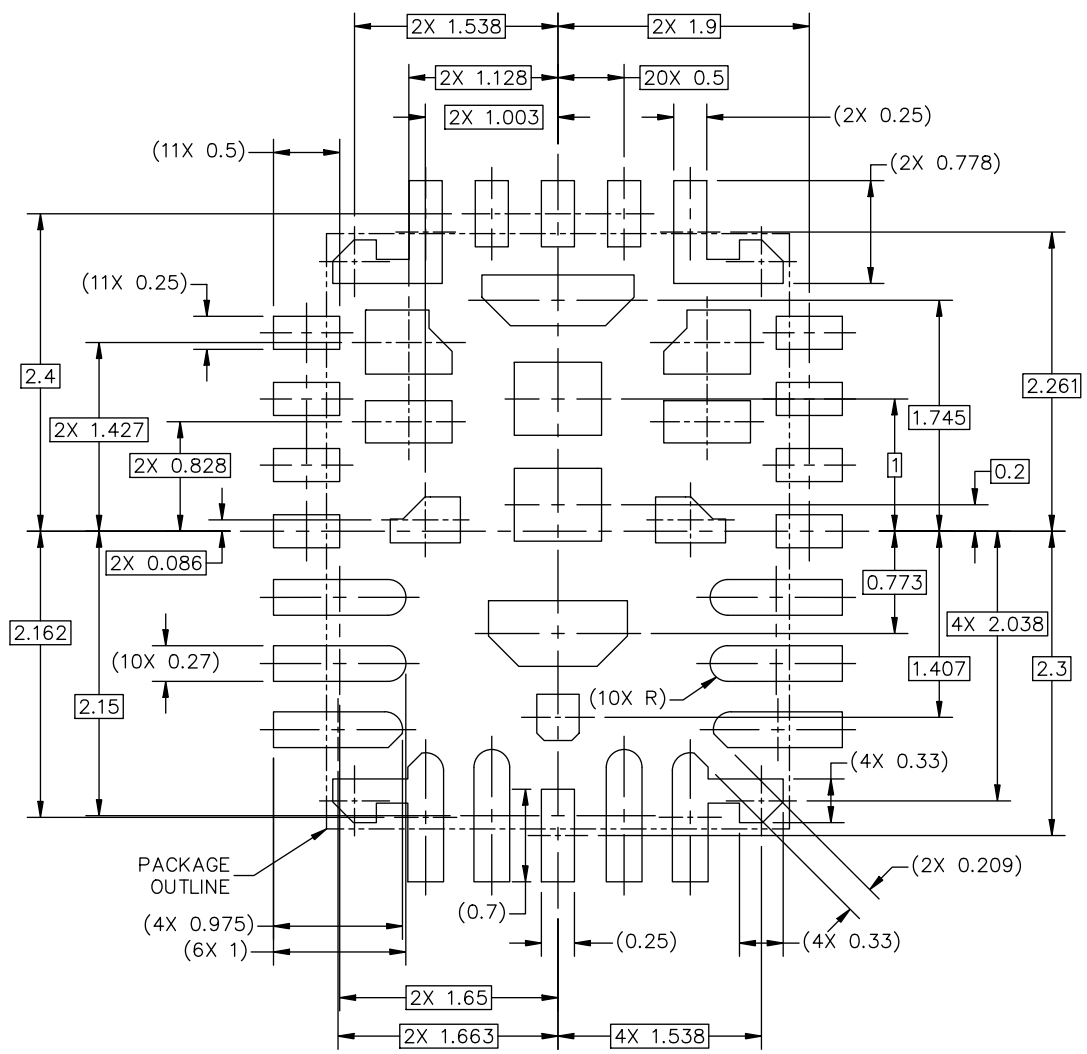


Figure 49. Reflow soldering footprint part5 for HVQFN24 (SOT2090-1(SC))

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

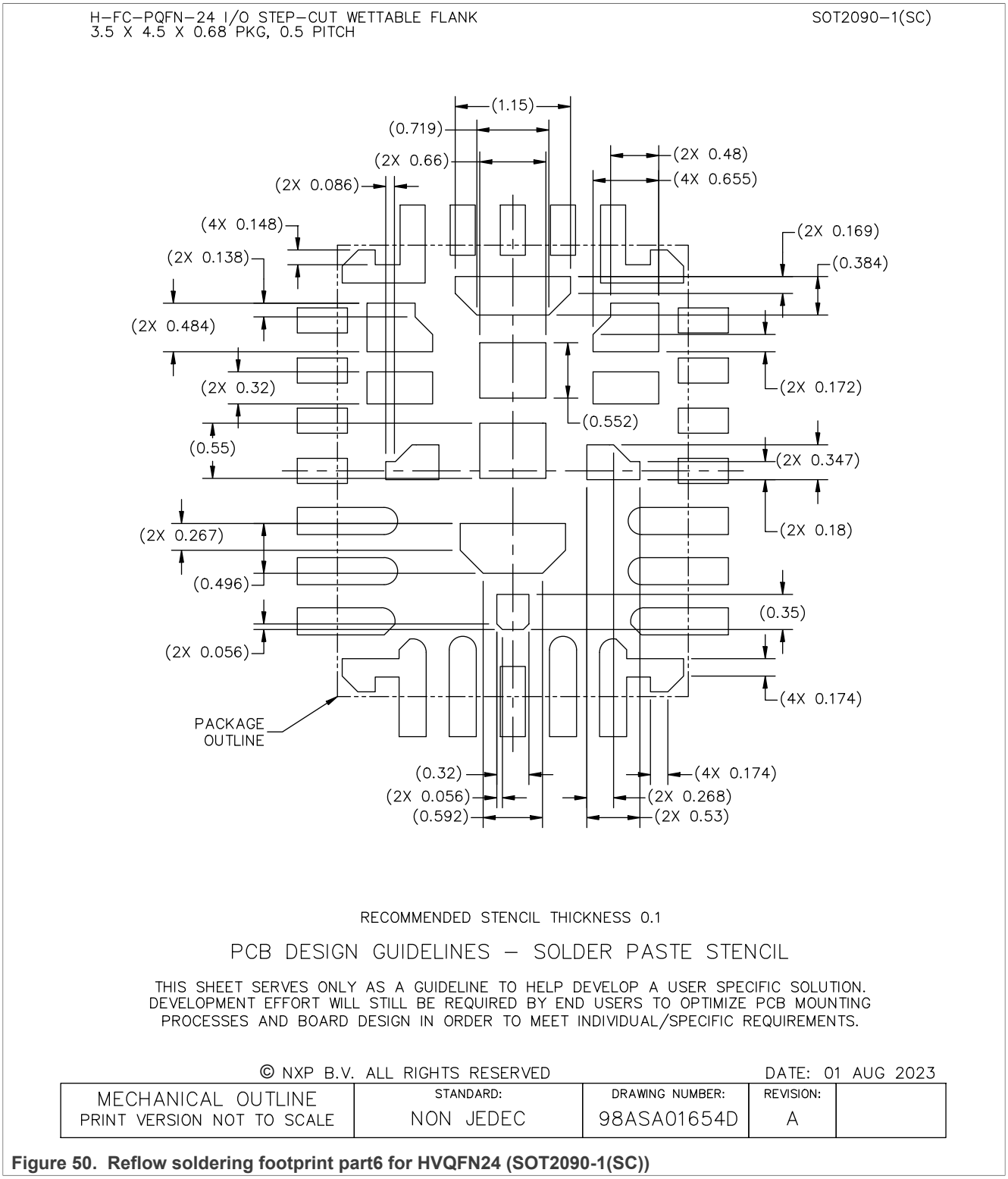


Figure 50. Reflow soldering footprint part6 for HVQFN24 (SOT2090-1(SC))

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

20.2 Industrial package, A

20.2.1 Package outline, A

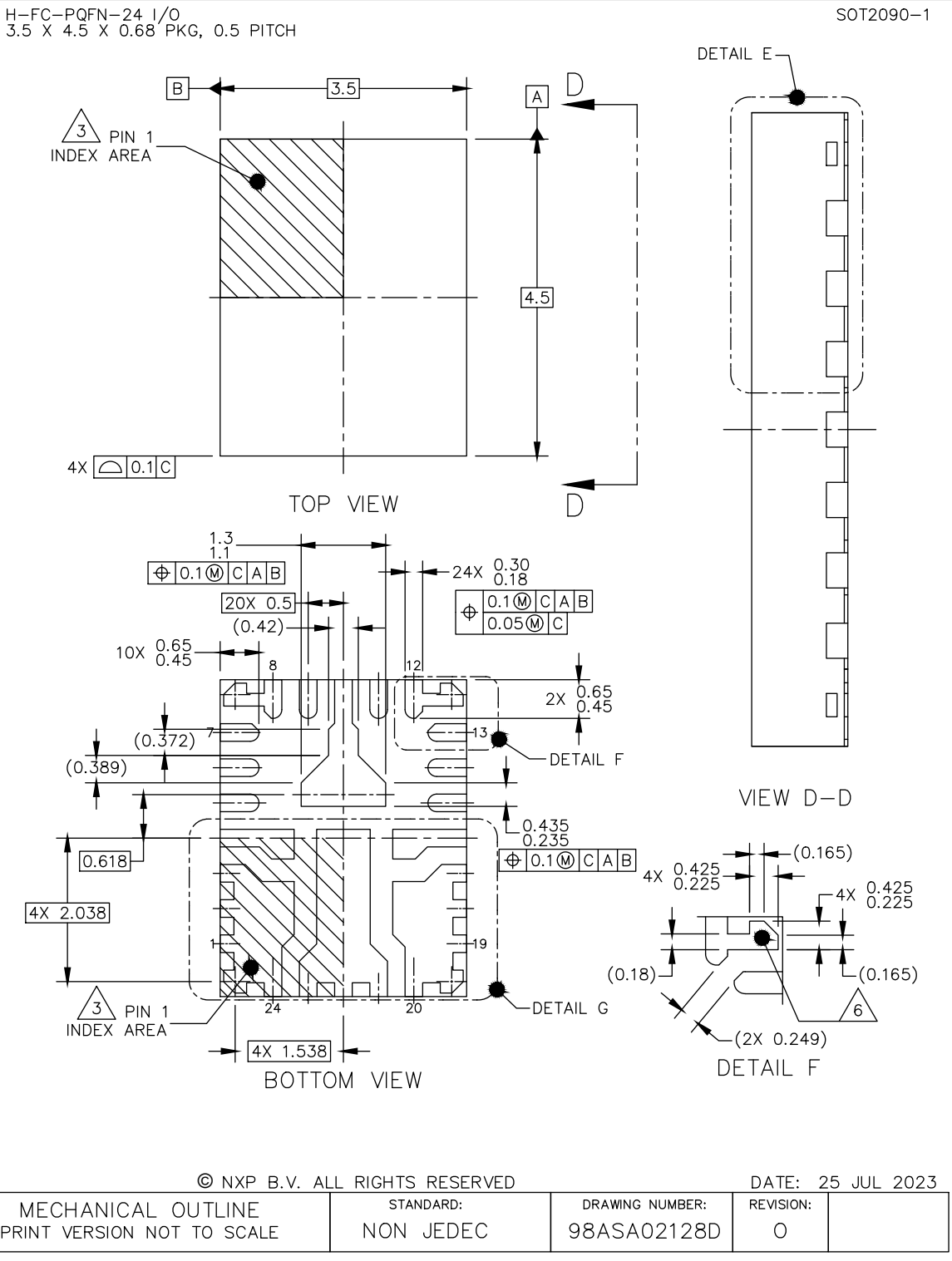


Figure 51. Package outline H-FC-PQFN24 (SOT2090-1)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

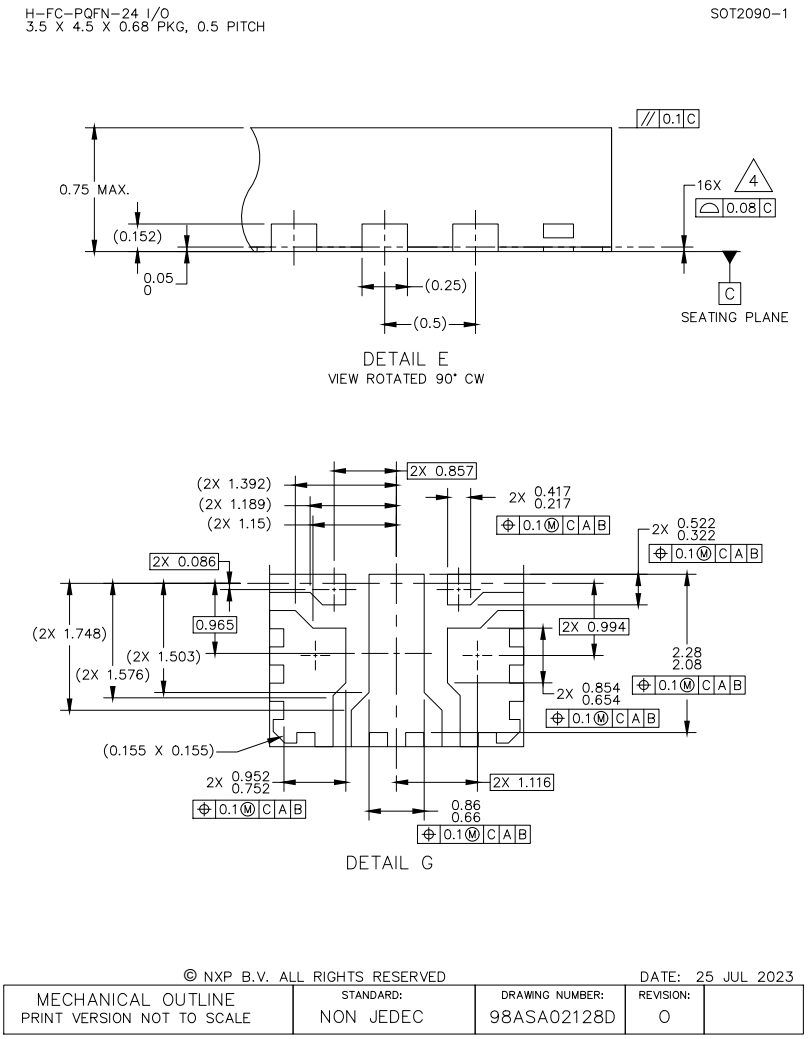


Figure 52. Package outline detail E and G of H-FC-PQFN24 (SOT2090-1)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

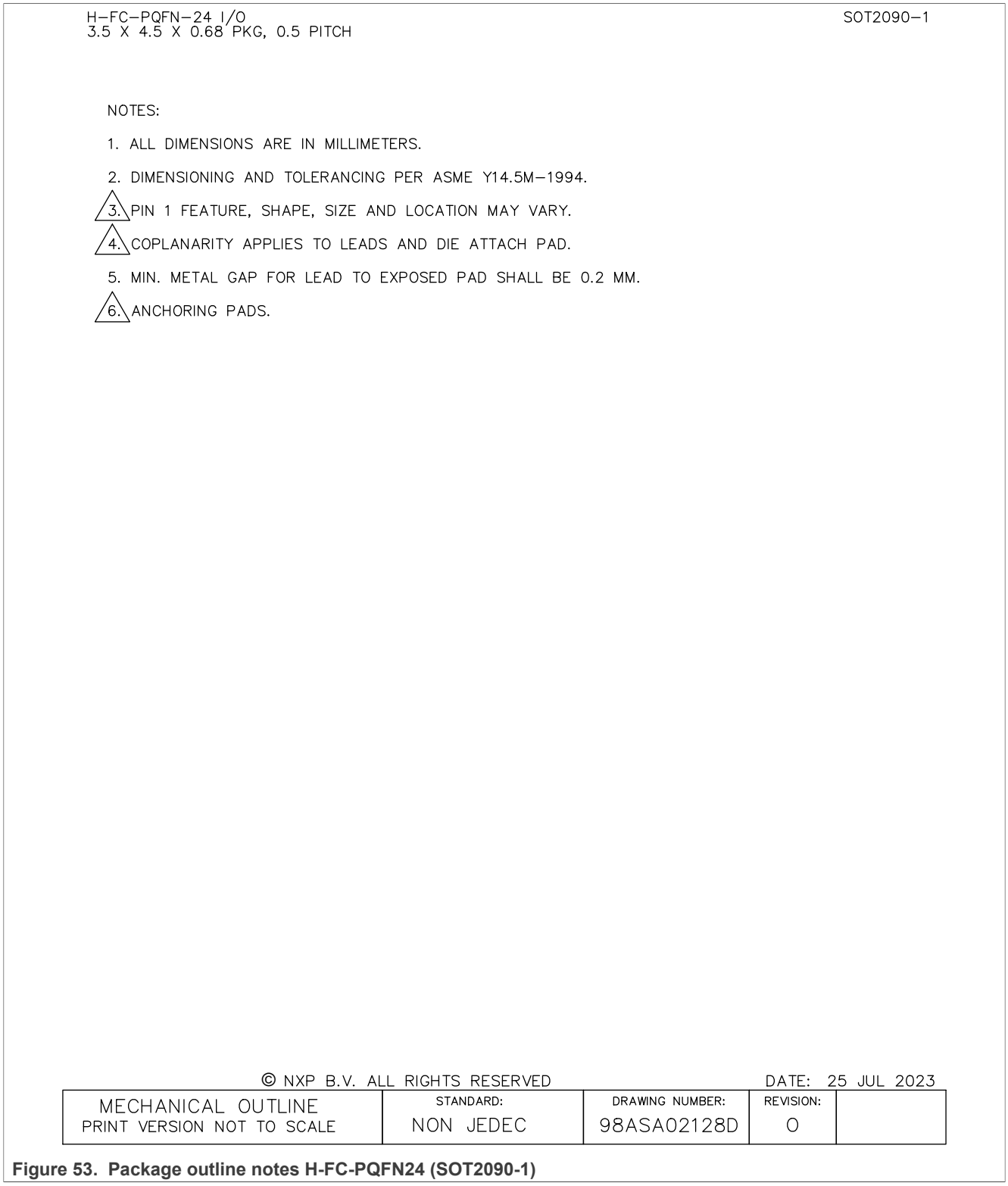


Figure 53. Package outline notes H-FC-PQFN24 (SOT2090-1)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

20.2.2 Soldering, A

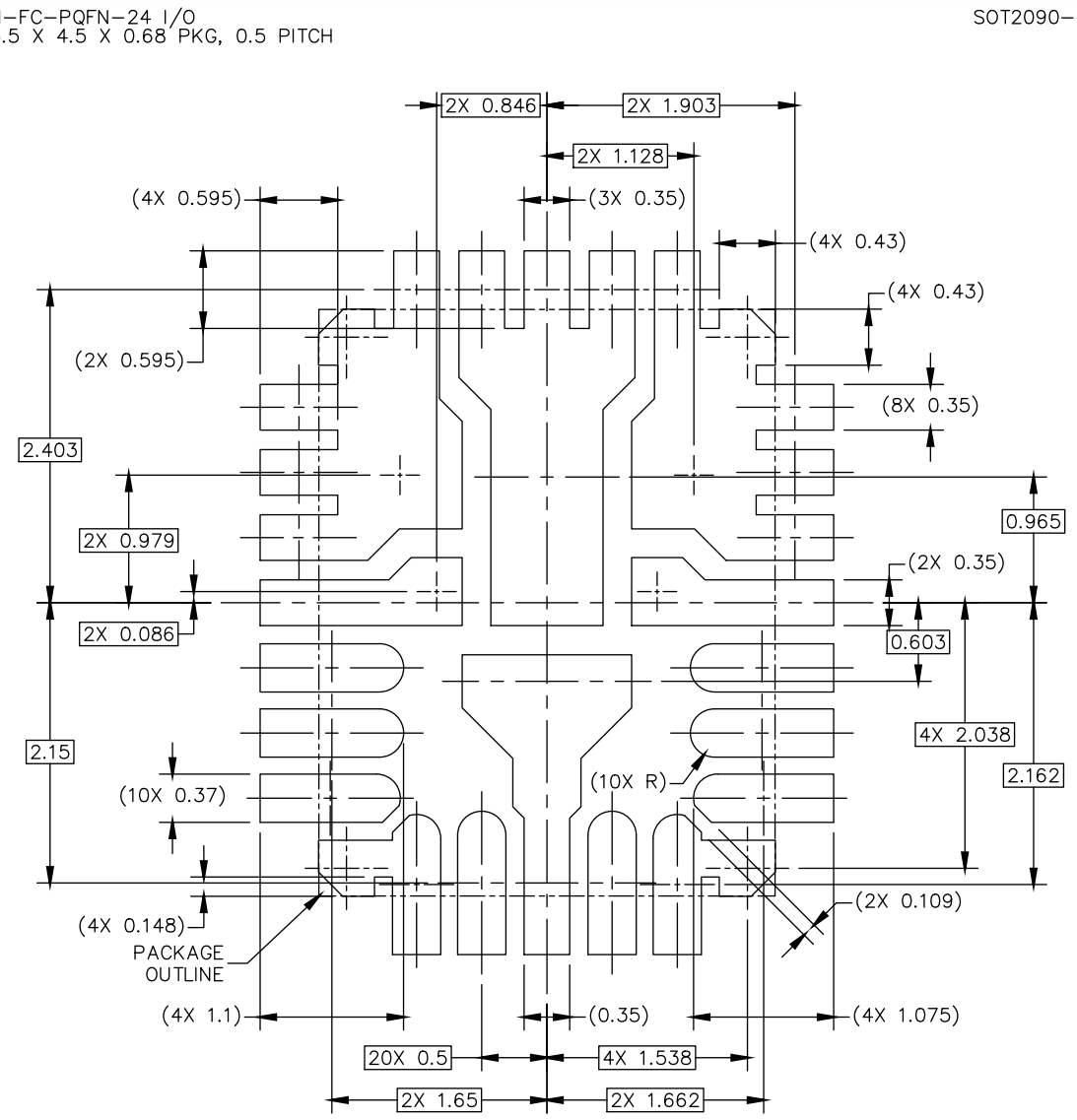
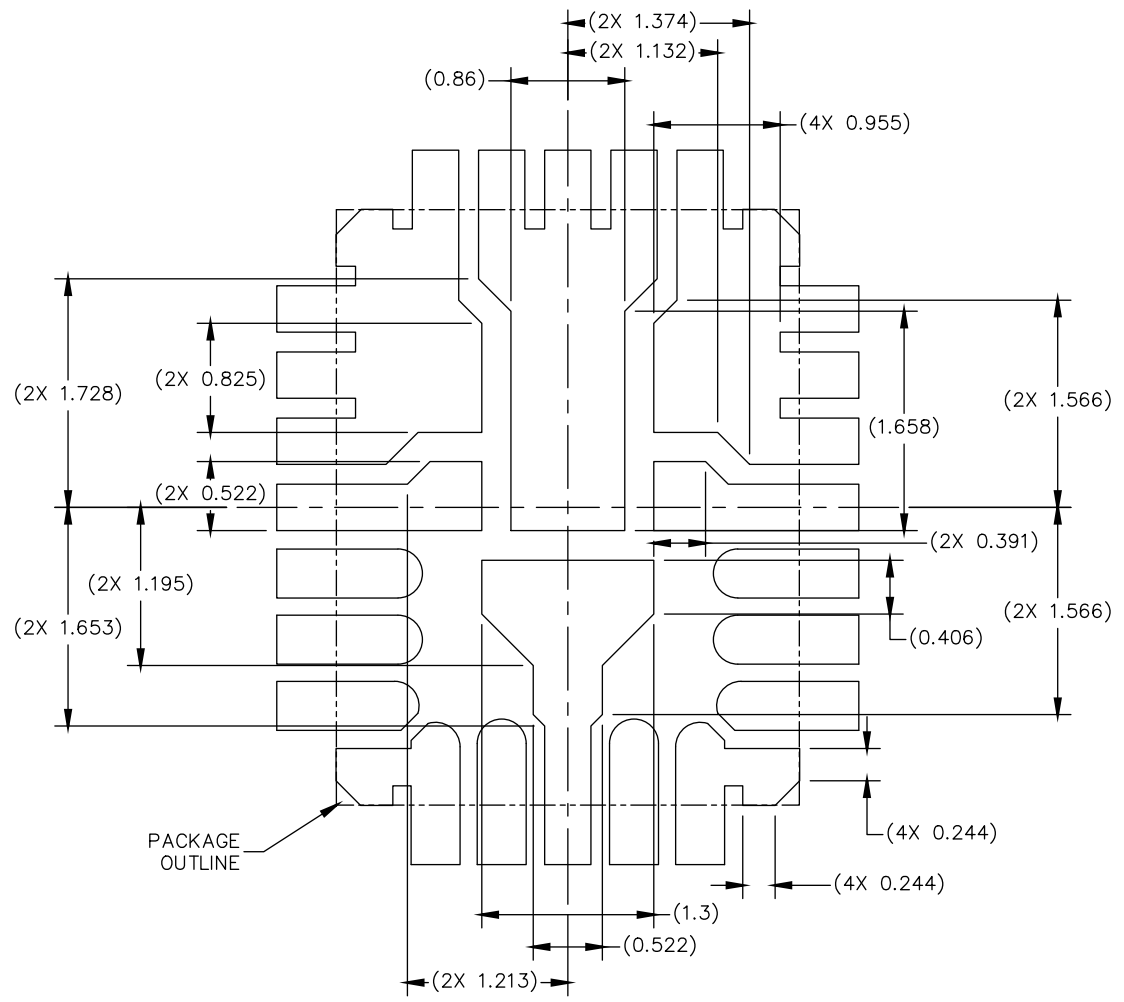


Figure 54. Reflow soldering footprint part1 H-FC-PQFN24 (SOT2090-1))

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

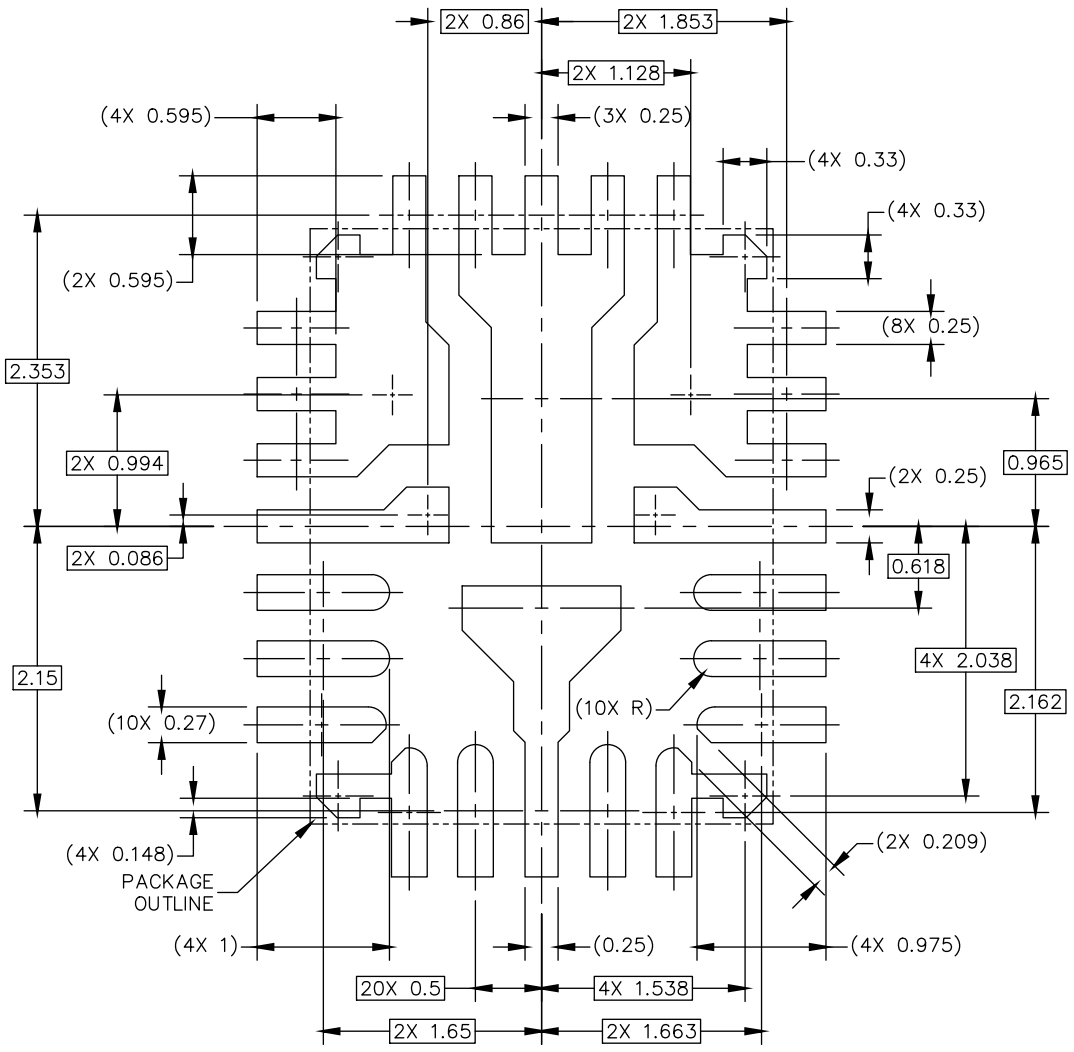
THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 25 JUL 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02128D	REVISION: O	

Figure 55. Reflow soldering footprint part2 H-FC-PQFN24 (SOT2090-1)



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

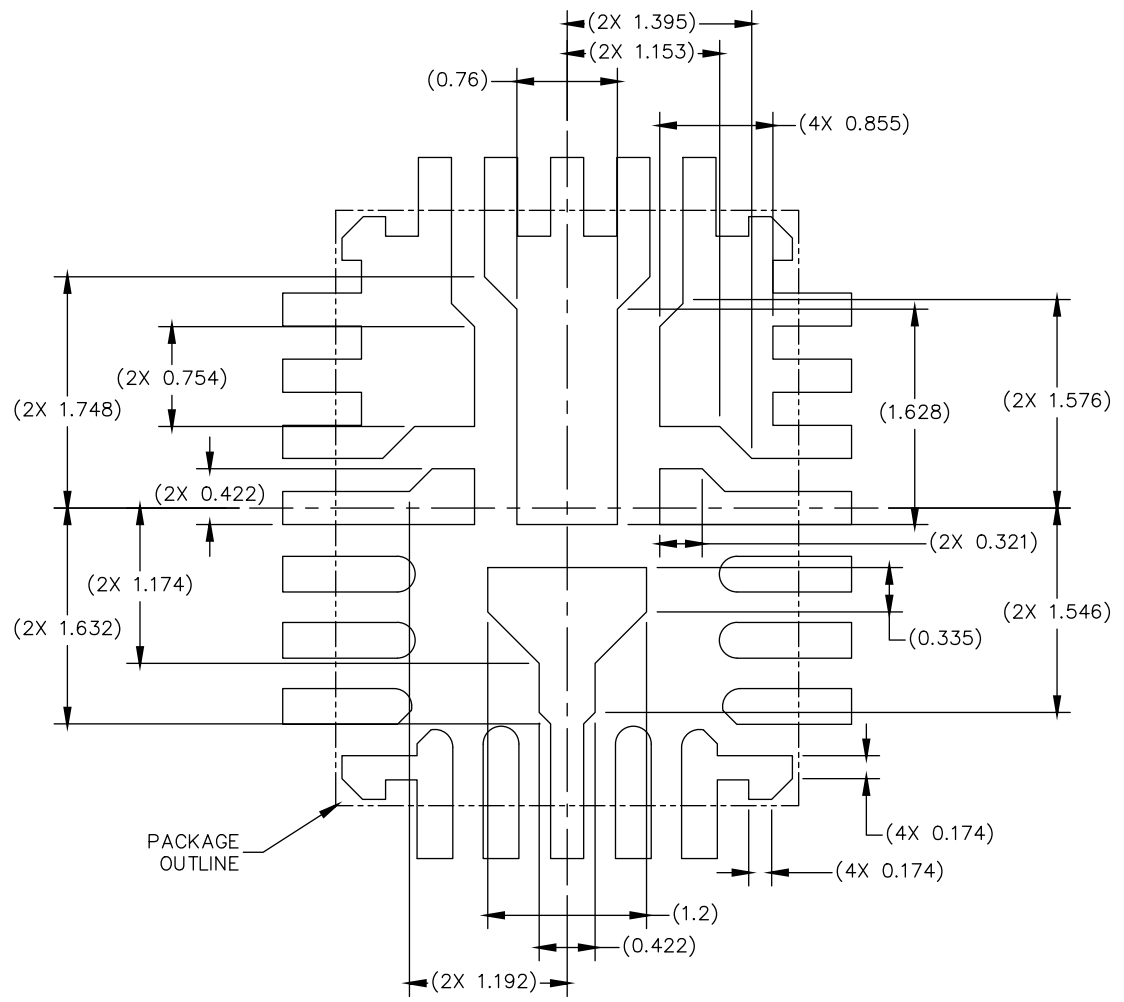
THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 25 JUL 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02128D	REVISION: O	

Figure 56. Reflow soldering footprint part3 H-FC-PQFN24 (SOT2090-1)



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

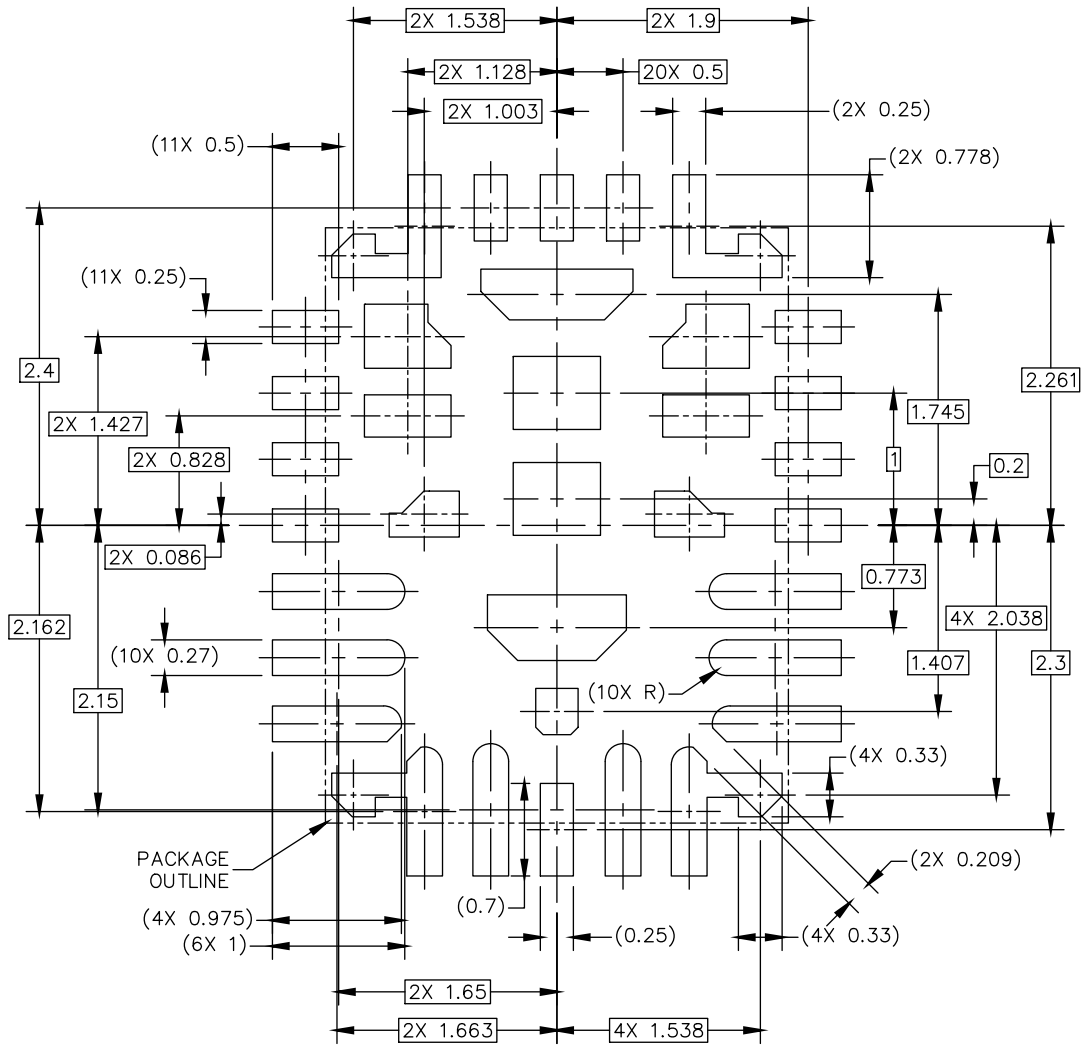
THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 25 JUL 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02128D	REVISION: O	

Figure 57. Reflow soldering footprint part4 H-FC-PQFN24 (SOT2090-1)



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 25 JUL 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02128D	REVISION: O	

Figure 58. Reflow soldering footprint part5 H-FC-PQFN24 (SOT2090-1)

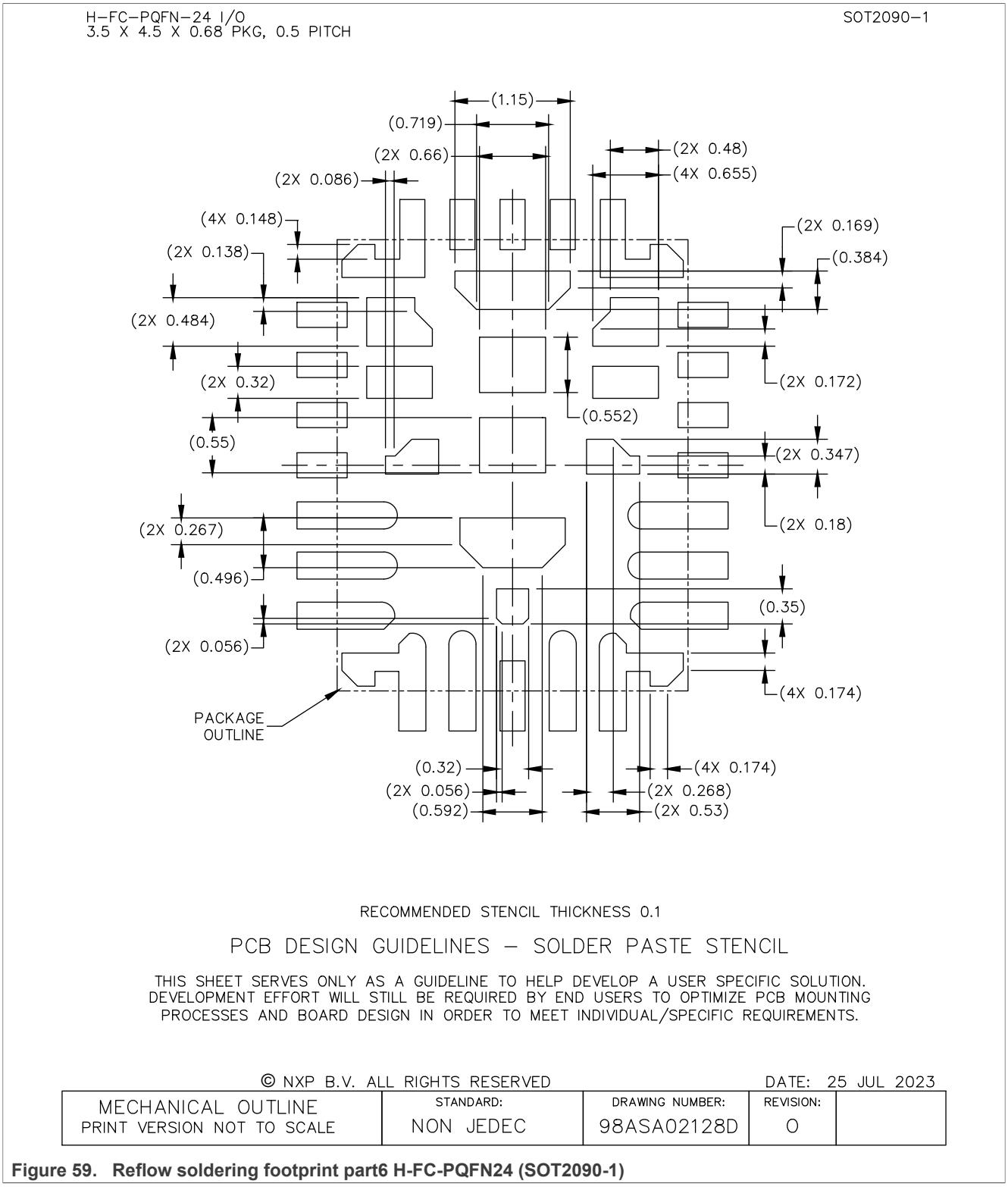


Figure 59. Reflow soldering footprint part6 H-FC-PQFN24 (SOT2090-1)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

20.3 Automotive package, B

20.3.1 Package outline, B

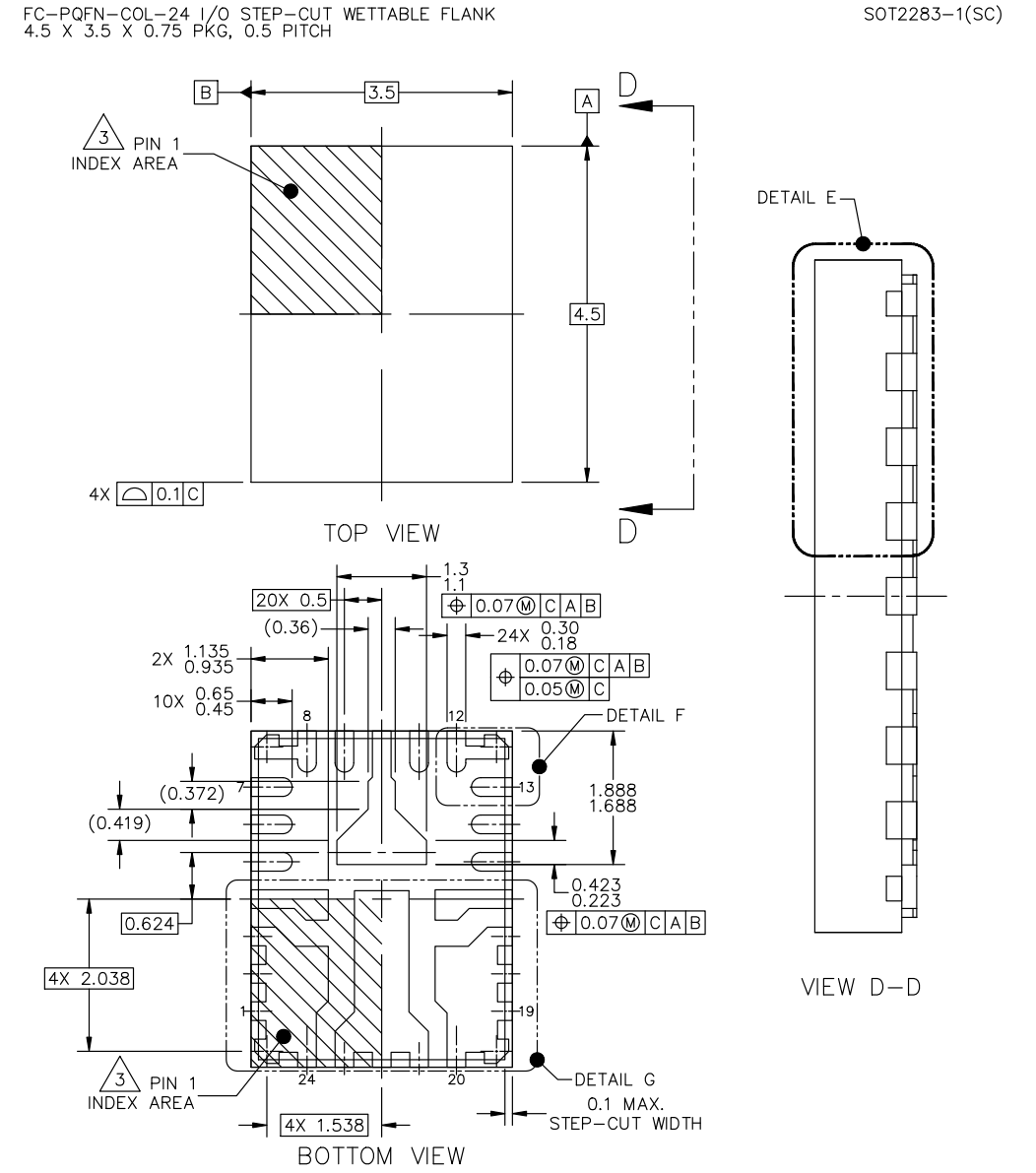


Figure 60. Package outline

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

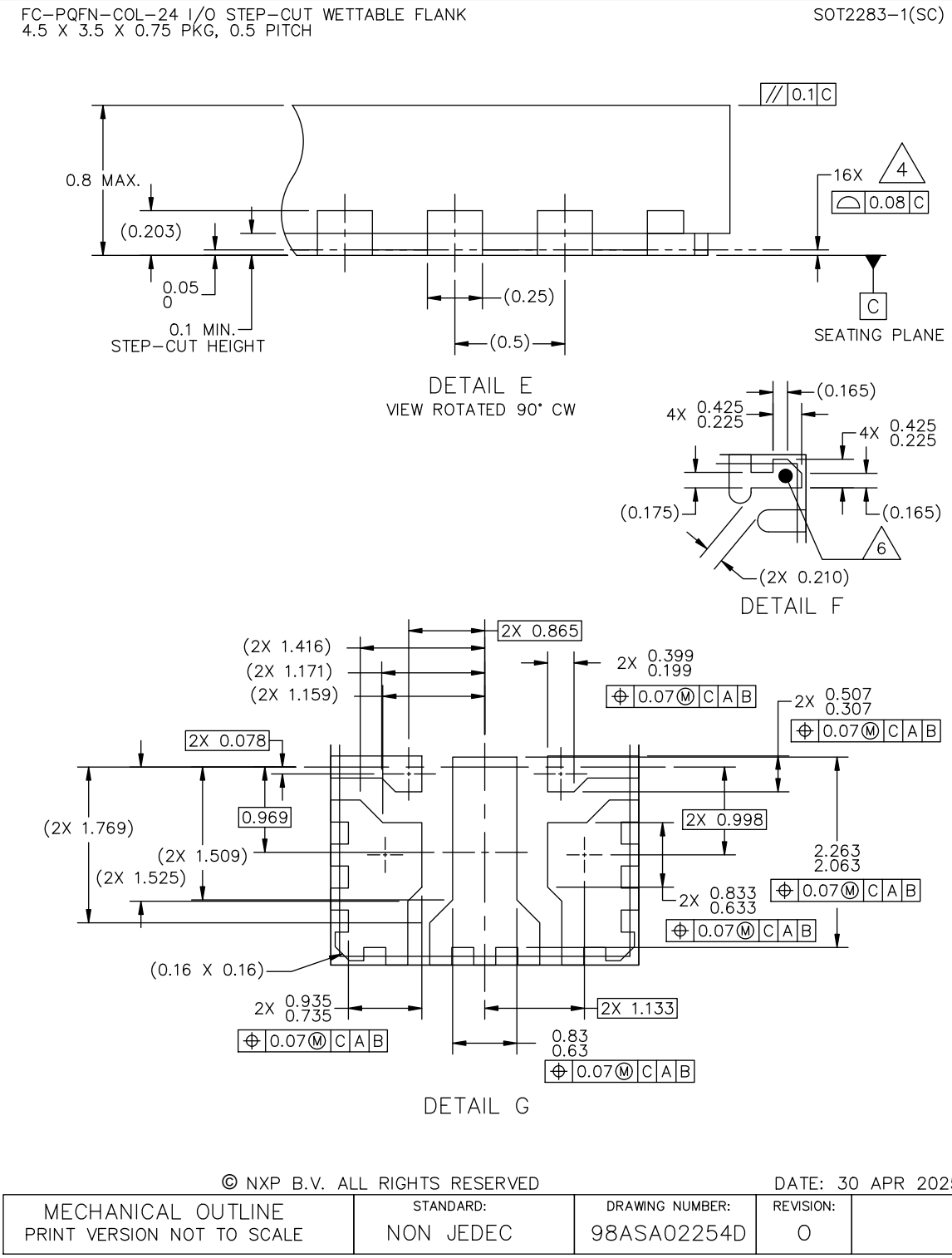


Figure 61. Package outline details

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

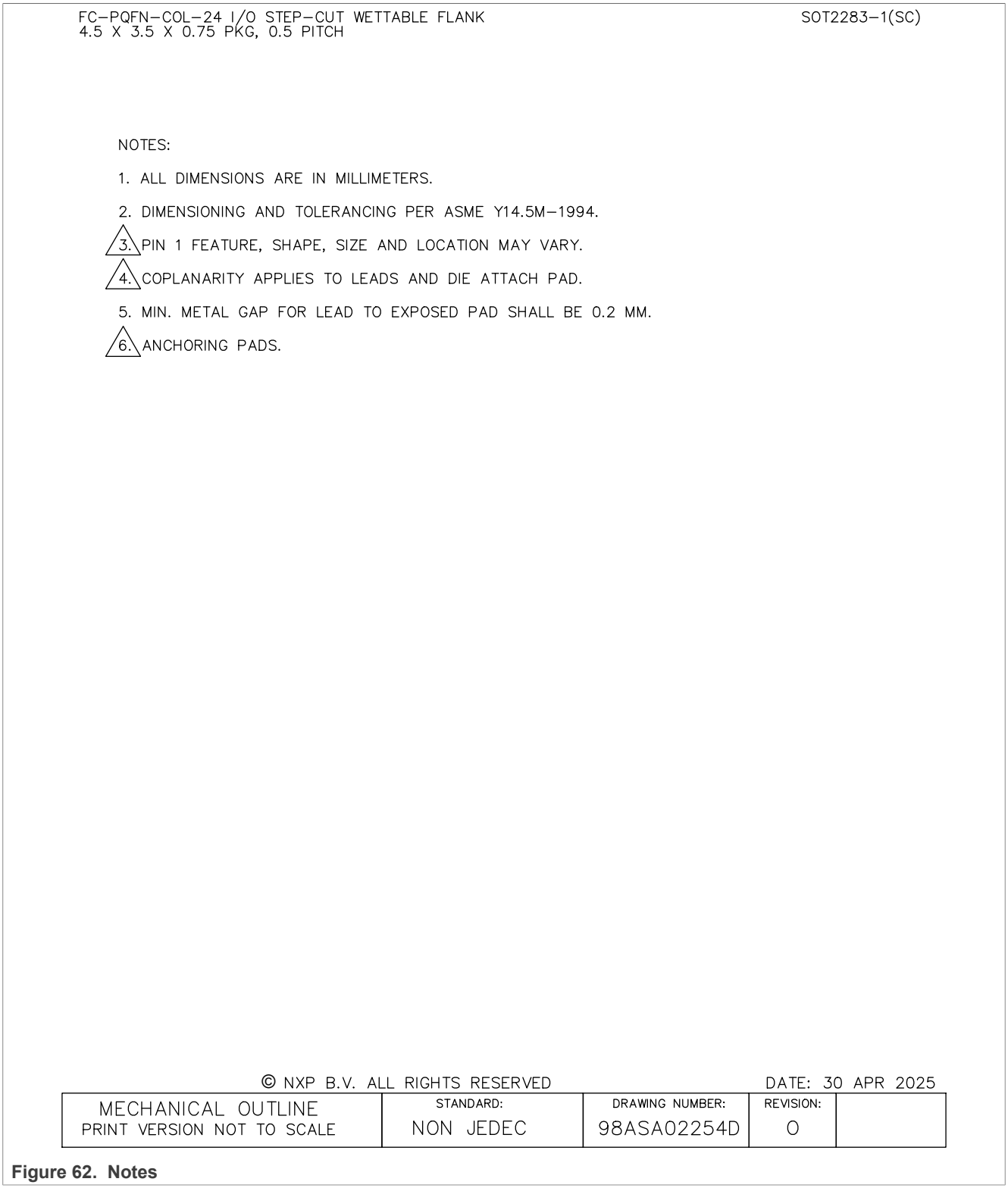


Figure 62. Notes

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

20.3.2 Soldering, B

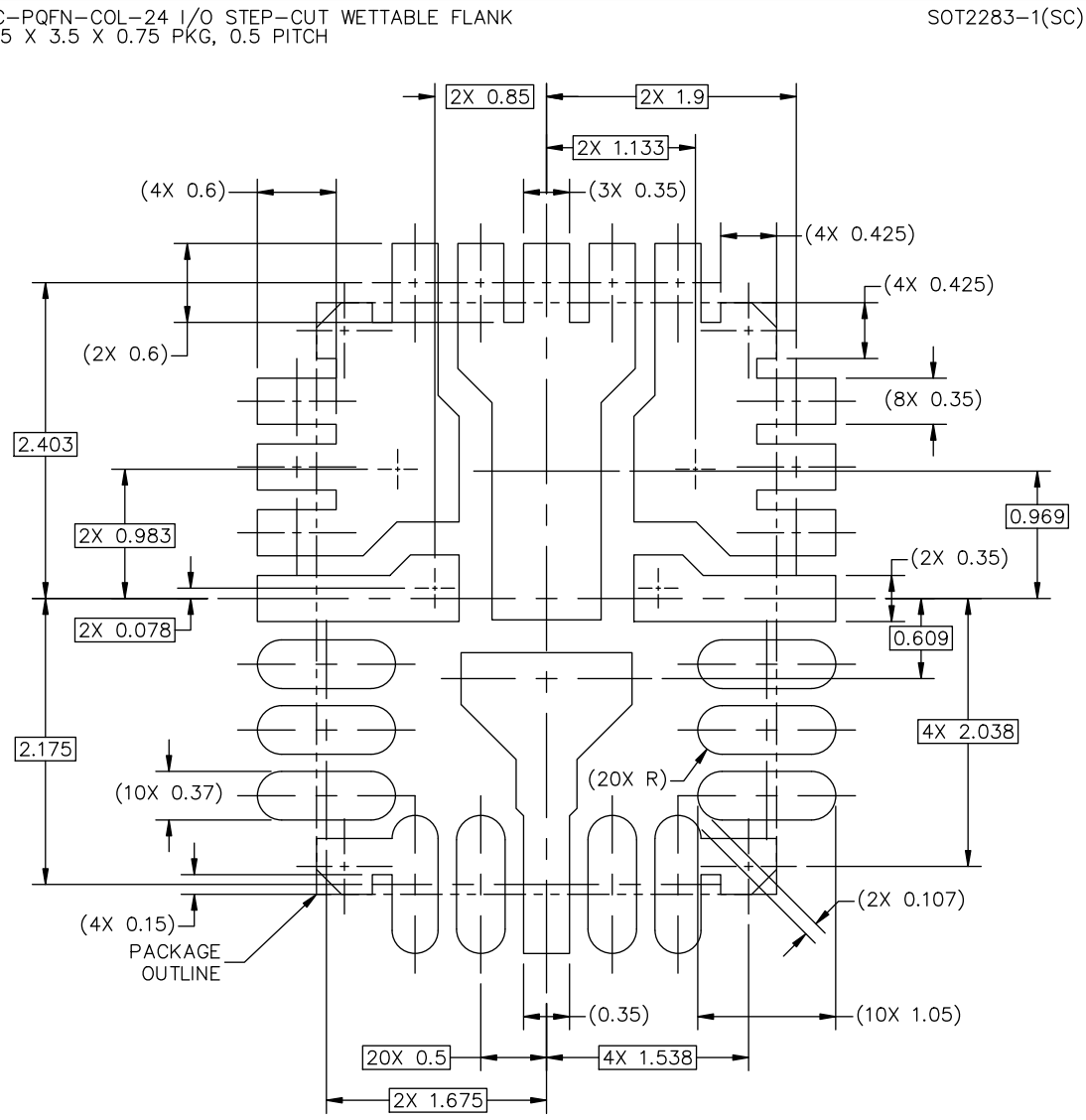
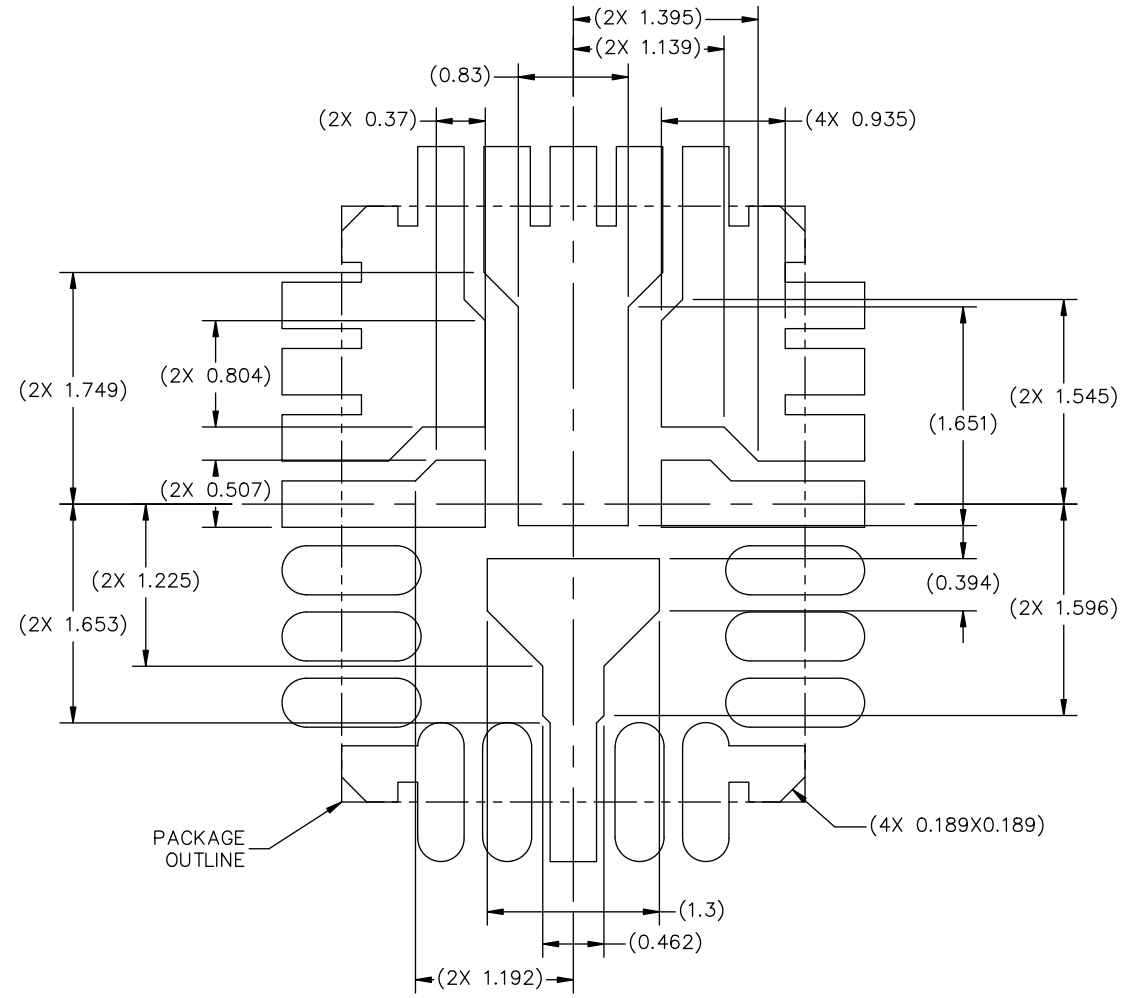


Figure 63. Reflow soldering footprint part1 for HVQFN24 (SOT2090-1(SC))

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 30 APR 2025

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02254D	REVISION: O	

Figure 64. Reflow soldering footprint part2 for HVQFN24 (SOT2283-1(SC))

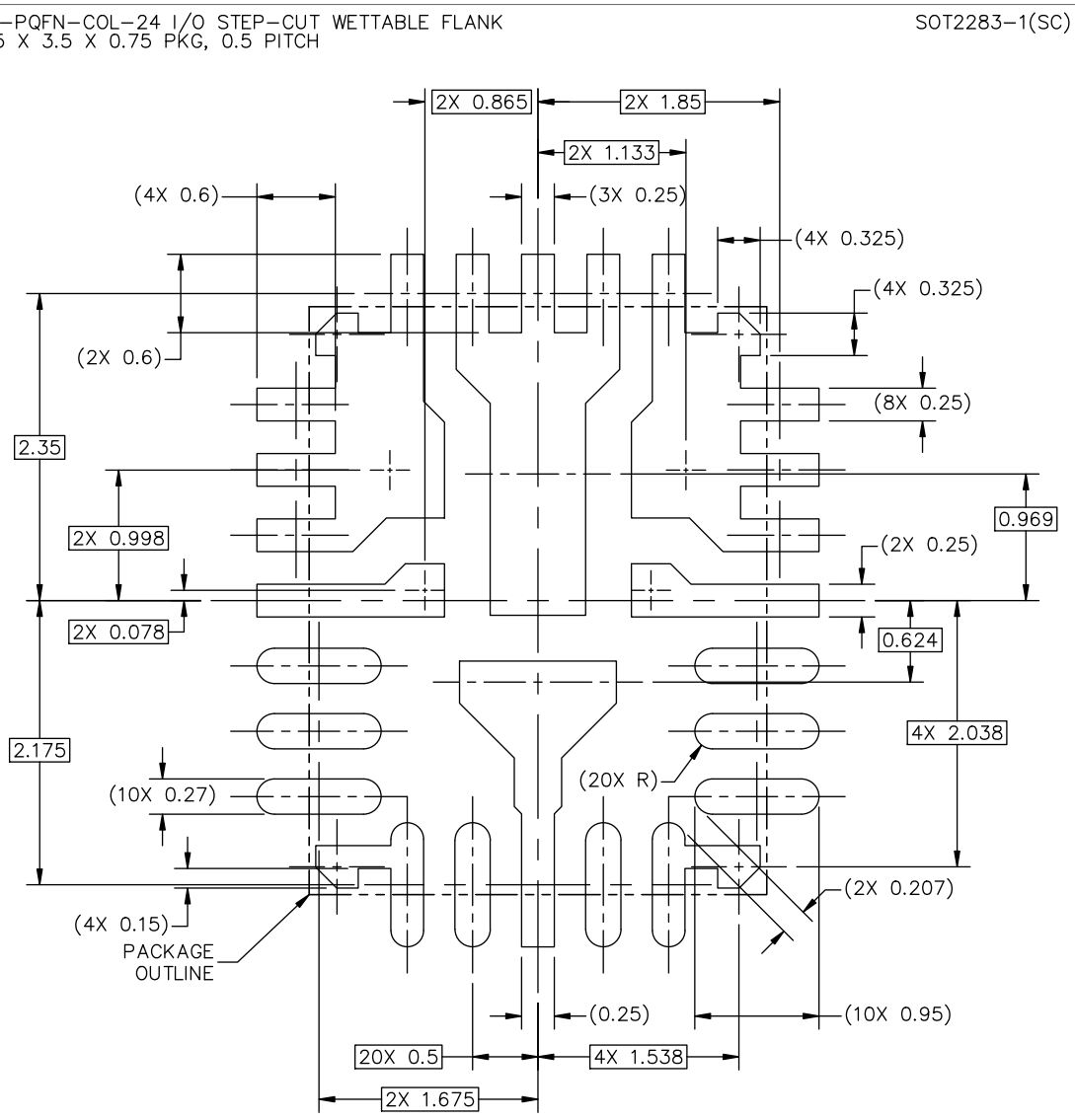


Figure 65. Reflow soldering footprint part3 for HVQFN24 (SOT2283-1(SC))

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

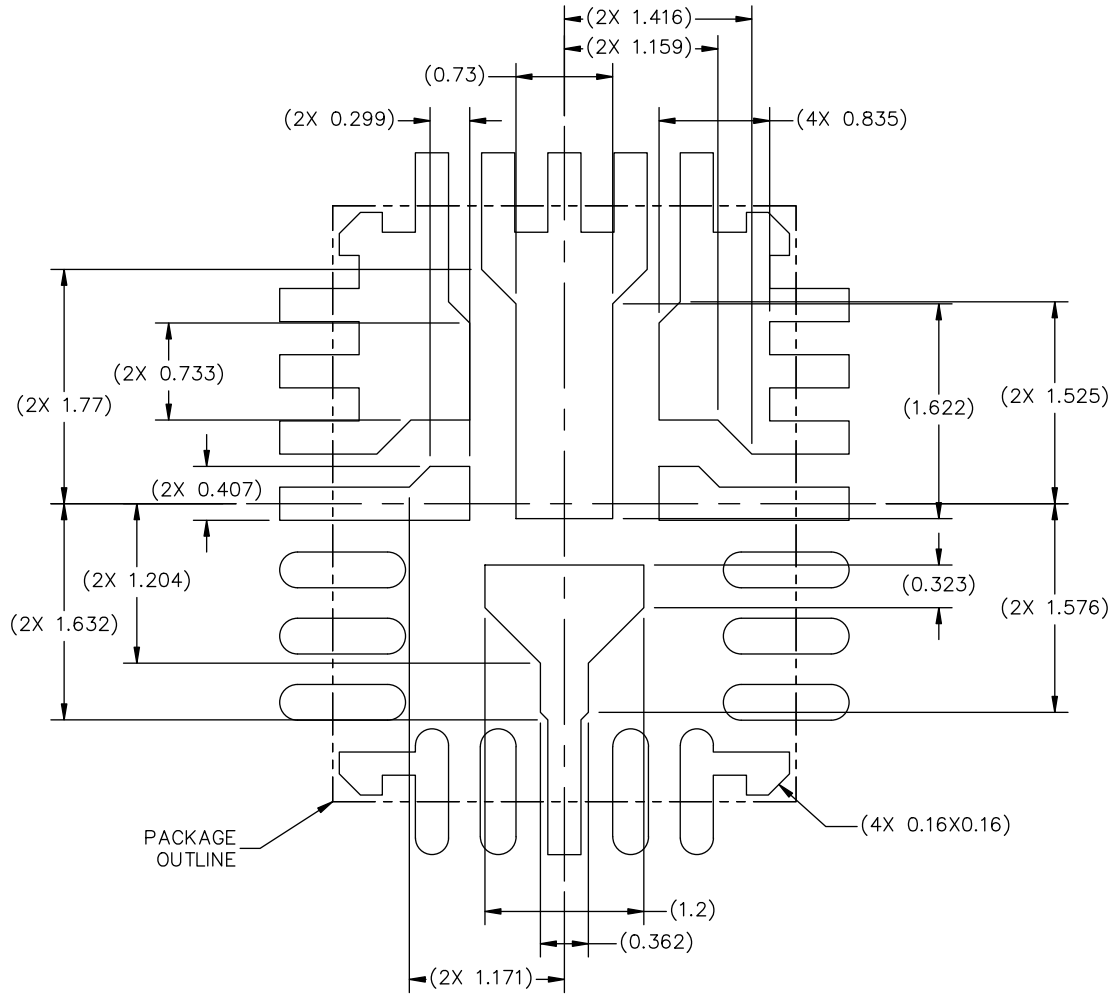


Figure 66. Reflow soldering footprint part4 for HVQFN24 (SOT2283-1(SC))

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

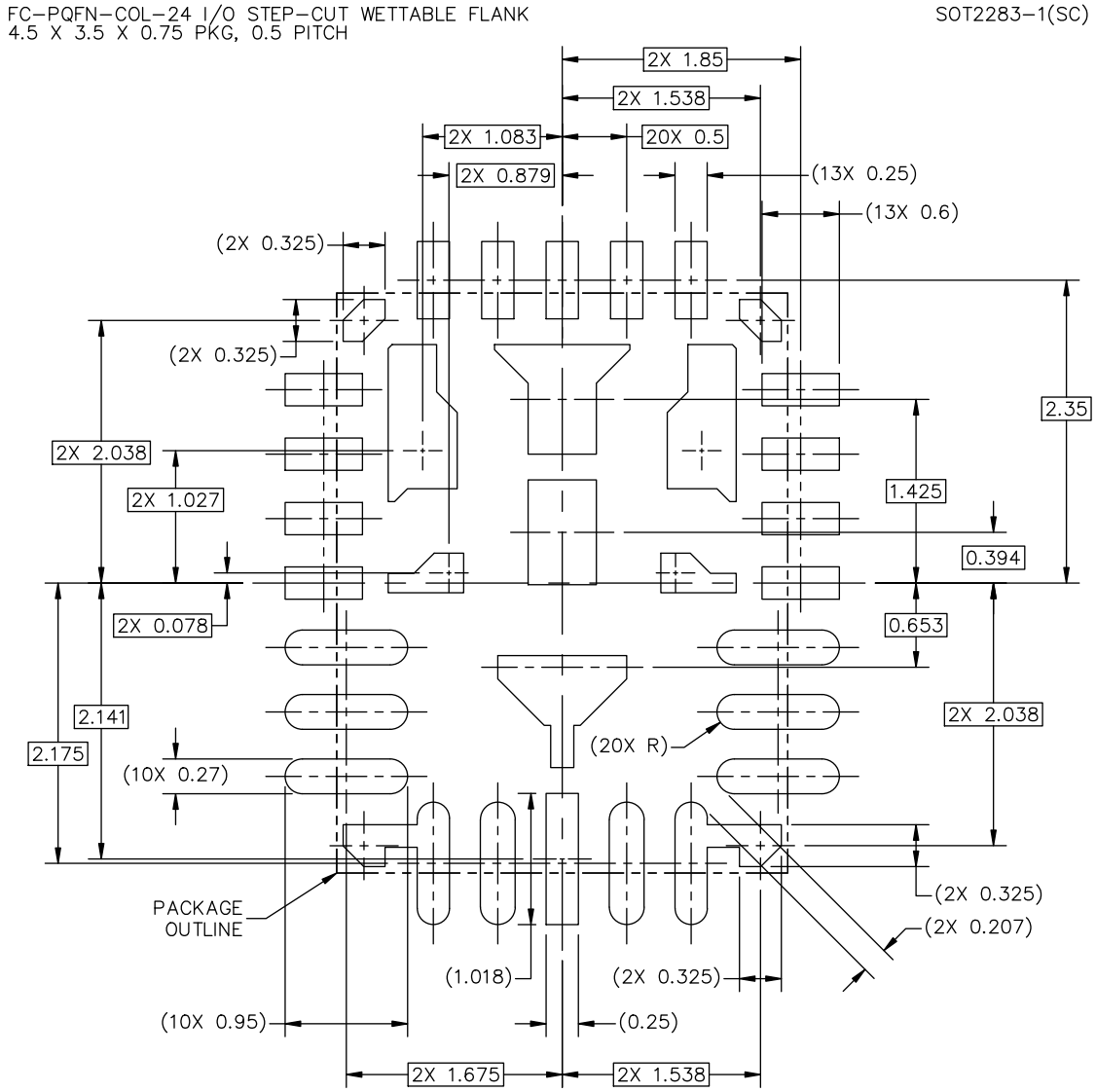


Figure 67. Reflow soldering footprint part5 for HVQFN24 (SOT2283-1(SC))

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

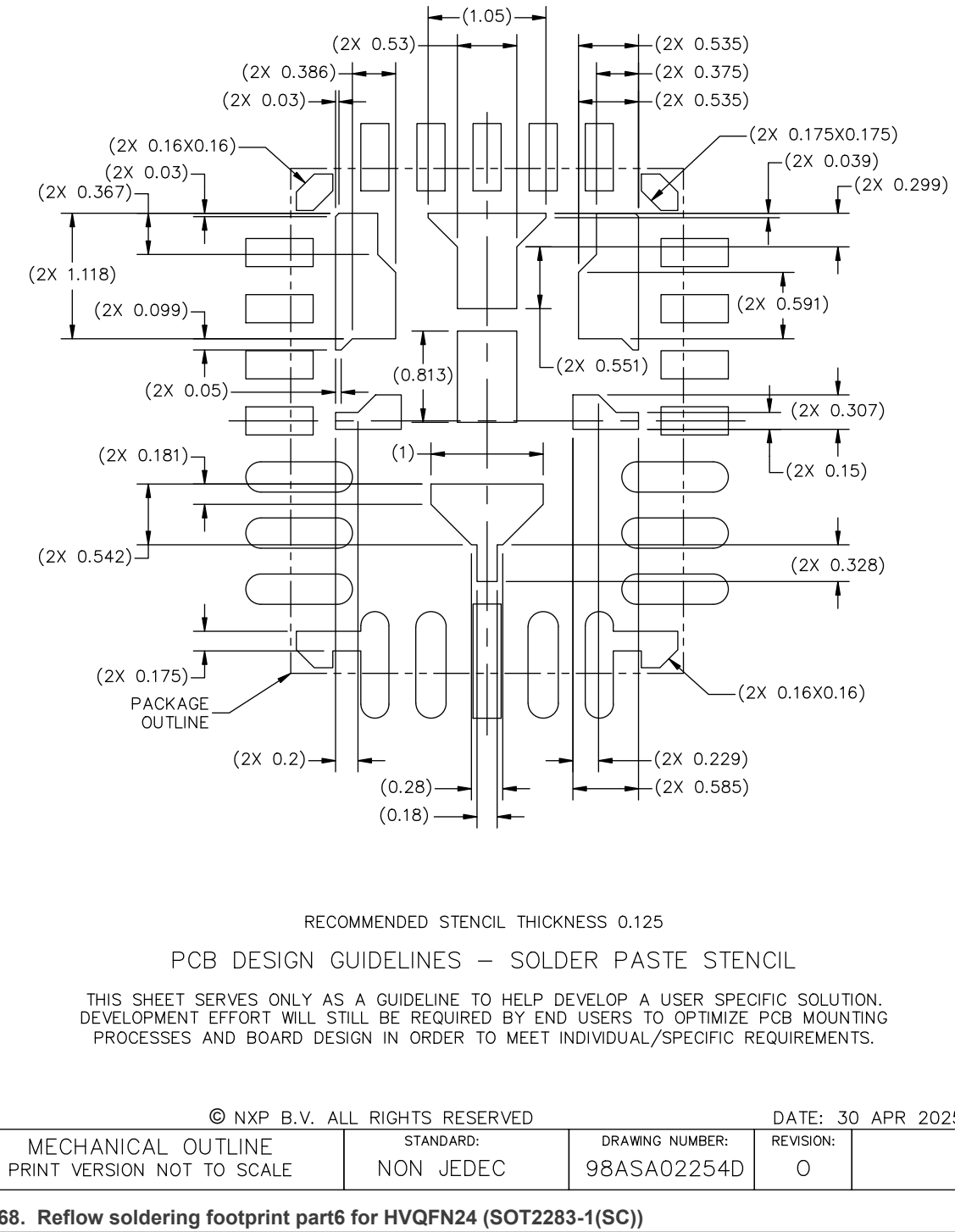


Figure 68. Reflow soldering footprint part6 for HVQFN24 (SOT2283-1(SC))

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

20.4 Industrial package, B

20.4.1 Package outline, B

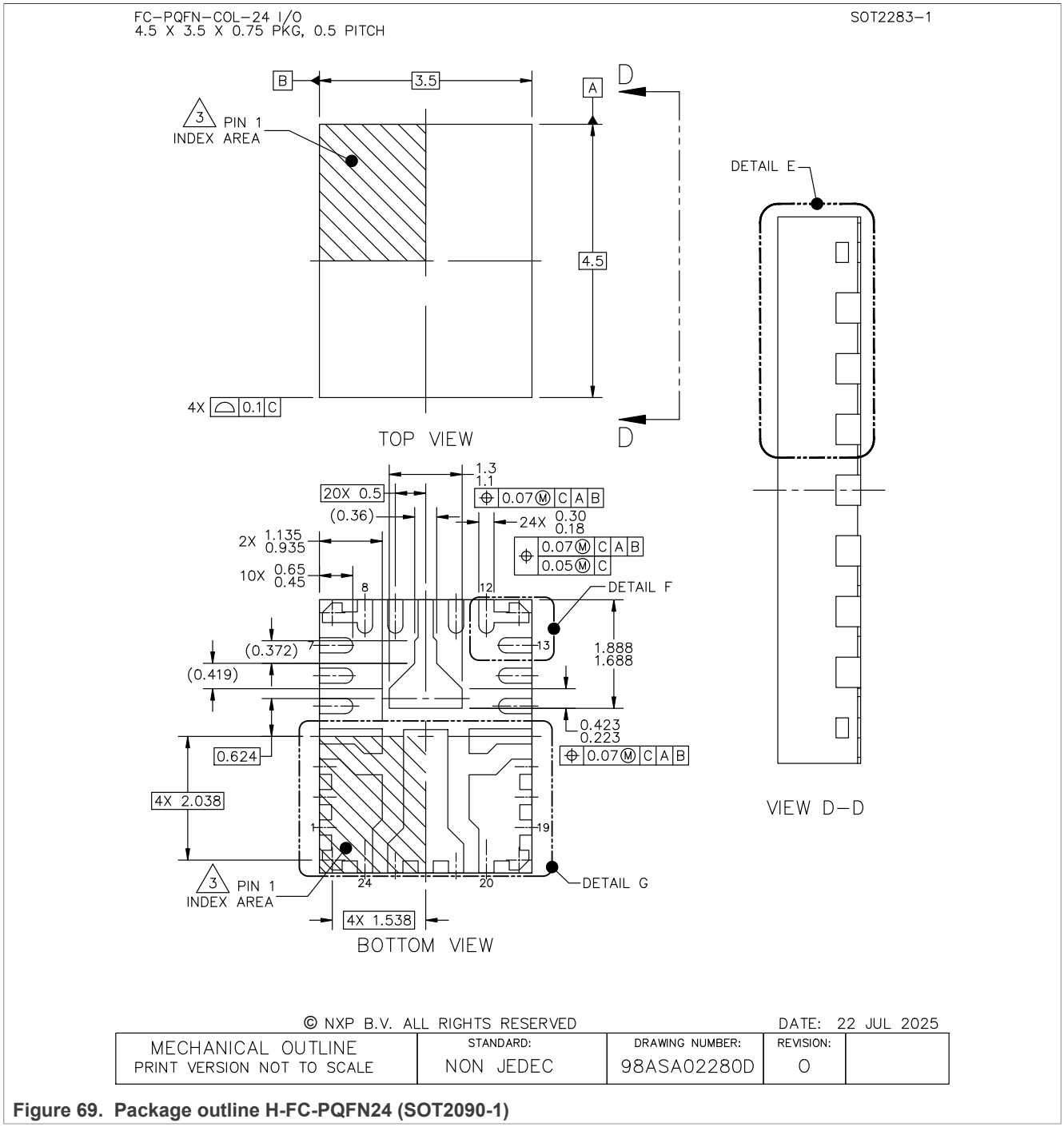


Figure 69. Package outline H-FC-PQFN24 (SOT2090-1)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

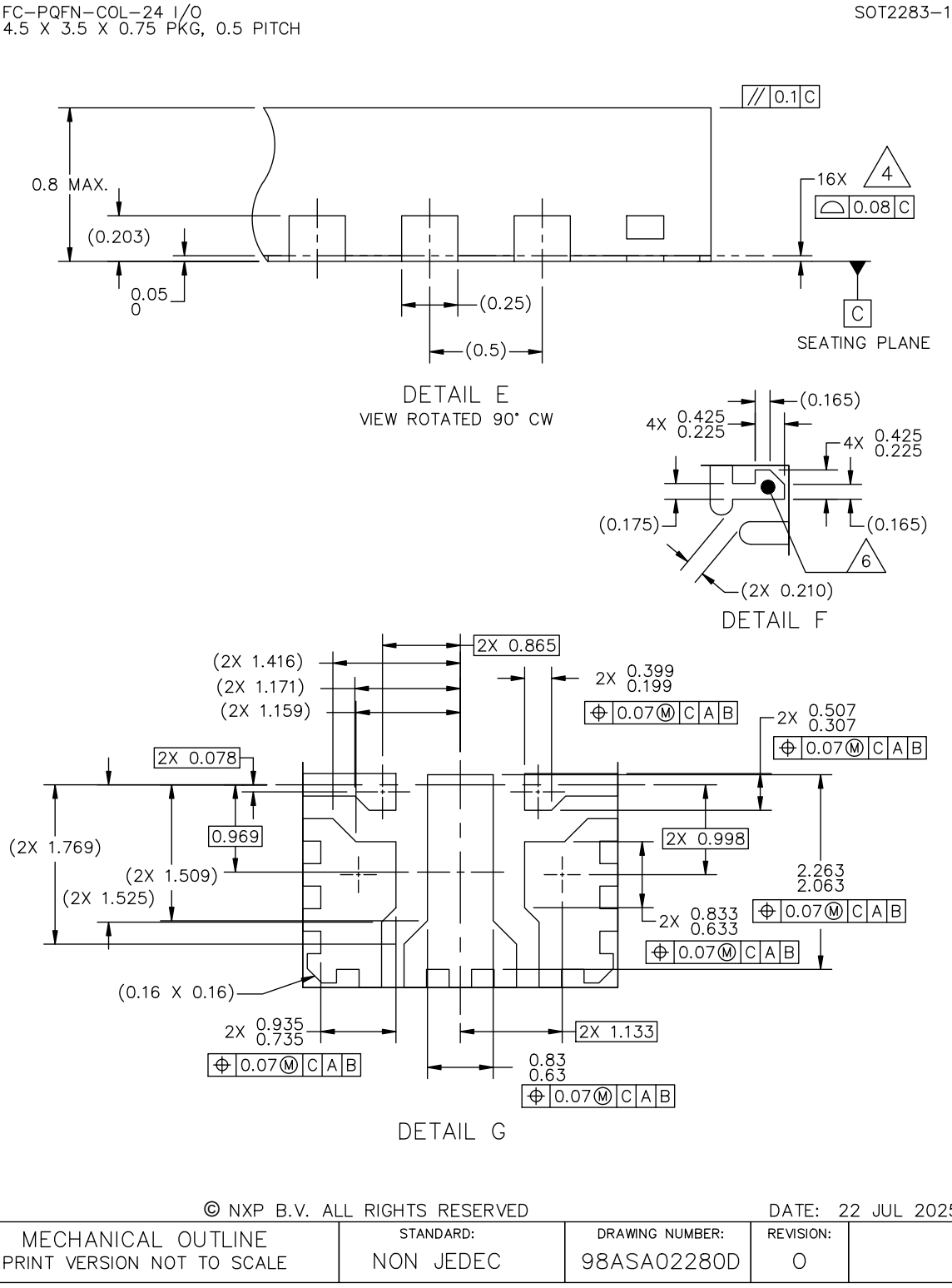


Figure 70. Package outline detail E and G of H-FC-PQFN24 (SOT2283-1)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

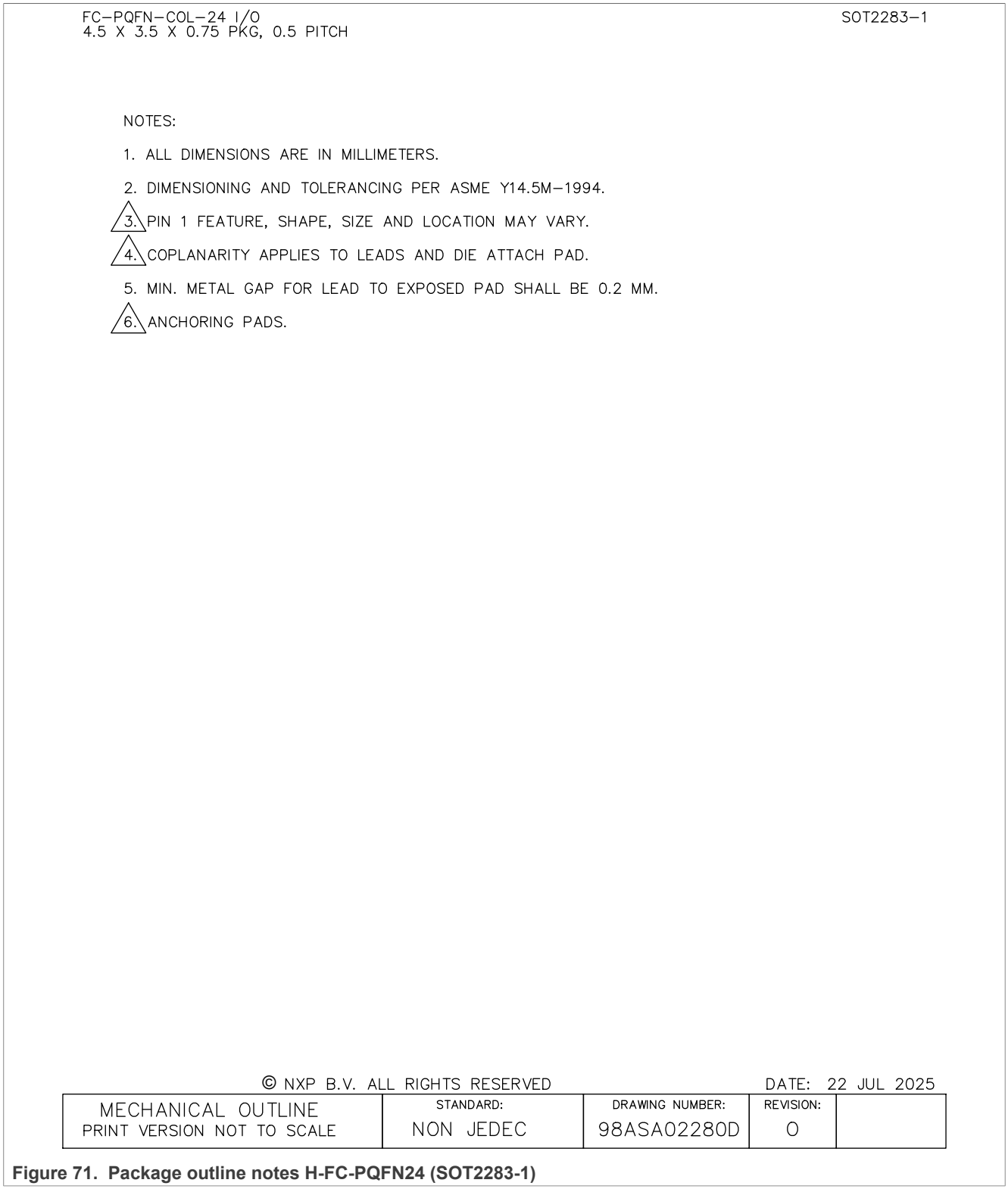


Figure 71. Package outline notes H-FC-PQFN24 (SOT2283-1)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

20.4.2 Soldering, B

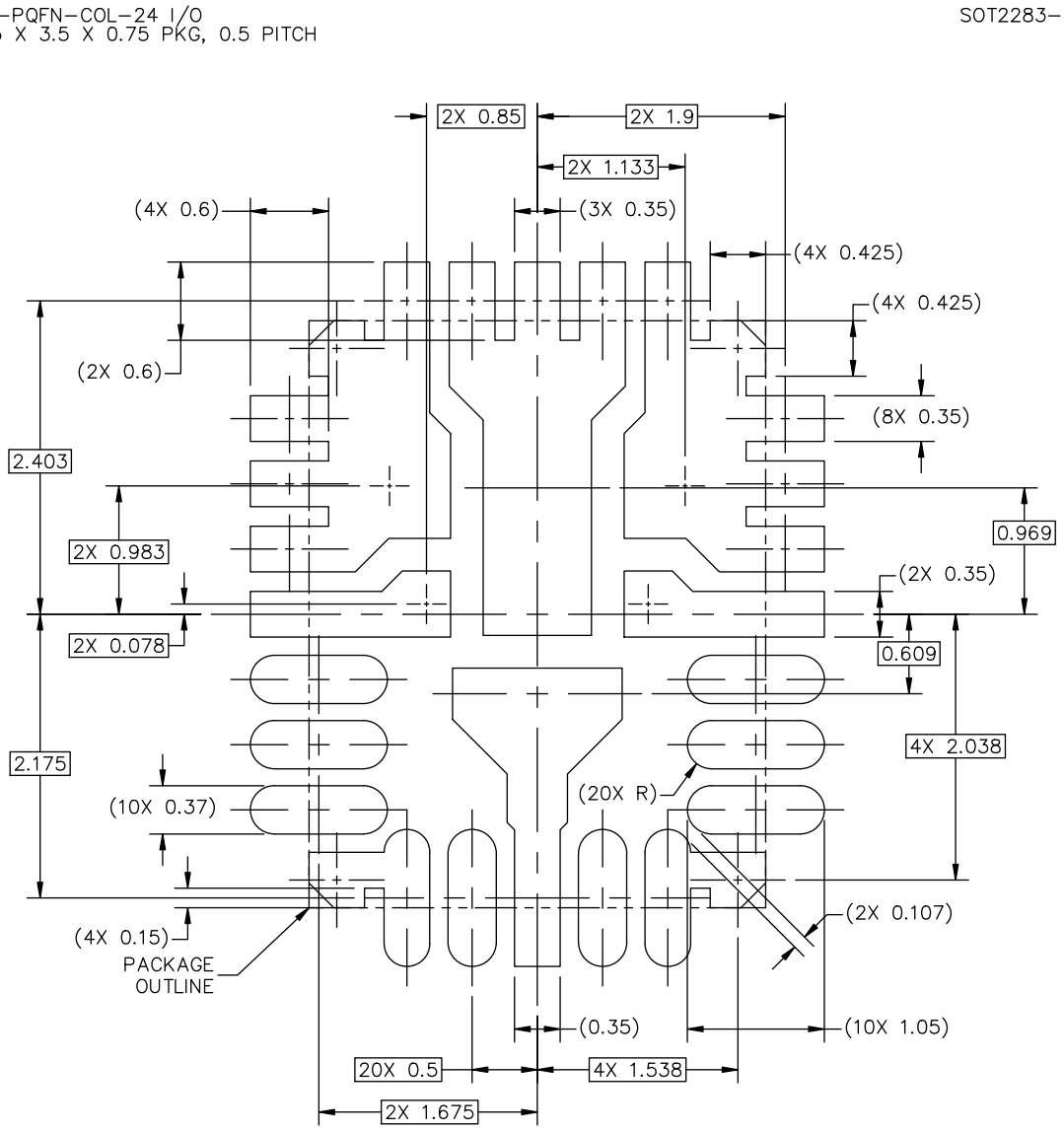


Figure 72. Reflow soldering footprint part1 H-FC-PQFN24 (SOT2283-1))

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

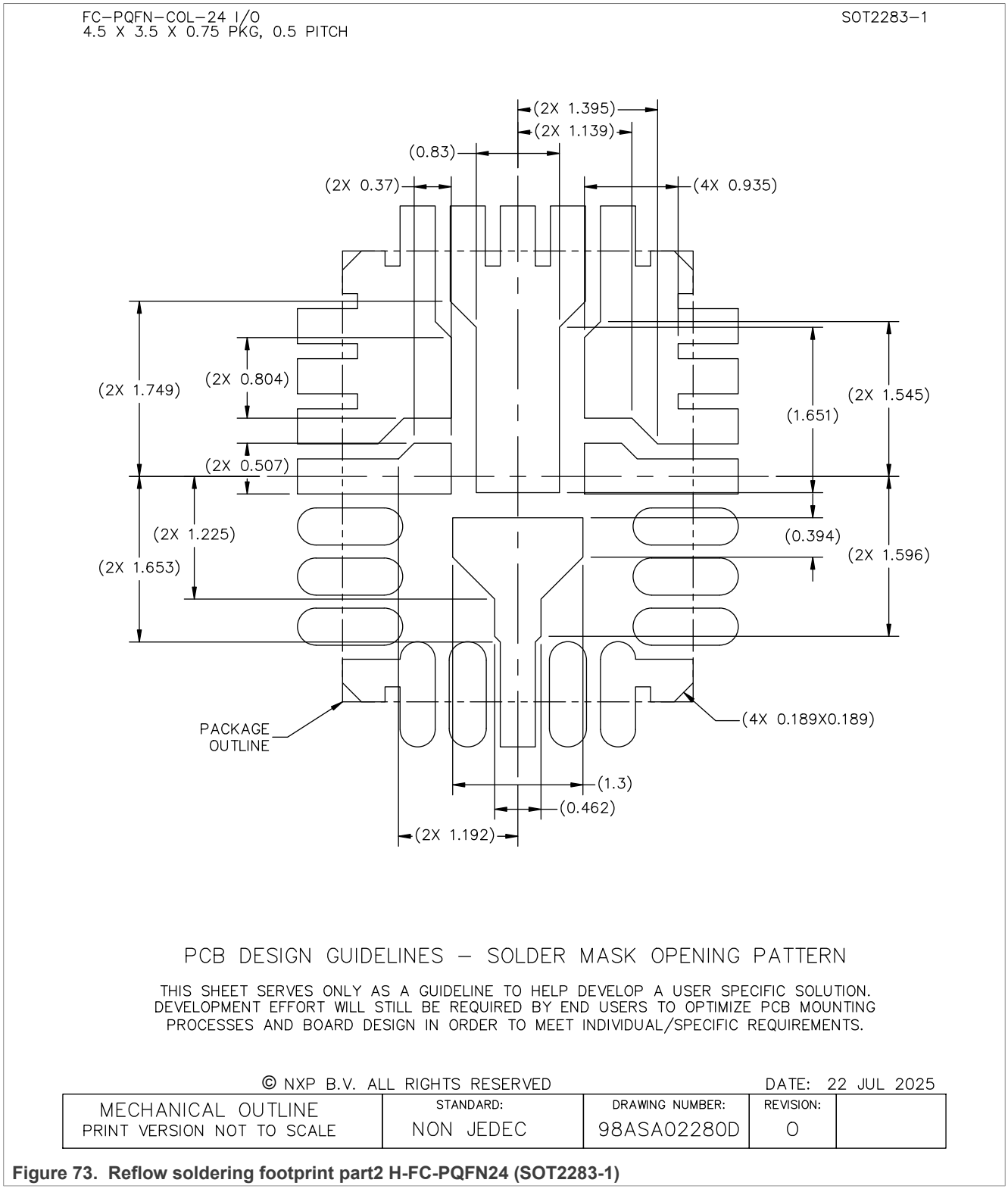


Figure 73. Reflow soldering footprint part2 H-FC-PQFN24 (SOT2283-1)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

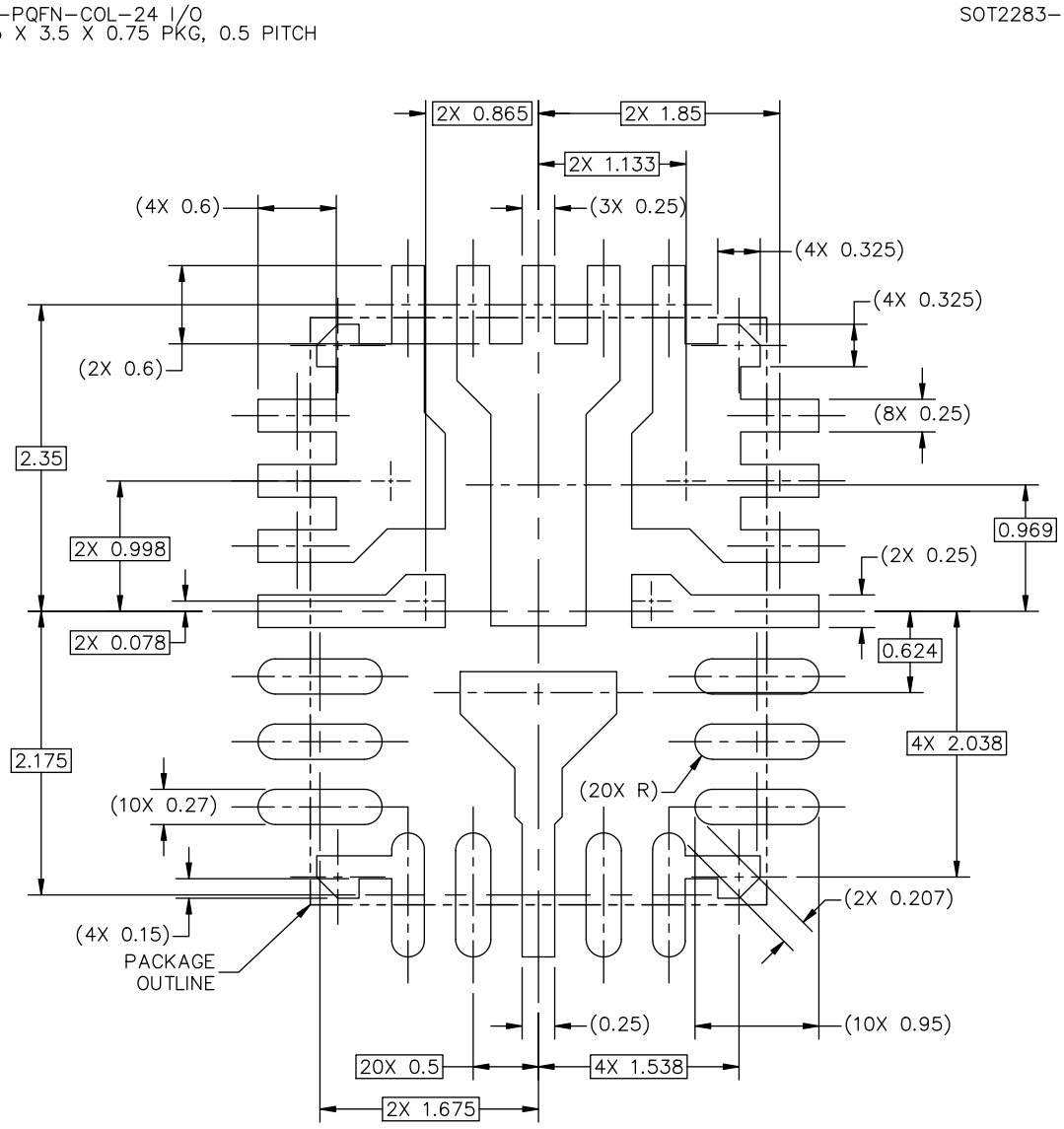
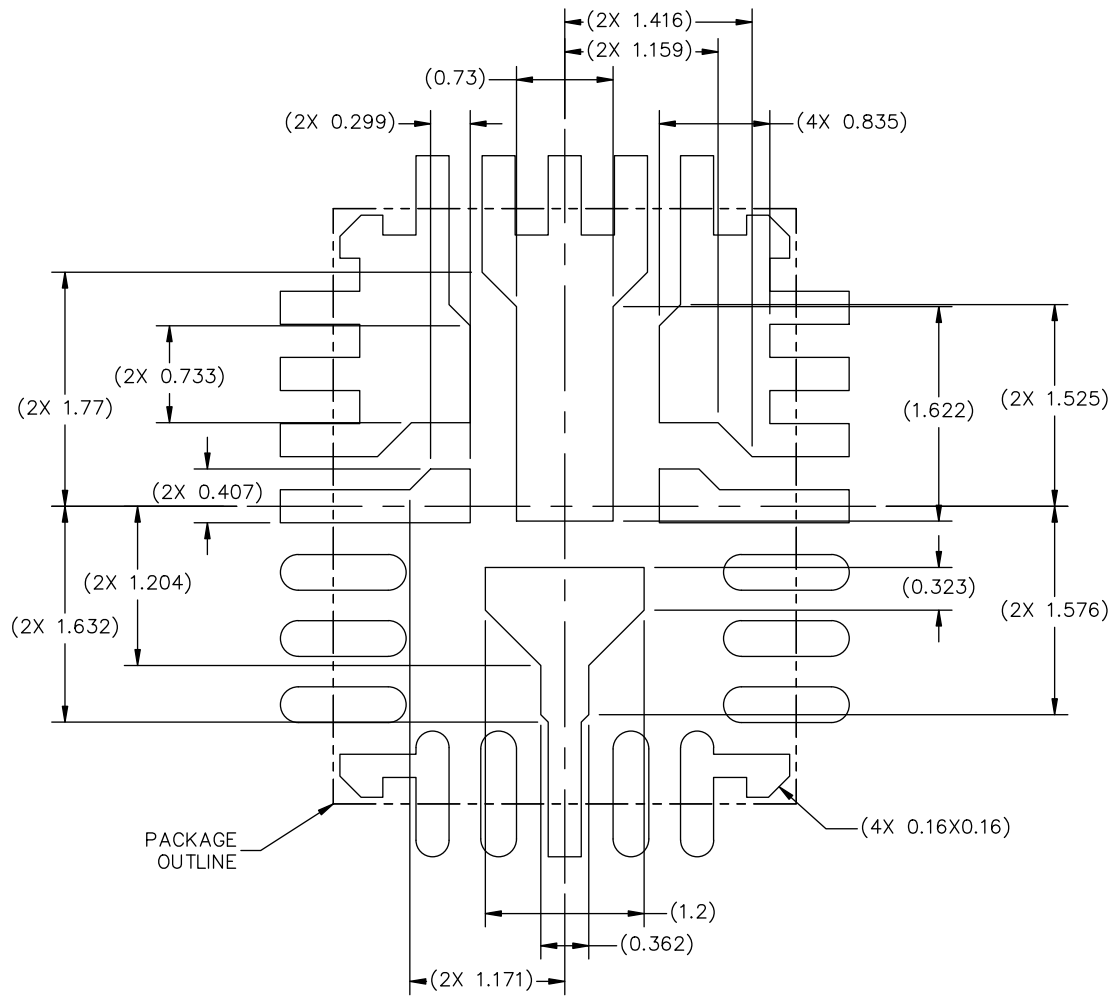


Figure 74. Reflow soldering footprint part3 H-FC-PQFN24 (SOT2283-1)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

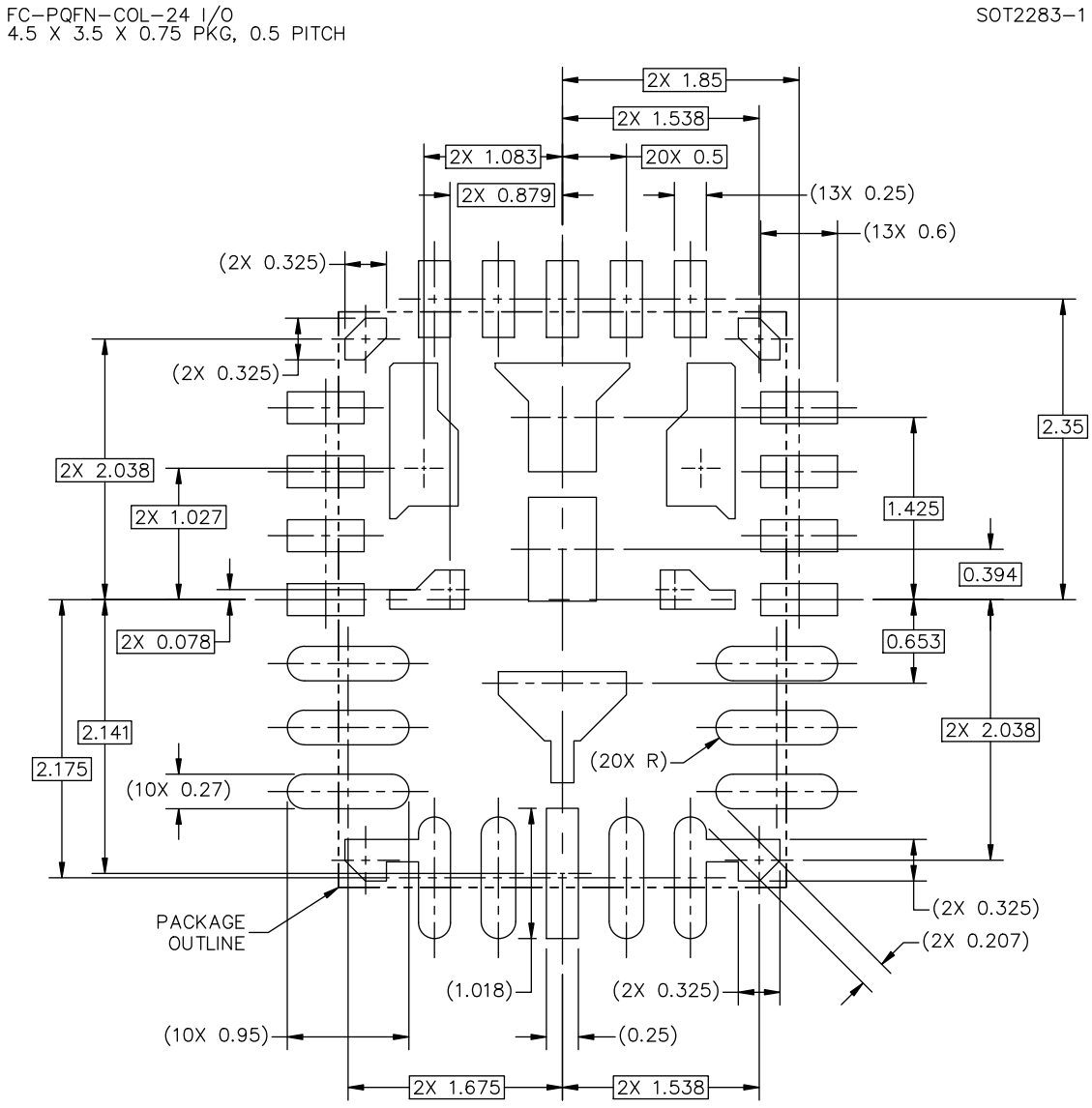
THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 22 JUL 2025

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02280D	REVISION: O	

Figure 75. Reflow soldering footprint part4 H-FC-PQFN24 (SOT2283-1)



RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 22 JUL 2025

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02280D	REVISION: O	

Figure 76. Reflow soldering footprint part5 H-FC-PQFN24 (SOT2283-1)

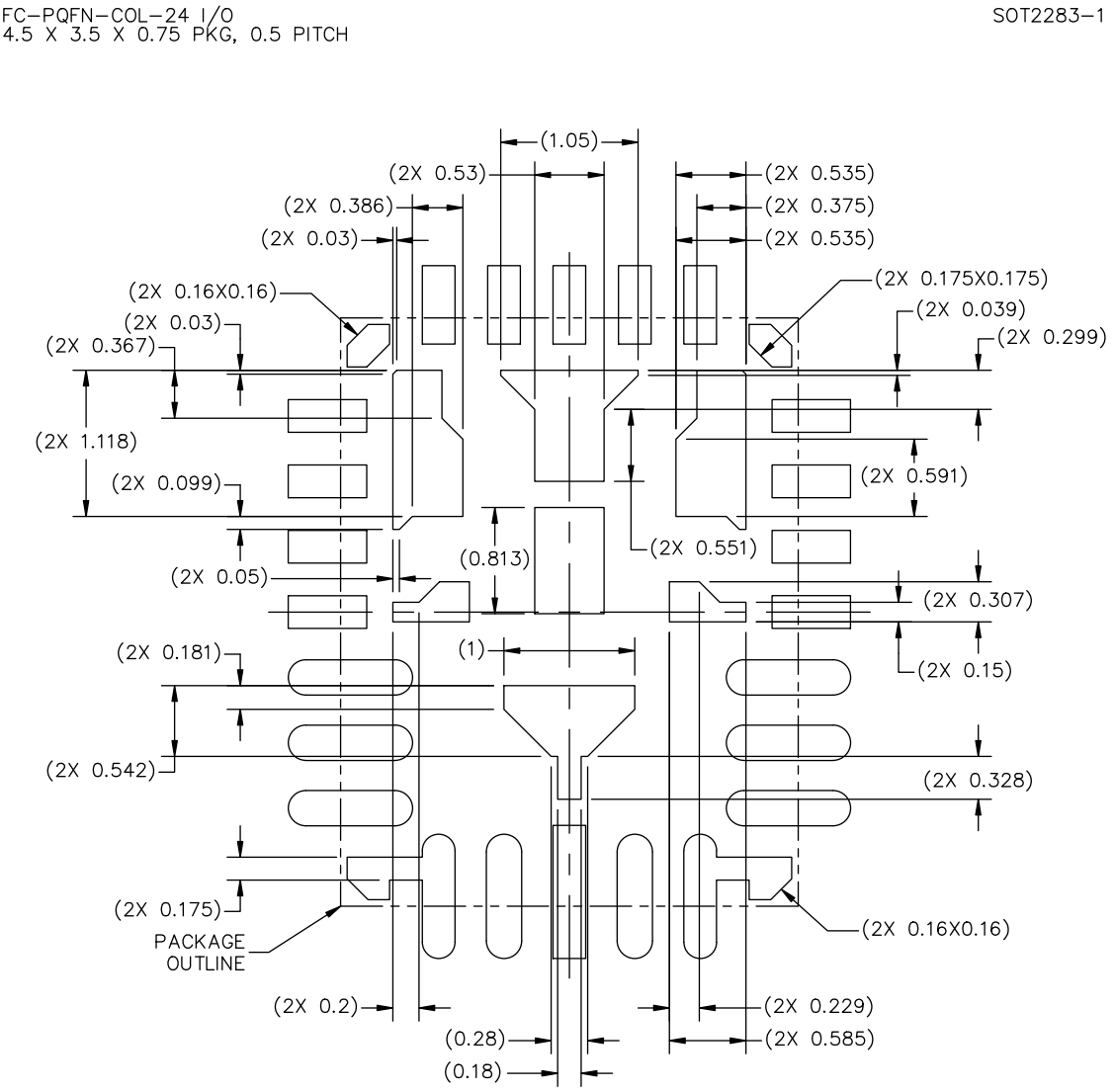


Figure 77. Reflow soldering footprint part6 H-FC-PQFN24 (SOT2283-1)

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

21 Revision history

Document ID	Release date	Description
PF5300_PF5301_ PF5302 v. 7.0	27 July 2026	• CIN 202605013I • Product data sheet • Revised Section 2 • Revised Table 1 • Added Table 2 • Revised Table 30 • Revised Figure 4 • Revised Section 13.1.6 • Added Table 31 • Revised Section 13.1.7 to add a note • Revised Table 33 to add PFM mode • Revised Table 97 • Revised Table 98 • Revised Table 122 • Removed footnote from Table 33 • Revised Table 147 • Revised Section 13.1.4.2 • Revised title of Figure 28 (was *SW1 efficiency, V_{out} = 1.0 V*) • Revised title of Figure 29 (was *SW1 efficiency, V_{out} = 0.9 V*) • Revised title of Figure 30 (was *SW1 efficiency, V_{out} = 0.8 V*) • Revised title of Figure 31 (was *SW1 efficiency, V_{out} = 0.7 V*) • Added Figure 32 • Added Figure 33 • Added Figure 34 • Added Figure 35 • Added Section 20.3 • Added Section 20.4
PF5300_PF5301_ PF5302 v6	13 November 2025	• CIN 202510025I • Table *Ordering information*: updated content

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Document ID	Release date	Description
PF5300_PF5301_ PF5302 v5	30 July 2025	• CIN 202506007I • Product data sheet • Changed security level from confidential to public • *Features*: added information about industrial versions • *Ordering information*: added OTP programming information, removed table *Feature set comparision* (formerly Table 2) • Table *Ordering information*: updated content and format • *I^2C CRC verification*: updated the polynomial to 0x1D • *Calculating output accuracy with AVP*: updated the first two equations • Removed section *SW1 diode emulation* (formerly 13.1.5.3) along with its figure and table • Table *SW1 electrical parameters*: updated maximum peak current limit for PF5301 • *PF5300 OTP mirror register map*: removed bit fields OTP_SW1_ DIODE_EM_TH[3:0] and OTP_SW1_DIODE_EM_EN • *OTP address 0x30*: removed bit field OTP_SW1_DIODE_EM_TH[3:0] • *OTP address 0x32*: removed bit field OTP_SW1_DIODE_EM_EN • Table *REV register, address 0x01 bit allocation*: changed reset value to 0010 0011 • Added Table *EMREV register, address 0x02 bit allocation* • Added Table *EMREV register bit description* • Added Table *PROGID register, address 0x03 bit allocation* • Added Table *PROGID register bit description* • *Debug operation*: updated procedure • *Layout guidelines*: added recommendations regarding PVIN/VIN, boot capacitor, and LX trace node • Added *Industrial package* • Added v2 changes that were inadvertently removed in the v4 release back into revision history • Updated legal information
PF5300 v4	20 February 2024	• CIN 202402010I • *Ordering information*: added statement about OTP emulation and programming • Updated legal information
PF5300 v3	29 November 2023	• Table *SW1 electrical parameters*: Changed Parameter name from "Switching frequency range" to "SW frequency range under steady state" • Table *ESD ratings*: Updated all "Min" and "Max values." • *Voltage monitoring* – Added paragraph beginning "… The debounce timer ..." – Added description text beginning "All parameters are specified ..." to Table *SW1 UV threshold selection*, Table *SW1 OV threshold selection*, Table *SW1 UV monitor debounce selection*, and Table *SW1 OV monitor debounce selection* • Table *OTP Address 0x30 bit description*: Changed Description of Bit 2 for "1b'0" from "DVS ramp down during power up" to "DVS ramp down during power down" • Updated Table *REV register bit description* • Updated *Package outline* and *Soldering*: Corrected typo in figures from "4.5 mm x 3.5 mm x 0.68 mm" to "3.5 mm x 4.5 mm x 0.68 mm"

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Document ID	Release date	Description
PF5300 v2	26 May 2023	Table *Ordering information*: changed package dimensions for all parts to 4.5 mm x 3.5 mm x 0.68 mm, from 4.5 mm x 3.5 mm x 0.75 mm. • Added *Soldering* • Added disclaimer regarding suitability for use in industrial applications (functional safety)
PF5300 v1	27 April 2023	Initial version

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

Suitability for use in automotive applications (functional safety) — This NXP product has been qualified for use in automotive applications. It has been developed in accordance with ISO 26262, and has been ASIL classified accordingly. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as "Critical Applications"), then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys' fees) that NXP may incur related to customer's incorporation of any product in a Critical Application.

Suitability for use in industrial applications (functional safety) — This NXP product has been qualified for use in industrial applications. It has been developed in accordance with IEC 61508, and has been SIL-classified accordingly. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as "Critical Applications"), then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys' fees) that NXP may incur related to customer's incorporation of any product in a Critical Application.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Tables

Tab. 1. Ordering information 4
Tab. 2. Feature comparison 5
Tab. 3. Pin descriptions 8
Tab. 4. Absolute maximum ratings 10
Tab. 5. ESD ratings 11
Tab. 6. Thermal characteristics 11
Tab. 7. QFN24 thermal resistance and package dissipation ratings 11
Tab. 8. Operating Conditions 12
Tab. 9. State transition table 15
Tab. 10. UVDET thresholds 25
Tab. 11. VIN_OVLO debounce configuration 25
Tab. 12. VIN_OVLO specifications 26
Tab. 13. Power-up timebase register 26
Tab. 14. Power-up sequence registers 27
Tab. 15. OTP_PD_SEQ_DLY[2:0] configuration 28
Tab. 16. Fault counter limit configuration 29
Tab. 17. Fault types and the corresponding PGOOD pin responses 31
Tab. 18. Interrupt Registers 33
Tab. 19. I/O Electrical Characteristics 33
Tab. 20. STANDBY/Syncin Configuration 34
Tab. 21. STANDBY pin polarity control 35
Tab. 22. PGOOD monitoring electrical parameters 36
Tab. 23. I2C address configuration 37
Tab. 24. SW1 voltage selection (Also applicable to SW1_STBY_VOLT[7:0]) 41
Tab. 25. AVP settings 42
Tab. 26. SW1 Current Sense and AVP Accuracy 43
Tab. 27. OTP_SW1_GM[3:0] selection 46
Tab. 28. OTP_SW1_ RCOMP[3:0] selection 47
Tab. 29. OTP_SW1_ COMP_C[3:0] selection 47
Tab. 30. SW1 Mode Selection 48
Tab. 31. VMON OV/UV settings 48
Tab. 32. SW1 slew rate selection 49
Tab. 33. SW1 electrical parameters 49
Tab. 34. SW1 UV threshold selection 50
Tab. 35. SW1 OV threshold selection 51
Tab. 36. SW1 UV monitor debounce selection 52
Tab. 37. SW1 OV monitor debounce selection 52
Tab. 38. Manual frequency tuning configuration 54
Tab. 39. Spread spectrum configuration 54
Tab. 40. Clock management specifications 56
Tab. 41. Thermal monitor specifications 57
Tab. 42. Thermal monitor bit description 58
Tab. 43. Watchdog window duration configuration 58
Tab. 44. Watchdog error count configuration 59
Tab. 45. PF5300 OTP map 62
Tab. 46. OTP address 0x2A bit allocation 63
Tab. 47. OTP address 0x2A bit description 63
Tab. 48. OTP address 0x2B bit allocation 63
Tab. 49. OTP address 0x2B bit description 64
Tab. 50. OTP address 0x2C bit allocation 64
Tab. 51. OTP address 0x2C bit description 64
Tab. 52. OTP address 0x2D bit allocation 64
Tab. 53. OTP address 0x2D bit description 65
Tab. 54. OTP address 0x2E bit allocation 65
Tab. 55. OTP address 0x2E bit description 65
Tab. 56. OTP address 0x2F bit allocation 66
Tab. 57. OTP address 0x2F bit description 66
Tab. 58. OTP address 0x20 bit allocation 67
Tab. 59. OTP address 0x20 bit description 67
Tab. 60. OTP address 0x21 bit allocation 68
Tab. 61. OTP address 0x21 bit description 68
Tab. 62. OTP address 0x22 bit allocation 68
Tab. 63. OTP address 0x22 bit description 69
Tab. 64. OTP address 0x23 bit allocation 70
Tab. 65. OTP address 0x23 bit description 70
Tab. 66. OTP address 0x24 bit allocation 70
Tab. 67. OTP address 0x24 bit description 71
Tab. 68. OTP address 0x25 bit allocation 72
Tab. 69. OTP address 0x25 bit description 73
Tab. 70. OTP address 0x26 bit allocation 74
Tab. 71. OTP address 0x26 bit description 74
Tab. 72. OTP address 0x27 bit allocation 75
Tab. 73. OTP address 0x27 bit description 75
Tab. 74. OTP address 0x28 bit allocation 76
Tab. 75. OTP address 0x28 bit description 76
Tab. 76. OTP address 0x29 bit allocation 77
Tab. 77. OTP address 0x29 bit description 77
Tab. 78. OTP address 0x30 bit allocation 78
Tab. 79. OTP address 0x30 bit description 78
Tab. 80. OTP address 0x31 bit allocation 78
Tab. 81. OTP address 0x31 bit description 79
Tab. 82. OTP address 0x32 bit allocation 79
Tab. 83. OTP address 0x32 bit description 80
Tab. 84. OTP address 0x33 bit allocation 80
Tab. 85. OTP address 0x33 bit description 80
Tab. 86. OTP address 0x34 bit allocation 81
Tab. 87. OTP address 0x34 bit description 81
Tab. 88. OTP address 0x35 bit allocation 82
Tab. 89. OTP address 0x35 bit description 82
Tab. 90. OTP address 0x36 bit allocation 83
Tab. 91. OTP address 0x36 bit description 83
Tab. 92. OTP address 0x37 bit allocation 84
Tab. 93. OTP address 0x37 bit description 84
Tab. 94. PF5300 functional register map 84
Tab. 95. DEVICE_ID register, address 0x00 bit allocation 86
Tab. 96. DEVICE_ID register bit description 86
Tab. 97. REV register, address 0x01 bit allocation 86
Tab. 98. REV register bit description 87
Tab. 99. CONFIG1 register, address 0x04 bit allocation 88
Tab. 100. CONFIG1 register bit description 89
Tab. 101. INT_STATUS1 register, address 0x05 bit allocation 90
Tab. 102. INT_STATUS1 register bit description 90
Tab. 103. INT_SENSE1 register, Address 0x06 bit allocation 91
Tab. 104. INT_SENSE1 register bit description 92

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Tab. 105. INT_STATUS2 register, address 0x07 bit allocation 93
Tab. 106. INT_STATUS2 register bit description 93
Tab. 107. EMREV register, address 0x02 bit allocation 94
Tab. 108. EMREV register bit description 95
Tab. 109. PROGID register, address 0x03 bit allocation 95
Tab. 110. PROGID register bit description 96
Tab. 111. INT_SENSE2 register, address 0x08 bit allocation 97
Tab. 112. INT_SENSE2 register bit description 97
Tab. 113. BIST_STAT1 register bit allocation 99
Tab. 114. BIST_STAT1 register bit description 99
Tab. 115. BIST_CTRL register, address 0x0A bit allocation 100
Tab. 116. BIST_CTRL register bit description 101
Tab. 117. STATE register, address 0x0B bit allocation .. 101
Tab. 118. STATE register bit description 102
Tab. 119. STATE_CTRL register, address 0x0C bit allocation 103
Tab. 120. STATE_CTRL register bit description 103
Tab. 121. SW1_VOLT register, address 0x0D bit allocation 104
Tab. 122. SW1_VOLT register bit description 104
Tab. 123. SW1_STBY_VOLT register, address 0x0E bit allocation 105
Tab. 124. SW1_STBY_VOLT register bit description 105
Tab. 125. SW1_CTRL1 register bit allocation table 105
Tab. 126. SW1_CTRL1 register bit description 105
Tab. 127. SW1_CTRL2 register, address 0x10 bit allocation 106
Tab. 128. SW1_CTRL2 register bit description 106
Tab. 129. SEQ_CTRL1 register, address 0x12 bit allocation 108
Tab. 130. SEQ_CTRL1 register bit description 108
Tab. 131. SEQ_CTRL2 register, address 0x13 bit allocation 109
Tab. 132. SEQ_CTRL2 register bit description 109
Tab. 133. RANDOM_CHK register, address 0x14 bit allocation 109
Tab. 134. RANDOM_CHK register bit description 109
Tab. 135. RANDOM_GEN register, address 0x15 bit allocation 110
Tab. 136. RANDOM_GEN register bit description 110
Tab. 137. WD_CTRL1 register, address 0x16 bit allocation 110
Tab. 138. WD_CTRL1 register bit description 110
Tab. 139. WD_SEED register, address 0x17 bit allocation 111
Tab. 140. WD_SEED register bit description 111
Tab. 141. WD_ANSWER register, address 0x18 bit allocation 112
Tab. 142. WD_ANSWER register bit description 112
Tab. 143. FLT_CNT1 register, address 0x19 bit allocation 112
Tab. 144. FLT_CNT1 register bit description 112
Tab. 145. FLT_CNT2 register, address 0x1A bit allocation 113
Tab. 146. FLT_CNT2 register bit description 113
Tab. 147. Iq and timing specifications 117

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Figures

Fig. 1. Simplified application diagram 3
Fig. 2. PF5300 internal block diagram 7
Fig. 3. PF5300 pinout (bottom view) 8
Fig. 4. Functional block diagram 13
Fig. 5. State machine diagram 14
Fig. 6. IO_Release state behavior - SW1 and PGOOD release during power-up sequence 21
Fig. 7. IO_Release state behavior - SW1 and PGOOD release during power-up sequence - PGOOD held low externally 21
Fig. 8. IO_Release state behavior - SW1 up during power-up sequence - PGOOD_SEQ = 0 (software release) 22
Fig. 9. IO_Release state behavior - SW1 up during power-up sequence; PGOOD_SEQ = 0 (software release) but externally asserted low 22
Fig. 10. SW1/PGOOD sequence example 1 28
Fig. 11. SW1/PGOOD sequence example 2 29
Fig. 12. Multi-PMIC interface diagram 33
Fig. 13. XFAILB during power up 36
Fig. 14. XFAILB during power down 37
Fig. 15. 8 bit SAE J1850 CRC polynomial 38
Fig. 16. SW1 DC-DC Architecture 40
Fig. 17. Adaptive-voltage positioning illustration 42
Fig. 18. Vout tolerance calculation 44
Fig. 19. TON extension for faster response 46
Fig. 20. Triangular spread-spectrum modulation 55
Fig. 21. Pseudo-random spread-spectrum modulation 55
Fig. 22. Thermal monitoring architecture 57
Fig. 23. Watchdog timer and error counter 60
Fig. 24. SW1 soft-start (MPF53BDAMMA1ES); 100 µs/DIV 118
Fig. 25. SW1 output ripple (MPF53BDAMMA1ES) ~ 3 mV 119
Fig. 26. SW1 load transient response with AVP 119
Fig. 27. SW1 load transient response without AVP 120
Fig. 28. PWM efficiency, Vout = 1.0 V 120
Fig. 29. PWM efficiency, Vout = 0.9 V 121
Fig. 30. PWM efficiency, Vout = 0.8 V 121
Fig. 31. PWM efficiency, Vout = 0.7 V 122
Fig. 32. PFM Mode 3.3 Vin 0.65 Vout 122
Fig. 33. PFM Mode 5 Vin 0.65 Vout 123
Fig. 34. PFM Mode 3.3 Vin 0.80 Vout 123
Fig. 35. PFM Mode 5 Vin 0.80 Vout 124
Fig. 36. SW1 load regulation at different AVP settings 124
Fig. 37. SW1 current limit entry and exit: Vout drops and recovers smoothly 125
Fig. 38. SW1 turn-off with OTP_SW1_RDIS = 1 and OTP_SW1_HIZOFF = 1 125
Fig. 39. Typical application schematic 126
Fig. 40. KITPF5300FRDMEVM top layout 127
Fig. 41. Boot capacitor placed at the bottom layer 128
Fig. 42. Package outline 129
Fig. 43. Package outline details 130
Fig. 44. Notes 131
Fig. 45. Reflow soldering footprint part1 for HVQFN24 (SOT2090-1(SC)) 132
Fig. 46. Reflow soldering footprint part2 for HVQFN24 (SOT2090-1(SC)) 133
Fig. 47. Reflow soldering footprint part3 for HVQFN24 (SOT2090-1(SC)) 134
Fig. 48. Reflow soldering footprint part4 for HVQFN24 (SOT2090-1(SC)) 135
Fig. 49. Reflow soldering footprint part5 for HVQFN24 (SOT2090-1(SC)) 136
Fig. 50. Reflow soldering footprint part6 for HVQFN24 (SOT2090-1(SC)) 137
Fig. 51. Package outline H-FC-PQFN24 (SOT2090-1) 138
Fig. 52. Package outline detail E and G of H-FC-PQFN24 (SOT2090-1) 139
Fig. 53. Package outline notes H-FC-PQFN24 (SOT2090-1) 140
Fig. 54. Reflow soldering footprint part1 H-FC-PQFN24 (SOT2090-1)) 141
Fig. 55. Reflow soldering footprint part2 H-FC-PQFN24 (SOT2090-1) 142
Fig. 56. Reflow soldering footprint part3 H-FC-PQFN24 (SOT2090-1) 143
Fig. 57. Reflow soldering footprint part4 H-FC-PQFN24 (SOT2090-1) 144
Fig. 58. Reflow soldering footprint part5 H-FC-PQFN24 (SOT2090-1) 145
Fig. 59. Reflow soldering footprint part6 H-FC-PQFN24 (SOT2090-1) 146
Fig. 60. Package outline 147
Fig. 61. Package outline details 148
Fig. 62. Notes 149
Fig. 63. Reflow soldering footprint part1 for HVQFN24 (SOT2090-1(SC)) 150
Fig. 64. Reflow soldering footprint part2 for HVQFN24 (SOT2283-1(SC)) 151
Fig. 65. Reflow soldering footprint part3 for HVQFN24 (SOT2283-1(SC)) 152
Fig. 66. Reflow soldering footprint part4 for HVQFN24 (SOT2283-1(SC)) 153
Fig. 67. Reflow soldering footprint part5 for HVQFN24 (SOT2283-1(SC)) 154
Fig. 68. Reflow soldering footprint part6 for HVQFN24 (SOT2283-1(SC)) 155
Fig. 69. Package outline H-FC-PQFN24 (SOT2090-1) 156
Fig. 70. Package outline detail E and G of H-FC-PQFN24 (SOT2283-1) 157
Fig. 71. Package outline notes H-FC-PQFN24 (SOT2283-1) 158
Fig. 72. Reflow soldering footprint part1 H-FC-PQFN24 (SOT2283-1)) 159

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Fig. 73. Reflow soldering footprint part2 H-FC-PQFN24 (SOT2283-1) 160
Fig. 74. Reflow soldering footprint part3 H-FC-PQFN24 (SOT2283-1) 161
Fig. 75. Reflow soldering footprint part4 H-FC-PQFN24 (SOT2283-1) 162
Fig. 76. Reflow soldering footprint part5 H-FC-PQFN24 (SOT2283-1) 163
Fig. 77. Reflow soldering footprint part6 H-FC-PQFN24 (SOT2283-1) 164

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

Contents

1 Overview 1
2 Features 2
3 Simplified application diagram 3
4 Ordering information 4
5 Applications 6
6 Internal block diagram 7
7 Pinning information 8
7.1 Pinout 8
7.2 Pin descriptions 8
8 Absolute maximum ratings 10
9 Characteristics 11
9.1 ESD ratings 11
9.2 Thermal characteristics 11
9.3 Recommended operating conditions 12
10 General description 13
10.1 Functional block diagram 13
11 State machine 14
11.1 State descriptions 19
11.1.1 ULP_Off state 19
11.1.2 Load fuses 19
11.1.3 LP_Off state 19
11.1.4 Self-test routine (PF5300 ASIL B and ASIL D only) 19
11.1.4.1 ABIST test on all voltage monitors 20
11.1.5 Power-up sequence 20
11.1.6 IO_Release state 20
11.1.7 INIT state 22
11.1.8 System ON state 23
11.1.9 Power-down state 23
11.1.10 Fail-safe state 23
12 General device operation 25
12.1 UVDET 25
12.2 VIN OVLO condition 25
12.3 Power up 26
12.3.1 Power-up events 26
12.3.2 Power-up sequencing 26
12.4 Power down 27
12.4.1 Turn-off events 27
12.4.2 Power-down sequencing 27
12.5 Fault management 29
12.6 Interrupt management 32
12.7 I/O interface pins 33
12.7.1 PWRON 34
12.7.2 STANDBY/SYNCIN 34
12.7.3 PGOOD 35
12.7.4 XFAILB 36
12.7.5 SDA and SCL (I²C bus) 37
12.7.5.1 I²C CRC verification 38
12.7.5.2 I²C secure write 38
13 Functional blocks 40
13.1 SW1: DC-DC regulator 40
13.1.1 SW1 architecture 40
13.1.2 SW1 output voltage selection 40
13.1.3 SW1 adaptive-voltage positioning (AVP) 42
13.1.4 Calculating output accuracy with AVP 43
13.1.4.1 Accuracy of the current sense circuit and the AVP loop 43
13.1.4.2 Calculating total output voltage tolerance with AVP 43
13.1.5 Compensating the SW1 loop 45
13.1.5.1 SW1 PLL 46
13.1.5.2 SW1 TON dominant operation 46
13.1.5.3 SW1 GM, RCOMP, and CCOMP 46
13.1.5.4 OTP_SW1_AVP_FILT[1:0] and OTP_SW1_LSEL[1:0] 48
13.1.6 SW1 operation mode selection 48
13.1.7 SW1 soft-start and DVS selection 48
13.2 Voltage monitoring 50
13.3 ABIST verification 52
13.4 Clock management 53
13.4.1 Low-frequency clock 53
13.4.2 High-frequency clock and SW1 switching frequency 53
13.4.3 Manual frequency tuning 54
13.4.4 Spread spectrum 54
13.4.5 Clock synchronization 55
13.5 Thermal monitoring 56
13.6 Watchdog timer 58
13.6.1 Simple watchdog (OTP_WD_SEL = 0) 60
13.6.2 Challenger watchdog (OTP_WD_SEL = 1) 60
14 I²C register map 61
14.1 PF5300 OTP mirror register map 62
14.1.1 OTP address 0x2A 63
14.1.2 OTP address 0x2B 63
14.1.3 OTP address 0x2C 64
14.1.4 OTP address 0x2D 64
14.1.5 OTP address 0x2E 65
14.1.6 OTP address 0x2F 66
14.1.7 OTP address 0x20 67
14.1.8 OTP address 0x21 68
14.1.9 OTP address 0x22 68
14.1.10 OTP address 0x23 70
14.1.11 OTP address 0x24 70
14.1.12 OTP address 0x25 72
14.1.13 OTP address 0x26 74
14.1.14 OTP address 0x27 75
14.1.15 OTP address 0x28 76
14.1.16 OTP address 0x29 77
14.1.17 OTP address 0x30 78
14.1.18 OTP address 0x31 78
14.1.19 OTP address 0x32 79
14.1.20 OTP address 0x33 80
14.1.21 OTP address 0x34 81
14.1.22 OTP address 0x35 82
14.1.23 OTP address 0x36 83
14.1.24 OTP address 0x37 84
14.2 PF5300 functional register map 84
14.2.1 DEVICE_ID register 86
14.2.2 REV register 86
14.2.3 CONFIG1 register 88
14.2.4 INT_STATUS1 register 90

All information provided in this document is subject to legal disclaimers.

© 2026 NXP B.V. All rights reserved.

14.2.5 INT_SENSE1 register 91
14.2.6 INT_STATUS2 register 93
14.2.7 EMREV and PROGID registers 94
14.2.8 INT_SENSE2 register 97
14.2.9 BIST_STAT1 register 99
14.2.10 BIST_CTRL register 100
14.2.11 STATE register 101
14.2.12 STATE_CTRL register 103
14.2.13 SW1_VOLT register 104
14.2.14 SW1_STBY_VOLT register 105
14.2.15 SW1_CTRL1 register 105
14.2.16 SW1_CTRL2 register 106
14.2.17 CLK_CTRL register 107
14.2.18 SEQ_CTRL1 register 108
14.2.19 SEQ_CTRL2 register 109
14.2.20 RANDOM_CHK register 109
14.2.21 RANDOM_GEN register 110
14.2.22 WD_CTRL1 register 110
14.2.23 WD_SEED register 111
14.2.24 WD_ANSWER register 112
14.2.25 FLT_CNT1 register 112
14.2.26 FLT_CNT2 register 113
15 OTP programming Debug mode 115
15.1 Debug operation 115
15.2 OTP fuse programming 115
16 Functional safety 116
16.1 System safety strategy 116
17 IC level current and timing specifications 117
18 Typical performance curves 118
19 Schematic and layout guidelines 126
19.1 Schematic example 126
19.2 Layout guidelines 127
20 Package drawing 129
20.1 Automotive package, A 129
20.1.1 Package outline, A 129
20.1.2 Soldering, A 132
20.2 Industrial package, A 138
20.2.1 Package outline, A 138
20.2.2 Soldering, A 141
20.3 Automotive package, B 147
20.3.1 Package outline, B 147
20.3.2 Soldering, B 150
20.4 Industrial package, B 156
20.4.1 Package outline, B 156
20.4.2 Soldering, B 159
21 Revision history 165
Legal information 168

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© 2026 NXP B.V. **All rights reserved.**

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View MPF5301AMBA0ES on WIN SOURCE
- NXP / Nexperia Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management