# THE DATASHEET OF

# LC75836WS-E

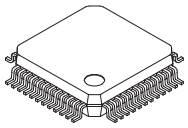
www.win-source.net 0086-755-83957316

# LC75836W

# 1/4-Duty General-Purpose LCD Driver

ON Semiconductor®

www.onsemi.com



SPQFP48 7x7 / SQFP48

## Overview

The LC75836W is 1/4-duty general-purpose microprocessor-controlled LCD driver that can be used in applications such as frequency display in products with electronic tuning. In addition to being able to drive up to 140 segments directly, the LC75836W can also control up to 4 general-purpose output ports.

## Features

- 1/4 duty, 1/3 bias drive (Up to 140 segment can be displayed.)
- Serial data input supports CCB* format communication with the system controller (support 3 V operation).
- Serial data control of the power-saving mode based backup function and the all segments forced off function.
- Serial data control of switching between the segment output port and general-purpose output port functions.
- Serial data control of the frame frequency of the common and segment output waveforms.
- Either RC oscillator operating or external clock operating mode can be selected with the serial control data.
- High generality, since display data is displayed directly without the intervention of a decoder circuit.
- The $\overline{\text{INH}}$ pin allows the display to be forced to the off state.
- RC oscillation circuit (with external resistor and capacitor)

* Computer Control Bus (CCB) is an ON Semiconductor's original bus format and the bus addresses are controlled by ON Semiconductor.

## ORDERING INFORMATION

See detailed ordering and shipping information on page 17 of this data sheet.

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## Specifications

### Absolute Maximum Ratings at Ta = 25°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum supply voltage | $V_{DD}$ max | $V_{DD}$ | −0.3 to +7.0 | V |
| Input voltage | $V_{IN}1$ | CE, CL, DI, $\overline{INH}$ | −0.3 to +7.0 | V |
| | $V_{IN}2$ | OSC, $V_{DD}1$, $V_{DD}2$ | −0.3 to $V_{DD}$+0.3 | |
| Output voltage | $V_{OUT}$ | S1 to S35, COM1 to COM4, P1 to P4, OSC | −0.3 to $V_{DD}$+0.3 | V |
| Output current | $I_{OUT}1$ | S1 to S35 | 300 | μA |
| | $I_{OUT}2$ | COM1 to COM4 | 3 | mA |
| | $I_{OUT}3$ | P1 to P4 | 5 | |
| Allowable power dissipation | Pdmax | Ta = 85°C | 100 | mW |
| Operating temperature | Topr | | −40 to +85 | °C |
| Storage temperature | Tstg | | −55 to +125 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### Allowable Operating Ranges at Ta = −40 to +85°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Supply voltage | $V_{DD}$ | $V_{DD}$ | 4.5 | | 6.0 | V |
| Input voltage | $V_{DD}1$ | $V_{DD}1$ | | 2/3$V_{DD}$ | $V_{DD}$ | V |
| | $V_{DD}2$ | $V_{DD}2$ | | 1/3$V_{DD}$ | $V_{DD}$ | |
| Input high-level voltage | $V_{IH}1$ | CE, CL, DI, $\overline{INH}$ | 0.4$V_{DD}$ | | 6.0 | V |
| | $V_{IH}2$ | OSC external clock operating mode | 0.4$V_{DD}$ | | $V_{DD}$ | |
| Input low-level voltage | $V_{IL}1$ | CE, CL, DI, $\overline{INH}$ | 0 | | 0.2$V_{DD}$ | V |
| | $V_{IL}2$ | OSC external clock operating mode | 0 | | 0.2$V_{DD}$ | |
| Recommended external resistor for RC oscillation | Rosc | OSC RC oscillator operating mode | | 39 | | kΩ |
| Recommended external capacitor for RC oscillation | Cosc | OSC RC oscillator operating mode | | 1000 | | pF |
| Guaranteed range of RC oscillation | fosc | OSC RC oscillator operating mode | 19 | 38 | 76 | kHz |
| External clock operating frequency | $f_{CK}$ | OSC external clock operating mode [Figure 4] | 19 | 38 | 76 | kHz |
| External clock duty cycle | $D_{CK}$ | OSC external clock operating mode [Figure 4] | 30 | 50 | 70 | % |
| Data setup time | tds | CL, DI [Figure 2] [Figure 3] | 160 | | | ns |
| Data hold time | tdh | CL, DI [Figure 2] [Figure 3] | 160 | | | ns |
| CE wait time | tcp | CE, CL [Figure 2] [Figure 3] | 160 | | | ns |
| CE setup time | tcs | CE, CL [Figure 2] [Figure 3] | 160 | | | ns |
| CE hold time | tch | CE, CL [Figure 2] [Figure 3] | 160 | | | ns |
| High-level clock pulse width | tϕH | CL [Figure 2] [Figure 3] | 160 | | | ns |
| Low-level clock pulse width | tϕL | CL [Figure 2] [Figure 3] | 160 | | | ns |
| Rise time | tr | CE, CL, DI [Figure 2] [Figure 3] | | 160 | | ns |
| Fall time | tf | CE, CL, DI [Figure 2] [Figure 3] | | 160 | | ns |
| $\overline{INH}$ switching time | tc | $\overline{INH}$, CE [Figure 5] | 10 | | | μs |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**Electrical Characteristics** for the Allowable Operating Ranges

| Parameter | Symbol | Pin | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | min | typ | max | |
| Hysteresis | $V_H$ | CE, CL, DI, $\overline{INH}$ | | | $0.03V_{DD}$ | | V |
| Input high-level current | $I_{IH}1$ | CE, CL, DI, $\overline{INH}$ | $V_I$ = 6.0 V | | | 5.0 | μA |
| | $I_{IH}2$ | OSC | $V_I = V_{DD}$ external clock operating mode | | | 5.0 | |
| Input low-level current | $I_{IL}1$ | CE, CL, DI, $\overline{INH}$ | $V_I$ = 0 V | −5.0 | | | μA |
| | $I_{IL}2$ | OSC | $V_I$ = 0 V external clock operating mode | −5.0 | | | |
| Output high-level voltage | $V_{OH}1$ | S1 to S35 | $I_O$ = −20 μA | $V_{DD}$−0.9 | | | V |
| | $V_{OH}2$ | COM1 to COM4 | $I_O$ = −100 μA | $V_{DD}$−0.9 | | | |
| | $V_{OH}3$ | P1 to P4 | $I_O$ = −1 mA | $V_{DD}$−0.9 | | | |
| Output low-level voltage | $V_{OL}1$ | S1 to S35 | $I_O$ = 20 μA | | | 0.9 | V |
| | $V_{OL}2$ | COM1 to COM4 | $I_O$ = 100 μA | | | 0.9 | |
| | $V_{OL}3$ | P1 to P4 | $I_O$ = 1 mA | | | 0.9 | |
| Output middle-level voltage *1 | $V_{MID}1$ | S1 to S35 | 1/3 bias $I_O$ = ±20 μA | $2/3V_{DD}$ −0.9 | | $2/3V_{DD}$ +0.9 | V |
| | $V_{MID}2$ | S1 to S35 | 1/3 bias $I_O$ = ±20 μA | $1/3V_{DD}$ −0.9 | | $1/3V_{DD}$ +0.9 | |
| | $V_{MID}3$ | COM1 to COM4 | 1/3 bias $I_O$ = ±100 μA | $2/3V_{DD}$ −0.9 | | $2/3V_{DD}$ +0.9 | |
| | $V_{MID}4$ | COM1 to COM4 | 1/3 bias $I_O$ = ±100 μA | $1/3V_{DD}$ −0.9 | | $1/3V_{DD}$ +0.9 | |
| Oscillator frequency | fosc | OSC | RC oscillator operating mode Rosc = 39 kΩ, Cosc = 1000 pF | 30.4 | 38 | 45.6 | kHz |
| Current drain | $I_{DD}1$ | $V_{DD}$ | Power-saving mode | | | 5 | μA |
| | $I_{DD}2$ | $V_{DD}$ | $V_{DD}$ = 6.0V output open RC oscillator operating mode fosc = 38 kHz | | 350 | 700 | |
| | $I_{DD}3$ | $V_{DD}$ | $V_{DD}$ = 6.0 V output open External clock operating mode $f_{CK}$ = 38 kHz $V_{IH}2 = 0.5V_{DD}$ $V_{IL}2 = 0.1V_{DD}$ | | 450 | 900 | |

Note: *1 Excluding the bias voltage generation divider resistors built in the $V_{DD}1$ and $V_{DD}2$. (See Figure 1.)

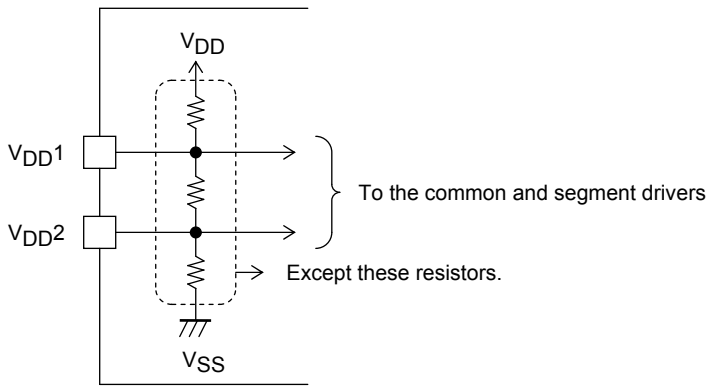



Figure 1

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. When CL is stopped at the low level

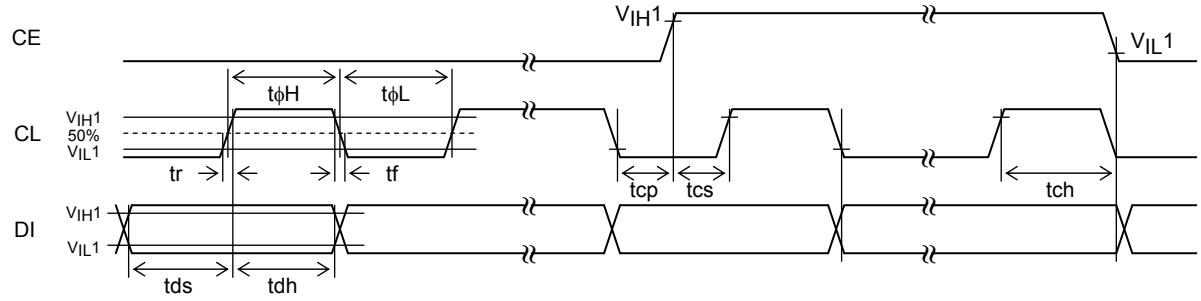



Figure 2

2. When CL is stopped at the high level

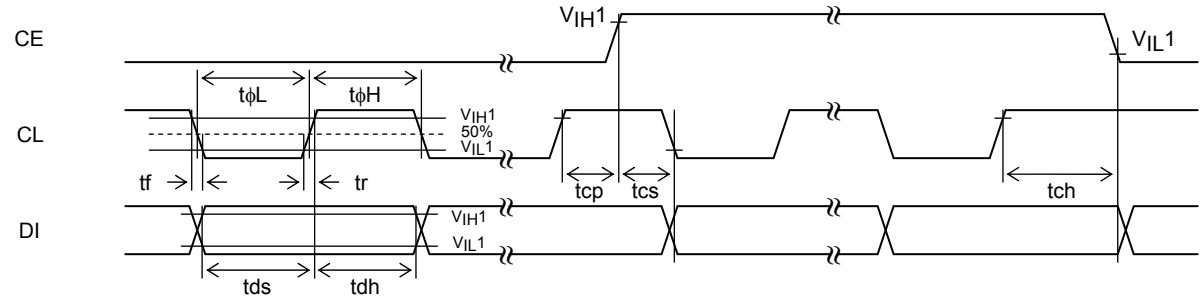
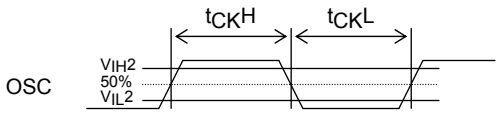



Figure 3

3. OSC pin clock timing in external clock operating mode




$$f_{CK}=\frac{1}{t_{CK}H+t_{CK}L}\ [kHz]$$

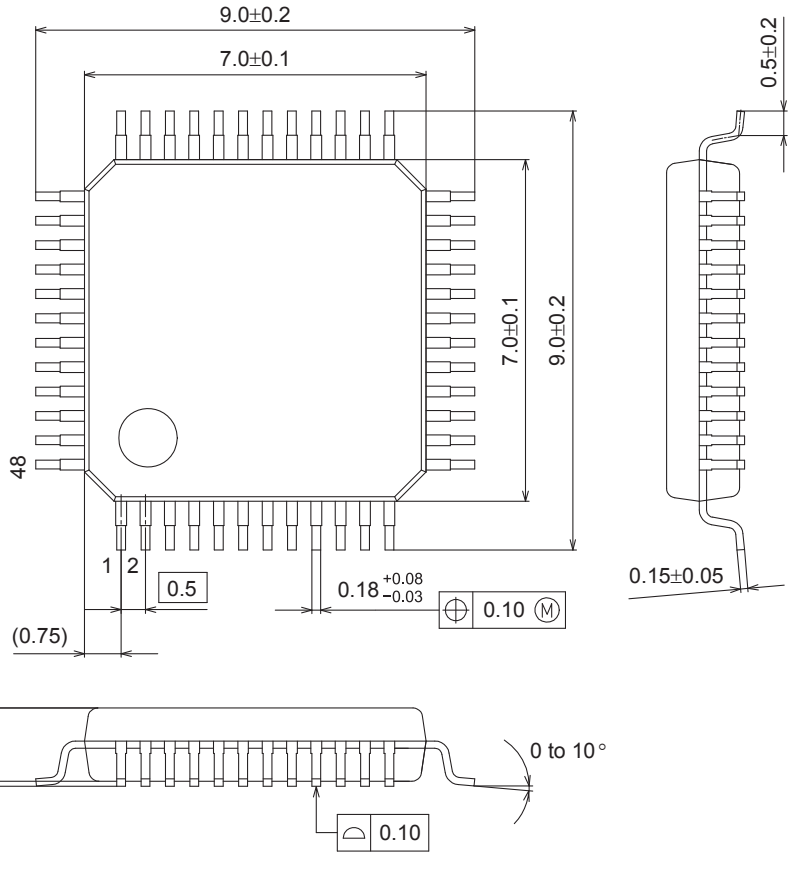
$$D_{CK}=\frac{t_{CK}H}{t_{CK}H+t_{CK}L}\times 100[\%]$$

Figure 4

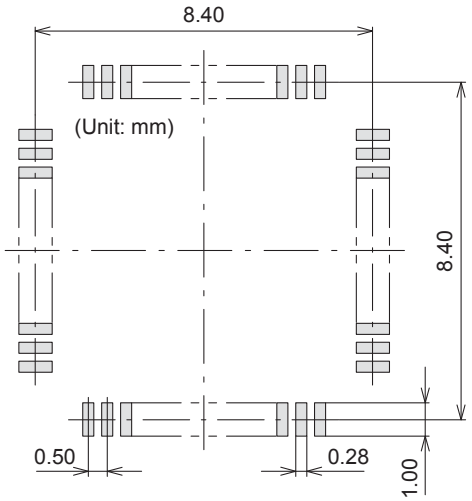
## Package Dimensions

unit : mm

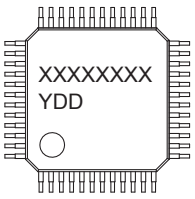
**SPQFP48 7x7 / SQFP48**
CASE 131AJ
ISSUE A



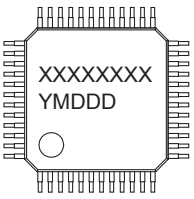

**SOLDERING FOOTPRINT***




**GENERIC MARKING DIAGRAM***




XXXXX = Specific Device Code
Y = Year
DD = Additional Traceability Data



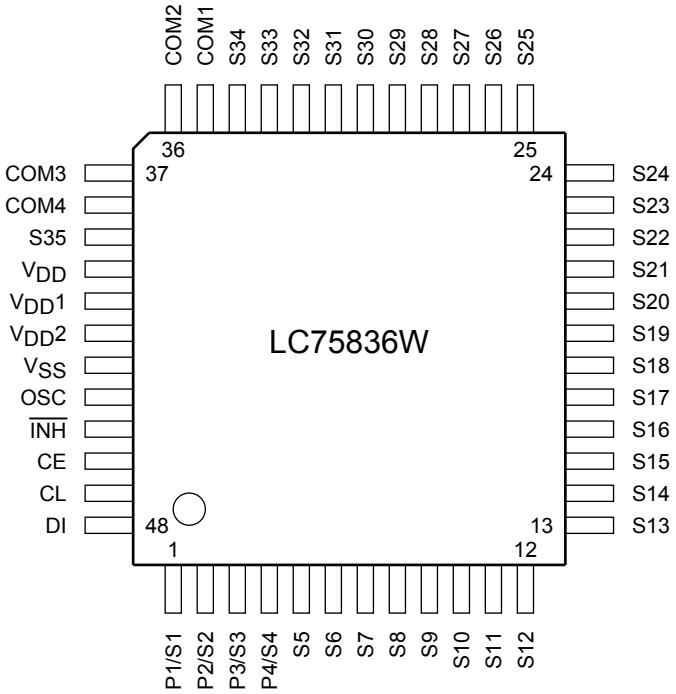

XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic.
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

NOTE: The measurements are not to guarantee but for reference only.

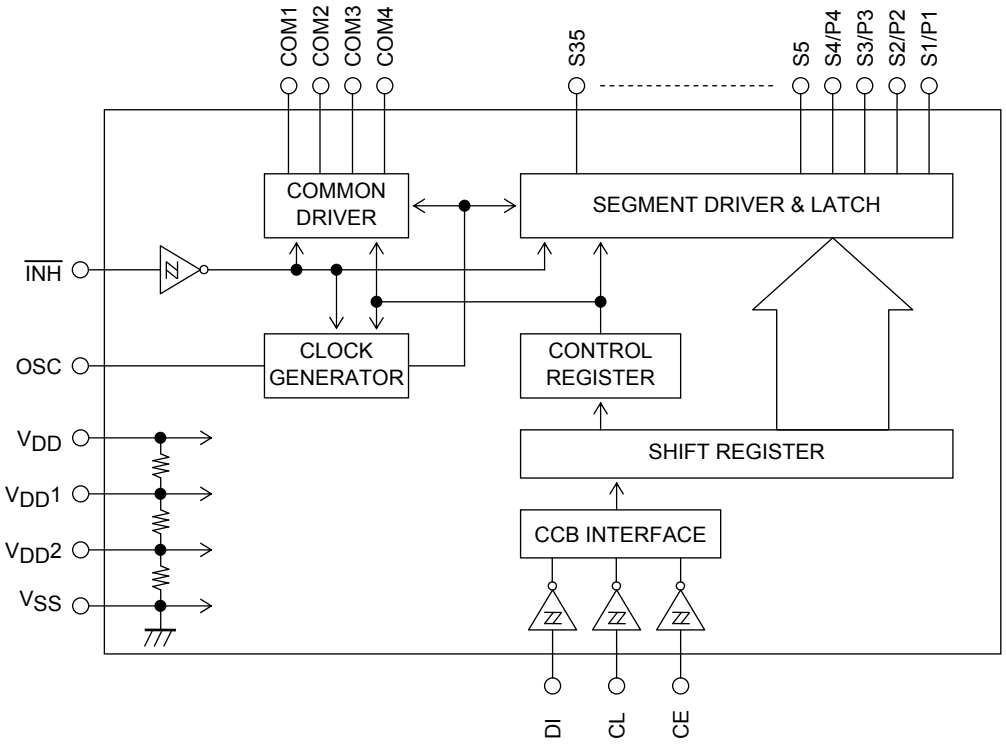
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## Pin Assignment




Top view

## Block Diagram

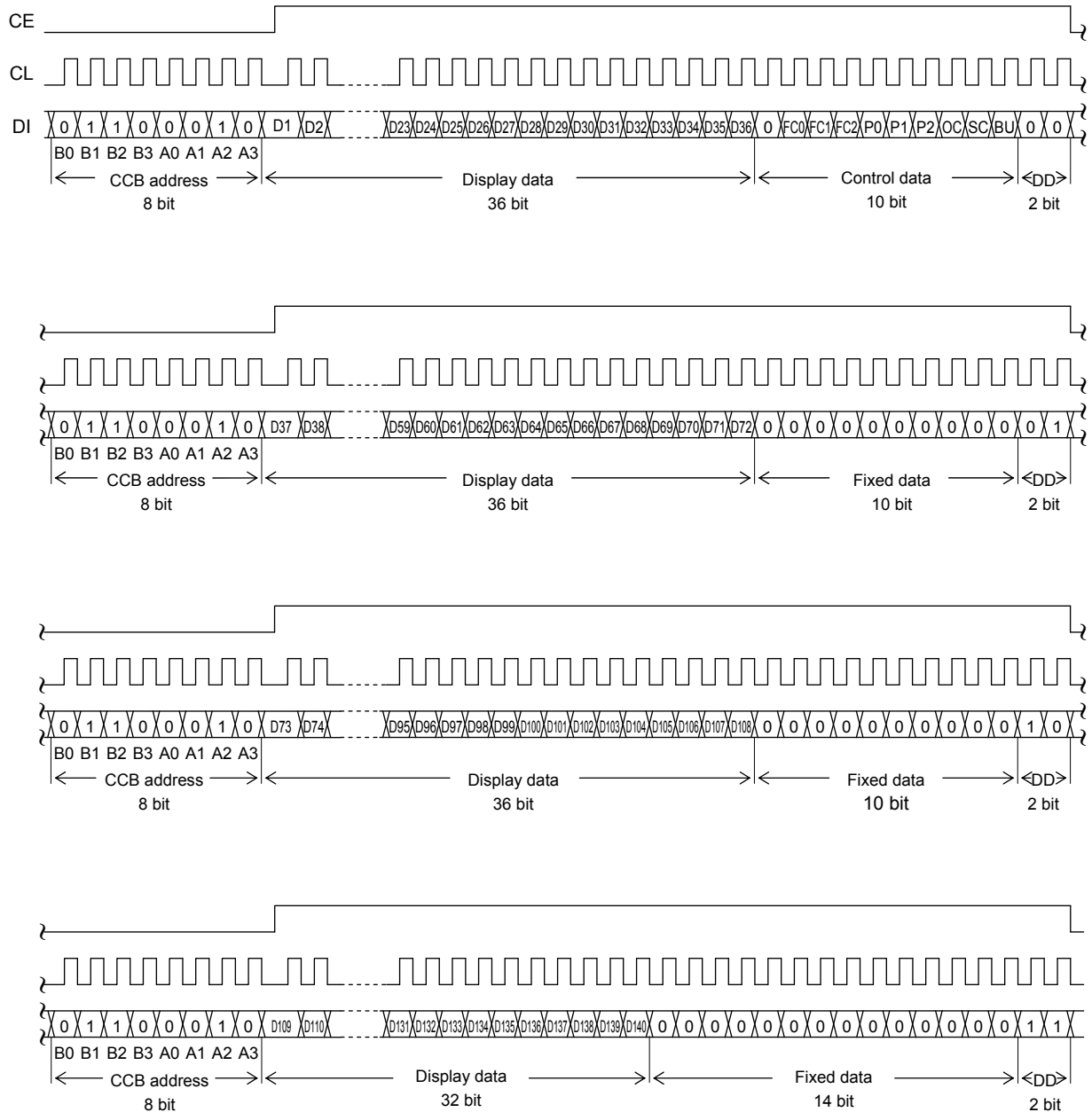


## Pin Functions

| Symbol | Pin No. | Function | Active | I/O | Handling when unused |
|---|---|---|---|---|---|
| S1/P1<br>to S4/P4<br>S5 to S34<br>S35 | 1 to 4<br><br>5 to 34<br>39 | Segment outputs for displaying the display data transferred by serial data input.<br>The S1/P1 to S4/P4 pins can be used as general-purpose output ports when so set up by the control data. | - | O | OPEN |
| COM1<br>to COM4 | 35 to 38 | Common driver outputs. The frame frequency is fo [Hz]. | - | O | OPEN |
| OSC | 44 | Oscillator connection. An oscillator circuit is formed by connecting an external resistor and capacitor to this pin. This pin can be used as the external clock input pin if external clock operating mode is selected with the control data. | - | I/O | $V_{DD}$ |
| CE<br>CL<br>DI | 46<br>47<br>48 | Serial data transfer inputs. Must be connected to the controller.<br>CE: Chip enable<br>CL: Synchronization clock<br>DI: Transfer data | H<br>↑<br>- | I<br>I<br>I | GND |
| $\overline{INH}$ | 45 | Display off control input<br>• $\overline{INH}$ = low ($V_{SS}$) ...Display forced off<br>S1/P1 to S4/P4 = low ($V_{SS}$)<br>(These pins are forcibly set to the segment output port function and held at the $V_{SS}$ level.)<br>S5 to S35 = low ($V_{SS}$)<br>COM1 to COM4 = low ($V_{SS}$)<br>OSC = Z (high impedance)<br>RC oscillation stopped<br>Inhibits external clock input.<br>• $\overline{INH}$ = high ($V_{DD}$)...Display on<br>RC oscillation enabled (RC oscillator operating mode)<br>Enables external clock input (external clock operating mode).<br>However, serial data transfer is possible when the display is forced off. | L | I | GND |
| $V_{DD}1$ | 41 | Used to apply the LCD drive 2/3 bias voltage externally. | - | I | OPEN |
| $V_{DD}2$ | 42 | Used to apply the LCD drive 1/3 bias voltage externally. | - | I | OPEN |
| $V_{DD}$ | 40 | Power supply pin. A power voltage of 4.5 to 6.0 V must be applied to this pin. | - | - | - |
| $V_{SS}$ | 43 | Ground pin. Must be connected to ground. | - | - | - |

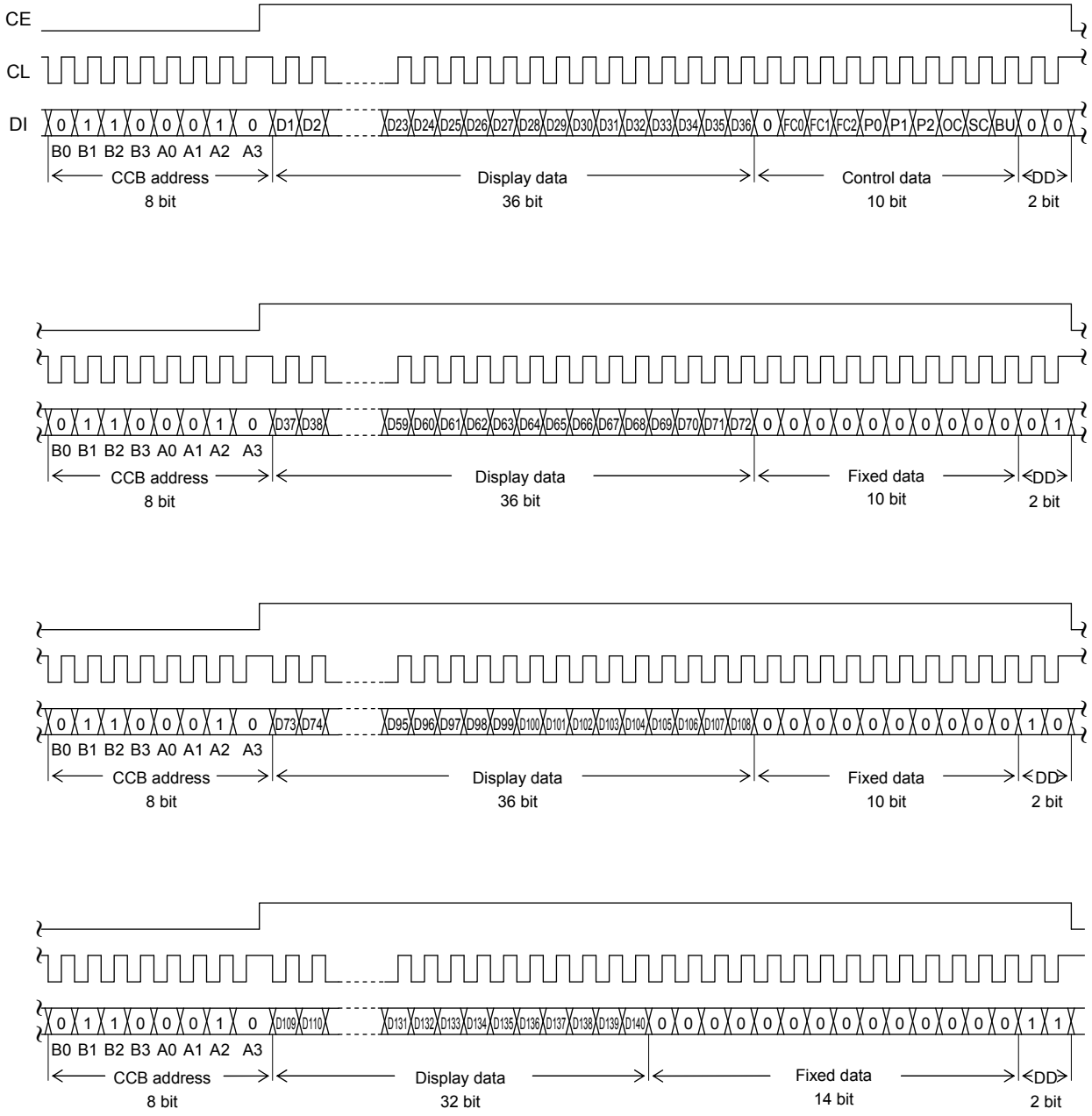
## Serial Data Transfer Formats

1. When CL is stopped at the low level




Note: DD is the direction data.

2. When CL is stopped at the high level




Note: DD is the direction data.

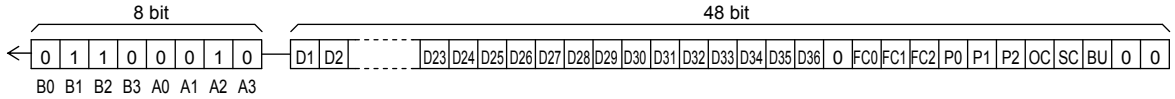
- CCB address ..... "46H"
- D1 to D140 ..... Display data
- FC0 to FC2 ..... Common/segment output waveform frame frequency control data
- P0 to P2 ..... Segment output port/general-purpose output port switching control data
- OC ..... RC oscillator operating mode/external clock operating mode switching control data
- SC ..... Segments on/off control data
- BU ..... Normal mode/power-saving mode control data

## Serial Data Transfer Example

• When 109 or more segments are used
All 192 bits of serial data must be sent.




• When fewer than 109 segments are used
Either 48, 96, or 144 bits of serial data must be sent, depending on the number of segments to be used. However, the serial data shown below (the D1 to D36 display data and the control data) must always be sent.



## Control Data Functions

1. FC0 to FC2: Common/segment output waveform frame frequency control data

These control data bits set the frame frequency of the common and segment output waveforms.

| Control data | | | Frame frequency fo [Hz] |
|---|---|---|---|
| FC0 | FC1 | FC2 | |
| 1 | 1 | 0 | fosc/768,$f_{CK}$/768 |
| 1 | 1 | 1 | fosc/576,$f_{CK}$/576 |
| 0 | 0 | 0 | fosc/384,$f_{CK}$/384 |
| 0 | 0 | 1 | fosc/288,$f_{CK}$/288 |
| 0 | 1 | 0 | fosc/192,$f_{CK}$/192 |

2. P0 to P2: Segment output port/general-purpose output port switching control data

These control data bits switch the segment output port/general-purpose output port functions of the S1/P1 to S4/P4 output pins.

| Control data | | | Output pin state | | | |
|---|---|---|---|---|---|---|
| P0 | P1 | P2 | S1/P1 | S2/P2 | S3/P3 | S4/P4 |
| 0 | 0 | 0 | S1 | S2 | S3 | S4 |
| 0 | 0 | 1 | P1 | S2 | S3 | S4 |
| 0 | 1 | 0 | P1 | P2 | S3 | S4 |
| 0 | 1 | 1 | P1 | P2 | P3 | S4 |
| 1 | 0 | 0 | P1 | P2 | P3 | P4 |

Note: Sn (n = 1 to 4): Segment output ports
Pn (n = 1 to 4): General-purpose output ports

Note that when the general-purpose output port function is selected, the correspondence between the output pins and the display data will be that shown in the table.

| Output pin | Corresponding display data |
|---|---|
| S1/P1 | D1 |
| S2/P2 | D5 |
| S3/P3 | D9 |
| S4/P4 | D13 |

For example, if the general-purpose output port function is selected for the S4/P4 output pin, that output pin will output a high level ($V_{DD}$) when the display data D13 is 1, and a low level ($V_{SS}$) when the D13 is 0.

3. OC: RC oscillator operating mode/external clock operating mode switching control data.

This control data bit switches the OSC pin function
(either RC oscillator operating mode or external clock operating mode).

| OC | OSC pin function |
|---|---|
| 0 | RC oscillator operating mode |
| 1 | External clock operating mode |

Note: An external resistor, Rosc, and an external capacitor, Cosc, must be connected to the OSC pin if RC oscillator operating mode is selected.

4. SC: Segment on/off control data

This control data bit controls the on/off state of the segments.

| SC | Display state |
|---|---|
| 0 | On |
| 1 | Off |

Note that when the segments are turned off by setting SC to 1, the segments are turned off by outputting segment off waveforms from the segment output pins.

5. BU: Normal mode/power-saving mode control data

This control data bit selects either normal mode or power saving mode.

| BU | Mode |
|---|---|
| 0 | Normal mode |
| 1 | Power saving mode.<br>In RC oscillator operating mode (OC = 0), the OSC pin oscillator is stopped, and in external clock operating mode (OC = 1), acceptance of the external clock is stopped. In this mode the common and segment output pins go to the $V_{SS}$ levels. However, S1/P1 to S4/P4 output pins that are set to be general-purpose output ports by the control data P0 to P2 can be used as general-purpose output ports. |

Display Data and Output Pin Correspondence

| Output pin | COM1 | COM2 | COM3 | COM4 |
|---|---|---|---|---|
| S1/P1 | D1 | D2 | D3 | D4 |
| S2/P2 | D5 | D6 | D7 | D8 |
| S3/P3 | D9 | D10 | D11 | D12 |
| S4/P4 | D13 | D14 | D15 | D16 |
| S5 | D17 | D18 | D19 | D20 |
| S6 | D21 | D22 | D23 | D24 |
| S7 | D25 | D26 | D27 | D28 |
| S8 | D29 | D30 | D31 | D32 |
| S9 | D33 | D34 | D35 | D36 |
| S10 | D37 | D38 | D39 | D40 |
| S11 | D41 | D42 | D43 | D44 |
| S12 | D45 | D46 | D47 | D48 |
| S13 | D49 | D50 | D51 | D52 |
| S14 | D53 | D54 | D55 | D56 |
| S15 | D57 | D58 | D59 | D60 |
| S16 | D61 | D62 | D63 | D64 |
| S17 | D65 | D66 | D67 | D68 |
| S18 | D69 | D70 | D71 | D72 |

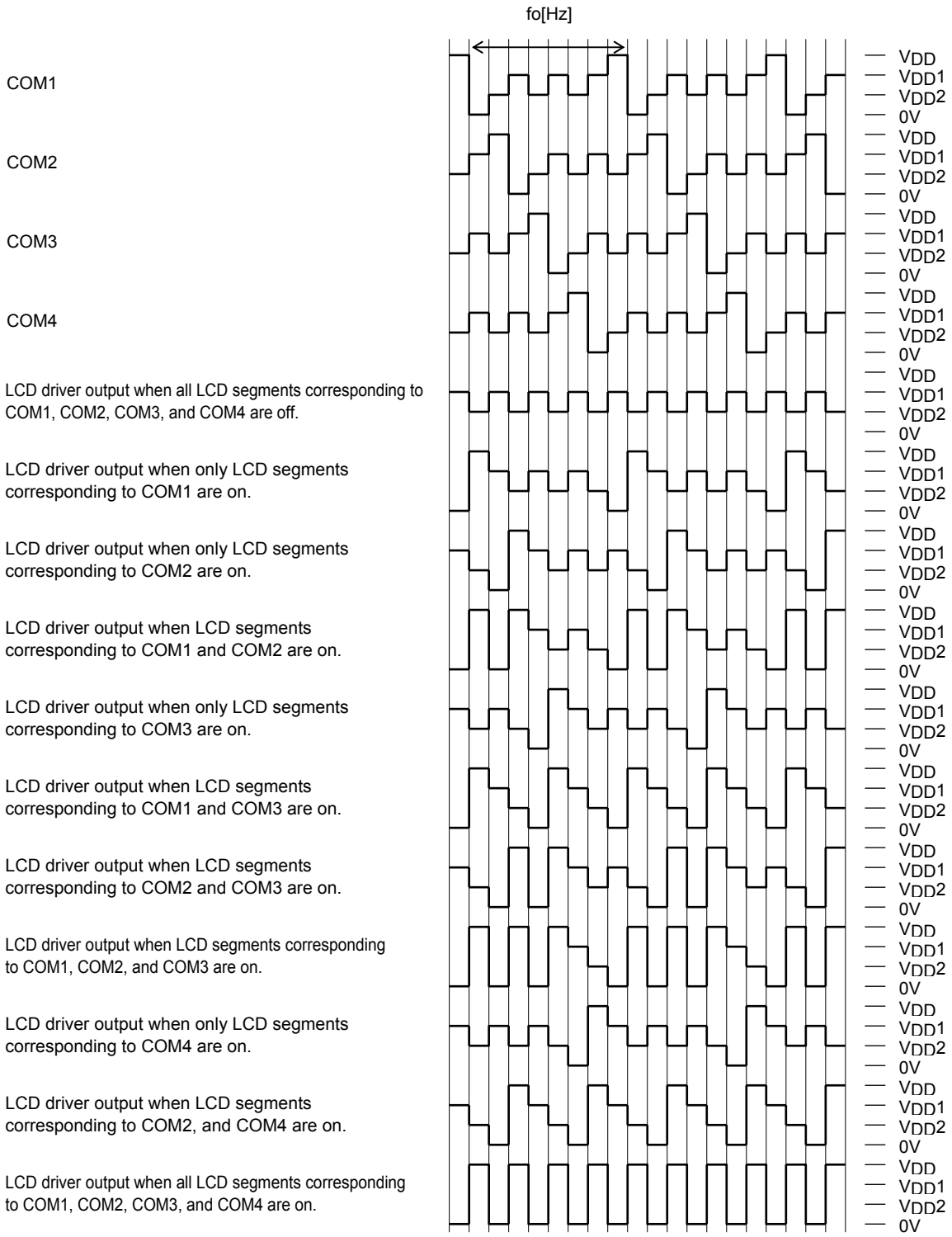
| Output pin | COM1 | COM2 | COM3 | COM4 |
|---|---|---|---|---|
| S19 | D73 | D74 | D75 | D76 |
| S20 | D77 | D78 | D79 | D80 |
| S21 | D81 | D82 | D83 | D84 |
| S22 | D85 | D86 | D87 | D88 |
| S23 | D89 | D90 | D91 | D92 |
| S24 | D93 | D94 | D95 | D96 |
| S25 | D97 | D98 | D99 | D100 |
| S26 | D101 | D102 | D103 | D104 |
| S27 | D105 | D106 | D107 | D108 |
| S28 | D109 | D110 | D111 | D112 |
| S29 | D113 | D114 | D115 | D116 |
| S30 | D117 | D118 | D119 | D120 |
| S31 | D121 | D122 | D123 | D124 |
| S32 | D125 | D126 | D127 | D128 |
| S33 | D129 | D130 | D131 | D132 |
| S34 | D133 | D134 | D135 | D136 |
| S35 | D137 | D138 | D139 | D140 |

Note: Applies when the S1/P1 to S4/P4 output pins are set to their segment output function.

For example, the table below lists the output states for the S21 output pin.

| Display data | | | | Output pin (S21) state |
|---|---|---|---|---|
| D81 | D82 | D83 | D84 | |
| 0 | 0 | 0 | 0 | The LCD segments corresponding to COM1, COM2, COM3, and COM4 are off. |
| 0 | 0 | 0 | 1 | The LCD segment corresponding to COM4 is on. |
| 0 | 0 | 1 | 0 | The LCD segment corresponding to COM3 is on. |
| 0 | 0 | 1 | 1 | The LCD segments corresponding to COM3 and COM4 are on. |
| 0 | 1 | 0 | 0 | The LCD segment corresponding to COM2 is on. |
| 0 | 1 | 0 | 1 | The LCD segments corresponding to COM2 and COM4 are on. |
| 0 | 1 | 1 | 0 | The LCD segments corresponding to COM2 and COM3 are on. |
| 0 | 1 | 1 | 1 | The LCD segments corresponding to COM2, COM3, and COM4 are on. |
| 1 | 0 | 0 | 0 | The LCD segment corresponding to COM1 is on. |
| 1 | 0 | 0 | 1 | The LCD segments corresponding to COM1 and COM4 are on. |
| 1 | 0 | 1 | 0 | The LCD segments corresponding to COM1 and COM3 are on. |
| 1 | 0 | 1 | 1 | The LCD segments corresponding to COM1, COM3, and COM4 are on. |
| 1 | 1 | 0 | 0 | The LCD segments corresponding to COM1 and COM2 are on. |
| 1 | 1 | 0 | 1 | The LCD segments corresponding to COM1, COM2, and COM4 are on. |
| 1 | 1 | 1 | 0 | The LCD segments corresponding to COM1, COM2, and COM3 are on. |
| 1 | 1 | 1 | 1 | The LCD segments corresponding to COM1, COM2, COM3, and COM4 are on. |

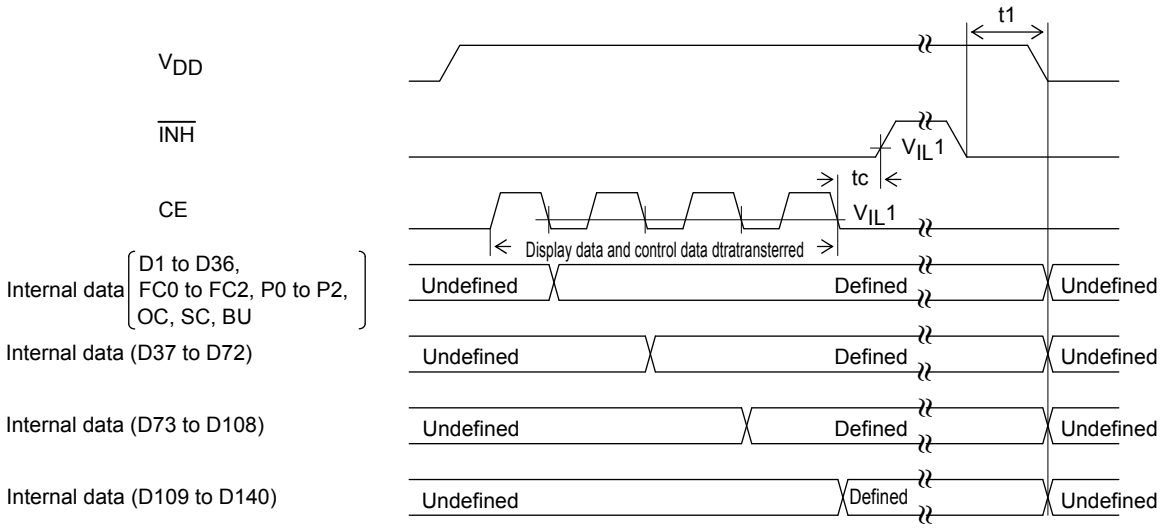
Output Waveforms (1/4-Duty 1/3-Bias Drive Scheme)




| Control data | | | Frame frequency fo [Hz] |
|---|---|---|---|
| FC0 | FC1 | FC2 | |
| 1 | 1 | 0 | fosc/768,$f_{CK}$/768 |
| 1 | 1 | 1 | fosc/576,$f_{CK}$/576 |
| 0 | 0 | 0 | fosc/384,$f_{CK}$/384 |
| 0 | 0 | 1 | fosc/288,$f_{CK}$/288 |
| 0 | 1 | 0 | fosc/192,$f_{CK}$/192 |

## Display Control and the $\overline{INH}$ Pin

Since the LSI internal data (the display data D1 to D140 and the control data) is undefined when power is first applied, applications should set the $\overline{INH}$ pin low at the same time as power is applied to turn off the display. (This sets the S1/P1 to S4/P4, S5 to S35, and COM1 to COM4 pins to the $V_{SS}$ level.) and during this period send serial data from the controller. The controller should then set the $\overline{INH}$ pin high after the data transfer has completed. This procedure prevents meaningless displays at power on.
(See Figure 5.)




Notes: t1>0
tc···10μs min

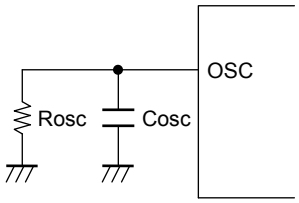
Figure 5

## Notes on Controller Transfer of Display Data

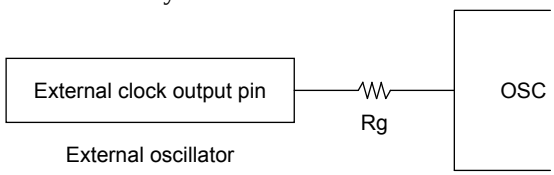
Since the LC75836W transfer the display data (D1 to D140) in four separate transfer operations, we recommend that applications make a point of completing all four data transfers within a period of less than 30ms to prevent observable degradation of display quality.

## OSC Pin Peripheral Circuit

(1) RC oscillator operating mode (control data OC = 0)
An external resistor, Rosc, and an external capacitor, Cosc, must be connected between the OSC pin and GND if RC oscillator operating mode is selected.



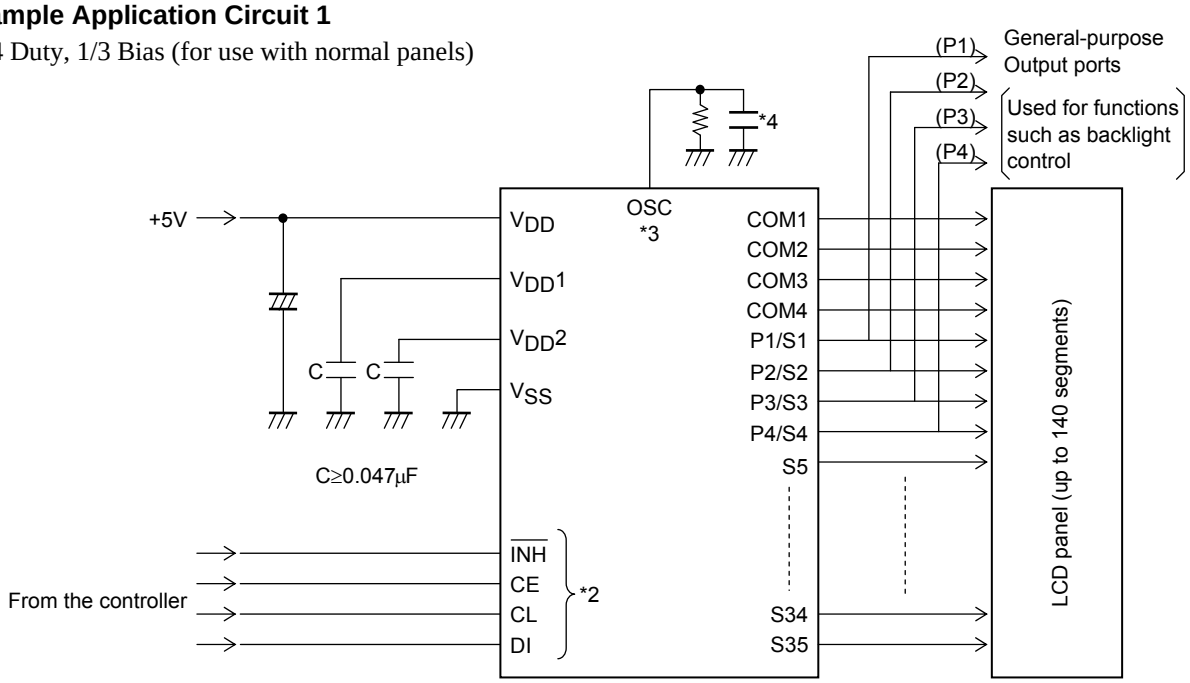

(2) External clock operating mode (control data OC = 1)
When the external clock operating mode is selected, insert a current protection resistor Rg (4.7 to 47 kΩ) between the OSC pin and external clock output pin (external oscillator). Determine the value of the resistance according to the allowable current value at the external clock output pin. Also make sure that the waveform of the external clock is not heavily distorted.




Note: Allowable current value at external clock output pin > $\frac{V_{DD}}{Rg}$

### Sample Application Circuit 1

1/4 Duty, 1/3 Bias (for use with normal panels)



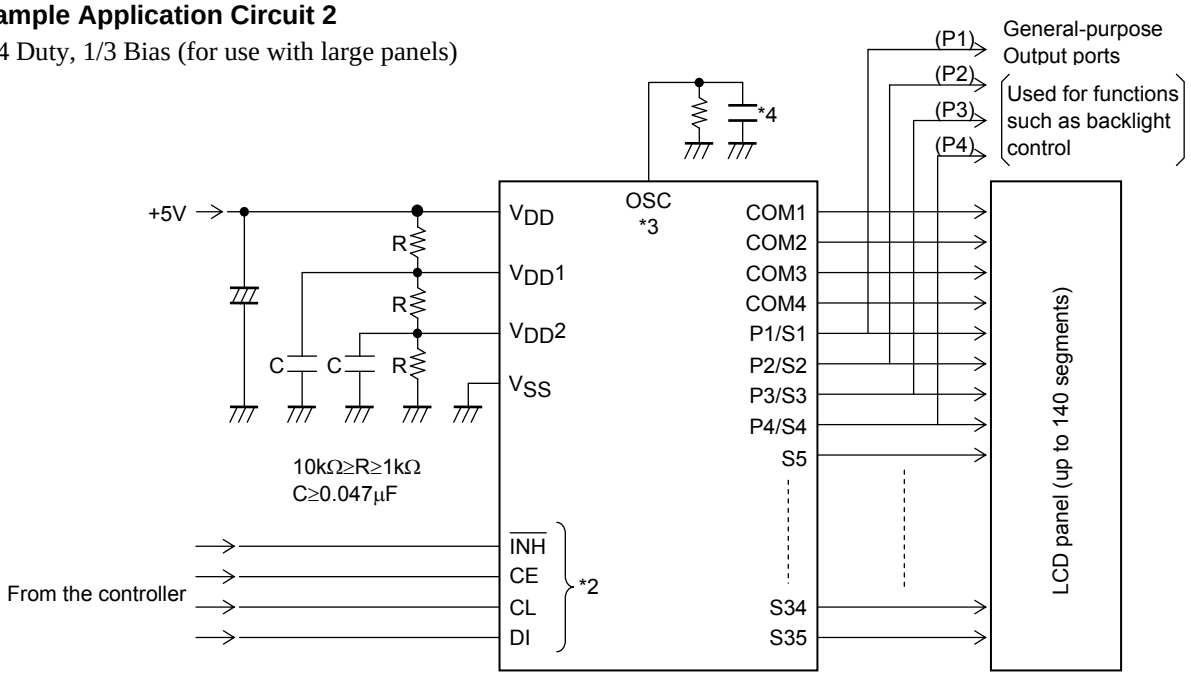

*2: The pins to be connected to the controller (CE, CL, DI, $\overline{INH}$) can handle 3 V.

*3: In RC oscillator operating mode, an external resistor, Rosc, and an external capacitor, Cosc, must be connected between the OSC pin and ground. If external clock operating mode is selected, a current protection resistor, Rg (4.7 to 47 kΩ), must be inserted between the external clock output pin (on the external oscillator) and the OSC pin. (See the "OSC Pin Peripheral Circuit" section.)

*4: When a capacitor except the recommended external capacitance (Cosc = 1000 pF) is connected to the OSC pin, it should be in the range 220 to 2200 pF.

### Sample Application Circuit 2

1/4 Duty, 1/3 Bias (for use with large panels)




*2: The pins to be connected to the controller (CE, CL, DI, $\overline{INH}$) can handle 3 V.

*3: In RC oscillator operating mode, an external resistor, Rosc, and an external capacitor, Cosc, must be connected between the OSC pin and ground. If external clock operating mode is selected, a current protection resistor, Rg (4.7 to 47 kΩ), must be inserted between the external clock output pin (on the external oscillator) and the OSC pin. (See the "OSC Pin Peripheral Circuit" section.)

*4: When a capacitor except the recommended external capacitance (Cosc = 1000 pF) is connected to the OSC pin, it should be in the range 220 to 2200 pF.

## ORDERING INFORMATION

| Device | Package | Shipping (Qty / Packing) |
|---|---|---|
| LC75836W-E | SQFP48 7x7 / SQFP48 (Pb-Free) | 1250 / Tray JEDEC |
| LC75836W-TBM-E | SQFP48 7x7 / SQFP48 (Pb-Free) | 1000 / Tape & Reel |
| LC75836WH-E | SQFP48 7x7 / SQFP48 (Pb-Free) | 1250 / Tray JEDEC |
| LC75836WS-E | SQFP48 7x7 / SQFP48 (Pb-Free) | 1250 / Tray JEDEC |

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

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