TS13501
Neo-Iso™ Solid State Relay

Features

- Supports DC and AC systems
- Switch to Controller scalable galvanic isolation
- Differential signaling interface for transient-immune differential serial protocol
- Device powered via galvanically-isolated interface CLK/NCLK. No power rail needed VGG for decoupling cap only
- Switch Characteristics
  - Bi-directional blocking in OFF state
  - Single 36V switch, 240mΩ $R_{DS(on)}$
  - Up to 1A operating current
  - Steady-state over-current protection, 1.5A nominal
  - Inrush current tolerant for 40ms, 3A nominal
- Transient protection for SW1 and SW2:
  - IEC 61000-4-2 (ESD) ±24kV (air), ±16kV (contact)
  - IEC 61000-4-4 (EFT) 40A (5/50ns) level 4
  - IEC 61000-4-5 (Surge/Lightning) 80V with 2Ω internal impedance (1.2/50µs)

Summary Specification

- Junction operating temperature -40 °C to 125 °C
- Packaged in a 8 pin SOIC-EP
- Product is lead-free, Halogen Free, RoHS / WEEE

Description

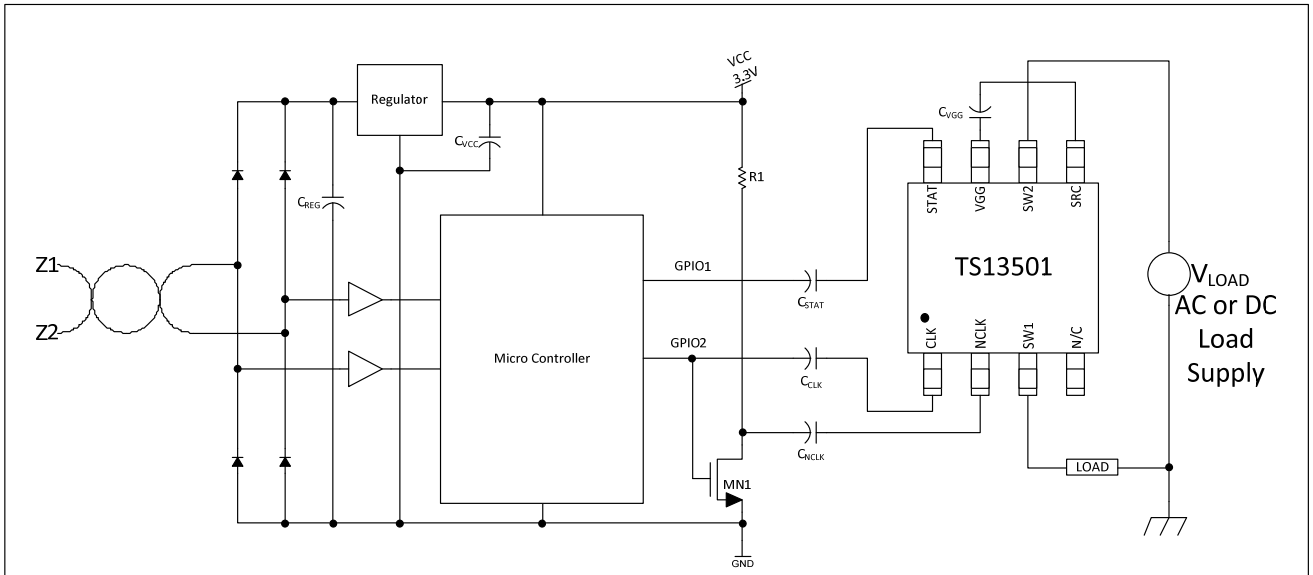
TS13501 is a bi-directional blocking 36V power DC or AC switch device which offers galvanic isolation between the control system and load. The device includes integrated 240mΩ 36V switch allowing high efficiency switching of power loads or other high current applications. The differential input controls the state of the switch by way of a transient-immune serial protocol.

The TS13501 includes an over-current protection feature. Load current is monitored when the switch is in on state, notifying the system microcontroller of over-current faults by way of the STAT status pin.

Applications

- Fire Safety Applications
- Automatic door controls
- Intrusion alarm sensors
- Industrial control
- Sprinkler control
- Power load/rail switching
- Input supply multiplexing

Typical Application Circuit

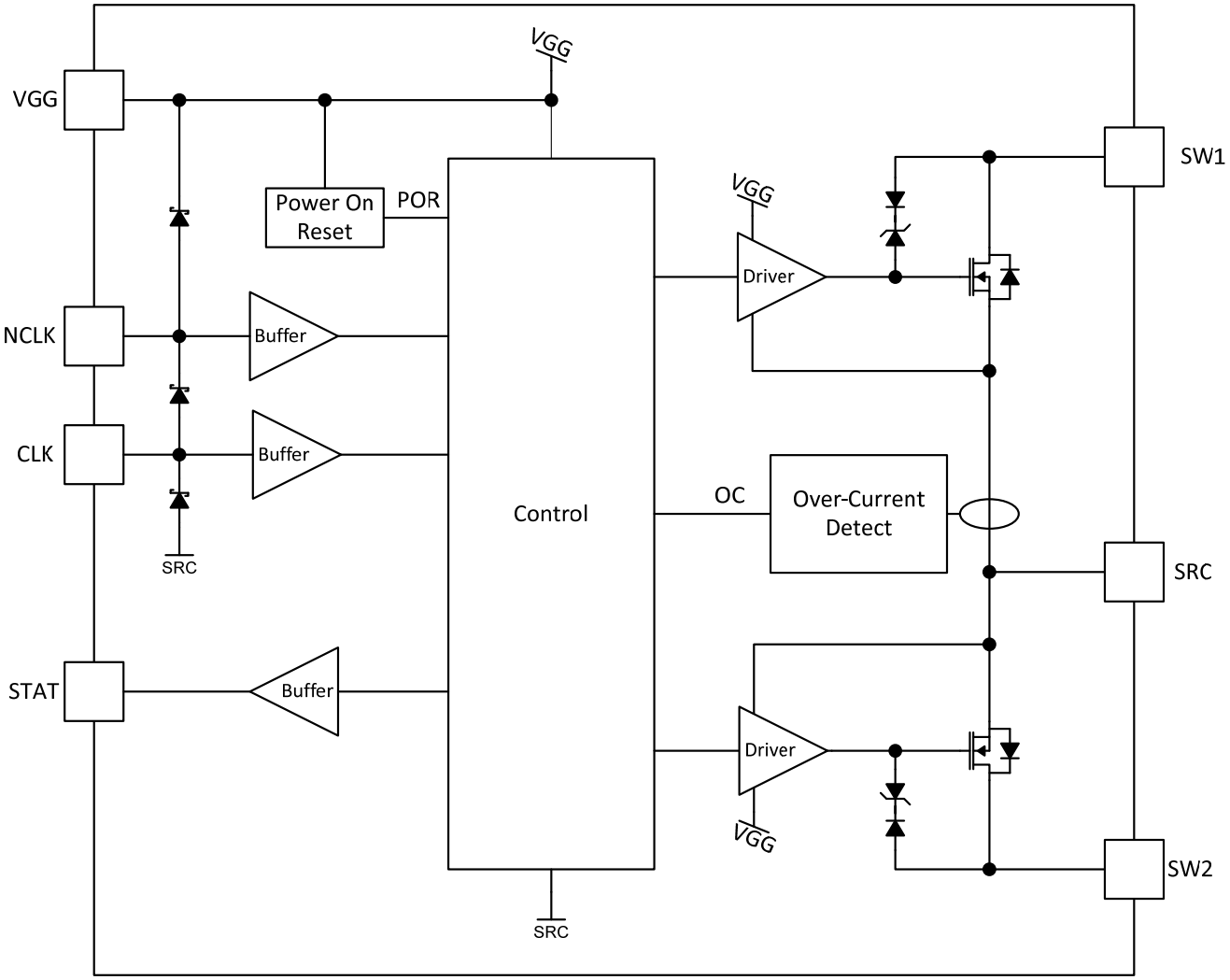


System Block Diagram

Pin Description

Pin Name	Pin #	Function	Description
CLK	1	Switch Control Input	Serial interface to control device when correct protocol sent
NCLK	2	CLK Compliment Input	Drive compliment of CLK on this pin
SW1	3	Switch Terminal 2	First switch terminal (Connect to Load or Supply)
N/C	4	No Connection	Pin not used
SRC	5	Supply Reference	Supply return
SW2	6	Switch Terminal 1	Second switch terminal (Connect to Load or Supply)
VGG	7	Internal Supply	Device internally generated supply (connect decoupling capacitor to SRC)
STAT	8	Device Status Output	Sends status output when switch is closed (Enabled)
SUB	PAD	Thermal Pad	Pad for improved thermal performance - **do not connect to any other net**

Functional Block Diagram



Absolute Maximum Ratings

Over operating free-air temperature range unless otherwise noted [1]

Parameter	Range	Unit
SW1, SW2[2]	-1 to 45	V
VGG, CLK, NCLK, STAT[2]	-0.3 to 5.5	V
Operating Ambient Temperature Range, T_A	-40 to 85	°C
Storage Temperature Range, T_{STG}	-65 to 150	°C
Electrostatic Discharge – Human Body Model	±4	kV
Electrostatic Discharge – Charged-Device Model	±1	kV
Electrostatic Discharge – IEC Contact (SW1 and SW2 Pins) [3]	±16	kV
Electrostatic Discharge – IEC Air Discharge (SW1 and SW2 Pins) [3]	±24	kV
Peak IR Reflow Temperature (10 to 30 seconds)	260	°C

Notes:

(1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated under "Recommended Operating Conditions" are not implied. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

(2) Voltage values are with respect to the SRC terminal.

(3) SW1 and SW2 pins only, may require special system board layout techniques to achieve these levels.

Thermal Characteristics

Symbol	Parameter	Value	Unit
θ_{JA}	Thermal Resistance, Junction to Ambient	40	°C/W
$T_{J\,MAX}$	Maximum Junction Temperature	150	°C
T_J	Operating Junction Temperature Range	-40 to 125	°C

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{SWX}	Switch Voltage, $\lvert V_{SW1} - V_{SW2} \rvert$		24	36	V
V_{IH}	CLK, NCLK Input High Voltage	1.7	3.3		V
V_{IL}	CLK, NCLK Input Low Voltage		0	0.5	V
C_{VGG}	VGG Bypass Capacitor		470		nF
C_{CLK}	CLK Isolation Capacitor		680		pF
C_{NCLK}	NCLK Isolation Capacitor		680		pF
C_{STAT}	STAT Isolation Capacitor		100		pF
V_{CLK}	CLK, NCLK Drive Voltage	1.7	3.3	5.5	V
F_{CLK}	CLK input frequency to turn on switch	75	100	1000	kHz
N_{CLKON}	Number of CLK pulses to Turn On after VGG POR		18		Pulses
T_{CLKOFF}	CLK low time to Turn-Off	50		150	µs
$T_{PRE\text{-}CHG}$	Pre-charge time before VGG POR; V_{CLK} = 3.0V; F_{CLK} = 100kHz		10		ms
F_{SYS}	System Supply Frequency (Switched Load Power Source)	0	60	65	Hz

Electrical Characteristics

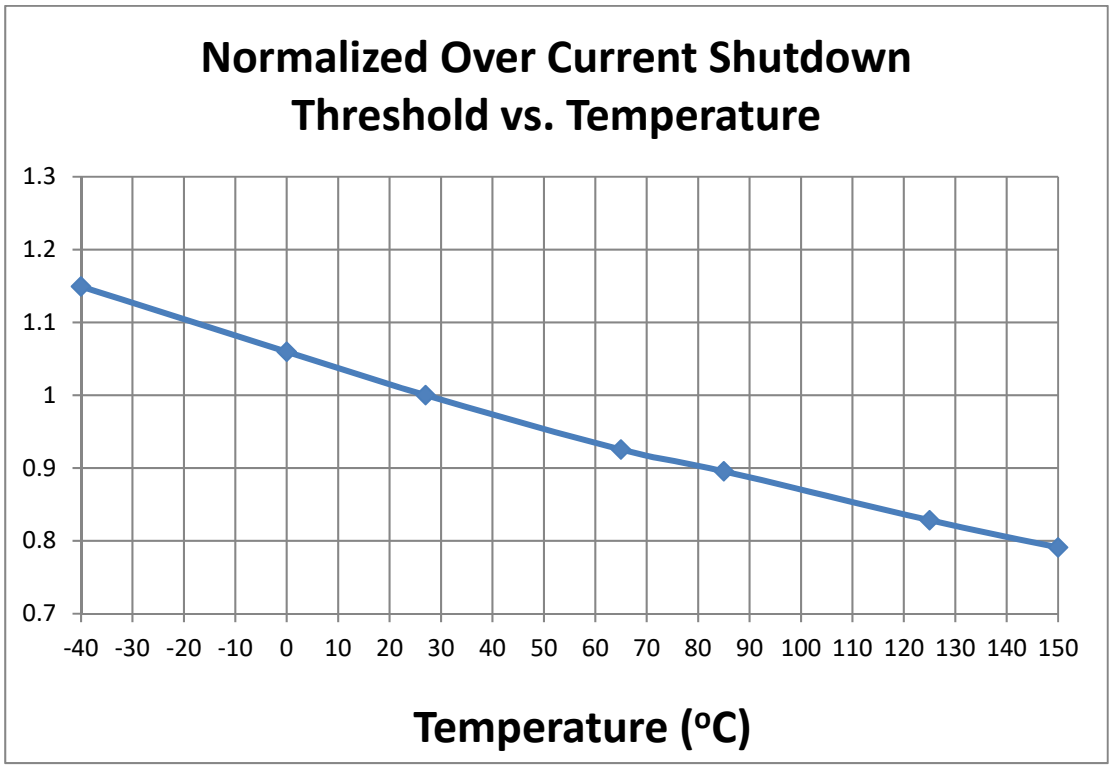
T_J = -40°C to 125°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltages						
V_{GG}	VGG Bias Output Voltage	With respect to SRC, CLK and NCLK drive = 3.0V(1)	4.5	5.0	5.5	V
I/O Parameters						
V_{STATH}	STAT Output High Voltage Drop	3.0V < V_{GG} < 5.5V; I_{OH} = -4mA $V_{STATH} = V_{GG} - V_{STAT}$		0.7	1.3	V
V_{STATL}	STAT Output Low Voltage	3.0V < V_{GG} < 5.5V; IOH = 4mA $V_{STATL} = V_{STAT} - V_{SRC}$		0.1	0.2	V
I_{IL}	Input Low-level Leakage Current	CLK Input; $V_{CLK} = V_{SRC}$	-1		1	µA
I_{IH}	Input High-level Leakage Current	$V_{CLK} = V_{GG}$	-1		15	µA
T_{STAT}	STAT Pulse Width	Switch in ON state		$4*T_{CLK}$		µs
Output Switch						
$R_{DS(on)}$	Switch On-Resistance	Across SWx Pins	150	240	405	mΩ
I_{SWX}	SW1/2 Leakage	V_{SWX} = 24V; V_{SRC}=0V, T_J<85°C	-3		3	µA
$IOUT_{OC}$	Over Current Shutdown Threshold	T_J=25°C	1	1.5		A
$IOUT_{PK}$	Inrush Current Shutdown Threshold	T_J=25°C	2	3		A
OC_{FILT}	Over Current Deglitch		7	11	15	µs
T_{IPK}	Inrush Duration	$2^{12}/F_{CLK}$(2)		41		ms
V_{CLAMP}	V_{SWX} Clamp Voltage	V_{SW1}-V_{SW2}, V_{SW2}-V_{SW1} ; I_{SW}=10mA	36	39	42	V

(1) Not tested in production

(2) CLK input must be present. Switch will be disabled (opened) if a CLK edge is not sensed within T_{CLKOFF}.

Product Characteristics



Detailed Description

Device Power Management

The TS13501 receives power through power transfer via the galvanically-isolated interface. Galvanic power transfer depends on the GPIO driving the isolation capacitors to have sufficient drive capacity (current and voltage) to transfer needed power to the TS13501. This is usually not a problem due to the low quiescent current draw of the device. The CLK and its compliment signal, NCLK, perform two important functions. First, these form a differential signaling system which is more robust in its ability to reject transients present in the system. Second, it allows a voltage-doubling of the GPIO supply to be created within the TS13501. This allows sufficient supply voltage for operation even if used with a micro-controller with a 1.8V GPIO supply.

The CLK and NCLK pins must be continually switched at their recommended frequency while the switch is closed. When the device has been unpowered for a period of time, the CLK and NCLK pins must be switched for a Pre-Charge period, $T_{PRE\text{-}CHG}$, of time to transfer sufficient charge to allow operation to begin.

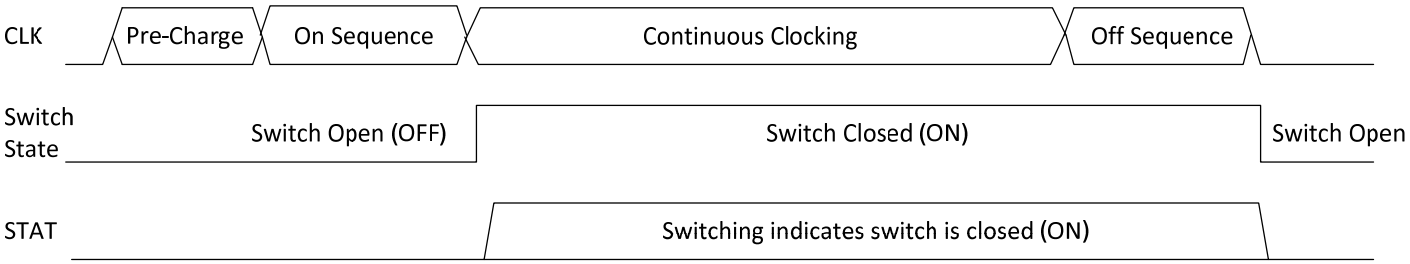


Figure 1: Switch Command Sequences

The On Sequence

An initial pre-charge period must be provided to the device in order to bring up the local supply, VGG. The switch will be closed a number of clock pulses, N_{CLKON}, after the VGG voltage has reached its internal Power Good threshold. At this point, the switch will transition to the closed (ON) state. This sequence is shown in Figure 2. The on-state of the switch can be verified by the presence of pulses on the STAT pin.

The system designer has some control over the total delay time to close the switch ($T_{PRE-CHG} + N_{CLKON} / F_{CLK}$), which is influenced by the CLK amplitude, FCLK, Isolation capacitor value and VGG bypass capacitor value.

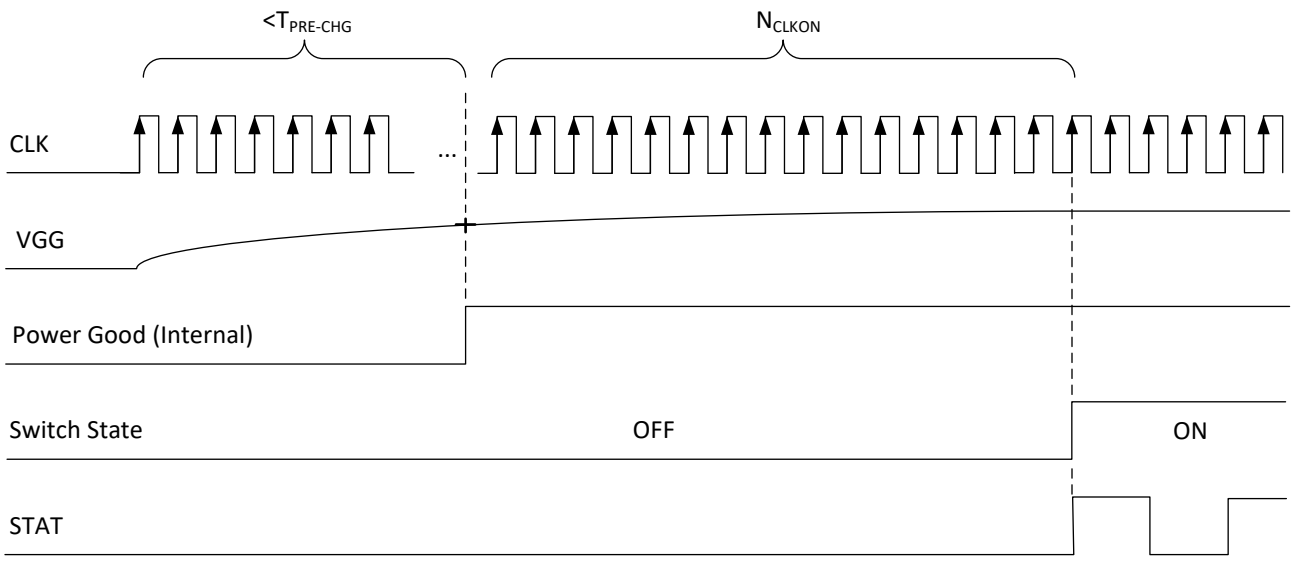


Figure 2: On Sequence

The Off Sequence

To transition the switch from a closed state to an open state, a valid Off Sequence must be received by the TS13501. The sequence consists of an interruption of the CLK input signal for a period of T_{CLKOFF}. A static period of duration T_{CLKOFF} will notify the device that the switch is to be transitioned to the open (OFF) state. Note that the STAT pin will indicate the switch state. The Off Sequence is illustrated in Figure 3.

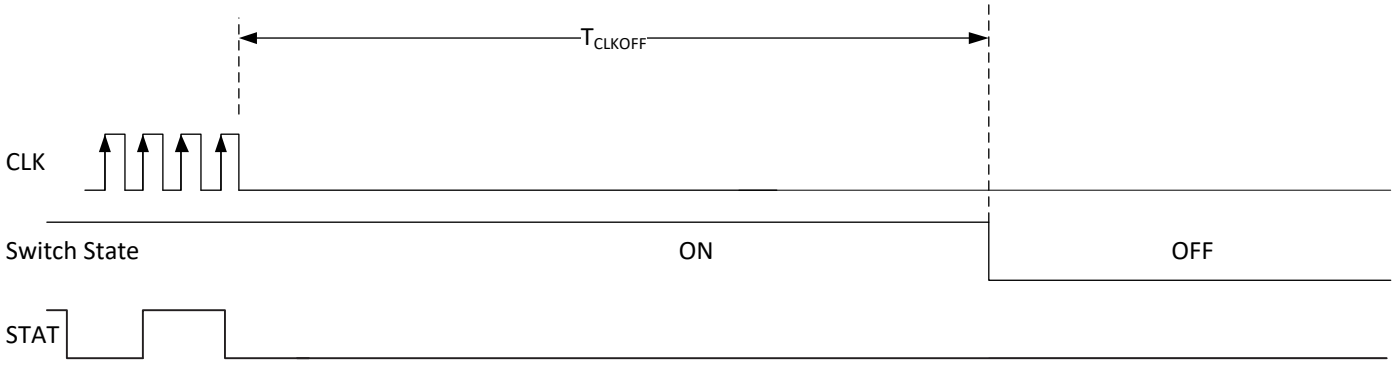


Figure 3: Off Sequence

Switch Status Reporting

The status of the switch may be determined by the STAT signaling from the TS13501. When a valid Turn-On Sequence has been received, the switch will close and a signal received at the STAT output will indicate this condition. The STAT pin will continue to switch at a frequency of $F_{STAT} = F_{CLK} / 4$ as long as a valid CLK input is driven to the device and the switch is in the closed (ON) state. The Status Functionality is shown in Figure 4.

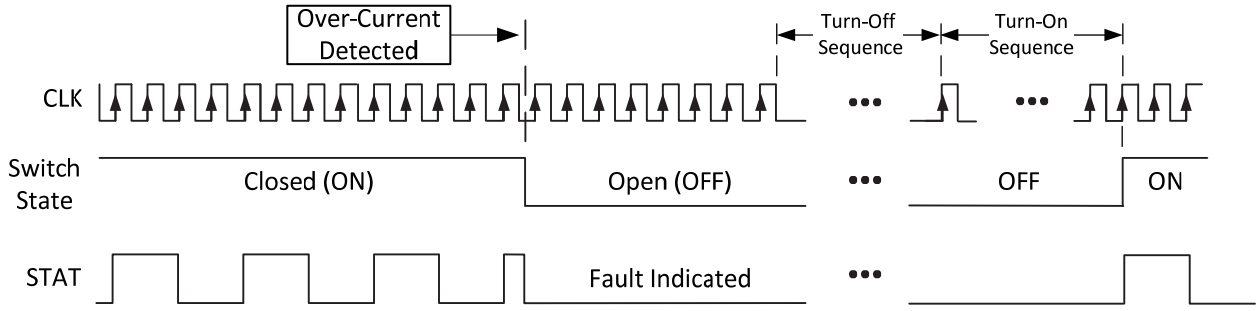


Figure 4: Status Functionality

Load Current Protection

The device has the ability to protect itself from excessive current due to load faults.

Shorted Load

The load current is continually evaluated when the switch is in the "ON" state. In the event that the load current exceeds the threshold limits ($IOUT_{OC}$ or $IOUT_{PK}$), the switch will be opened and the state is indicated by the STAT pin, which will cease switching as shown in Figure 4.

Inrush Current

A system may present loads to the switch which result in high inrush currents when initially energized, but rapidly decrease to a lower level. If the inrush level is higher than the switch over-current shutdown ($IOUT_{PK}$), it may be impossible to activate the load. This device allows the activation of loads with inrush currents on the order of twice their normal operating current for a short period of time. During the inrush period, the switch over-current shutdown is elevated, allowing current to build in the load, ensuring actuation. After the inrush delay period, T_{IPK}, the over-current threshold is reduced to a lower level to allow protection against faults. Figure 5 illustrates the time-variant peak load current in an AC system and how the inrush over-current shutdown threshold can be used to energize a load successfully when the higher inrush current would otherwise have tripped the lower steady-state over-current threshold ($IOUT_{OC}$). As long as the load current stays within the red boundary area, the switch will remain closed.

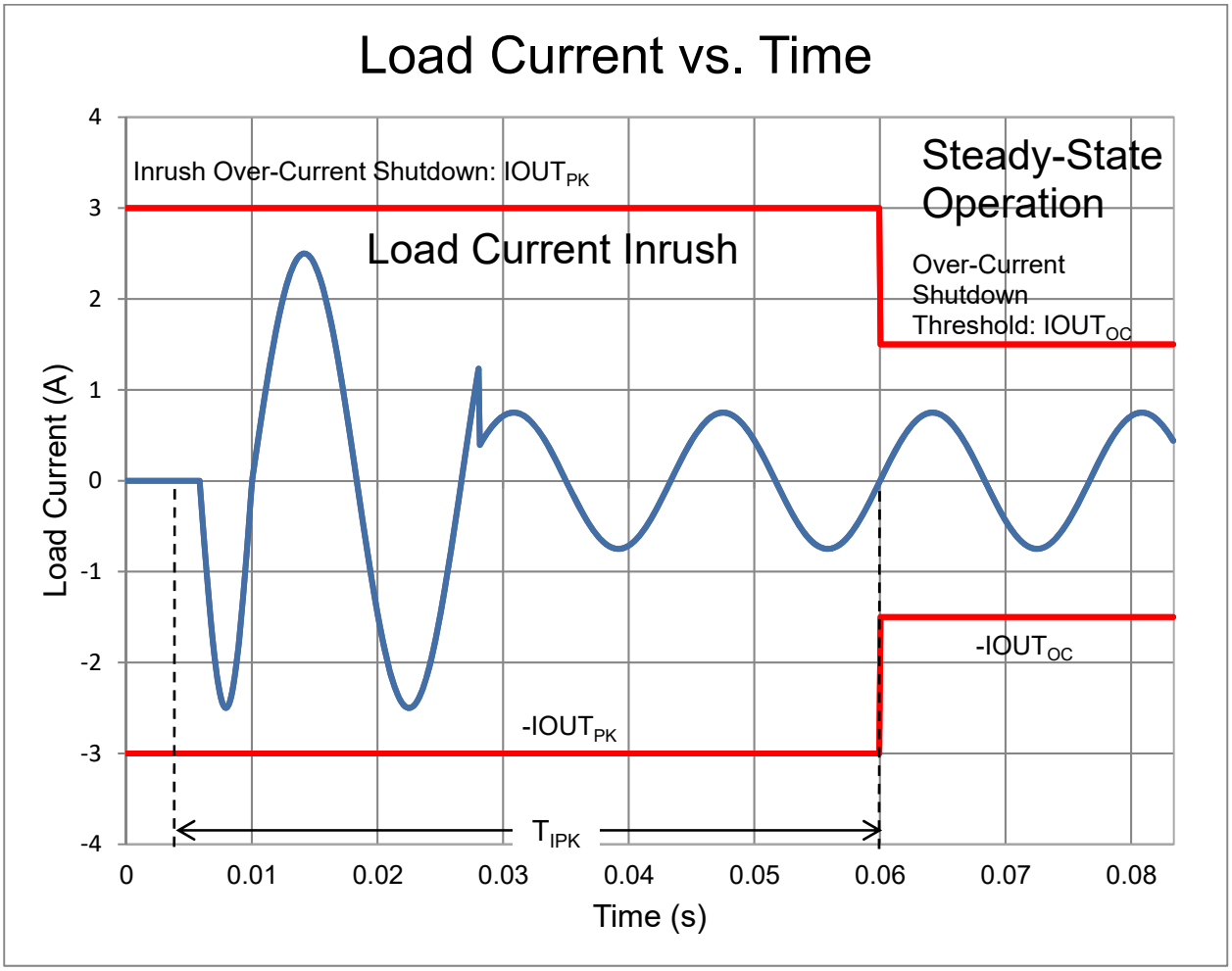


Figure 5: Inrush Waveform

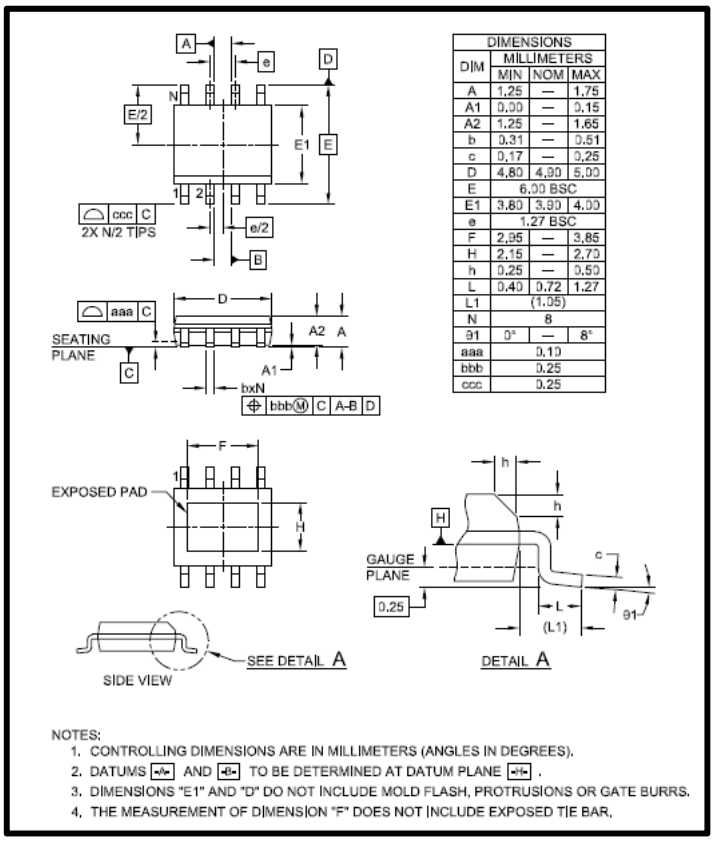
The device uses the CLK input signal to provide a time reference for the inrush period, T_{IPK}. Therefore, T_{IPK} is defined as:

$$T_{IPK} = \frac{2^{12}}{F_{CLK}}$$

If it is desired to change this time, it is possible to change the CLK input frequency to extend or shorten the inrush time period. Note that if there is no clock edge received by the TS13501 in 50µs, the switch will be opened. This is to prevent creating overly long inrush times and to protect the switch and load in the event that control is lost. It is recommended that the inrush period be only as long as is required by the load in the system.

Typical inrush periods, T_{IPK}, would be 41ms when a 100kHz CLK input is supplied. If the CLK input frequency is reduced to the minimum allowed (half-period of 50µs), the time would be 410ms. The maximum CLK input frequency that can be used for peak inrush current timing is 1MHz, which would yield an inrush time of 4ms.

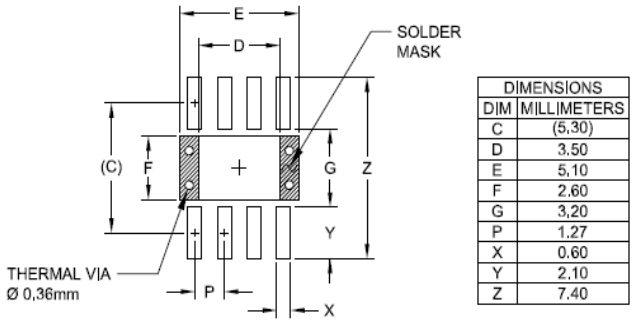
Package Drawing for SOIC-8 EP



DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	1.25	—	1.75
A1	0.00	—	0.15
A2	1.25	—	1.65
b	0.31	—	0.51
c	0.17	—	0.25
D	4.80	4.90	5.00
E	6.00 BSC		
E1	3.80	3.90	4.00
e	1.27 BSC		
F	2.95	—	3.85
H	2.15	—	2.70
h	0.25	—	0.50
L	0.40	0.72	1.27
L1	(1.05)		
N	8		
θ1	0°	—	8°
aaa	0.10		
bbb	0.25		
ccc	0.25		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. THE MEASUREMENT OF DIMENSION "F" DOES NOT INCLUDE EXPOSED TIE BAR.

Landing Pattern for SOIC-8 EP

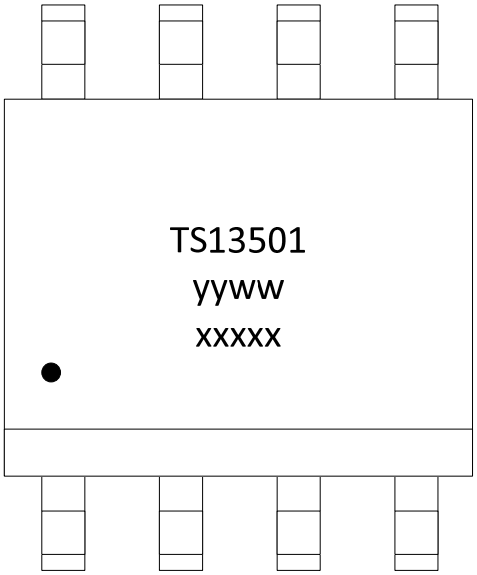


DIMENSIONS	
DIM	MILLIMETERS
C	(5,30)
D	3,50
E	5,10
F	2,60
G	3,20
P	1,27
X	0,60
Y	2,10
Z	7,40

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSE ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.
4. REFERENCE IPC-SM-782A, SECTION 9.1, RLP NO. 300A.

Package Marking for SOIC-8 EP



Marking (Top View)

Marking for the SOIC 8-Lead Package:
Part Number (TS13501)
yyww = Date Code (Example: 1752, 52nd week of 2017)
xxxxx = Semtech Lot No. (Example: E9010)

Ordering Information

Device	Package
TS13501STRT	SOIC-8 EP Tape & Reel (2500 parts/reel)
TS13501-EVB	Evaluation Board

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