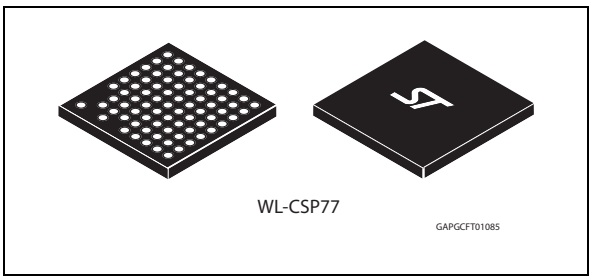
STA8088CWG

GPS/Galileo/Glonass/QZSS receiver

Data brief



Features

- STMicroelectronics® 3rd generation positioning receiver with 32 Tracking channels and 2 fast acquisition channels compatible with GPS, Galileo and Glonass systems
- Embedded RF Front-End with separate GPS/Galieo/QZSS and Glonass IF outputs
- Embedded low noise amplifier
- -162 dBm indoor sensitivity (tracking mode)
- Fast TTFF <1 s in Hot start and 35s in Cold Start
- High performance ARM946 MCU (up to 208 MHz)
- 256 Kbyte embedded SRAM
- Real Time Clock (RTC) circuit
- 32-bit Watch-dog timer
- 2 UARTs
- 1 I^2C master/slave interface
- 1 External SQI Flash interface
- USB2.0 dual-role full speed (12 MHz) with integrated physical layer transceiver
- 2 Controller Area Network (CAN)
- 2 channels ADC (10 bits)
- 3 Embedded 1.8 V voltage regulators
- I/O level selectable 1.8 V or 3.3 V
- Operating condition:
  - V_{DD12}: 1.2 V ±10%
  - $V_{DD18/RF18}$: 1.8 V ±5%
  - V_{LPVR} 1.62 V to 3.6 V
  - V_{ddIO}: 1.8 V ±5%; 3.3 V ±10%
- Package:
  - WL-CSP77 (4 x4 x0.6 mm)
- Ambient temperature range: -40/+85°C

Description

STA8088CWG is a single die standalone positioning receiver IC working on multiple constellations (GPS/Galileo/Glonass/QZSS).

The minimum BOM and small WL-CSP package (16 mm^2) make STA8088CWG the ideal solution for low-cost and small footprint products such hand-held computers, cameras, data loggers, and sports accessories.

The device is offered with a complete GNSS firmware which performs all GNSS operations including tracking, acquisition, navigation and data output.

For further information contact your local STMicroelectronics sales office. www.st.com

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1 Overview

STA8088CWG is a highly integrated System-On-Chip device designed for positioning systems applications.

The low power consumption and minimum BOM make STA8088CWG the ideal solution for low-cost and battery-operated portable products such handheld, computers, cameras, data loggers and sports accessories, as well as automotive application.

It combines a high performance ARM946 microprocessor with embedded enhanced peripherals and I/O capabilities with ST next generation triple-constellation positioning engine. The RF front-end and base band processor are able to support GPS/Galileo and Glonass navigation systems. The device is offered with a complete firmware which performs all positioning operations including tracking, acquisition, navigation and data output.

It also provides clock generation via PLL, backup logic with real time clock and it supports USB2.0 standard at full speed, (12 Mbps) with on-chip PHY.

STA8088CWG is software compatible with the ARM processor family.

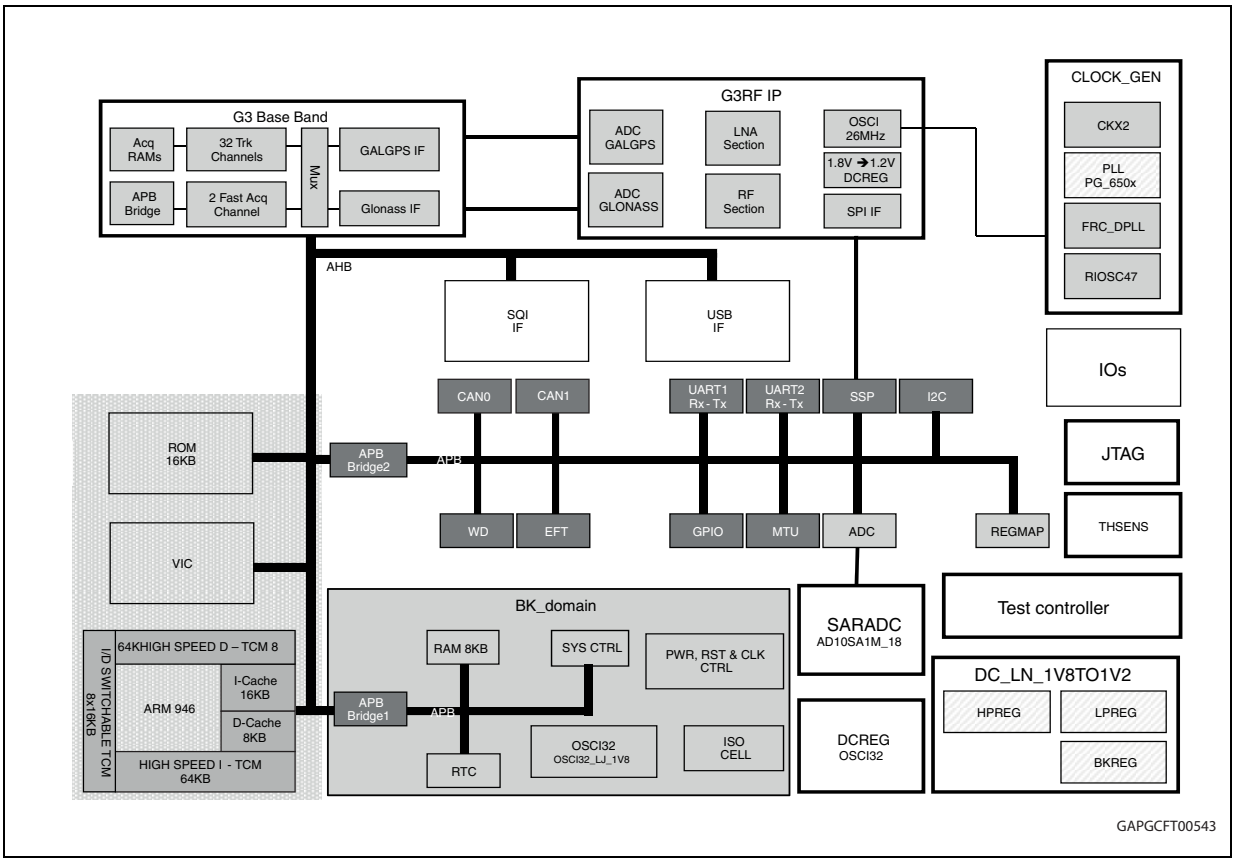
The device is power supplied with 1.8V and uses three on-chip voltage regulators to internally supply the RF front-end, core logic and the backup logic. In order to reduce the power consumption the chip can be directly powered with 1.2 V bypassing the embedded voltage regulators which will be put in power down mode. I/O lines are compatible with 1.8 V and 3.3 V.

The chip, using STMicroelectronics CMOSRF Technology, is housed in a WL-CSP77 (4 x 4 x 0.6 mm) package.

2 Pin description

2.1 Block diagram

Figure 1. STA8088CWG system block diagram



2.2 WL-CSP77 ball out

Table 1. WL-CSP77 ball out (top view)

	1	2	3	4	5	6	7	8	9
A	VDD_ IOR1	VDD_IOR1	VDD_ IOR3	VDD12_ MVR2	USB_DM	TDO	TDI	VDD_ IOR5	GND
B	SQI_ SIO0_SI	SQI_SIO1_ SO	GPIO53	USB_DP	CAN0TX	CAN0RX	I2C_SD	I2C_SCLK	TMS
C	SQI_CEN	SQI_SCK	SQI_SIO3	GND	GND	GND	TCK	TRSTn	VDD18_ MVR2
D	SQI_SIO2	Timer_ OCMPB	Timer_ OCMPA	GND	GND	GND	GND	TP_IF_N	TP_IF_P
E	UART2_ RX	GPIO14	Timer_ ICAPA	UART2_TX	GND	GND	GND	VRF12_ LNA	VRF12_ RFADC
F	GPIO0	ADC_IN5	GND	VDD12_ LPVR	GND	GND	GND_ LNA	LNA_IN	GND_LNA
G	ADC_IN1	VDD12_ MVR3	RTC_XTI	VDD12_ MVR1	XTAL_ OUT	GND	VRF18_ RFVR	LNA_OUT	—
H	VDD18_ MVR1	RTC_XTO	WAKEUP	STDBYn	XTAL_IN	VRF12_ MIX_IF	VRF12_ RFA	VRF12OUT_ RFVR	—
J	VDD18_ MVR1	VDD_ LPVR	RSTn	STDBY_ OUT	VRF12_ RFVCO	—	RFA_IN	—	VRF12_ RFA

2.3 Power supply pins

Table 2. Power supply pins

Symbol	I/O	Functions	WL-CSP77
VDD18_MVR[1,2]	Pwr	Digital supply voltage for main voltage regulator (1.8 V)	H1, J1, C9
VDD12_MVR[1,2,3]	Pwr	Digital supply voltage for core circuitry (1.2 V). When using the MVR, this pin shall not be driven by an external voltage supply, but a capacitance shall be connected between these pins and GND to guarantee on-chip voltage stability.	G4, A4, G2
VDD_LPVR	Pwr	Digital supply voltage for low power voltage regulator (1.62 - 3.6 V)	J2
VDD12_LPVR	Pwr	Digital supply voltage for backup logic (1.2 V). When using the LPVR, this pin shall not be driven by an external voltage supply, but a capacitance shall be connected between these pins and GND to guarantee on-chip voltage stability.	F4
VDD_IOR1	Pwr	Digital supply voltage for I/O ring 1 (1.8 or 3.3 V)	A1, A2
VDD_IOR3	Pwr	Digital supply voltage for I/O ring 3 (1.8 V); this pin can be connected to Ground if the related I/O ring is not used	A3
VDD_IOR5	Pwr	Digital supply voltage for I/O ring 5 (3.3 V); this pin can be connected to Ground if the related I/O ring is not used	A8

Table 2. Power supply pins (continued)

Symbol	I/O	Functions	WL-CSP77
VRF18_RFVR	Pwr	Analog supply voltage for RF voltage regulator (1.8 V)	G7
VRF12OUT_RFVR	Pwr	RF voltage regulator 1.2 V output	H8
VRF12_LNA	Pwr	Analog supply voltage for LNA (1.2 V)	E8
VRF12_RFA	Pwr	Analog supply voltage for RFA (1.2 V)	H8, J9
VRF12_MIX_IF	Pwr	Analog supply voltage for Mixer and IF (1.2 V)	H6
VRF12_RFVCO	Pwr	Analog supply voltage for VCO (1.2 V)	J5
VRF12_RFADC	Pwr	Analog supply voltage for RF ADC (1.2 V)	E9
GND_LNA	GND	Analog supply ground for LNA	F7, F9
GND	GND	Analog and digital supply ground	A9, C4, C5, C6, D4, D5, D6, D7, E5, E6, E7, F3, F5, F6, G6

2.4 Main function pins

Table 3. Main function pins

Symbol	I/O voltage	I/O	Functions	WL_CSP77
STDBYn	1.2V	I	When low, the chip is forced in Standby Mode - All pins in high impedance except the ones powered by Backup supply	H4
STDBY_OUT	1.2V	O	When low, indicates the chips is in Standby Mode	J4
RSTn(1)	1.2V	I	Reset Input with Schmitt-Trigger characteristics and noise filter.	J3
WAKEUP(2)	1.2V	I	WAKEUP from STANDBY mode	H3
RTC_XTI	1.5V (Max)	I	Input of the 32KHz oscillator amplifier circuit and input of the internal real time clock circuit.	G3
RTC_XTO	1.5V (Max)	O	Output of the oscillator amplifier circuit.	H2
ADC_IN[1,5]	1.4V – 0 Typ Range	I	ADC Analog input [1,5]	G1, F2
USB_DP/ UART1_TX	VDD_IOR5	USB/O	USB D+ signal/ UART1 Tx data	B4
USB_DM/ UART1_RX	VDD_IOR5	USB/I	USB D- signal/ UART1 Rx data	A5
CAN0TX	VDD_IOR5	O	CAN0 - transmit data output	B5
CAN0RX	VDD_IOR5	I	CAN0 - receive data input	B6

1. When RSTn is de-asserted, pin WAKEUP must be low.
2. The WAKEUP pulse must be longer than 500 µs.

2.5 Test/emulated dedicated pins

Table 4. Test/emulated dedicated pins

Symbol	I/O voltage	I/O	Functions	WL_CSP77
TDO	VDD_IOR5	O	JTAG test data out	A6
TDI	VDD_IOR5	I	JTAG test data in	A7
TCK	VDD_IOR5	I	JTAG test clock	C7
TMS	VDD_IOR5	I	JTAG test mode select	B9
TRSTn(1)	VDD_IOR5	I	JTAG test circuit reset	C8
TP_IF_P	VRF12_IF	O	Diff. test point for IF – positive	D9
TP_IF_N	VRF12_IF	O	Diff. test point for IF – negative	D8

1. If JTAG interface is not used, pin TRSTn must be asserted low.

2.6 RF front-end pins

Table 5. RF front-end pins

Symbol	I/O voltage	I/O	Functions	WL_CSP77
LNA_IN	VRF12_LNA	I	Low noise amplifier input	F8
LNA_OUT	VRF12_LNA	O	Low noise amplifier output	G8
RFA_IN	VRF12_RFA	I	RF amplifier input	J7
XTAL_IN	VRF12_RFVCO	I	Input side of crystal oscillator or TCXO input	H5
XTAL_OUT	VRF12_RFVCO	O	Output side of crystal oscillator	G5

2.7 Port 0 pins

Port 0 consists of a 32-bit bidirectional I/O port (only 7-bit are used in STA8088CWG).

It can be either used as general purpose Input or Output port, or configured according to the associated alternate functions.

Table 6. Port 0 pins

Symbol	I/O voltage	I/O	Mode	Functions	WL_CSP77
P0.0	VDD_IOR1	I/O	Default	GPIO.0: General Purpose I/O	F1
		I	A	PPS_IN: Pulse Per Second Input	
		O	B	PPS_OUT: Pulse Per Second Output	
P0.8	VDD_IOR5	O	Default	CAN1TX: CAN1 Transmit Data Output	B7
		I/O	A	GPIO.8: General Purpose I/O	
		I/O	B	I2C_SD: I2C Serial Data	

Table 6. Port 0 pins (continued)

Symbol	I/O voltage	I/O	Mode	Functions	WL_CSP77
P0.9	VDD_IOR5	I	Default	CAN1RX: CAN1 Receive Data Input	B8
		I/O	A	GPIO.9: General Purpose I/O	
		O	B	I2C_SCLK: I2C Clock	
P0.14	VDD_IOR5	I/O	A	GPIO.14: General Purpose I/O	E2
P0.15	VDD_IOR5	I/O	A	GPIO.15: General Purpose I/O	E3
		O	B	Timer_ICAPA: extended function timer - input capture A	
P0.16	VDD_IOR5	I/O	A	GPIO.16: General Purpose I/O	D3
		O	B	Timer_OCMPA: extended function timer - output compare A	
P0.18	VDD_IOR5	I/O	A	GPIO.18: General Purpose I/O	D2
		O	B	Timer_OCMPB: extended function timer - output compare B	

2.8 Port 1 pins

Port 1 consists of a 32-bit bidirectional I/O port (only9-bit are used in STA8088CWG).

It can be either used as general purpose Input or Output port, or configured according to the associated alternate functions.

Table 7. Port 1 pins

Symbol	I/O Voltage	I/O	Mode	Functions	WL_CSP77
P1.0	VDD_IOR1	O	Default	SQI_CEN: SQI Flash chip enable I/O. Ring 1 power selection	C1
		I/O	A	GPIO32: general purpose I/O	
		I/O	B	SIGNGGPS: GGPS 3-bit coding output (sign)	
P1.1	VDD_IOR1	O	Default	SQI_CLK: SQI Flash clock	C2
		I/O	A	GPIO33: general purpose I/O	
		I/O	B	CLOCK_GGPS: GGPS clock out	
P1.2	VDD_IOR1	I/O	Default	SQI_SIO0/SI: SQI Flash data I/O 0 / ser. I	B1
		I/O	A	GPIO34: general purpose I/O	
		I/O	B	SIGNGNS: GNS 3-bit coding output (sign)	
P1.3	VDD_IOR1	I/O	Default	SQI_SIO1/SO: SQI Flash data I/O 1 / ser. O	B2
		I/O	A	GPIO35: general purpose I/O	
		I/O	B	CLOCK_GNS: GNS clock out	

Table 7. Port 1 pins (continued)

Symbol	I/O Voltage	I/O	Mode	Functions	WL_CSP77
P1.4	VDD_IOR1	I	Default	UART2_RX: UART 2 Rx data	E1
		I/O	A	GPIO36: general purpose I/O	
P1.5	VDD_IOR1	I/O	Default	UART2_TX / BOOT_0: UART 2 Tx data / ARM Boot 0	E4
		I/O	A	GPIO37: general purpose I/O	
P1.6	VDD_IOR1	I/O	Default	SQI_SIO2: SQI Flash data I/O 2	D1
		I/O	A	GPIO38: general purpose I/O	
P1.7	VDD_IOR1	I/O	Default	SQI_SIO3/BOOT_1: SQI Flash data I/O 3/ARMBoot 1	C3
		I/O	A	GPIO39: general purpose I/O	
P1.21	VDD_IOR3	I/O	A	GPIO53: general purpose I/O	B3

3 Package and packing information

3.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

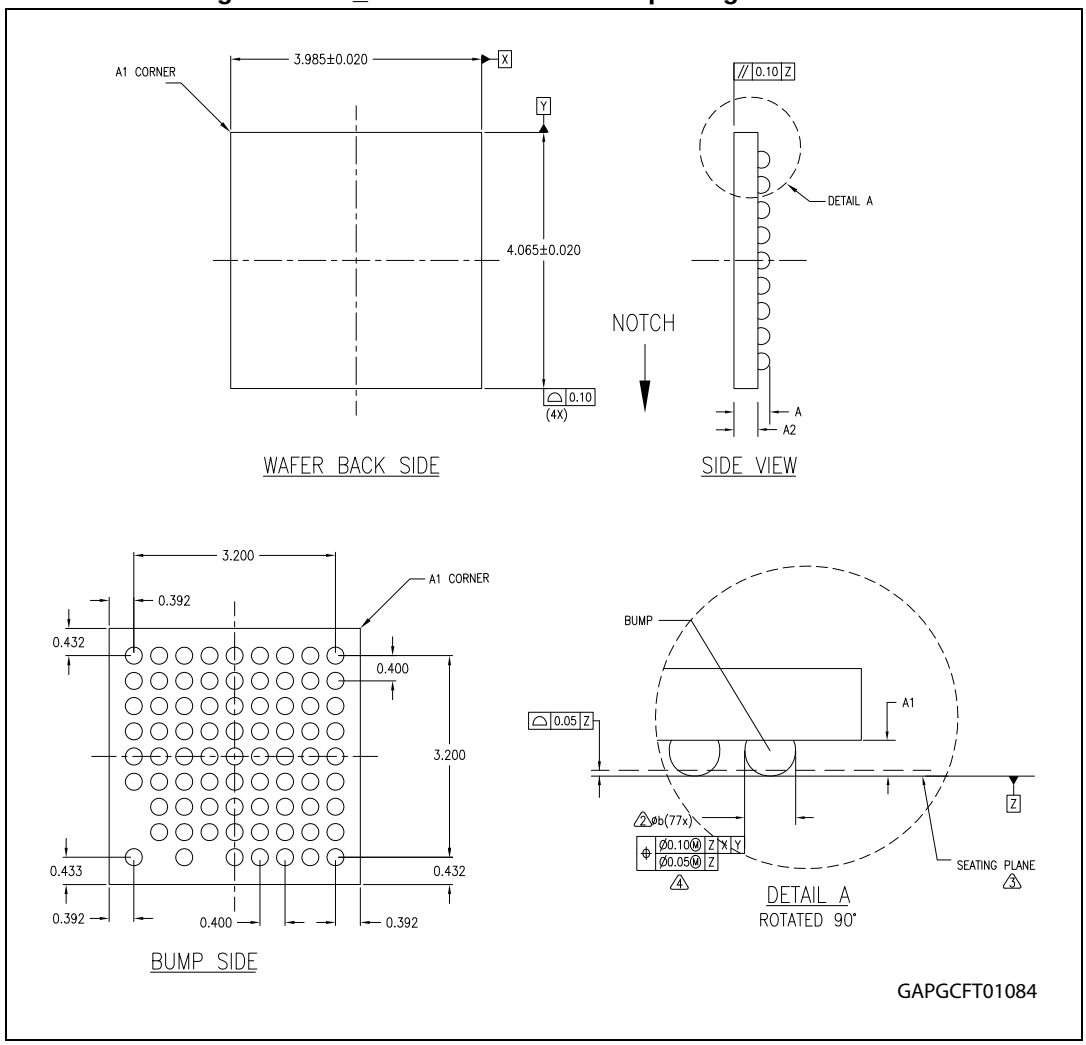
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3.2 WL_CSP77 package information

Table 8. WL_CSP77 4 x 4 x 0.6 mm package dimensions

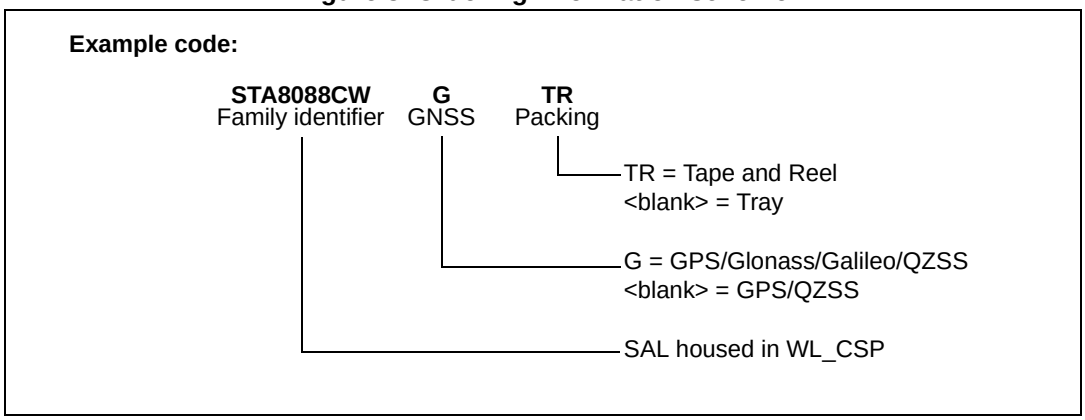
Symbol	Min.	Typ.	Max
A	0.54	0.57	0.6
A1	0.175	0.19	0.205
A2	0.355	0.38	0.405
b	0.245	0.27	0.295
X		3.985	
Y		4.065	
Number of bumps: 77			

Figure 2. WL_CSP77 4 x 4 x 0.6 mm package dimension



4 Ordering information

Figure 3. Ordering information scheme



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
10-Jan-2014	1	Initial release.
12-Feb-2014	2	Updated *Features* list *Table 3: Main function pins*: – CAN0TX, CAN0TX: removed note *Table 6: Port 0 pins*: – P0.8, P0.9: removed note *Figure 3: Ordering information scheme*
24-Sep-2014	3	*Table 3: Main function pins*: – RSTn, WAKEUP: added note *Table 4: Test/emulated dedicated pins*: – TRSTn: added note

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