THE DATASHEET OF

AFE2124E

BURR-BROWN®



AFE2124

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Dual HDSL/SDSL ANALOG FRONT END

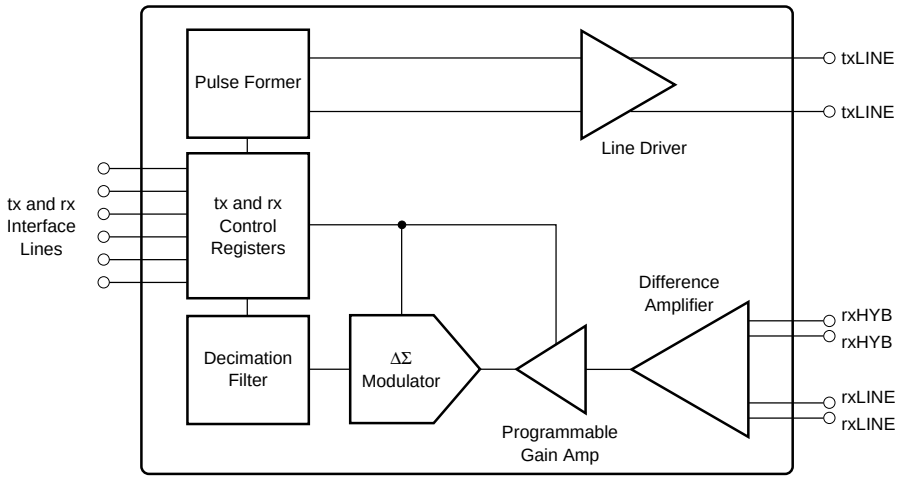
FEATURES

- SERIAL DIGITAL INTERFACE
- 48-LEAD SSOP PACKAGE
- E1, T1 AND SDSL OPERATION
- 64kbps TO 1168kbps OPERATION
- SCALEABLE DATA RATE
- 250mW POWER DISSIPATION PER CHANNEL
- TWO COMPLETE HDSL ANALOG INTERFACES
- +5V POWER (5V or 3.3V Digital)

DESCRIPTION

Burr-Brown's dual Analog Front End chip greatly reduces the size and cost of a DSL (Digital Subscriber Line) system by providing all of the active analog circuitry needed to connect two digital signal processors to external compromise hybrids and line transformers. The AFE2124 is optimized for HDSL (High bit rate DSL) and for SDSL (symmetrical DSL) applications. Because the transmit and receive filter responses automatically change with clock frequency, the AFE2124 is particularly suitable for multiple rate DSL systems. The device operates over a wide range of data rates from 64kbps to 1168kbps.

Functionally, each half of this unit consists of a transmit and a receive section. The transmit section generates analog signals from 2-bit digital symbol data and filters the analog signals to create 2B1Q symbols. The onboard differential line driver provides a 13.5dBm signal to the telephone line. The receive section filters and digitizes the symbol data received on the telephone line. This IC operates on a single 5V supply. The digital circuitry in the unit can be connected to a supply from 3.3V to 5V. It is housed in a 48-lead SSOP package.



1/2 of AFE2124

Patents Pending

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SPECIFICATIONS

Typical at 25°C, AV_{DD} = +5V, DV_{DD} = +3.3V, and txBaudCLK = 584kHz (E1 rate), unless otherwise noted.Specifications apply to each channel of the AFE2124.

PARAMETER	COMMENTS	AFE2124E MIN	AFE2124E TYP	AFE2124E MAX	UNITS
RESOLUTION		14			Bits
RECEIVE CHANNEL					
Number of Inputs	Differential	2			
Input Voltage Range	Balanced Differential(1)		±3.0		V
Common-Mode Voltage			AV_{DD}/2		V
Input Impedance All Inputs			See Typical Performance Curves		
Input Capacitance			10		pF
Input Gain Matching	Line Input vs Hybrid Input		±2		%
Programmable Gain	0dB, 3dB, 6dB, 9dB and 12dB	0		+12	dB
Settling Time	For Any Change in Gain or txBaud CLK		6		Symbol Periods
Gain + Offset Error	Tested at Each Gain Range		5		%FSR(2)
Output Data Coding	Two's Complement				
Output Symbol Rate, rxSYNC(3)		32		584	kHz
Output Bit Rate, rxSYNC(3)		64		1168	kbits/sec
TRANSMIT CHANNEL					
Transmit Clock Rate, txBaudCLK	Symbol Rate	32		584	kHz
T1 Transmit –3dB Point	ETSI RTR/TM - Compliant		196		kHz
T1 Rate Power(4, 5)	txBoost = 0	13		14	dBm
E1 Transmit –3dB Point	ETSI RTR/TM - Compliant		292		kHz
E1 Transmit Power(4, 5)	txBoost = 0	13		14	dBm
Pulse Output			See Typical Performance Curves		
Common-Mode Voltage, V_{CM}			AV_{DD}/2		V
Output Resistance(6)	DC to 1MHz		1		Ω
TRANSCEIVER PERFORMANCE					
Uncancelled Echo(5)	rxGAIN = 0dB, Loopback Enabled		–71	–68.5	dB
	rxGAIN = 0dB, Loopback Disabled		–71	–68.5	dB
	rxGAIN = 3dB, Loopback Disabled		–74	–71	dB
	rxGAIN = 6dB, Loopback Disabled		–76	–73.5	dB
	rxGAIN = 9dB, Loopback Disabled		–78	–75.5	dB
	rxGAIN = 12dB, Loopback Disabled		–80	–77.5	dB
DIGITAL INTERFACE(6)					
Logic Levels					
V_{IH}	$\|I_{IH}\| < 10\mu A$	DV_{DD} – 1		DV_{DD} + 0.3	V
V_{IL}	$\|I_{IL}\| < 10\mu A$	–0.3		+0.8	V
V_{OH}	$I_{OH} = –20\mu A$	DV_{DD} – 0.5			V
V_{OL}	$I_{OL} = 20\mu A$			+0.4	V
t_{rx1} Interface		9		14	ns
POWER					
Analog Power Supply Voltage	Specification		5		V
Analog Power Supply Voltage	Operating Range	4.75		5.25	V
Digital Power Supply Voltage	Specification		3.3		V
Digital Power Supply Voltage	Operating Range	3.15		5.25	V
Power Dissipation(4, 5)	AV_{DD} = 5V, DV_{DD} = 3.3V,		250		mW
Power Dissipation(4, 5)	$AV_{DD} = DV_{DD}$ = 5V		300		mW
Power Supply Rejection Ratio (PSRR)			55		dB
TEMPERATURE RANGE					
Operating(6)		–40		+85	°C

NOTES: (1) With a balanced differential signal, the positive input is 180° out of phase with the negative input, therefore, the actual voltage swing about the common-mode voltage on each pin is ±1.5V to achieve a total input range of ±3.0V or 6Vp-p. (2) FSR is Full-Scale Range. (3) The output data is available at twice the symbol rate. (4) With a pseudo-random equiprobable sequence of HDSL pulses; 13.5dBm applied to the transformer (16.5dBm output from txLINEP and txLINEN). (5) See the Discussion of Specifications section of this data sheet for more information. (6) Guaranteed by design and characterization.

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ABSOLUTE MAXIMUM RATINGS

Analog Inputs: Current	±100mA, Momentary
	±10mA, Continuous
Voltage	AGND –0.3V to AV_{DD} +0.3V
Analog Outputs Short Circuit to Ground (+25°C)	Continuous
AV_{DD} to AGND	–0.3V to 6V
DV_{DD} to DGND	–0.3V to 6V
Digital Input Voltage to DGND	–0.3V to DV_{DD} +0.3V
Digital Output Voltage to DGND	–0.3V to DV_{DD} +0.3V
AGND, DGND, Differential Voltage	0.3V
Junction Temperature (T_J)	+150°C
Storage Temperature Range	–40°C to +125°C
Lead Temperature (soldering, 3s)	+260°C
Power Dissipation	700mW

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

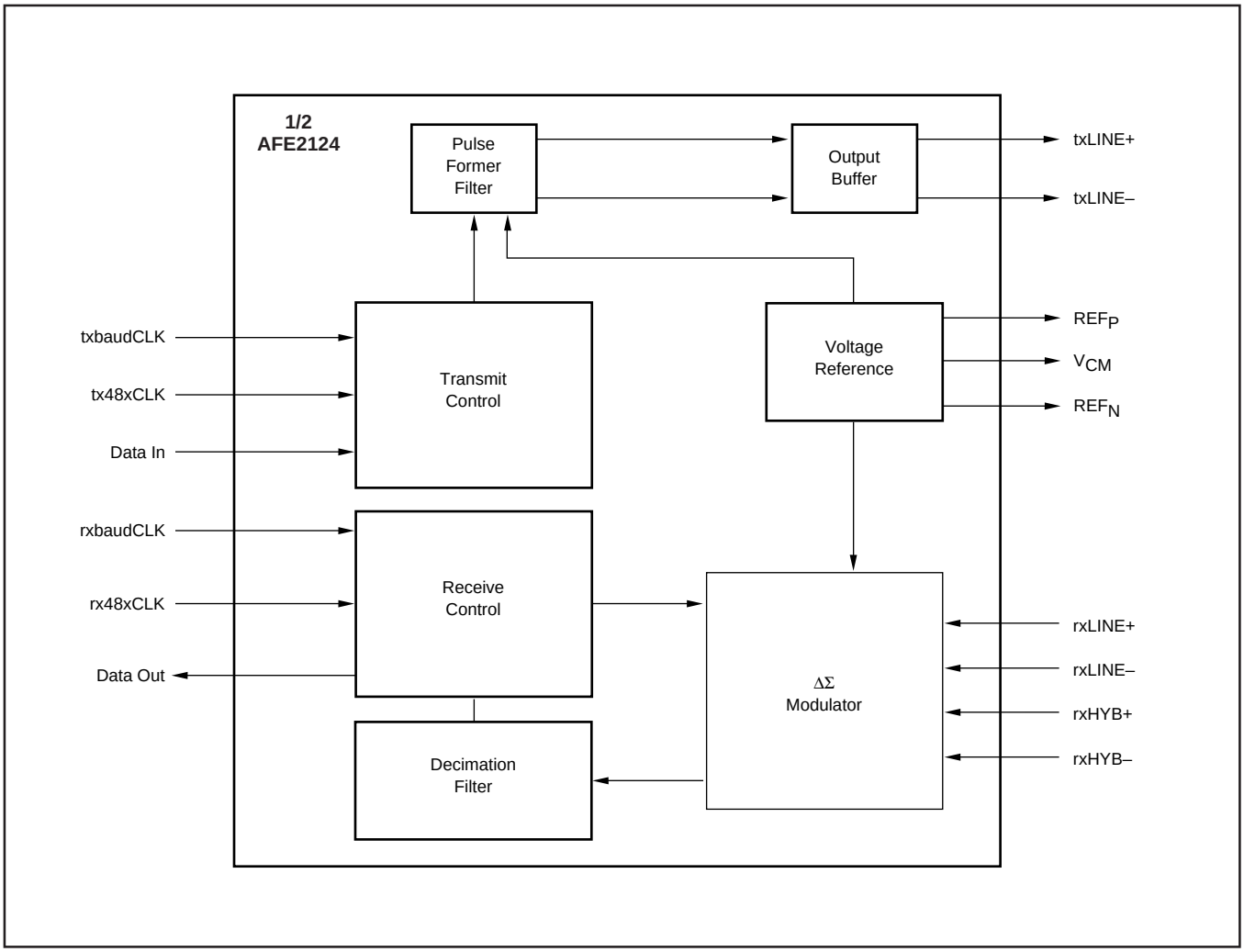
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

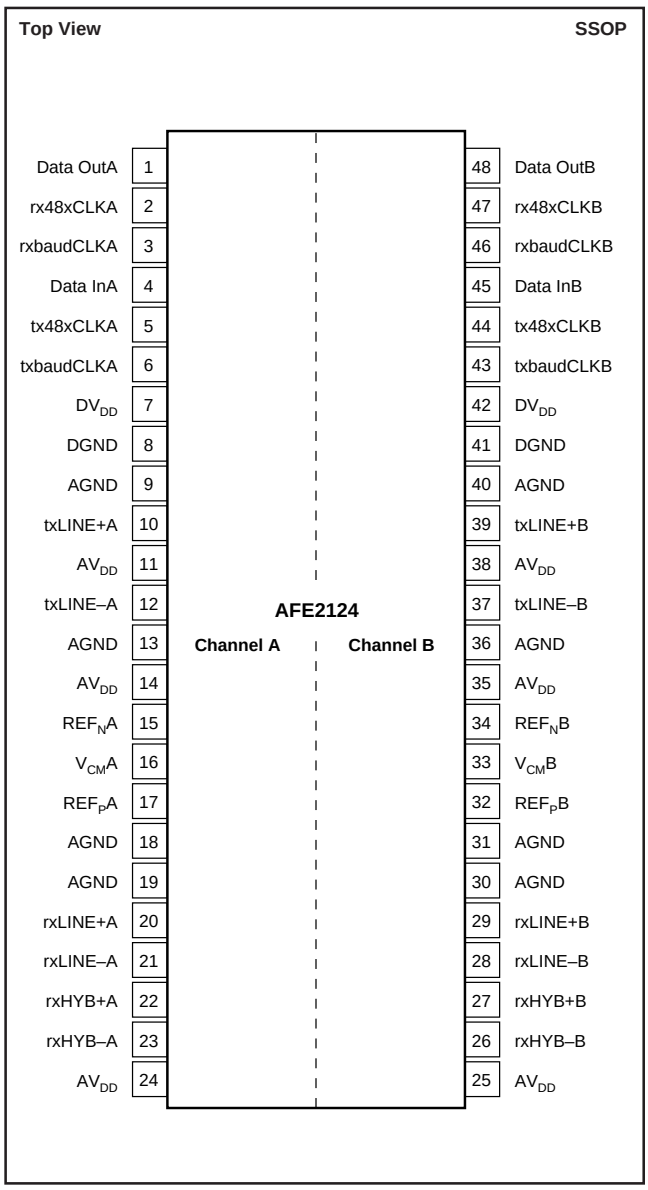
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(2)	TRANSPORT MEDIA
AFE2124E	SSOP-48	333	–40°C to +85°C	AFE2124E	AFE2124E	Rails
"	"	"	"	"	AFE2124E/1K	Tape and Reel

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of "AFE2124E/1K" will get a single 1000-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

BLOCK DIAGRAM



PIN CONFIGURATION



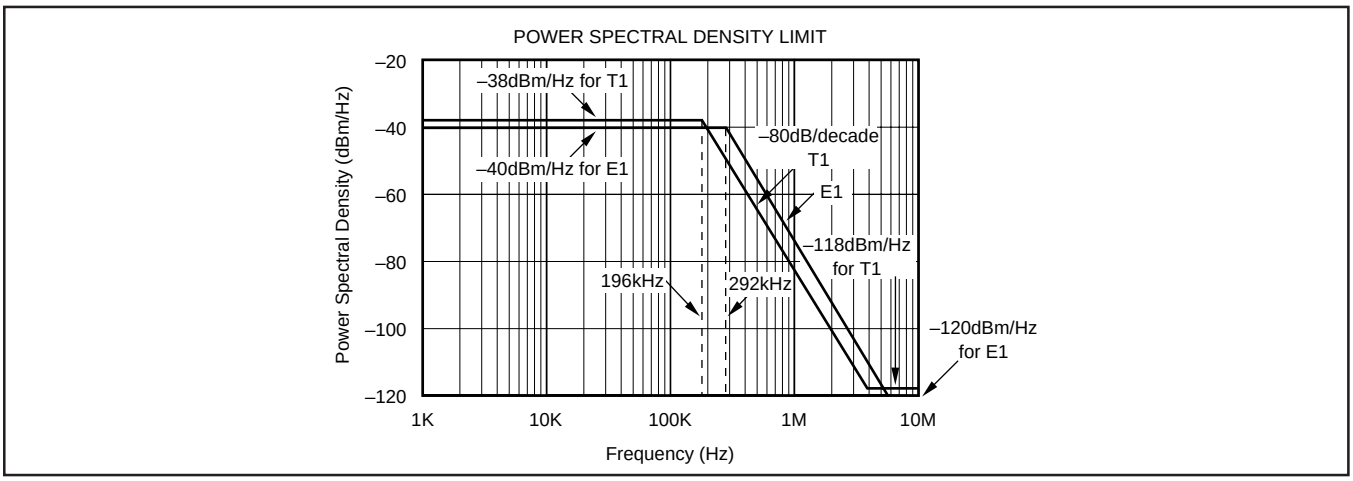
PIN DESCRIPTIONS

PIN #	TYPE	NAME	DESCRIPTION
CHANNEL A			
1	Output	Data OutA	Output Data Word
2	Input	rx48xCLKA	Receive Clock at 48x Baud Clock (23.032MHz for E1)
3	Input	rxbaudCLKA	Receive Baud Clock (584kHz for E1)
4	Input	Data InA	Input Data Word
5	Input	tx48xCLKA	Transmit Clock (584kHz for E1)
6	Input	txbaudCLKA	Transmit Baud Clock at 48x Baud Clock (584kHz for E1)
7	Power	DV_{DD}	Digital Supply (+3.3V to +5V)
8	Ground	DGND	Digital Ground
9	Ground	AGND	Analog Ground
10	Output	txLINE+A	Transmit Line Driver Output, Positive
11	Power	AV_{DD}	Analog Supply (+5V)
12	Output	txLINE–A	Transmit Line Driver Output, Negative
13	Ground	AGND	Analog Ground
14	Power	AV_{DD}	Analog Supply (+5V)
15	Output	REF_NA	Negative Reference Output
16	Output	$V_{CM}A$	Common-Mode Voltage (buffered)
17	Output	REF_PA	Positive Reference Output
18	Ground	AGND	Analog Ground
19	Ground	AGND	Analog Ground
20	Input	rxLINE+A	Positive Line Input
21	Input	rxLINE–A	Negative Line Input
22	Input	rxHYB+A	Positive Input from Hybrid Network
23	Input	rxHYB–A	Negative Input from Hybrid Network
24	Power	AV_{DD}	Analog Supply (+5V)
25	Power	AV_{DD}	Analog Supply (+5V)
CHANNEL B			
26	Input	rxHYB–B	Negative Input from Hybrid Network
27	Input	rxHYB+B	Positive Input from Hybrid Network
28	Input	rxLINE–B	Negative Line Input
29	Input	rxLINE+B	Postiive Line Input
30	Ground	AGND	Analog Ground
31	Ground	AGND	Analog Ground
32	Output	REF_PB	Positive Reference Output
33	Output	$V_{CM}B$	Common-Mode Voltage (buffered)
34	Output	REF_NB	Negative Reference Output
35	Power	AV_{DD}	Analog Supply (+5V)
36	Ground	AGND	Analog Ground
37	Output	txLINE–B	Transmit LIne Driver Output, Negative
38	Power	AV_{DD}	Analog Supply (+5V)
39	Output	txLINE+B	Transmit Line Driver Output, Positive
40	Ground	AGND	Analog Ground
41	Ground	DGND	Digital Ground
42	Power	DV_{DD}	Digital Supply (+3.3V to +5V)
43	Input	txbaudCLKB	Transmit Baud Clock (584kHz for E1)
44	Input	tx48xCLKB	Transmit Clock at 48x Baud Clock (28.032MHz for E1)
45	Input	Data InB	Input Data Word
46	Input	rxbaudCLKB	Receive Baud Clock (584kHz for E1)
47	Input	rx48xCLKB	Receive Clock at 48x Baud Clock (28.032MHz for E1)
48	Output	Data OutB	Output Data Word

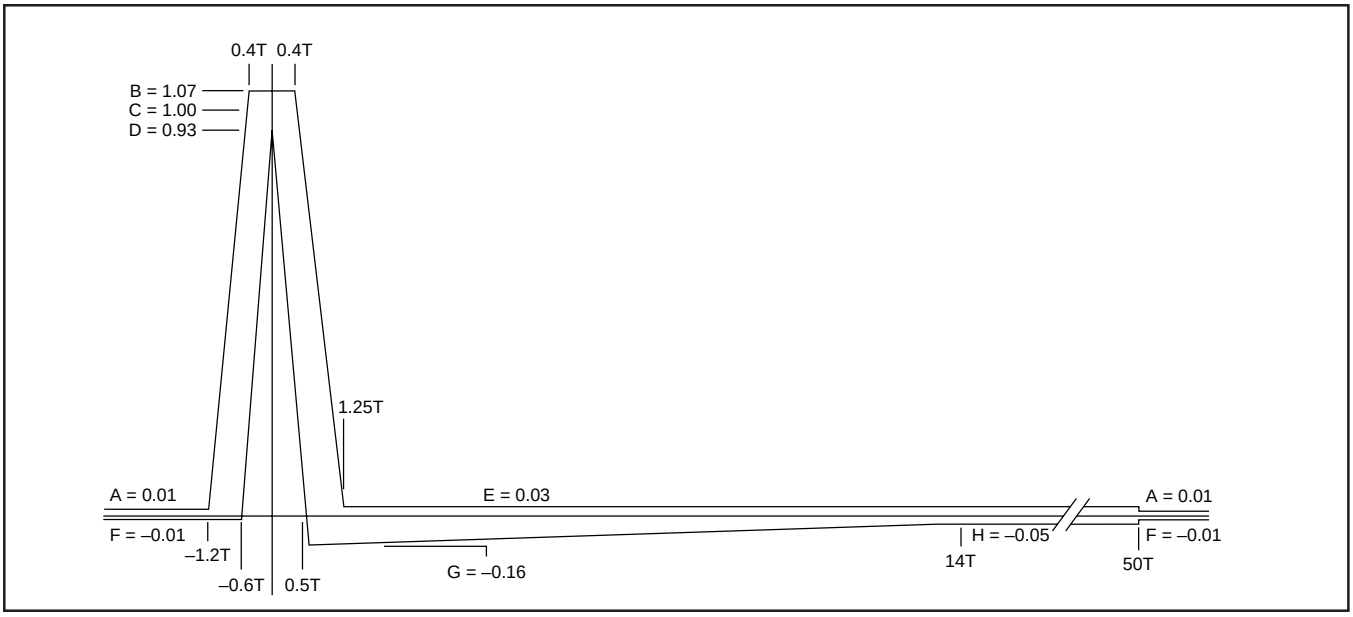
TYPICAL PERFORMANCE CURVES

At Output of HDSL Pulse Transformer

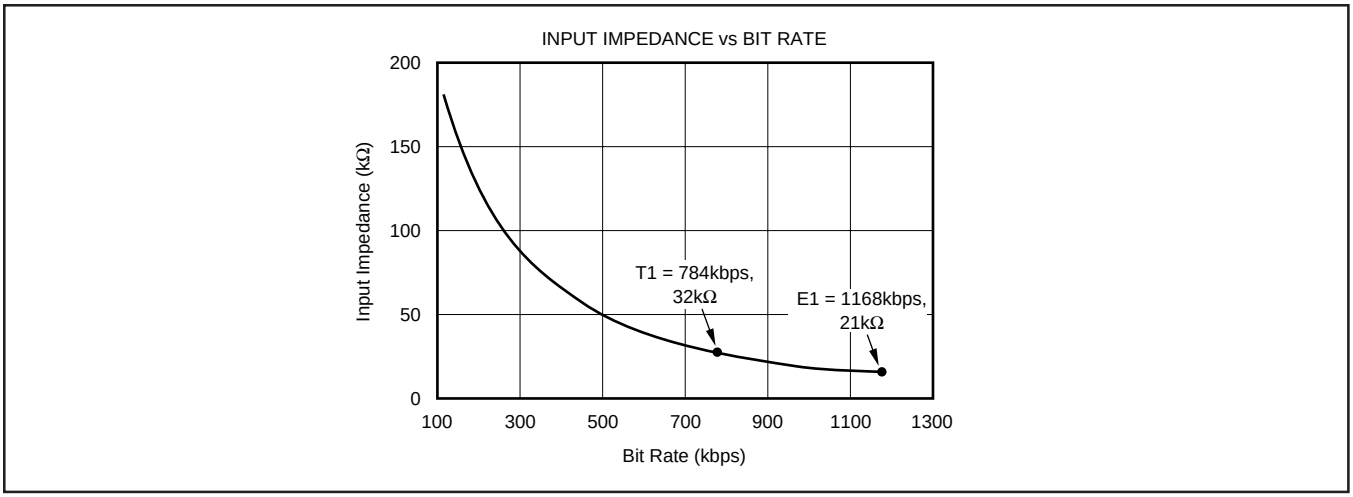
The curves shown below are measured at the line output of the HDSL transformer. Typical at 25°C, AV_{DD}+ = +5V, DV_{DD}+ = +3.3V, txBaudCLK = 584kHz (E1), unless otherwise specified.



CURVE 1. Upper Bound of Power Spectral Density Measured at Output of HDSL Transformer.



CURVE 2. Transmitted Pulse Template Measured at HDSL Transformer Output.



CURVE 3. Input Impedance of rxLINE and rxHYB.

THEORY OF OPERATION

The AFE2124 has two HDSL Analog Front End (AFE) circuits on chip (channel A and channel B). Each AFE is functionally equivalent to an AFE1124. Each AFE consists of a transmit and a receive channel which interfaces to a HDSL DSP through a six-wire serial interface—three wires for the transmit channel and three wires for the receive channel. It interfaces to the HDSL telephone line transformer and external compromise hybrid through transmit and receive analog connections.

The transmit channel consists of a switched-capacitor pulse forming network followed by a differential line driver. The pulse-forming network receives 2-bit digital symbol data and generates a filtered 2B1Q analog output waveform. The differential line driver uses a composite output stage combining class B operation (for high efficiency driving large signals) with class AB operation (to minimize crossover distortion).

The receive channel is designed around a fourth-order delta sigma analog-to-digital converter. It includes a difference amplifier designed to be used with an external compromise hybrid for first-order analog echo cancellation. A programmable gain amplifier with gains of 0dB to +12dB is also included. The delta sigma modulator, operating at a 24x oversampling ratio, produces a 14-bit output at rates up to 584kHz (1.168Mbps).

The receive channel operates by summing the two differential inputs, one from the line (rxLINE) and the other from the compromise hybrid (rxHYB). The connection of these two inputs so that the hybrid signal is subtracted from the line signal is described in the paragraph titled “Echo Cancellation in the AFE.” The equivalent gain for each input in the difference amp is one. The resulting signal then passes to a programmable gain amplifier which can be set for gains of 0dB through +12dB. Following the PGA, the ADC converts the signal to a 14-bit digital word.

The serial interface consists of three wires for transmit and three wires for receive. The three-wire transmit interface is transmit baud rate clock, transmit 48x oversampling clock and Data Out. The three-wire receive interface is receive baud rate clock, receive 48x oversampling clock and Data In. The transmit and receive clocks are supplied to the AFE2124 from the DSP and are completely independent.

DIGITAL DATA INTERFACE

Data is received by the AFE2124 from the DSP on the Data In line. Data is transmitted from the AFE2124 to the DSP on the Data Out line. The following paragraphs describe the timing of these signals and data structure.

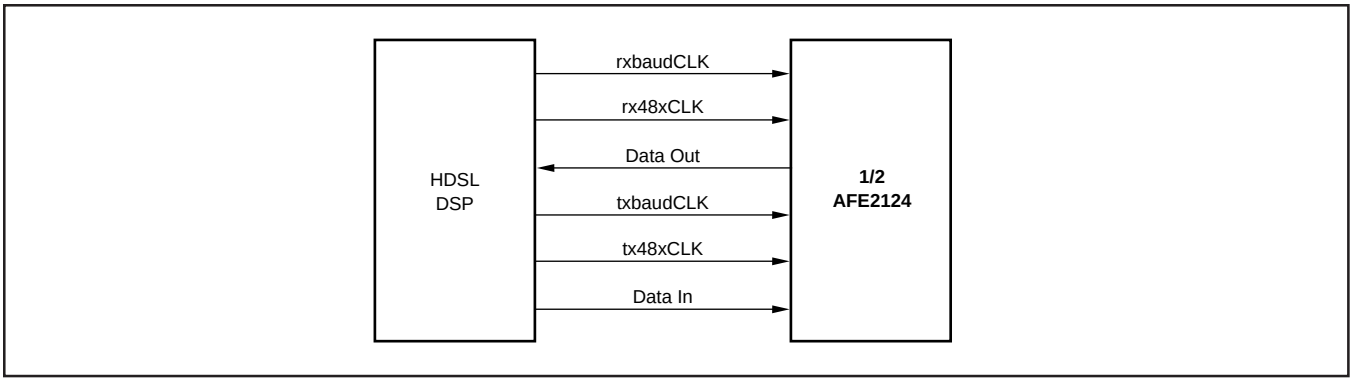
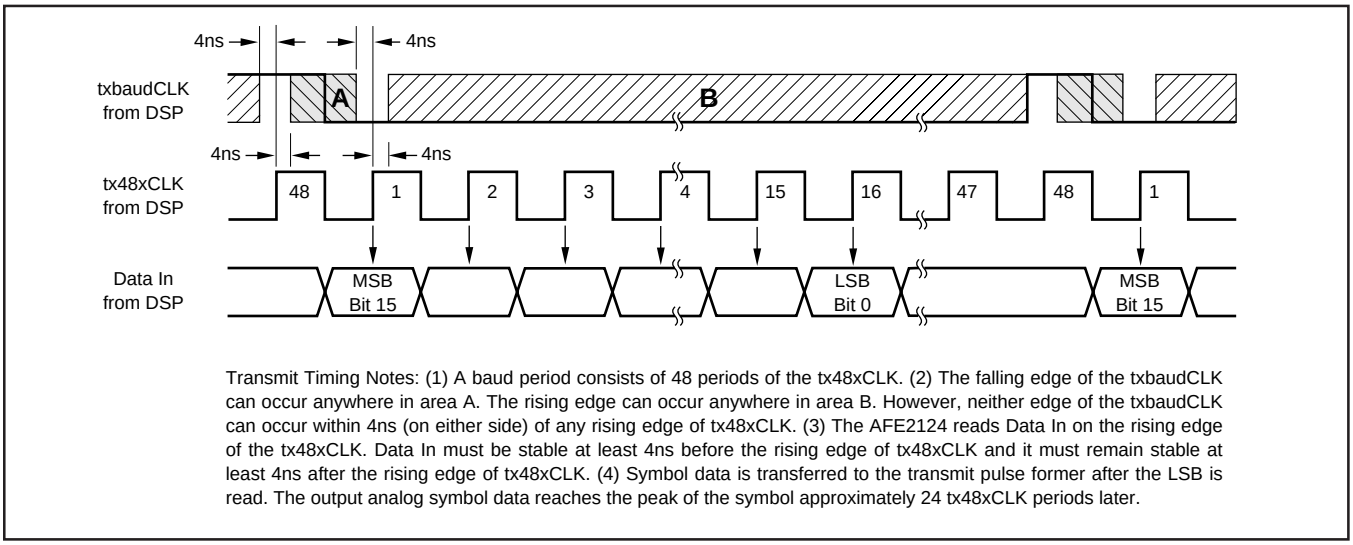


FIGURE 1. DSP Interface.



Transmit Timing Notes: (1) A baud period consists of 48 periods of the tx48xCLK. (2) The falling edge of the txbaudCLK can occur anywhere in area A. The rising edge can occur anywhere in area B. However, neither edge of the txbaudCLK can occur within 4ns (on either side) of any rising edge of tx48xCLK. (3) The AFE2124 reads Data In on the rising edge of the tx48xCLK. Data In must be stable at least 4ns before the rising edge of tx48xCLK and it must remain stable at least 4ns after the rising edge of tx48xCLK. (4) Symbol data is transferred to the transmit pulse former after the LSB is read. The output analog symbol data reaches the peak of the symbol approximately 24 tx48xCLK periods later.

FIGURE 2. Transmit Timing Diagram.

Data is transmitted and received in synchronization with the 48x transmit and receive clocks (tx48xCLK and rx48xCLK). There are 48-bit times in each baud period. Data In is received in the first 16 bits of each baud period. The remaining 32-bit periods are not used for Data In. Data Out is transmitted during the first 16 bits of the baud period. A second interpolated value is transmitted in subsequent bits of the baud period.

txbaudCLK: The transmit data baud rate, generated by the DSP. It is 392kHz for T1 or 584kHz for E1. It may vary from 32kHz (64kbps) to 584kHz (1.168Mbps).

tx48xCLK: The transmit pulse former oversampling sampling clock, generated by the DSP. It is 48x the transmit symbol rate or 28.032MHz for 584kHz symbol rate. This clock should run continuously.

Data In: This is a 16-bit output data word sent from the DSP to the AFE. The sixteen bits include tx symbol information and other control bits, as described below. The data should be clocked out of the DSP on the falling edge and should be valid on the rising edge of the tx48xCLK. The AFE2124 reads Data In on the rising edge of the tx48xCLK. The bits are defined in Table I. Data In is read by the AFE2124 during the first 16 bits periods of each baud period. Only the first 8 bits are used in the AFE2124. The second 8 bits are reserved for use in the future products. The remaining 32 bits periods of the baud period are not used for Data In.

Data In Bits

tx Enable Signal—This bit controls the tx Symbol definition bits. If this bit is 0, only a 0 symbol is transmitted regardless of the state of the tx Symbol definition bits. If this bit is 1, the tx Symbol definition bits determine the output symbol.

tx Symbol Definition—These two bits determine the output 2B1Q symbol transmitted.

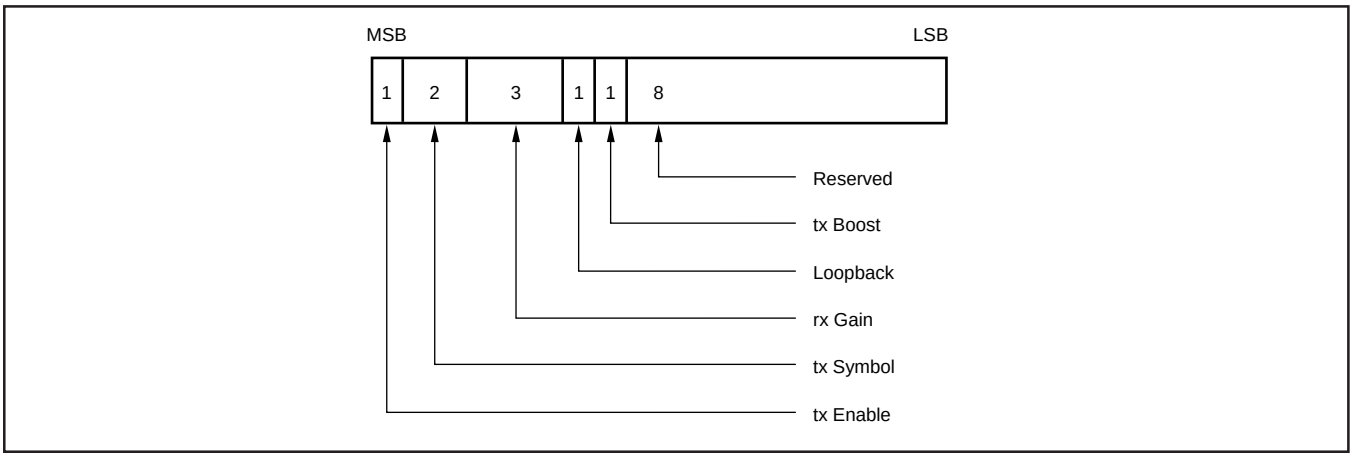
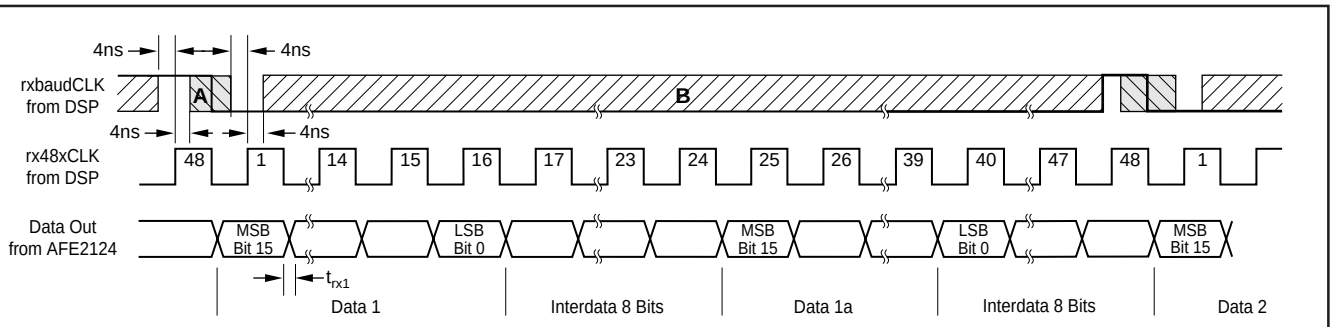


FIGURE 3. Data In Word.



Receive Timing Notes: (1) A baud period consists of 48 periods of the tx48xCLK. (2) The falling edge of the rxbaudCLK can occur anywhere in area A. The rising edge can occur anywhere in area B. However, neither edge of the rxbaudCLK can occur within 4ns (on either side) of any rising edge of rx48xCLK. (3) For all data bits after the MSB of Data 1, the AFE2124 transfers Data Out on the falling edge of the rx48xCLK. The time from the falling edge of rx48xCLK until Data Out is stable is t_{rx1}.

	min	max
t_{rx1}	9ns	14ns

(4) The AFE2124 transfers the MSB of Data 1 on the falling edge of rxbaudCLK. If the falling edge of rxbaudCLK is synchronized with the falling edge of rx48xCLK, all of the Data Out bits will be the same width. In any case, the time from the falling edge of rxbaudCLK until the MSB of Data 1 is stable is t_{rx1}.

FIGURE 4. Receive Timing Diagram.

BIT	DESCRIPTION	BIT STATE	OUTPUT STATE
15 (MSB)	tx Enable Signal	0 1	AFE Transmits a 0 Symbol AFE Transmits HDSL Symbol as defined by bits 14 and 13
14 and 13	tx Symbol Definition	00 01 11 10	–3 Transmit Symbol –1 Transmit Symbol +1 Transmit Symbol +3 Transmit Symbol
12 - 10	rx Gain Settings	000 001 010 011 100 101 110 111	rx gain in AFE 0dB rx gain in AFE 3dB rx gain in AFE 6dB rx gain in AFE 9dB rx gain in AFE 12dB rx gain in AFE Reserved rx gain in AFE Reserved rx gain in AFE Reserved
9	Loopback Control	1 0	Loopback Mode Normal Operation
8	tx Boost	0 1	Normal Transmit Power +0.5dB Transmit Power Boost
7 - 0	SPARE		NA

TABLE I. Data In.

Rx Gain Settings—These bits set the gain of the receive channel programmable gain amplifier.

Loopback Control—This bit controls the operation of loopback. When enabled (logic 1), the rxLINE+ and rxLINE– inputs are disconnected from the AFE. The rxHYB+ and rxHYB– inputs remain connected. When disabled, the rxLINE+ and rxLINE– inputs are connected.

txBoost—This bit controls the addition of 0.5dB additional power to the output line driver.

rxbaudCLK: This is the receive data baud rate (symbol clock), generated by the DSP. It is 392kHz for T1 or 584kHz for E1. It can vary from 32kHz (64kbps) to 584kHz (1.168Mbps).

rx48xCLK: This is the A/D converter oversampling clock, generated by the DSP. It is 48x the receive symbol rate or 28.032MHz for 584kHz symbol rate. This clock should run continuously.

Data Out: This is the 14-bit A/D converter output data (+2 spare bits) sent from the AFE to the DSP. The 14 bits from the A/D Converter will be the upper bits of the 16-bit word (bits 15-2). The spare bits (1 and 0) will be always be low. Eight additional (interdata) bits follow, which are always high. The data is clocked out on the falling edge of rx48xCLK. The bandwidth of the A/D converter decimation filter is equal to one-half of the symbol rate. The nominal output rate of the A/D converter is one conversion per symbol period. For more flexible post processing, there is a second true A/D conversion available in each symbol period. In Figure 4, the first conversion is shown as Data 1 and the second conversion is shown as Data 1a. It is suggested that rxbaudCLK is used with the rx48xCLK to read Data 1 while Data 1a is ignored. However, either or both outputs may be used for more flexible post-processing.

DATA OUT PER SYMBOL PERIOD

DATA	BITS
Data 1	16
Interdata Bits	8
Data 1a	16
Interdata bits	8
Total Bits/Symbol Period	48

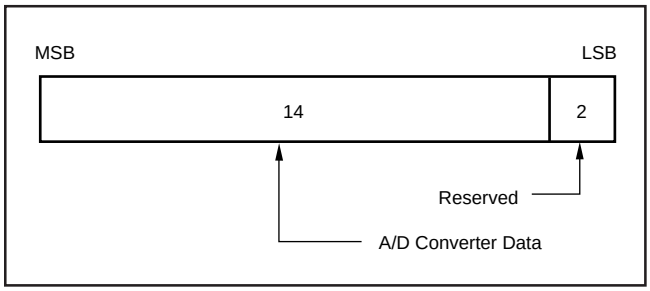


FIGURE 5. Data Out Word.

ANALOG-TO-DIGITAL CONVERTER DATA

The A/D converter data from the receive channel is coded in Binary Two's Complement.

ANALOG INPUT	A/D CONVERTER DATA
	MSB LSB
Positive Full Scale	01111111111111
Mid Scale	00000000000000
Negative Full Scale	10000000000000

ECHO CANCELLATION IN THE AFE

The rxHYB input is subtracted from the rxLINE input for first order echo cancellation. For correct operation, be certain that the rxLINE input is connected to the same polarity signal at the transformer (+ to + and – to –) while the rxHYB input is connected to opposite polarity through the compromise hybrid (– to + and + to –) as shown in Figure 6.

SCALEABLE TIMING

The AFE2124 scales operation with the clock frequency. All internal filters and the pulse former change frequency with the clock speed so that the unit can be used at different frequencies just by changing the clock speed.

For the receive channel, the digital filtering of the delta sigma converter scales directly with the clock speed. The bandwidth of the converter's decimation filter is always one-half of the symbol rate. The only receive channel issue in changing baud rate is the passive single pole anti-alias filter (see the "rxHYB and rxLINE Input Anti-Aliasing Filters" section). For systems implementing a broad range of speeds, selectable cutoff frequencies for the passive anti-alias filter should be used.

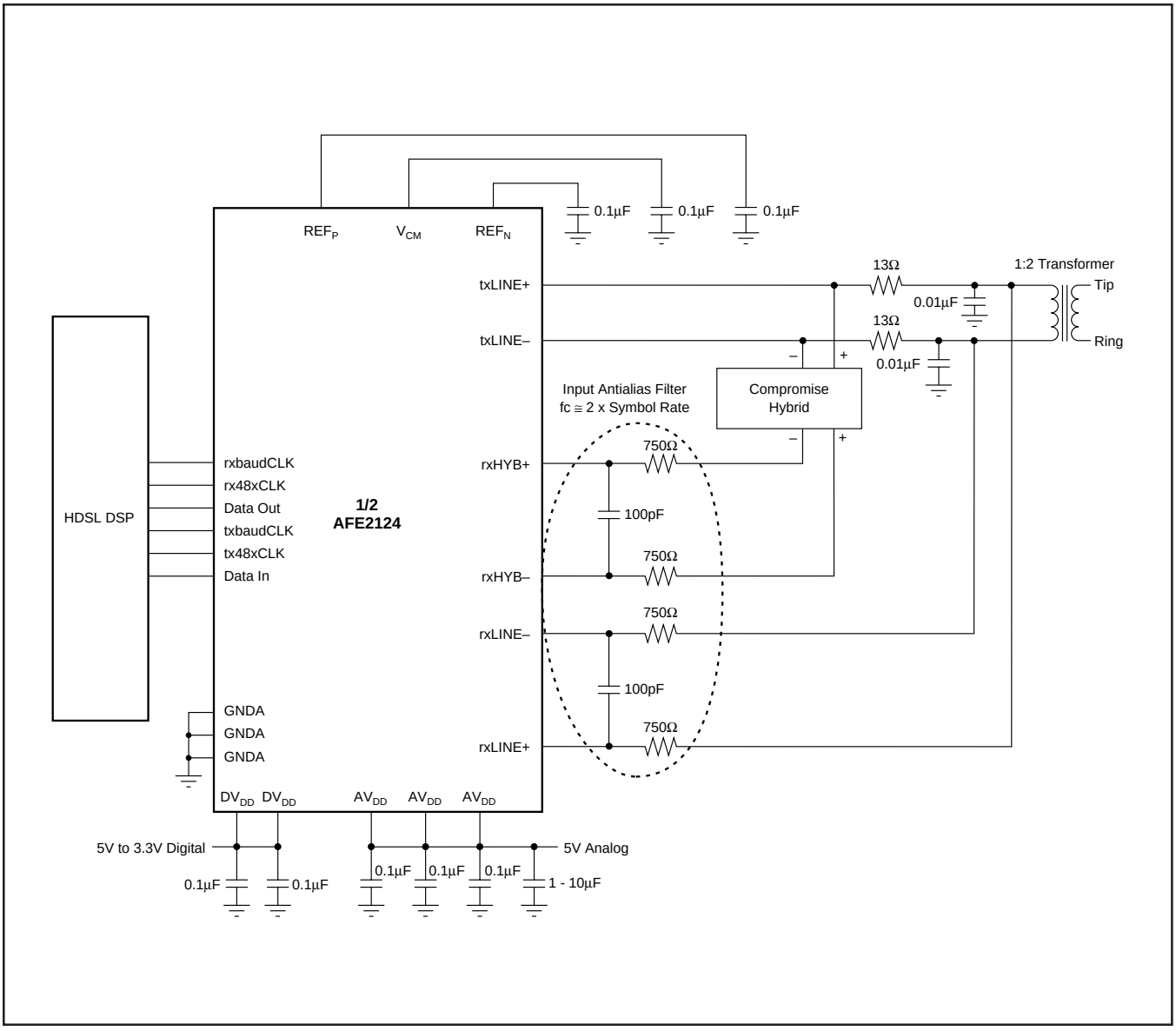


FIGURE 6. Basic Connection Diagram for Each Channel of the AFE2124.

For the transmit channel, the pulse shape and the power spectral density scale directly with the clock rate. The power spectral density shown in Curve 1 and the pulse template shown in Curve 2 are measured at the output of the transformer. The transformer and the RC circuit on the output provide some smoothing for the output transmission. At lower bit rates, the amount of smoothing will be less.

rxHYB AND rxLINE INPUT ANTI-ALIASING FILTERS

An external input antialiasing filter is needed on the hybrid and line inputs as shown in Figure 6. The –3dB frequency of the input anti-aliasing filter for the rxLINE and rxHYB differential inputs should be approximately 1MHz for T1 and E1 symbol rates. Suggested values for the filter are 750Ω for each of the two input resistors and 100pF for the capacitor. Together, the two 750Ω resistors and the 100pF capacitor result in a 3dB frequency of just over 1MHz. The 750Ω input resistors will result in minimal voltage divider loss with the input impedance of the AFE2124.

The anti-aliasing filters will give best performance with 3dB frequency approximately equal to the bit rate. For example, a 3dB frequency of 320kHz may be used for a single line bit rate of 320k bits per second.

DISCUSSION OF SPECIFICATIONS

UNCANCELED ECHO

A key measure of transceiver performance is uncancelled echo. Uncancelled echo is the summation of all of the errors in the transmit and receive paths of the AFE2124. It includes effects of linearity, distortion and noise. Uncancelled echo is tested in production by Burr-Brown with a circuit that is similar to the one shown in Figure 7.

The measurement of uncancelled echo is made as follows: The AFE is connected to an output circuit including a typical 1:2 line transformer. The line is simulated by a 135Ω resistor. Symbol sequences are generated by the tester and applied both to the AFE and to the input of an adaptive filter. The output of the adaptive filter is subtracted from the AFE output to form the uncanceled echo signal. Once the filter taps have converged, the RMS value of the uncancelled echo is calculated. Since there is no far-end signal source or additive line noise, the uncanceled echo contains only noise and linearity errors generated in the transmit and receive sections of the AFE2124.

The data sheet value for uncancelled echo is the ratio of the rms uncanceled echo (referred to the receiver input through the receiver gain) to the nominal transmitted signal (13.5dBm into 135Ω, or 1.74Vrms). This echo value is measured under a variety of conditions: with loopback enabled (line input disconnected); with loopback disabled under all receiver gain ranges; and with the line shorted (S_1 closed in Figure 7).

POWER DISSIPATION

Approximately 80% of the power dissipation in the AFE2124 is in the analog circuitry, and this component does not change with clock frequency. However, the power dissipation in the digital circuitry does decrease with lower clock frequency. In addition, the power dissipation in the digital section is decreased when operating from a smaller supply voltage, such as 3.3V. (The analog supply, AV_{DD}, must remain in the range 4.75V to 5.25V).

The power dissipation listed in the Specifications Table applies under these normal operating conditions: 5V analog power supply; 3.3V digital power supply; standard 13.5dBm delivered to the line; and a pseudo-random equiprobable sequence of HDSL output pulses. The power dissipation specifications includes all power dissipated in the AFE2124; however, it does not include power dissipated in the external load. The external power is 16.5dBm, 13.5dBm to the line, and 13.5dBm to the impedance matching resistors. The external load power of 16.5dBm is 45mW. The typical power dissipation for each half of the AFE2124 under various conditions is shown in Table II.

The T1 and E1 power measurements in the Specifications are made with the output circuit shown in Figure 7. This circuit uses a 1:2 transformer. The power measurements shown in Table II use an equivalent resistive load instead of the transformer to eliminate frequency dependent impedances of the transformer.

BIT RATE (symbols/sec)	DV_{DD} (V)	TYPICAL POWER DISSIPATION IN THE AFE2124 (per channel) (mW)
584 (E1)	+3.3	250
584 (E1)	+5	300
392 (T1)	+3.3	240
392 (T1)	+5	270
146 (E1/4)	+3.3	230
146 (E1/4)	+5	245

TABLE II. Typical Power Dissipation (per channel).

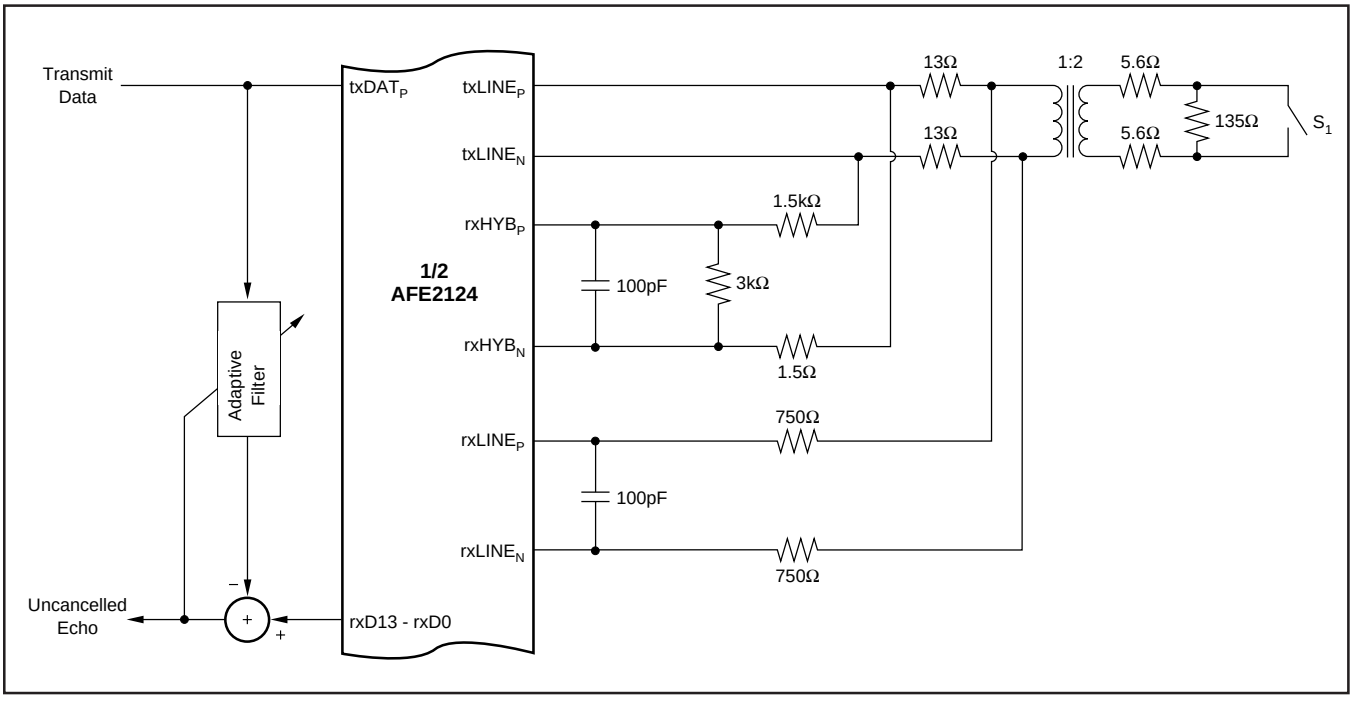


FIGURE 7. Uncancelled Echo Test Diagram.

LAYOUT

The analog front end of an HDSL system has two conflicting requirements. It must accept and deliver moderately high rate digital signals and it must generate, drive, and convert precision analog signals. To achieve optimal system performance with the AFE2124, both the digital and the analog sections must be treated carefully in board layout design.

The power supply for the digital section of the AFE2124 can range from 3.3V to 5V. This supply should be decoupled to digital ground with ceramic 0.1µF capacitors placed as close to DGND and DV_{DD} as possible. One capacitor should be placed between pins 7 and 8 and the second capacitor, between pins 41 and 42. Ideally, both a digital power supply plane and a digital ground plane should run up to and underneath the digital pins of the AFE2124 (pins 1 through 6, and pins 43 through 48). However, DV_{DD} may be supplied by a wide printed circuit board (PCB) trace. A digital ground plane underneath all digital pins is strongly recommended.

The remaining portion of the AFE2124 should be considered analog. All AGND pins should be connected directly to a common analog ground plane and all AV_{DD} pins should be connected to an analog 5V power plane. Both of these planes should have a low impedance path to the power supply. The analog power supply pins should be decoupled to analog ground with ceramic 0.1µF capacitors placed as close to the AFE2124 as possible. One 10µF tantalum capacitor should also be used with each AFE2124 between the analog supply and analog ground.

Ideally, all ground planes and traces and all power planes and traces should return to the power supply connector before being connected together (if necessary). Each ground and power pair should be routed over each other, should not overlap any portion of another pair, and the pairs should be separated by a distance of at least 0.25 inch (6mm). One exception is that the digital and analog ground planes should be connected together underneath the AFE2124 by a small trace.

PACKAGING INFORMATION

ORDERABLE DEVICE	STATUS(1)	PACKAGE TYPE	PACKAGE DRAWING	PINS	PACKAGE QTY
AFE2124E	ACTIVE	SSOP	DL	48	30
AFE2124E/1K	ACTIVE	SSOP	DL	48	1000

(1) The marketing status values are defined as follows:
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