THE DATASHEET OF

BQ3285ESS

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UNITRODE

bq3285E/L

Real-Time Clock (RTC)

Features

- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- Functionally compatible with the DS1285
  - Closely matches MC146818A pin configuration
- 2.7–3.6V operation (bq3285L); 4.5–5.5V operation (bq3285E)
- 242 bytes of general nonvolatile storage
- 32.768kHz output for power management
- System wake-up capability—alarm interrupt output active in battery-backup mode
- Less than 0.5µA load under battery operation
- Selectable Intel or Motorola bus timing
- 14 bytes for clock/calendar and control
- BCD or binary format for clock and calendar data
- Calendar in day of the week, day of the month, months, and years, with automatic leap-year adjustment
- Time of day in seconds, minutes, and hours
  - 12- or 24-hour format
  - Optional daylight saving adjustment
- Programmable square wave output
- Three individually maskable interrupt event flags:
  - Periodic rates from 122µs to 500ms
  - Time-of-day alarm once per second to once per day
  - End-of-clock update cycle
- 24-pin plastic DIP, SOIC, or SSOP

General Description

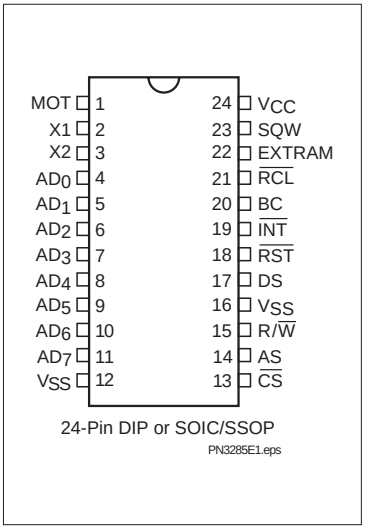
The CMOS bq3285E/L is a low-power microprocessor peripheral providing a time-of-day clock and 100-year calendar with alarm features and battery operation. The bq3285L supports 3V systems. Other bq3285E/L features include three maskable interrupt sources, square-wave output, and 242 bytes of general nonvolatile storage.

A 32.768kHz output is available for sustaining power-management activities. Wake-up capability is provided by an alarm interrupt, which is active in battery-backup mode.

The bq3285E/L write-protects the clock, calendar, and storage registers during power failure. A backup battery then maintains data and operates the clock and calendar.

The bq3285E/L is a fully compatible real-time clock for IBM AT-compatible computers and other applications. The only external components are a 32.768kHz crystal and a backup battery.

Pin Connections



24-Pin DIP or SOIC/SSOP

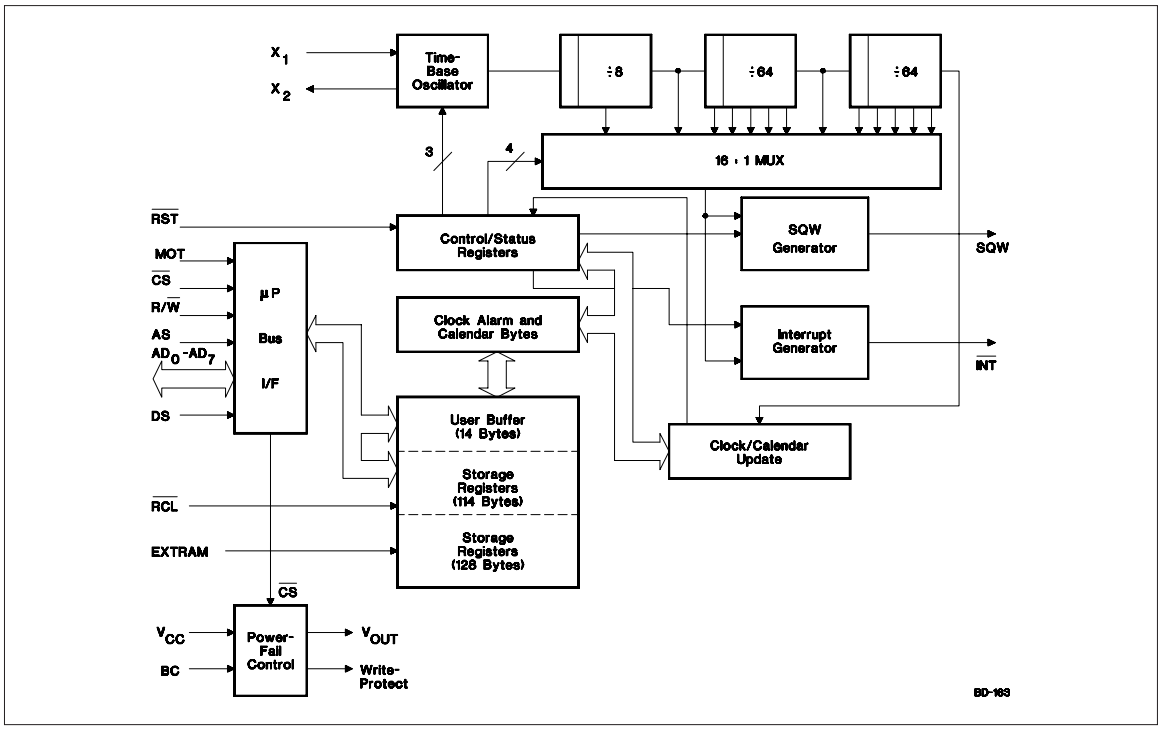
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Pin Names

AD_0–AD_7	Multiplexed address/ data input/output	$\overline{RST}$	Reset input
		SQW	Square wave output
MOT	Bus type select input	EXTRAM	Extended RAM enable
$\overline{CS}$	Chip select input	$\overline{RCL}$	RAM clear input
AS	Address strobe input	BC	3V backup cell input
DS	Data strobe input	X1–X2	Crystal inputs
R/$\overline{W}$	Read/write input	V_{CC}	Power supply
$\overline{INT}$	Interrupt request output	V_{SS}	Ground

SLUS004A -DECEMBER 1993 - REVISED MAY 2004

Block Diagram



Pin Descriptions

MOT **Bus type select input**

MOT selects bus timing for either Motorola or Intel architecture. This pin should be tied to V_{CC} for Motorola timing or to V_{SS} for Intel timing (see Table 1). The setting should not be changed during system operation. MOT is internally pulled low by a 30KΩ resistor.

Table 1. Bus Setup

Bus Type	MOT Level	DS Equivalent	R/$\overline{W}$ Equivalent	AS Equivalent
Motorola	V_{CC}	DS, E, or Φ2	R/$\overline{W}$	AS
Intel	V_{SS}	$\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$	$\overline{WR}$, $\overline{MEMW}$, or $\overline{I/OW}$	ALE

AD_0–AD_7 **Multiplexed address/data input/ output**

The bq3285E/L bus cycle consists of two phases: the address phase and the data-transfer phase. The address phase precedes the data-transfer phase. During the address phase, an address placed on AD_0–AD_7 and EXTRAM is latched into the bq3285E/L on the falling edge of the AS signal. During the data-transfer phase of the bus cycle, the AD_0–AD_7 pins serve as a bidirectional data bus.

AS **Address strobe input**

AS serves to demultiplex the address/data bus. The falling edge of AS latches the address on AD_0–AD_7 and EXTRAM. This demultiplexing process is independent of the $\overline{CS}$ signal. For DIP and SOIC packages with MOT = V_{SS}, the AS input is provided a signal similar to ALE in an Intel-based system.

DS **Data strobe input**

When MOT = V_{CC}, DS controls data transfer during a bq3285E/L bus cycle. During a read cycle, the bq3285E/L drives the bus after the rising edge on DS. During a write cycle, the falling edge on DS is used to latch write data into the chip.

When MOT = V_{SS}, the DS input is provided a signal similar to $\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$ in an Intel-based system. The falling edge on DS is used to enable the outputs during a read cycle.

R/$\overline{W}$ **Read/write input**

When MOT = V_{CC}, the level on R/$\overline{W}$ identifies the direction of data transfer. A high level on R/$\overline{W}$ indicates a read bus cycle, whereas a low on this pin indicates a write bus cycle.

When MOT = V_{SS}, R/$\overline{W}$ is provided a signal similar to $\overline{WR}$, $\overline{MEMW}$, or $\overline{I/OW}$ in an Intel-based system. The rising edge on R/$\overline{W}$ latches data into the bq3285E/L.

$\overline{CS}$ **Chip select input**

$\overline{CS}$ should be driven low and held stable during the data-transfer phase of a bus cycle accessing the bq3285E/L.

$\overline{INT}$ **Interrupt request output**

$\overline{INT}$ is an open-drain output. This allows alarm $\overline{INT}$ to be valid in battery-backup mode. To use this feature, $\overline{INT}$ must be connected to a power supply other than V_{CC}. $\overline{INT}$ is asserted low when any event flag is set and the corresponding event enable bit is also set. $\overline{INT}$ becomes high-impedance whenever register C is read (see the Control/Status Registers section).

SQW **Square-wave output**

SQW may output a programmable frequency square-wave signal during normal (V_{CC} valid) system operation. Any one of the 13 specific frequencies may be selected through register A. This pin is held low when the square-wave enable bit (SQWE) in register B is 0 (see the Control/Status Registers section).

A 32.768kHz output is enabled by setting the SQWE bit in register B to 1 and the 32KE bit in register C to 1 after setting OSC2–OSC0 in register A to 011 (binary).

EXTRAM **Extended RAM enable**

Enables 128 bytes of additional nonvolatile SRAM. It is connected internally to a 30K Ω pull-down resistor. To access the RTC registers, EXTRAM must be low.

$\overline{RCL}$ **RAM clear input**

A low level on the $\overline{RCL}$ pin causes the contents of each of the 242 storage bytes to be set to FF(hex). The contents of the clock and control registers are unaffected. This pin should be used as a user-interface input (pushbutton to ground) and not connected to the output of any active component. $\overline{RCL}$ input is only recognized when held low for at least 125ms in the presence of V_{CC}. Using RAM clear does not affect the battery load. This pin is connected internally to a 30KΩ pull-up resistor.

BC **3V backup cell input**

BC should be connected to a 3V backup cell for RTC operation and storage register nonvolatility in the absence of system power. When V_{CC} slews down past V_{BC} (3V typical), the integral control circuitry switches the power source to BC. When V_{CC} returns above V_{BC}, the power source is switched to V_{CC}.

Upon power-up, a voltage within the V_{BC} range must be present on the BC pin for the oscillator to start up.

$\overline{RST}$ **Reset input**

The bq3285E/L is reset when $\overline{RST}$ is pulled low. When reset, $\overline{INT}$ becomes high impedance, and the bq3285E/L is not accessible. Table 4 in the Control/Status Registers section lists the register bits that are cleared by a reset.

Reset may be disabled by connecting $\overline{RST}$ to V_{CC}. This allows the control bits to retain their states through power-down/power-up cycles.

X1–X2 **Crystal inputs**

The X1–X2 inputs are provided for an external 32.768kHz quartz crystal, Daiwa DT-26 or equivalent, with 6pF load capacitance. A trimming capacitor may be necessary for extremely precise time-base generation.

In the absence of a crystal, a 32.768kHz waveform can be fed into the X1 input.

Functional Description

Address Map

The bq3285E/L provides 14 bytes of clock and control/status registers and 242 bytes of general nonvolatile storage. Figure 1 illustrates the address map for the bq3285E/L.

Update Period

The update period for the bq3285E/L is one second. The bq3285E/L updates the contents of the clock and calendar locations during the update cycle at the end of each update period (see Figure 2). The alarm flag bit may also be set during the update cycle.

The bq3285E/L copies the local register updates into the user buffer accessed by the host processor. When a 1 is written to the update transfer inhibit bit (UTI) in register B, the user copy of the clock and calendar bytes remains unchanged, while the local copy of the same bytes continues to be updated every second.

The update-in-progress bit (UIP) in register A is set t_{BUC} time before the beginning of an update cycle (see Figure 2). This bit is cleared and the update-complete flag (UF) is set at the end of the update cycle.

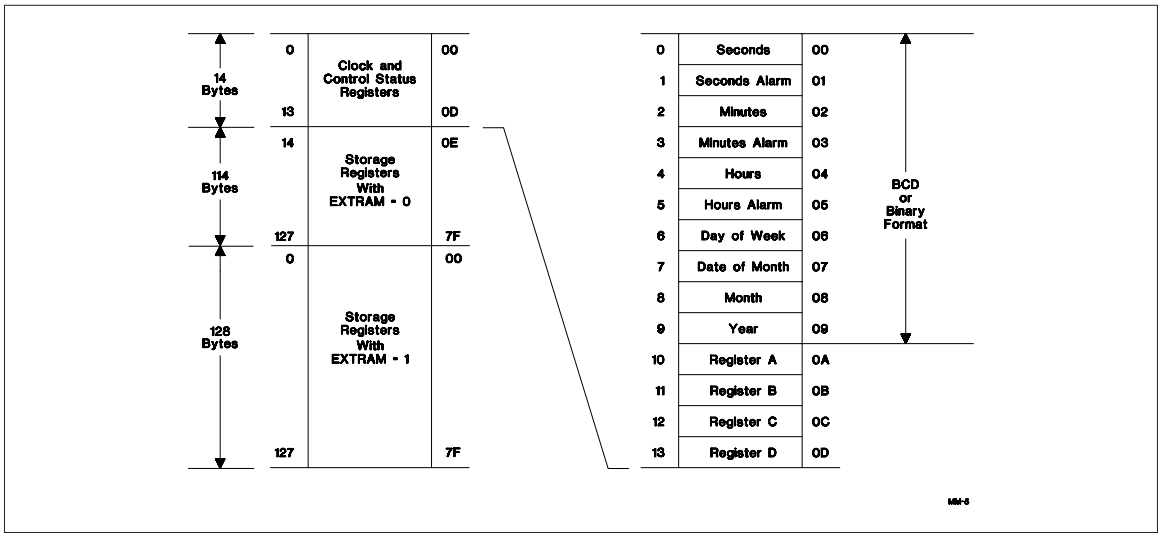


Figure 1. Address Map

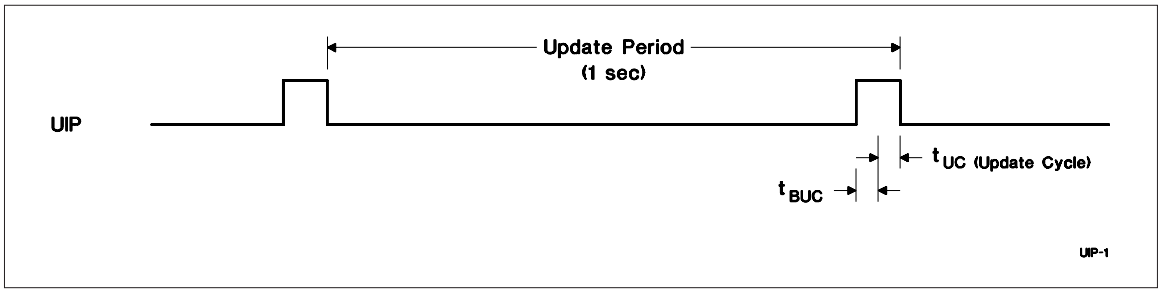


Figure 2. Update Period Timing and UIP

Programming the RTC

The time-of-day, alarm, and calendar bytes can be written in either the BCD or binary format (see Table 2).

These steps may be followed to program the time, alarm, and calendar:

1. Modify the contents of register B:
   a. Write a 1 to the UTI bit to prevent transfers between RTC bytes and user buffer.
   b. Write the appropriate value to the data format (DF) bit to select BCD or binary format for all time, alarm, and calendar bytes.
   c. Write the appropriate value to the hour format (HF) bit.
2. Write new values to all the time, alarm, and calendar locations.
3. Clear the UTI bit to allow update transfers.

On the next update cycle, the RTC updates all 10 bytes in the selected format.

Table 2. Time, Alarm, and Calendar Formats

Address	RTC Bytes	Range		
		Decimal	Binary	Binary-Coded Decimal
0	Seconds	0–59	00H–3BH	00H–59H
1	Seconds alarm	0–59	00H–3BH	00H–59H
2	Minutes	0–59	00H–3BH	00H–59H
3	Minutes alarm	0–59	00H–3BH	00H–59H
4	Hours, 12-hour format	1–12	01H–OCH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours, 24-hour format	0–23	00H–17H	00H–23H
5	Hours alarm, 12-hour format	1–12	01H–OCH AM; 81H–8CH PM	01H–12H AM; 81H–92H PM
	Hours alarm, 24-hour format	0–23	00H–17H	00H–23H
6	Day of week (1=Sunday)	1–7	01H–07H	01H–07H
7	Day of month	1–31	01H–1FH	01H–31H
8	Month	1–12	01H–0CH	01H–12H
9	Year	0–99	00H–63H	00H–99H

Square-Wave Output

The bq3285E/L divides the 32.768kHz oscillator frequency to produce the 1Hz update frequency for the clock and calendar. Thirteen taps from the frequency divider are fed to a 16:1 multiplexer circuit. The output of this mux is fed to the SQW output and periodic interrupt generation circuitry. The four least-significant bits of register A, RS0–RS3, select among the 13 taps (see Table 3). The square-wave output is enabled by writing a 1 to the square-wave enable bit (SQWE) in register B. A 32.768kHz output may be selected by setting OSC2–OSC0 in register A to 011 while SQWE = 1 and 32KE = 1.

Interrupts

The bq3285E/L allows three individually selected interrupt events to generate an interrupt request. These three interrupt events are:

- The periodic interrupt, programmable to occur once every 122µs to 500ms.
- The alarm interrupt, programmable to occur once per second to once per day, is active in battery-backup mode, providing a "wake-up" feature.
- The update-ended interrupt, which occurs at the end of each update cycle.

Each of the three interrupt events is enabled by an individual interrupt-enable bit in register B. When an event occurs, its event flag bit in register C is set. If the corresponding event enable bit is also set, then an interrupt request is generated. The interrupt request flag bit (INTF) of register C is set with every interrupt request. Reading register C clears all flag bits, including INTF, and makes INT high-impedance.

Two methods can be used to process bq3285E/L interrupt events:

- Enable interrupt events and use the interrupt request output to invoke an interrupt service routine.
- Do not enable the interrupts and use a polling routine to periodically check the status of the flag bits.

The individual interrupt sources are described in detail in the following sections.

Table 3. Square-Wave Frequency/Periodic Interrupt Rate

Register A Bits							Square Wave		Periodic Interrupt	
OSC2	OSC1	OSC0	RS3	RS2	RS1	RS0	Frequency	Units	Period	Units
0	1	0	0	0	0	0	None		None	
0	1	0	0	0	0	1	256	Hz	3.90625	ms
0	1	0	0	0	1	0	128	Hz	7.8125	ms
0	1	0	0	0	1	1	8.192	kHz	122.070	µs
0	1	0	0	1	0	0	4.096	kHz	244.141	µs
0	1	0	0	1	0	1	2.048	kHz	488.281	µs
0	1	0	0	1	1	0	1.024	kHz	976.5625	µs
0	1	0	0	1	1	1	512	Hz	1.95315	ms
0	1	0	1	0	0	0	256	Hz	3.90625	ms
0	1	0	1	0	0	1	128	Hz	7.8125	ms
0	1	0	1	0	1	0	64	Hz	15.625	ms
0	1	0	1	0	1	1	32	Hz	31.25	ms
0	1	0	1	1	0	0	16	Hz	62.5	ms
0	1	0	1	1	0	1	8	Hz	125	ms
0	1	0	1	1	1	0	4	Hz	250	ms
0	1	0	1	1	1	1	2	Hz	500	ms
0	1	1	X	X	X	X	32.768	kHz	same as above defined by RS3–RS0	

Periodic Interrupt

The mux output used to drive the SQW output also drives the interrupt-generation circuitry. If the periodic interrupt event is enabled by writing a 1 to the periodic interrupt enable bit (PIE) in register C, an interrupt request is generated once every 122µs to 500ms. The period between interrupts is selected by the same bits in register A that select the square wave frequency (see Table 3). Setting OSC2–OSC0 in register A to 011 does not affect the periodic interrupt timing.

Alarm Interrupt

The alarm interrupt is active in battery-backup mode, providing a "wake-up" capability. During each update cycle, the RTC compares the hours, minutes, and seconds bytes with the three corresponding alarm bytes. If a match of all bytes is found, the alarm interrupt event flag bit, AF in register C, is set to 1. If the alarm event is enabled, an interrupt request is generated.

An alarm byte may be removed from the comparison by setting it to a "don't care" state. An alarm byte is set to a "don't care" state by writing a 1 to each of its two most-significant bits. A "don't care" state may be used to select the frequency of alarm interrupt events as follows:

- If none of the three alarm bytes is "don't care," the frequency is once per day, when hours, minutes, and seconds match.
- If only the hour alarm byte is "don't care," the frequency is once per hour, when minutes and seconds match.
- If only the hour and minute alarm bytes are "don't care," the frequency is once per minute, when seconds match.
- If the hour, minute, and second alarm bytes are "don't care," the frequency is once per second.

Update Cycle Interrupt

The update cycle ended flag bit (UF) in register C is set to a 1 at the end of an update cycle. If the update interrupt enable bit (UIE) of register B is 1, and the update transfer inhibit bit (UTI) in register B is 0, then an interrupt request is generated at the end of each update cycle.

Accessing RTC bytes

The EXTRAM pin must be low to access the RTC registers. Time and calendar bytes read during an update cycle may be in error. Three methods to access the time and calendar bytes without ambiguity are:

- Enable the update interrupt event to generate interrupt requests at the end of the update cycle. The interrupt handler has a maximum of 999ms to access the clock bytes before the next update cycle begins (see Figure 3).
- Poll the update-in-progress bit (UIP) in register A. If UIP = 0, the polling routine has a minimum of t_{BUC} time to access the clock bytes (see Figure 3).
- Use the periodic interrupt event to generate interrupt requests every t_{PI} time, such that UIP = 1 always occurs between the periodic interrupts. The interrupt handler has a minimum of $t_{PI}/2 + t_{BUC}$ time to access the clock bytes (see Figure 3).

Oscillator Control

When power is first applied to the bq3285E/L and V_{CC} is above V_{PFD}, the internal oscillator and frequency divider are turned on by writing a 010 pattern to bits 4 through 6 of register A. A pattern of 011 behaves as 010 but additionally transforms register C into a read/write register. This allows the 32.768kHz output on the square wave pin to be turned on. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. Any other pattern to these bits keeps the oscillator off.

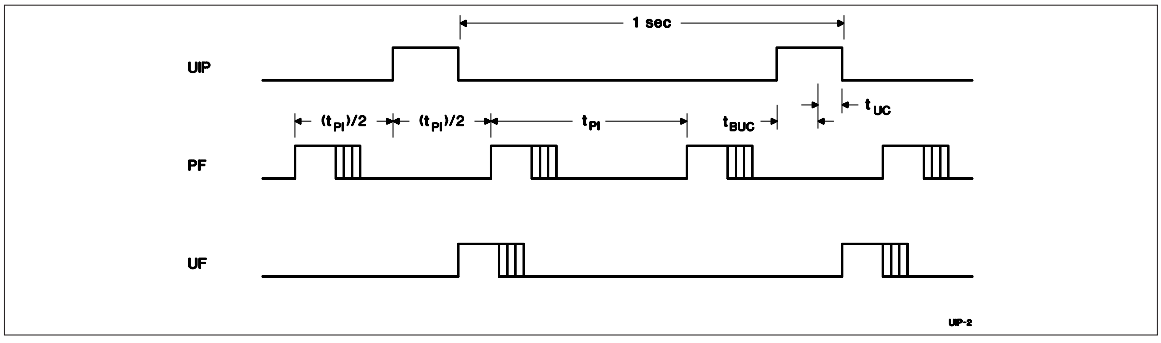


Figure 3. Update-Ended/Periodic Interrupt Relationship

Power-Down/Power-Up Cycle

The bq3285E and bq3285L power-up/power-down cycles are different. The bq3285L continuously monitors V_{CC} for out-of-tolerance. During a power failure, when V_{CC} falls below V_{PFD} (2.53V typical), the bq3285L write-protects the clock and storage registers. The power source is switched to BC when V_{CC} is less than V_{PFD} and BC is greater than V_{PFD}, or when V_{CC} is less than V_{BC} and V_{BC} is less than V_{PFD}. RTC operation and storage data are sustained by a valid backup energy source. When V_{CC} is above V_{PFD}, the power source is V_{CC}. Write-protection continues for t_{CSR} time after V_{CC} rises above V_{PFD}.

The bq3285E continuously monitors V_{CC} for out-of-tolerance. During a power failure, when V_{CC} falls below V_{PFD} (4.17V typical), the bq3285E write-protects the clock and storage registers. When V_{CC} is below V_{BC} (3V typical), the power source is switched to BC. RTC operation and storage data are sustained by a valid backup energy source. When V_{CC} is above V_{BC}, the power source is V_{CC}. Write-protection continues for t_{CSR} time after V_{CC} rises above V_{PFD}.

Control/Status Registers

The four control/status registers of the bq3285E/L are accessible regardless of the status of the update cycle (see Table 4).

Register A

Register A Bits							
7	6	5	4	3	2	1	0
UIP	OS2	OS1	OS0	RS3	RS2	RS1	RS0

Register A programs:

- The frequency of the square-wave and the periodic event rate.
- Oscillator operation.

Register A provides:

- Status of the update cycle.

RS0–RS3 - Frequency Select

7	6	5	4	3	2	1	0
-	-	-	-	RS3	RS2	RS1	RS0

These bits select one of the 13 frequencies for the SQW output and the periodic interrupt rate, as shown in Table 3.

OS0–OS2 - Oscillator Control

7	6	5	4	3	2	1	0
-	OS2	OS1	OS0	-	-	-	-

These three bits control the state of the oscillator and divider stages. A pattern of 010 enables RTC operation by turning on the oscillator and enabling the frequency divider. A pattern of 011 behaves as 010 but additionally transforms register C into a read/write register. This allows the 32.768kHz output on the square wave pin to be turned on. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. When 010 is written, the RTC begins its first update after 500ms.

UIP - Update Cycle Status

7	6	5	4	3	2	1	0
UIP	-	-	-	-	-	-	-

This read-only bit is set prior to the update cycle. When UIP equals 1, an RTC update cycle may be in progress. UIP is cleared at the end of each update cycle. This bit is also cleared when the update transfer inhibit (UTI) bit in register B is 1.

Table 4. Control/Status Registers

Reg.	Loc. (Hex)	Read	Write	Bit Name and State on Reset															
				7 (MSB)		6		5		4		3		2		1		0 (LSB)	
A	0A	Yes	Yes[1]	UIP	na	OS2	na	OS1	na	OS0	na	RS3	na	RS2	na	RS1	na	RS0	na
B	0B	Yes	Yes	UTI	na	PIE	0	AIE	0	UIE	0	SQWE	0	DF	na	HF	na	DSE	na
C	0C	Yes	No[2]	INTF	0	PF	0	AF	0	UF	0	-	0	32KE	na	-	0	-	0
D	0D	Yes	No	VRT	na	-	0	-	0	-	0	-	0	-	0	-	0	-	0

Notes: na = not affected.
1. Except bit 7.
2. Read/write only when OSC2–OSC0 in register A is 011 (binary).

Register B

Register B Bits							
7	6	5	4	3	2	1	0
UTI	PIE	AIE	UIE	SQWE	DF	HF	DSE

Register B enables:

- Update cycle transfer operation
- Square-wave output
- Interrupt events
- Daylight saving adjustment

Register B selects:

- Clock and calendar data formats

All bits of register B are read/write.

DSE - Daylight Saving Enable

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	DSE

This bit enables daylight-saving time adjustments when written to 1:

- On the last Sunday in October, the first time the bq3285E/L increments past 1:59:59 AM, the time falls back to 1:00:00 AM.
- On the first Sunday in April, the time springs forward from 2:00:00 AM to 3:00:00 AM.

HF - Hour Format

7	6	5	4	3	2	1	0
-	-	-	-	-	-	HF	-

This bit selects the time-of-day and alarm hour format:

1 = 24-hour format

0 = 12-hour format

DF - Data Format

7	6	5	4	3	2	1	0
-	-	-	-	-	DF	-	-

This bit selects the numeric format in which the time, alarm, and calendar bytes are represented:

1 = Binary

0 = BCD

SQWE - Square-Wave Enable

7	6	5	4	3	2	1	0
-	-	-	-	SQWE	-	-	-

This bit enables the square-wave output:

1 = Enabled

0 = Disabled and held low

UIE - Update Cycle Interrupt Enable

7	6	5	4	3	2	1	0
-	-	-	UIE	-	-	-	-

This bit enables an interrupt request due to an update ended interrupt event:

1 = Enabled

0 = Disabled

The UIE bit is automatically cleared when the UTI bit equals 1.

AIE - Alarm Interrupt Enable

7	6	5	4	3	2	1	0
-	-	AIE	-	-	-	-	-

This bit enables an interrupt request due to an alarm interrupt event:

1 = Enabled

0 = Disabled

PIE - Periodic Interrupt Enable

7	6	5	4	3	2	1	0
-	PIE	-	-	-	-	-	-

This bit enables an interrupt request due to a periodic interrupt event:

1 = Enabled

0 = Disabled

UTI - Update Transfer Inhibit

7	6	5	4	3	2	1	0
UTI	-	-	-	-	-	-	-

This bit inhibits the transfer of RTC bytes to the user buffer:

1 = Inhibits transfer and clears UIE

0 = Allows transfer

Register C

Register C is the read-only event status register.

Register C Bits							
7	6	5	4	3	2	1	0
INTF	PF	AF	UF	0	32KE	0	0

Bits 0, 1, 3 - Unused Bits

These bits are always set to 0.

7	6	5	4	3	2	1	0
-	-	-	-	0	-	0	0

32KE - 32kHz Enable Output

This bit may be set to a 1 only when the OSC2–OSC0 bits in register A are set to 011. Setting OSC2–OSC0 to

7	6	5	4	3	2	1	0
-	-	-	-	-	32KE	-	-

anything other than 011 clears this bit. If SQWE in register B and 32KE are set, a 32.768kHz waveform is output on the square wave pin.

UF - Update Event Flag

This bit is set to a 1 at the end of the update cycle.

7	6	5	4	3	2	1	0
-	-	-	UF	-	-	-	-

Reading register C clears this bit.

AF - Alarm Event Flag

This bit is set to a 1 when an alarm event occurs. Reading register C clears this bit.

7	6	5	4	3	2	1	0
-	-	AF	-	-	-	-	-

PF - Periodic Event Flag

This bit is set to a 1 every t_{PI} time, where t_{PI} is the time period selected by the settings of RS0–RS3 in register A. Reading register C clears this bit.

7	6	5	4	3	2	1	0
-	PF	-	-	-	-	-	-

INTF - Interrupt Request Flag

This flag is set to a 1 when any of the following is true:

AIE = 1 and AF = 1

PIE = 1 and PF = 1

7	6	5	4	3	2	1	0
INTF	-	-	-	-	-	-	-

UIE = 1 and UF = 1

Reading register C clears this bit.

Register D

Register D is the read-only data integrity status register.

Bits 0–6 - Unused Bits

These bits are always set to 0.

VRT - Valid RAM and Time

Register D Bits							
7	6	5	4	3	2	1	0
VRT	0	0	0	0	0	0	0

1 = Valid backup energy source

0 = Backup energy source is depleted

7	6	5	4	3	2	1	0
-	0	0	0	0	0	0	0

When the backup energy source is depleted (VRT = 0), data integrity of the RTC and storage registers is not guaranteed.

7	6	5	4	3	2	1	0
VRT	-	-	-	-	-	-	-

Absolute Maximum Ratings—bq3285E

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Absolute Maximum Ratings—bq3285L

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 6.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 6.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions—bq3285E ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IL}	Input low voltage	-0.3	-	0.8	V
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V
V_{BC}	Backup cell voltage	2.5	-	4.0	V

Note: Typical values indicate operation at T_A = 25°C.

Recommended DC Operating Conditions—bq3285L ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Supply voltage	2.7	3.15	3.6	V
V_{SS}	Supply voltage	0	0	0	V
V_{IL}	Input low voltage	-0.3	-	0.6	V
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V
V_{BC}	Backup cell voltage	2.4	-	4.0	V

Note: Typical values indicate operation at T_A = 25°C.

Crystal Specifications—bq3285E/L (DT-26 or Equivalent)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
f_O	Oscillation frequency	-	32.768	-	kHz
C_L	Load capacitance	-	6	-	pF
T_P	Temperature turnover point	20	25	30	°C
k	Parabolic curvature constant	-	-	-0.042	ppm/°C
Q	Quality factor	40,000	70,000	-	
R_1	Series resistance	-	-	45	KΩ
C_0	Shunt capacitance	-	1.1	1.8	pF
C_0/C_1	Capacitance ratio	-	430	600	
D_L	Drive level	-	-	1	µW
$\Delta f/f_O$	Aging (first year at 25°C)	-	1	-	ppm

DC Electrical Characteristics—bq3285E ($T_A = T_{OPR}$, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	AD_0–AD_7, $\overline{INT}$, and SQW in high impedance, $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -2.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 4.0 mA
I_{CC}	Operating supply current	-	7	15	mA	Min. cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
I_{CCSB}	Standby supply current	-	300	-	µA	$V_{IN} = V_{SS}$ or V_{CC}, $\overline{CS} \geq V_{CC}$ - 0.2
V_{SO}	Supply switch-over voltage	-	V_{BC}	-	V	
I_{CCB}	Battery operation current	-	0.3	0.5	µA	V_{BC} = 3V, T_A = 25°C
V_{PFD}	Power-fail-detect voltage	4.0	4.17	4.35	V	
I_{RCL}	Input current when $\overline{RCL} = V_{SS}$.	-	-	185	µA	Internal 30K pull-up
I_{MOTH}	Input current when MOT = V_{CC}	-	-	-185	µA	Internal 30K pull-down
	Input current when MOT = V_{SS}	-	-	0	µA	Internal 30K pull-down
I_{XTRAM}	Input current when EXTRAM = V_{CC}	-	-	-185	µA	Internal 30K pull-down
	Input current when EXTRAM = V_{SS}	-	-	0	µA	Internal 30K pull-down

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V or V_{BC} = 3V.

DC Electrical Characteristics—bq3285L ($T_A = T_{OPR}$, V_{CC} = 3.15V ±0.45V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	AD_0–AD_7 and $\overline{INT}$ in high impedance, $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output high voltage	2.2	-	-	V	I_{OH} = -1.0 mA
V_{OL}	Output low voltage	-	-	0.4	V	I_{OL} = 2.0 mA
I_{CC}	Operating supply current	-	5	9	mA	Min. cycle, duty = 100%, I_{OH} = 0mA, I_{OL} = 0mA
I_{CCSB}	Standby supply current	-	100	-	µA	$V_{IN} = V_{SS}$ or V_{CC}, $\overline{CS} \geq V_{CC}$ - 0.2
V_{SO}	Supply switch-over voltage	-	V_{PFD}	-	V	$V_{BC} > V_{PFD}$
		-	V_{BC}	-	V	$V_{BC} < V_{PFD}$
I_{CCB}	Battery operation current	-	0.3	0.5	µA	V_{BC} = 3V, T_A = 25°C, $V_{CC} < V_{BC}$
V_{PFD}	Power-fail-detect voltage	2.4	2.53	2.65	V	
I_{RCL}	Input current when $\overline{RCL} = V_{SS}$.	-	-	120	µA	Internal 30K pull-up
I_{MOTH}	Input current when MOT = V_{CC}	-	-	-120	µA	Internal 30K pull-down
	Input current when MOT = V_{SS}	-	-	0	µA	Internal 30K pull-down
I_{XTRAM}	Input current when EXTRAM = V_{CC}	-	-	-120	µA	Internal 30K pull-down
	Input current when EXTRAM = V_{SS}	-	-	0	µA	Internal 30K pull-down

Note: Typical values indicate operation at T_A = 25°C, V_{CC} = 3V.

Capacitance—bq3285E/L (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	7	pF	V_{OUT} = 0V
C_{IN}	Input capacitance	-	-	5	pF	V_{IN} = 0V

Note: This parameter is sampled and not 100% tested. It does not include the X1 or X2 pin.

AC Test Conditions—bq3285E

Parameter	Test Conditions
Input pulse levels	0 to 3.0 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 4 and 5

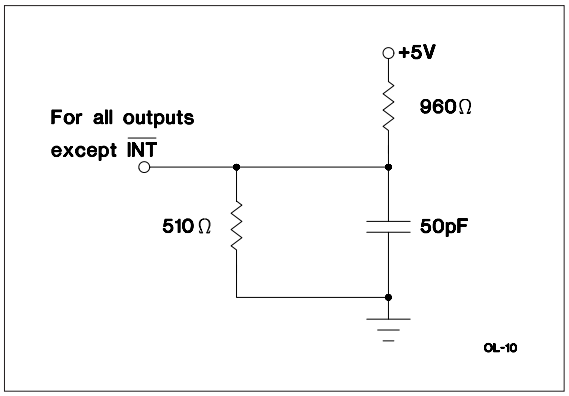


Figure 4. Output Load A—bq3285E

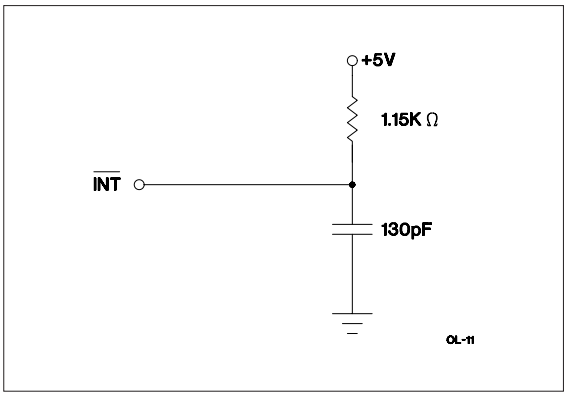


Figure 5. Output Load B—bq3285E

AC Test Conditions—bq3285L

Parameter	Test Conditions
Input pulse levels	0 to 2.3 V
Input rise and fall times	5 ns
Input and output timing reference levels	1.2 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 6 and 7

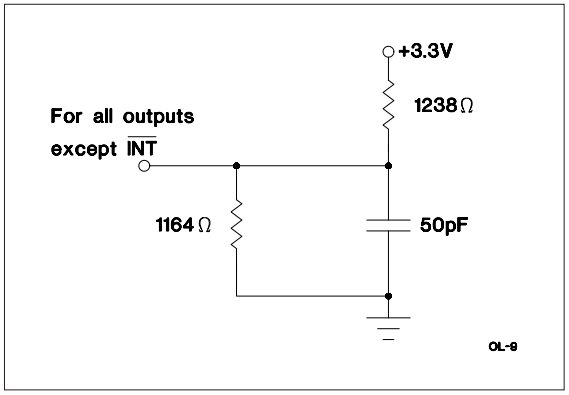


Figure 6. Output Load A—bq3285L

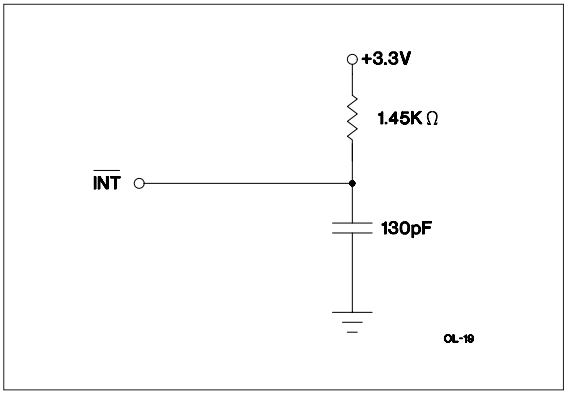


Figure 7. Output Load B—bq3285L

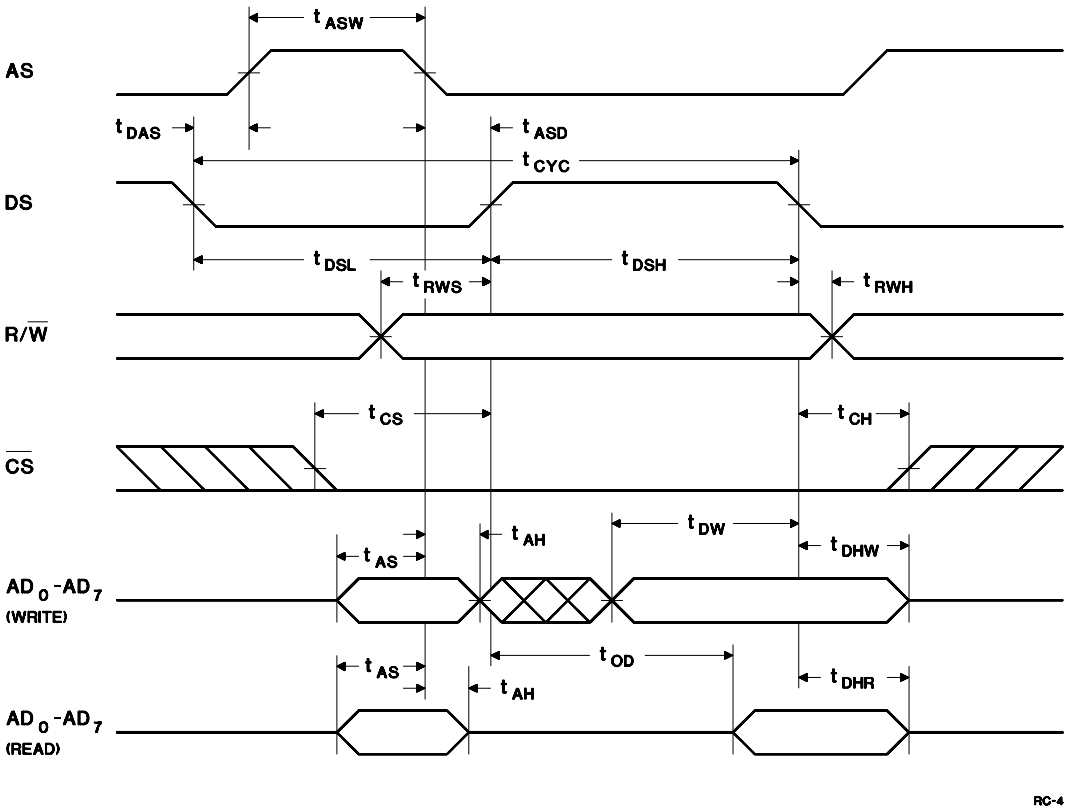
Read/Write Timing—bq3285E ($T_A = T_{OPR}$, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYC}	Cycle time	160	-	-	ns	
t_{DSL}	DS low or $\overline{RD}/\overline{WR}$ high time	80	-	-	ns	
t_{DSH}	DS high or $\overline{RD}/\overline{WR}$ low time	55	-	-	ns	
t_{RWH}	R/$\overline{W}$ hold time	0	-	-	ns	
t_{RWS}	R/$\overline{W}$ setup time	10	-	-	ns	
t_{CS}	Chip select setup time	5	-	-	ns	
t_{CH}	Chip select hold time	0	-	-	ns	
t_{DHR}	Read data hold time	0	-	25	ns	
t_{DHW}	Write data hold time	0	-	-	ns	
t_{AS}	Address setup time	20	-	-	ns	
t_{AH}	Address hold time	5	-	-	ns	
t_{DAS}	Delay time, DS to AS rise	10	-	-	ns	
t_{ASW}	Pulse width, AS high	30	-	-	ns	
t_{ASD}	Delay time, AS to DS rise ($\overline{RD}/\overline{WR}$ fall)	35	-	-	ns	
t_{OD}	Output data delay time from DS rise ($\overline{RD}$ fall)	-	-	50	ns	
t_{DW}	Write data setup time	30	-	-	ns	
t_{BUC}	Delay time before update cycle	-	244	-	µs	
t_{PI}	Periodic interrupt time interval	-	-	-	-	See Table 3
t_{UC}	Time of update cycle	-	1	-	µs	

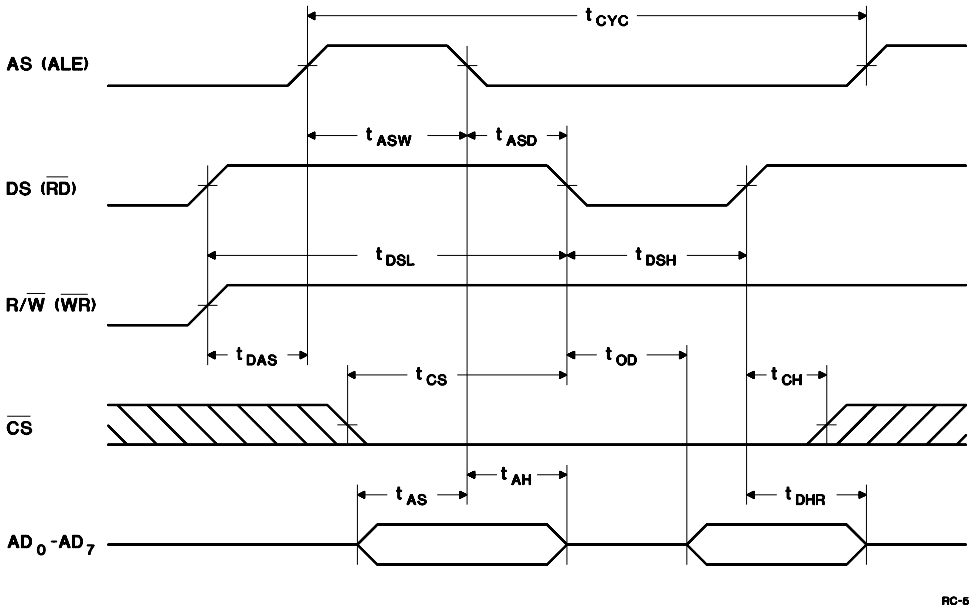
Read/Write Timing—bq3285L ($T_A = T_{OPR}$, V_{CC} = 3.15V ± 0.45V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYC}	Cycle time	270	-	-	ns	
t_{DSL}	DS low or $\overline{RD}/\overline{WR}$ high time	135	-	-	ns	
t_{DSH}	DS high or $\overline{RD}/\overline{WR}$ low time	90	-	-	ns	
t_{RWH}	R/$\overline{W}$ hold time	0	-	-	ns	
t_{RWS}	R/$\overline{W}$ setup time	15	-	-	ns	
t_{CS}	Chip select setup time	8	-	-	ns	
t_{CH}	Chip select hold time	0	-	-	ns	
t_{DHR}	Read data hold time	0	-	40	ns	
t_{DHW}	Write data hold time	0	-	-	ns	
t_{AS}	Address setup time	30	-	-	ns	
t_{AH}	Address hold time	15	-	-	ns	
t_{DAS}	Delay time, DS to AS rise	15	-	-	ns	
t_{ASW}	Pulse width, AS high	50	-	-	ns	
t_{ASD}	Delay time, AS to DS rise ($\overline{RD}/\overline{WR}$ fall)	55	-	-	ns	
t_{OD}	Output data delay time from DS rise ($\overline{RD}$ fall)	-	-	100	ns	
t_{DW}	Write data setup time	50	-	-	ns	
t_{BUC}	Delay time before update cycle	-	244	-	µs	
t_{PI}	Periodic interrupt time interval	-	-	-	-	See Table 3
t_{UC}	Time of update cycle	-	1	-	µs	

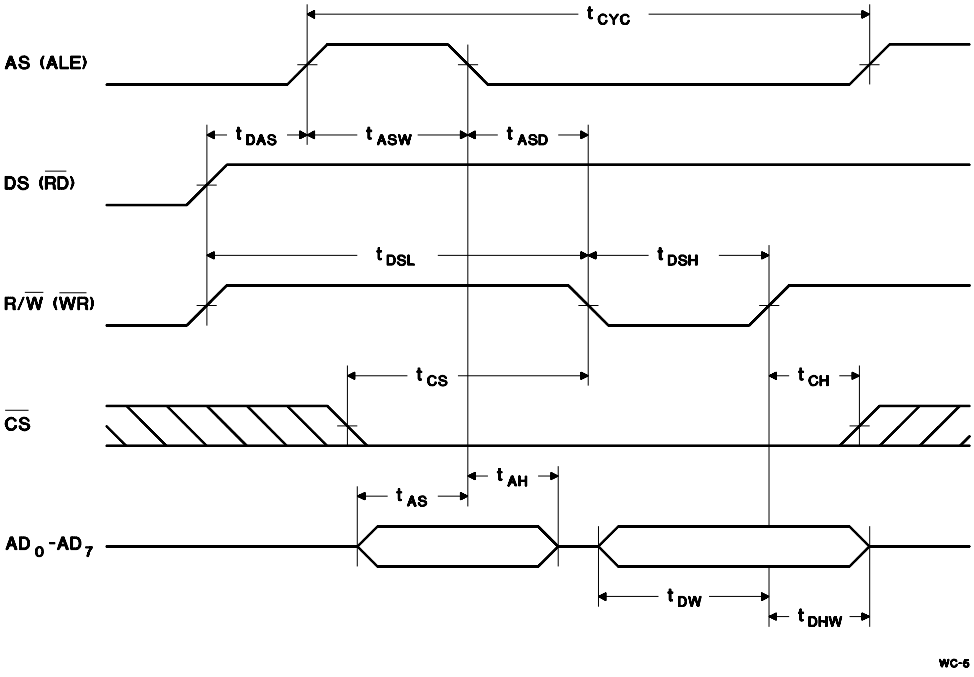
Motorola Bus Read/Write Timing—bq3285E/L



Intel Bus Read Timing—bq3285E/L



Intel Bus Write Timing—bq3285E/L

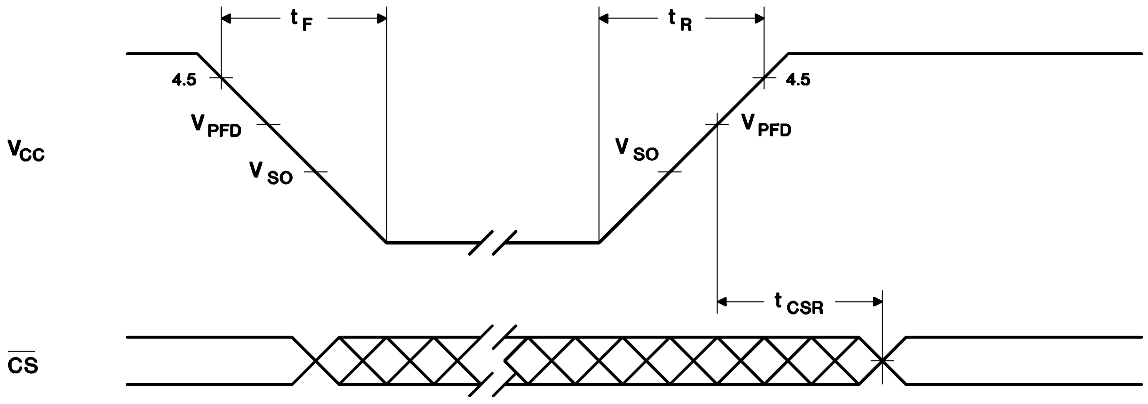


Power-Down/Power-Up Timing—bq3285E ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 4.5V to 0V	300	-	-	µs	
t_R	V_{CC} slew from 0V to 4.5V	100	-	-	µs	
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	20	-	200	ms	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

Power-Down/Power-Up Timing—bq3285E



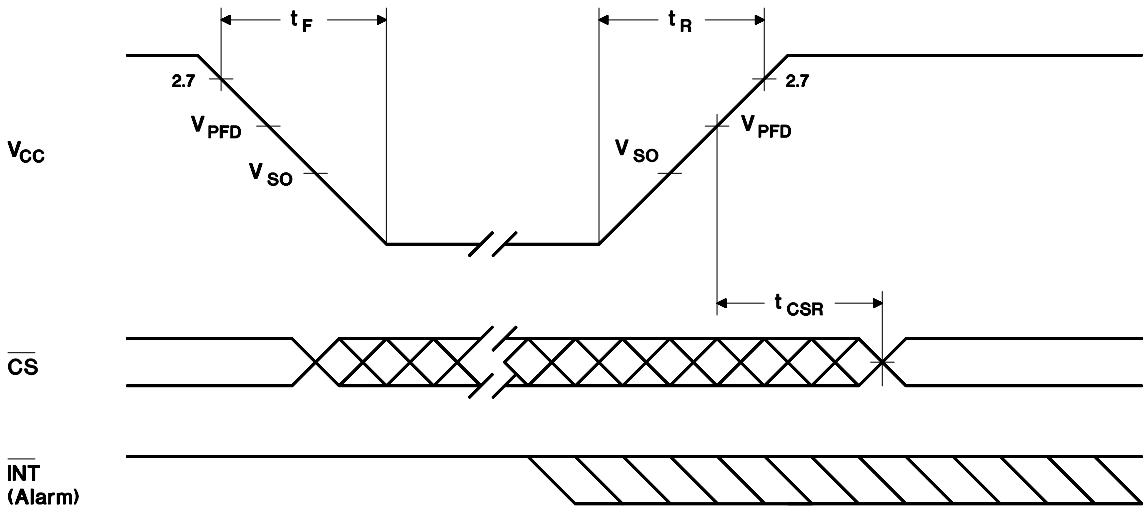
PD-4A

Power-Down/Power-Up Timing—bq3285L ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 2.7V to 0V	300	-	-	µs	
t_R	V_{CC} slew from 0V to 2.7V	100	-	-	µs	
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	20	-	200	ms	Internal write-protection period after V_{CC} passes V_{PFD} on power-up.

Caution: Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.

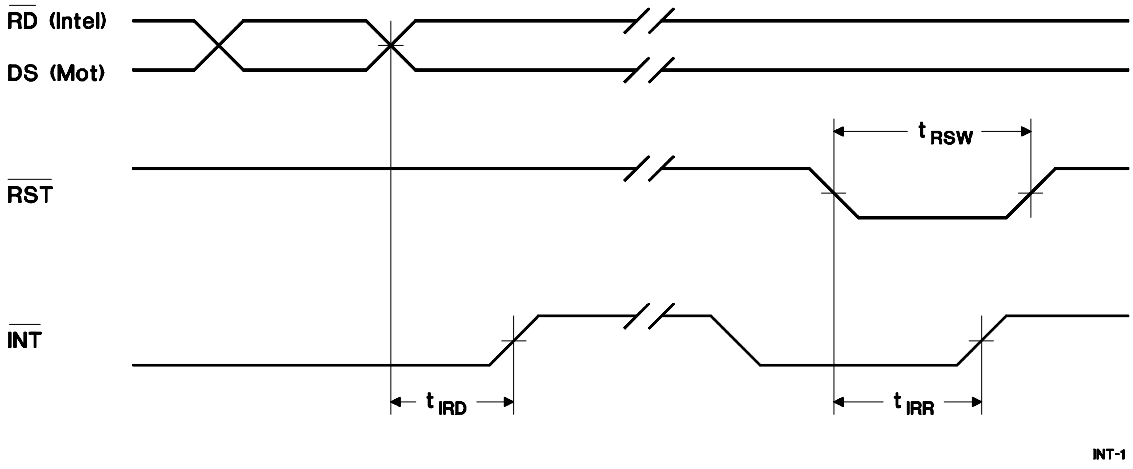
Power-Down/Power-Up Timing—bq3285L



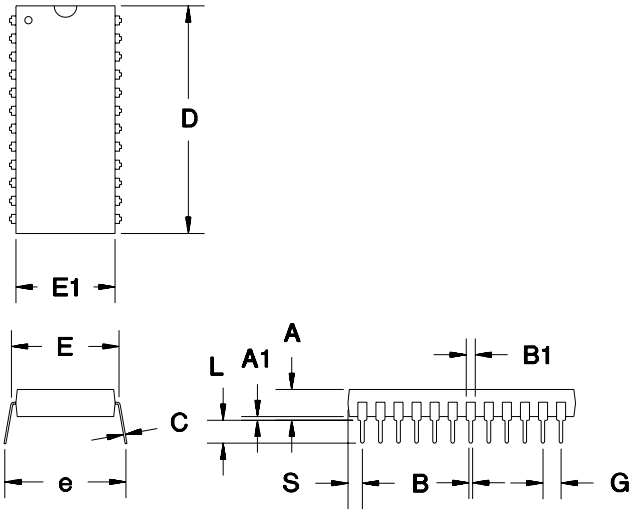
Interrupt Delay Timing—bq3285E/L ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{RSW}	Reset pulse width	5	-	-	µs
t_{IRR}	$\overline{INT}$ release from $\overline{RST}$	-	-	2	µs
t_{IRD}	$\overline{INT}$ release from DS	-	-	2	µs

Interrupt Delay Timing—bq3285E/L



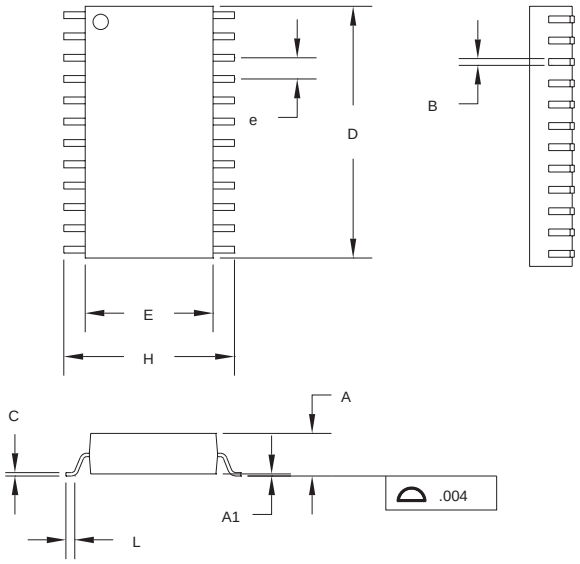
24-Pin DIP (P)



24-Pin DIP (0.600" DIP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.190	4.06	4.83
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.013	0.20	0.33
D	1.240	1.280	31.50	32.51
E	0.600	0.625	15.24	15.88
E1	0.530	0.570	13.46	14.48
e	0.600	0.670	15.24	17.02
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.070	0.090	1.78	2.29

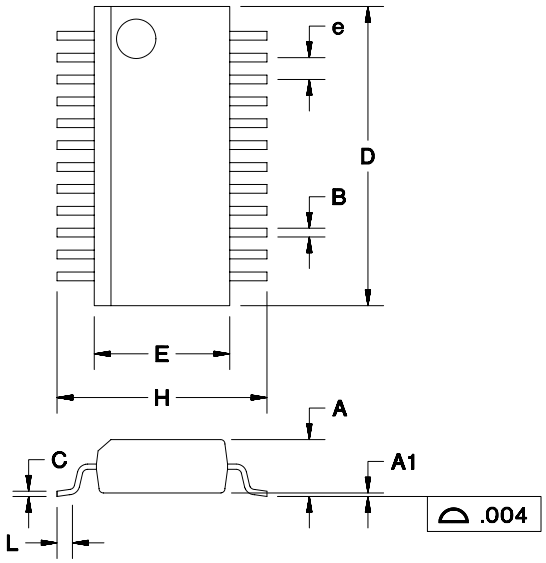
24-Pin SOIC (S)



24-Pin S (0.300" SOIC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.095	0.105	2.41	2.67
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.008	0.013	0.20	0.33
D	0.600	0.615	15.24	15.62
E	0.290	0.305	7.37	7.75
e	0.045	0.055	1.14	1.40
H	0.395	0.415	10.03	10.54
L	0.020	0.040	0.51	1.02

24-Pin SSOP (SS)



24-Pin SS (0.150" SSOP)

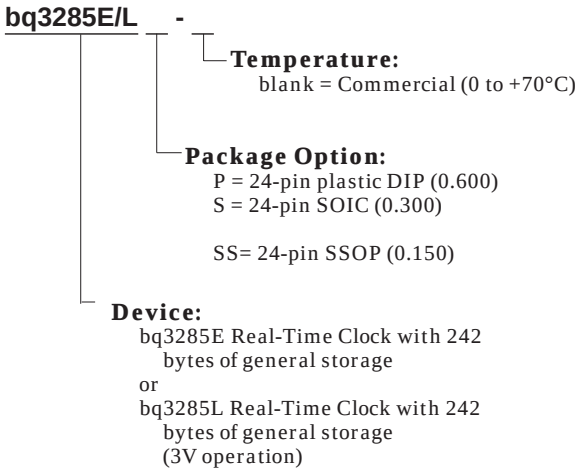
Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.061	0.068	1.55	1.73
A1	0.004	0.010	0.10	0.25
B	0.008	0.012	0.20	0.30
C	0.007	0.010	0.18	0.25
D	0.337	0.344	8.56	8.74
E	0.150	0.157	3.81	3.99
e	.025 BSC		0.64 BSC	
H	0.230	0.244	5.84	6.20
L	0.016	0.035	0.41	0.89

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	8	Register C, bit 2	Was 0; is na (not affected)
1	18	Output data delay time t_{OD}	Was 80 ns max; is 100 ns max
2	1, 24, 26	Package option change	Lst time buy for some package options.
3	1, 24, 26	Package option change	Removed PLCC and added industrial SSOP package options
4	1, 11	Package option change	Industrial package option removed

Note: Change 1 = Jan. 1995 B “Final” changes from Dec. 1993 A “Preliminary”.
Change 2 = Jan. 1999 C changes from Jan. 1995 B
Change 3 = Apr. 1999 D changes from Jan. 1999 C.
Change 4 = May 2004 (SLUS004A) changes from Apr. 1999 D

Ordering Information



bq3285L only available in 24-pin SSOP (0.150).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ3285ES	NRND	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	3285ES -B2	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

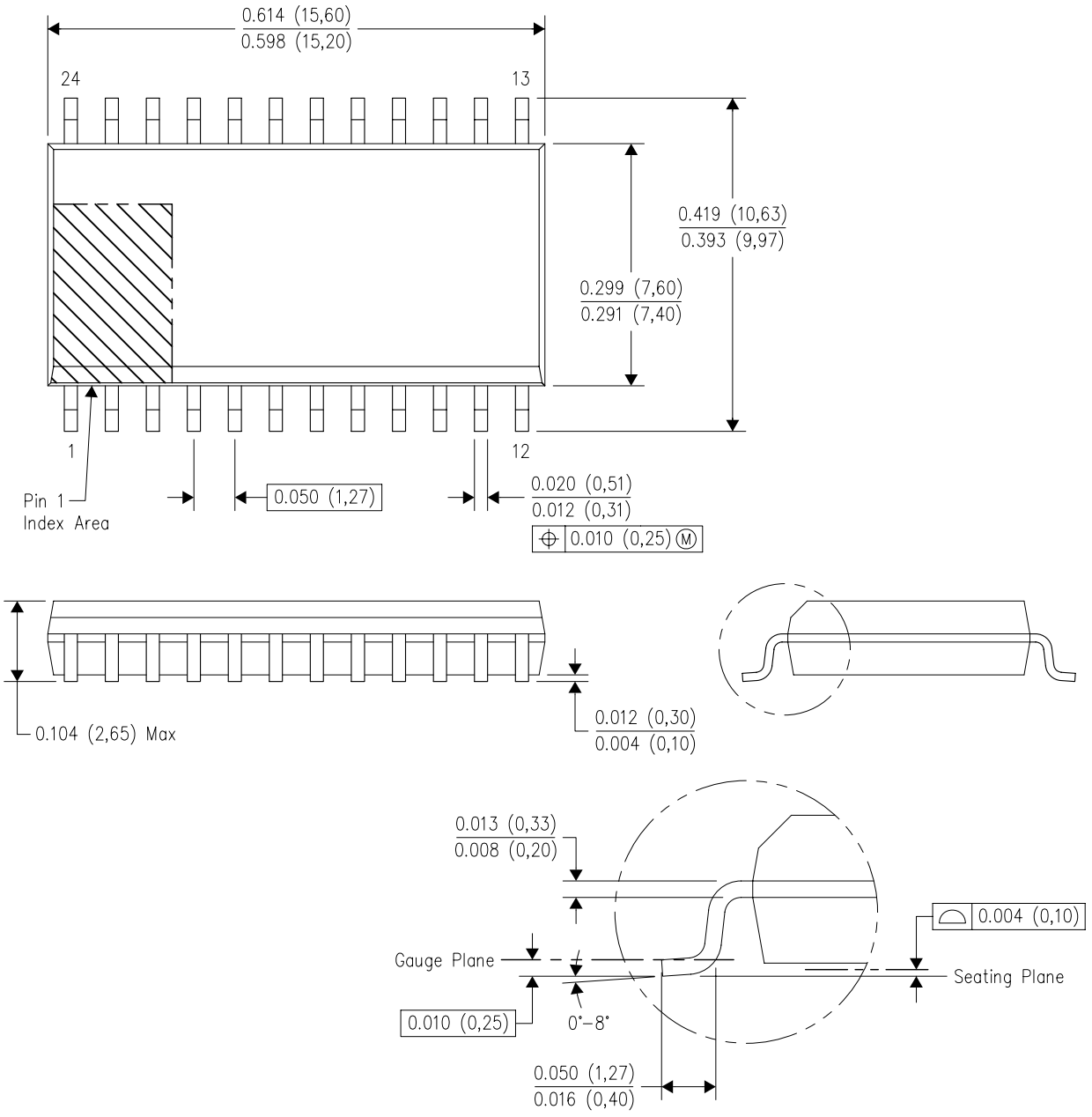
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

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