bq5105xB High-Efficiency Qi v1.2-Compliant Wireless Power Receiver and Battery Charger

1 Features

- Single-Stage Wireless Power Receiver and Li-Ion/Li-Pol Battery Charger
  - Combines Wireless Power Receiver, Rectifier, and Battery Charger in a Single, Small Package
  - 4.20-V, 4.35-V, and 4.40-V Output Voltage Options
  - Supports a Charging Current up to 1.5 A
  - 93% Peak AC-DC Charging Efficiency
- Robust Architecture
  - 20-V Maximum Input Voltage Tolerance, With Input Overvoltage Protection
  - Thermal Shutdown and Overcurrent Protection
  - Temperature Monitoring and Fault Detection
- Compatible With WPC v1.2 Qi Industry Standard
- Power Stage Output Tracks Rectifier and Battery Voltage to Ensure Maximum Efficiency Across the Full Charge Cycle
- Available in Small DSGBA and VQFN Packages

2 Applications

- Battery Packs
- Cell Phones and Smart Phones
- Headsets
- Portable Media Players
- Other Handheld Devices

3 Description

The bq5105x device is a high-efficiency, Qi-compliant wireless power receiver with an integrated Li-Ion/Li-Pol battery charge controller for portable applications. The bq5105xB devices provide efficient AC-DC power conversion, integrates the digital controller required to comply with Qi v1.2 communication protocol, and provides all necessary control algorithms needed for efficient and safe Li-Ion and Li-Pol battery charging. Together with the bq500212A transmitter-side controller, the bq5105x enables a complete wireless power transfer system for direct battery charger solutions. By using near-field inductive power transfer, the receiver coil embedded in the portable device can pick up the power transmitted by transmitter coil. The AC signal from the receiver coil is then rectified and conditioned to apply power directly to the battery. Global feedback is established from the receiver to the transmitter to stabilize the power transfer process. This feedback is established by using the Qi v1.2 communication protocol.

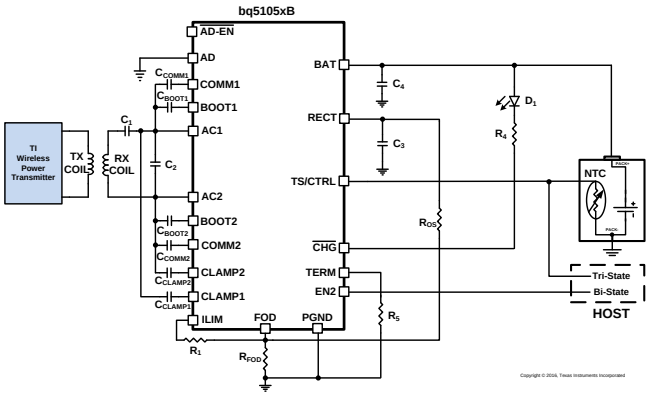
The bq5105xB devices integrate a low-impedance synchronous rectifier, low-dropout regulator (LDO), digital control, charger controller, and accurate voltage and current loops in a single package. The entire power stage (rectifier and LDO) use low-resistance N-MOSFETs (100-mΩ typical Rdson) to ensure high efficiency and low power dissipation.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq51050B bq51051B bq51052B	VQFN (20)	4.50 mm × 3.50 mm
	DSBGA (28)	3.00 mm × 1.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (March 2015) to Revision F — **Page**

- Changed all Qi v1.1 and WPC v1.1 To: Qi v1.2 and WPC v1.2 throughout the document ... 1
- Added the *Adaptive Communication Limit* section ... 24
- Deleted R_1 = 29.402 kΩ R_3 = 14.302 kΩ and added a link to SLUS629 in the *Internal Temperature Sense (TS Function of the TS/CTRL Pin)* section ... 25

Changes from Revision D (January 2014) to Revision E — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added the bq51052B 4.40-V option ... 1
- Updated pinout images ... 4
- Added thermal pad description in *Pin Functions* table ... 4
- Added AD voltage to *Recommended Operating Conditions* ... 6
- Changed RECT overvoltage specification name from V_{RECT} to V_{OVP} ... 7
- Changed to $I_{LIM_SHORT,\ OK}$ from I_{LIM_SC} for clarity ... 7
- Added V_{OREG} for bq51052B ... 8
- Added minimum current for K_{ILIM} ... 8
- Changed K_{ILIM} TYP value from 300 to 314 (min / max also changed) ... 8
- Added I_{BULK} spec for charging minimum and maximum ... 8
- Added V_{RECH} for bq51052B ... 8
- Added new spec $I_{Termination}$ ... 8
- Changed to VTSB from VTS for clarity ... 8
- Changed from $I_{TS\text{-}Bias}$ for clarity ... 8
- Deleted $V_{0C\text{-}F}$ as redundant ... 8
- Changed typical JEITA regulation on bq51050B from 4.10 V to 4.06 V ... 8

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- Changed to clarify CTRL pin high and low levels ... 8
- Changed Thermal shutdown name to T_{J-SD} for clarity ... 9
- Added section to describe Adapter Enable function ... 9
- Changed Synchronous rectifer switchover name to I_{BAT-SR} for clarity ... 9
- Added synchronous mode entry for bq51052B ... 9
- Deleted note regarding internal junction monitor reducing current - it is not applicable. ... 19
- Added section on modified JEITA profile for bq51052B ... 21
- Changed TS/CTRL function to correct Termination Packet value ... 22
- Added Taper mode completion for Termination Packet ... 22
- Changed Beta value from 4500 to 3380 to match NTC datasheet ... 25
- Changed received power maximum error from 250 mW to 375 mW to comply with latest WPC v1.2 specification ... 27

Changes from Revision C (February 2013) to Revision D **Page**

- Changed the ABSOLUTE MAXIMUM RATINGS - moved AC1 and AC2 onto a single row with a Min value of –0.8 ... 6
- Added section: Details of a Qi Wireless Power System and bq5105xB Power Transfer Flow Diagrams ... 15
- Changed text in the Battery Charge Profile section ... 19
- Changed Battery failure Conditions in Table 1 ... 22
- Changed Equation 3 and Equation 4 ... 25
- Changed R_2 = 7.81 kΩ To: R_1 = 29.402 kΩ ... 25
- Changed R_3 = 13.98 kΩ To: R_3 = 14.302 kΩ in the *Internal Temperature Sense (TS Function of the TS/CTRL Pin)* section ... 25
- Changed T_{HOT} = 0°C To: T_{HOT} = 60°C ... 25
- Changed Equation 6 ... 29

Changes from Revision B (September 2012) to Revision C **Page**

- First release of the full data sheet ... 1

Changes from Revision A (August 2012) to Revision B **Page**

- Changed last features bullet from: 1.9 x 3.0mm WCSP and 4.5 x 3.5mm QFN Package Options to: Available in small WCSP and QFN packages ... 1
- Changed Figure 1 and changed caption from: Wireless Power Consortium (WPC or Qi) Inductive Power Charging System, to: Typical System blocks shows bq5105xB used as a Wireless Power Li-Ion/Li-Pol Battery Charger ... 1
- Added note: Visit ti.com/wirelesspower for product details and design resources ... 1

Changes from Original (August 2012) to Revision A **Page**

- Changed Regulated BAT(output) voltage ... 8
- Changed Recharge threshold for bq51052B ... 8
- Deleted $I_{TS-Bias-Max}$ ... 8
- Changed V_{COLD} to V_{OC} and values ... 8
- Changed V_{45C} values ... 8
- Changed V_{60C} values ... 8
- Changed Figure 25 ... 21
- Changed Figure 25 ... 22

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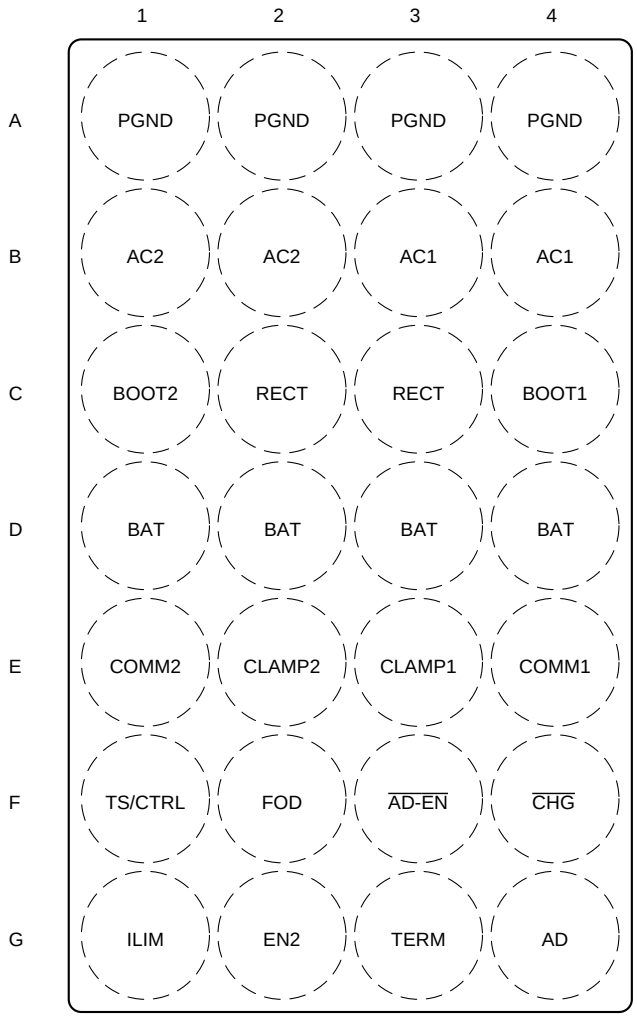
5 Device Options

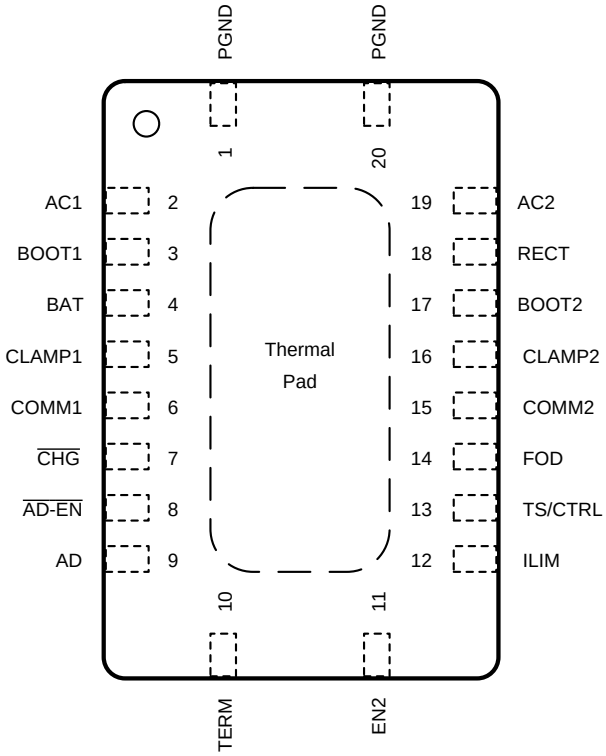
DEVICE	FUNCTION	$V_{RECT-OVP}$	$V_{RECT-REG}$	$V_{BAT-REG}$	NTC MONITORING
bq51050B	4.20-V Li-Ion Wireless Battery Charger	15 V	Track	4.20 V	JEITA
bq51051B	4.35-V Li-Ion Wireless Battery Charger	15 V	Track	4.35 V	JEITA
bq51052B	4.40-V Li-Ion Wireless Battery Charger	15 V	Track	4.40 V	Modified JEITA

6 Pin Configuration and Functions

YFP Package
28-Pin DSBGA
Top View



RHL Package
20-Pin VQFN With Exposed Thermal Pad
Top View



The exposed thermal pad should be connected to ground.

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Pin Functions

Pin			I/O	DESCRIPTION
NAME	DSBGA	VQFN		
AC1	B3, B4	2	I	Input power from receiver coil.
AC2	B1, B2	19	I	Input power from receiver coil.
AD	G4	9	I	If AD functionality is used, connect this pin to the wired adapter input. When $V_{AD\text{-}Pres}$ is applied to this pin wireless charging is disabled and AD_ENn is driven low. Connect a 1-µF capacitor from AD to PGND. If unused, the capacitor is not required and AD should be connected directly to PGND.
$\overline{\text{AD-EN}}$	F3	8	O	Push-pull driver for external PFET when wired charging is active. Float if not used.
BAT	D1	4	O	Output pin, delivers power to the battery while applying the internal charger profile.
	D2			
	D3			
	D4			
BOOT1	C4	3	O	Bootstrap capacitors for driving the high-side FETs of the synchronous rectifier. Connect a 10-nF ceramic capacitor from BOOT1 to AC1 and from BOOT2 to AC2.
BOOT2	C1	17	O	
$\overline{\text{CHG}}$	F4	7	O	Open-drain output – active when BAT is enabled. Float if not used.
CLAMP1	E3	5	O	Open-drain FETs which are used for a non-power dissipative overvoltage AC clamp protection. When the RECT voltage goes above 15 V, both switches will be turned on and the capacitors will act as a low impedance to protect the device from damage. If used, capacitors are used to connect CLAMP1 to AC1 and CLAMP2 to AC2. Recommended connections are 0.47-µF capacitors.
CLAMP2	E2	16	O	
COMM1	E4	6	O	Open-drain outputs used to communicate with primary by varying reflected impedance. Connect a capacitor from COMM1 to AC1 and a capacitor from COMM2 to AC2 for capacitive load modulation. For resistive modulation connect COMM1 and COMM2 to RECT through a single resistor. See *Communication Modulator* for more information.
COMM2	E1	15	O	
EN2	G2	11	I	Used to set priority between wireless power and wired power. EN2 low enables wired charging source if AD input voltage is present. EN2 high disables wired charging source and wireless power is enabled if present.
FOD	F2	14	I	Input for the rectified power measurement. See *WPC v1.2 Compatibility* for details.
ILIM	G1	12	I/O	Programming pin for the battery charge current. The total resistance from ILIM to PGND (R_{ILIM}) sets the charge current. Figure 32 shows R_{ILIM} to be $R_1 + R_{FOD}$. Details can be found in *Electrical Characteristics* and *Battery Charge Current Setting Calculations*.
PGND	A1	1, 20	–	Power ground
	A2			
	A3			
	A4			
RECT	C2, C3	18	O	Filter capacitor for the internal synchronous rectifier. Connect a ceramic capacitor to PGND. Depending on the power levels, the value may be from 4.7 µF to 22 µF.
TERM	G3	10	I	Input that is used to set the termination threshold. Termination current is the battery current level below which the charge process will cease. The termination current is set as a percentage of the charge current. See *Battery Charge Current Setting Calculations* for more details.
TS/CTRL	F1	13	I	Temperature Sense (TS) and Control (CTRL) pin functionality. For the TS functionality connect TS/CTRL to ground through a Negative Temperature Coefficient (NTC) resistor. If an NTC function is not desired, connect to PGND with a 10-kΩ resistor. As a CTRL pin pull low to send end power transfer (EPT) fault to the transmitter or pull up to an internal rail to send EPT termination to the transmitter. See *Internal Temperature Sense (TS Function of the TS/CTRL Pin)* for more details.
—	—	PAD	—	The exposed thermal pad should be connected to ground (PGND).

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7 Specifications

7.1 Absolute Maximum Ratings(1)(2)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	RECT, COMM1, COMM2, BAT, $\overline{CHG}$, CLAMP1, CLAMP2	–0.3	20	V
	AC1, AC2	–0.8	20	V
	AD, $\overline{AD\text{-}EN}$	–0.3	30	V
	BOOT1, BOOT2	–0.3	26	V
	EN2, TERM, FOD, TS/CTRL, ILIM	–0.3	7	V
Input current	AC1, AC2		2	A(RMS)
Output current	BAT		1.5	A
Output sink current	$\overline{CHG}$		15	mA
	COMM1, COMM2		1.0	A
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the VSS terminal, unless otherwise noted.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V_{IN}	Input voltage range	RECT		4	10	V
I_{IN}	Input current	Internal Rectifier (voltage monitored at RECT node)			1.5	A
I_{BAT}	BAT(output) current	BAT	bq51050B, bq51051B		1.5	A
			bq51052B		0.8	
V_{AD}	Adapter voltage	AD			15	V
$I_{AD\text{-}EN}$	Sink current	$\overline{AD\text{-}EN}$			1	mA
I_{COMM}	COMM sink current	COMM			500	mA
T_J	Junction temperature			0	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		bq51050B, bq51051B, bq51052B		UNIT
		YFP (DSGBA)	RHL (VQFN)	
		28 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.9	37.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.2	35.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.1	13.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.9	13.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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Thermal Information (continued)

THERMAL METRIC(1)		bq51050B, bq51051B, bq51052B		UNIT
		YFP (DSGBA)	RHL (VQFN)	
		28 PINS	20 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	2.7	°C/W

7.5 Electrical Characteristics

Over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{UVLO}	Undervoltage lockout	V_{RECT}: 0 V → 3 V		2.6	2.7	2.8	V
$V_{HYS-UVLO}$	Hysteresis on UVLO	V_{RECT}: 3 V → 2 V			250		mV
V_{OVP}	Input overvoltage threshold	V_{RECT}: 5 V → 16 V		14.5	15	15.5	V
$V_{HYS-OVP}$	Hysteresis on OVP	V_{RECT}: 16 V → 5 V			150		mV
$V_{RECT-REG}$(1)	V_{RECT} regulation voltage				5.11		V
I_{LOAD}	I_{LOAD} Hysteresis for dynamic V_{RECT} thresholds as a % of I_{ILIM}	I_{LOAD} falling			5%		
V_{TRACK}	Tracking V_{RECT} regulation above V_{BAT}	V_{BAT} = 3.5 V, I_{BAT} ≥ 500 mA			300		mV
$V_{RECT-REV}$	Rectifier reverse voltage protection at the BAT(output)	$V_{RECT-REV} = V_{BAT} - V_{RECT}$, V_{BAT} = 10 V			8.3	9	V
$V_{RECT-DPM}$	Rectifier undervoltage protection, restricts I_{BAT} at $V_{RECT-DPM}$			3	3.1	3.2	V
QUIESCENT CURRENT							
I_{RECT}	Active chip quiescent current consumption from RECT (when wireless power is present)	I_{BAT} = 0 mA, 0°C ≤ T_J ≤ 85°C			8	10	mA
		I_{BAT} = 300 mA, 0°C ≤ T_J ≤ 85°C			2	3	mA
I_Q	Quiescent current at the BAT when wireless power is disabled (Standby)	V_{BAT} = 4.2 V, 0°C ≤ T_J ≤ 85°C			12	20	µA
ILIM SHORT PROTECTION							
$R_{ILIM-SHORT}$	Highest value of ILIM resistor considered a fault (short). Monitored for I_{BAT} > $I_{LIM_SHORT,\ OK}$	R_{ILIM}: 200 Ω → 50 Ω. I_{BAT} latches off, cycle power to reset	bq51050B, bq51051B			120	Ω
			bq51052B			235	
$t_{DGL-Short}$	Deglitch time transition from ILIM short to I_{BAT} disable				1		ms
$I_{LIM_SHORT,\ OK}$	$I_{LIM-SHORT,OK}$ enables the I_{ILIM} short comparator when I_{BAT} is greater than this value	I_{BAT}: 0 mA → 200 mA	bq51050B, bq51051B	110	145	165	mA
			bq51052B	55	75	95	
$I_{LIM-SHORT,\ OK\ HYSTERESIS}$	Hysteresis for $I_{LIM-SHORT,OK}$ comparator	I_{BAT}: 200 mA → 0 mA			30		mA
I_{BAT-CL}	Maximum output current limit	Maximum I_{BAT} that will be delivered for up to 1 ms when ILIM is shorted to PGND				2.4	A
BATTERY SHORT PROTECTION							
$V_{BAT(SC)}$	BAT pin short-circuit detection/precharge threshold	V_{BAT}: 3 V → 0.5 V, no deglitch		0.75	0.8	0.85	V
$V_{BAT(SC)-HYS}$	$V_{BAT(SC)}$ hysteresis	V_{BAT}: 0.5 V → 3 V			100		mV
$I_{BAT(SC)}$	Source current to BAT pin during short-circuit detection	V_{BAT} = 0 V	bq51050B, bq51051B	12	18	22	mA
			bq51052B	12	18	25	
VOLTAGE REGULATION PHASE							
$I_{EndTrack}$	I_{BAT} threshold during Voltge Regulation Phase that changes V_{RECT} level from V_{BAT}+V_{TRACK} to $V_{RECT-REG}$	I_{BAT} decreasing	bq51050B, bq51051B		0.35 * I_{BULK}		mA
			bq51052B		0.05 * I_{BULK}		

(1) $V_{RECT-REG}$ is overridden when rectifier foldback mode is active ($V_{RECT-REG}$-V_{TRACK}).

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Electrical Characteristics (continued)

Over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
PRECHARGE							
V_{LOWV}	Precharge to fast charge transition threshold	V_{BAT}: 2 V → 4 V		2.9	3.0	3.1	V
K_{PRECHG}	Precharge current as a percentage of the programmed charge current setting (I_{BULK})	$V_{LOWV} > V_{BAT} > V_{BAT(SC)}$ I_{BAT}: 50 mA – 300 mA		18%	20%	23%	V
I_{PRECHG}	I_{BAT} during precharge	$V_{LOWV} > V_{BAT} > V_{BAT(SC)}$, I_{BULK} = 500 mA			100		mA
$t_{precharge}$	Precharge time-out	$V_{BAT(SC)} < V_{BAT} < V_{LOWV}$			30		min
$t_{DGL1(LOWV)}$	Deglitch time, pre- to fast-charge				25		ms
$t_{DGL2(LOWV)}$	Deglitch time, fast- to precharge				25		ms
OUTPUT							
V_{OREG}	Regulated BAT(output) voltage	I_{BAT} = 1000 mA	bq51050B	4.16	4.20	4.22	V
			bq51051B	4.30	4.35	4.37	
			bq51052B	4.36	4.40	4.44	
V_{DO}	Drop-out voltage, RECT to BAT	I_{BAT} = 1 A			110	190	mV
K_{ILIM}	Current programming factor	$R_{LIM} = K_{ILIM} / I_{IBULK}$ (500 mA - 1.5 A)	bq51050B, bq51051B	303	314	321	AΩ
		$R_{LIM} = K_{ILIM} / I_{IBULK}$ (500 mA - 1.0 A)	bq51052B				
I_{BULK}	Battery charging current limits	K_{ILIM} 303 to 321	bq51050B, bq51051B	500		1,500	mA
			bq51052B	500		1,000	
$t_{fast-charge}$	Fast-charge timer	$V_{LOWV} < V_{BAT} < V_{BAT-REG}$			10		hours
I_{BAT-R}	Battery charge current limit programming range					1500	mA
$I_{COMM-CL}$	Current limit during communication			330	390	420	mA
TERMINATION							
K_{TERM}	Programmable termination current as a percentage of I_{IBULK}	R_{TERM} = %I_{IBULK} x K_{TERM} (I_{BULK} = 500 mA)		200	240	280	Ω/%
$I_{TERM-Th}$	Termination current from BAT, defined with K_{TERM}, as the current that terminates the charge cycle	I_{BAT} decreasing, R_{TERM} = 2.4k Ω, I_{BULK} = 1000 mA			100		mA
I_{TERM}	Constant current at the TERM pin to bias the termination reference			40	50	55	µA
V_{RECH}	Recharge threshold	bq51050B		$V_{BAT-REG}$ –135mV	$V_{BAT-REG}$ –110mV	$V_{BAT-REG}$ –90mV	V
		bq51051B		$V_{BAT-REG}$ –125mV	$V_{BAT-REG}$ –95mV	$V_{BAT-REG}$ –70mV	
		bq51052B		$V_{BAT-REG}$ –125mV	$V_{BAT-REG}$ –95mV	$V_{BAT-REG}$ –70mV	
$I_{Termination}$	Termination current setting limits			120			mA
TS / CTRL FUNCTIONALITY							
V_{TSB}	Internal TS bias voltage (V_{TS} is the voltage at the TS/CTRL pin, V_{TSB} is the internal bias voltage)	I_{TSB}< 100 µA (periodically driven see $t_{TS/CTRL-Meas}$)		2	2.2	2.4	V
V_{0C-R}	Rising threshold	V_{TS}: 50% → 60%		57	58.7	60	%V_{TSB}
$V_{0C-Hyst}$	Hysteresis on 0°C Comparator	V_{TS}: 60% → 50%			2.4		%V_{TSB}
V_{10C}	Rising threshold	V_{TS}: 40% → 50%		46	47.8	49	%V_{TSB}
$V_{10C-Hyst}$	Hysteresis on 10°C Comparator	V_{TS}: 50% → 40%			2		%V_{TSB}
V_{45C}	Falling threshold	V_{TS}: 25% → 15%		18	19.6	21	%V_{TSB}
$V_{45C-Hyst}$	Hysteresis on 45°C Comparator	V_{TS}: 15% → 25%			3		%V_{TSB}
V_{60C}	Falling threshold	V_{TS}: 20% → 5%		12	13.1	14	%V_{TSB}
$V_{60C-Hyst}$	Hysteresis on 60°C Comparator	V_{TS}: 5% → 20%			1		%V_{TSB}
I_{45C}	I_{BULK} reduction percentage at 45°C (in full JEITA mode - N/A for bq51052B)	V_{TS}: 25% → 15%, I_{BAT} = I_{BULK}		45%	50%	55%	
V_{O-J}	Voltage regulation during JEITA temperature range	bq51050B			4.06		V
		bq51051B			4.2		
		bq51052B			4.2		
$V_{CTRL-HI}$	Voltage on CTRL pin for a high			0.2		5	V

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Electrical Characteristics (continued)

Over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{CTRL-LOW}$	Voltage on CTRL pin for a low			0		0.1	V
$t_{TS/CTRL-Meas}$	Time period of TS/CTRL measurements (when V_{TSB} is being driven internally)	TS bias voltage is only driven when communication packets are sent			24		ms
$t_{TS-Deglitch}$	Deglitch time for all TS comparators				10		ms
NTC-Pullup	Pullup resistor for the NTC network. Pulled up to the TS bias LDO.			18	20	22	kΩ
NTC-R_{NOM}	Nominal resistance requirement at 25°C of the NTC resistor				10		kΩ
NTC-Beta	Beta requirement for accurate temperature sensing through the above specified thresholds				3380		Ω
THERMAL PROTECTION							
T_{J-SD}	Thermal shutdown temperature				155		°C
T_{J-Hys}	Thermal shutdown hysteresis				20		°C
OUTPUT LOGIC LEVELS ON $\overline{CHG}$							
V_{OL}	Open-drain $\overline{CHG}$ pin	I_{SINK} = 5 mA				500	mV
$I_{OFF,CHG}$	$\overline{CHG}$ leakage current when disabled	V_{CHG} = 20 V, 0°C ≤ T_J ≤ 85°C				1	µA
COMM PIN							
$R_{DS-ON(COMM)}$	COMM1 and COMM2	V_{RECT} = 2.6 V			1		Ω
f_{COMM}	Signaling frequency on COMM pin				2		kb/s
$I_{OFF,COMM}$	COMM pin leakage current	V_{COMM1} = 20 V, V_{COMM2} = 20 V				1	µA
CLAMP PIN							
$R_{DS-ON(CLAMP)}$	CLAMP1 and CLAMP2				0.75		Ω
ADAPTER ENABLE							
$V_{AD-Pres}$	V_{AD} Rising threshold voltage. EN-UVLO	V_{AD} 0 V → 5 V		3.5	3.6	3.8	V
$V_{AD-PresH}$	$V_{AD-Pres}$ hysteresis, EN-HYS	V_{AD} 5 V → 0 V			400		mV
I_{AD}	Input leakage current	V_{RECT} = 0 V, V_{AD} = 5 V				60	µA
R_{AD}	Pullup resistance from $\overline{AD-EN}$ to BAT when adapter mode is disabled and VBAT > VAD, EN-OUT	V_{AD} = 0 V, V_{BAT} = 5 V			200	350	Ω
$V_{AD-Diff}$	Voltage difference between V_{AD} and V_{AD-EN} when adapter mode is enabled, EN-ON	V_{AD} = 5 V, 0°C ≤ T_J ≤ 85°C		3	4.5	5	V
SYNCHRONOUS RECTIFIER							
I_{BAT-SR}	I_{BAT} at which the synchronous rectifier enters half synchronous mode, SYNC_EN	I_{BAT} 200 mA → 0 mA	bq51050B, bq51051B	80	115	140	mA
			bq51052B	20	50	65	
$I_{BAT-SRH}$	Hysteresis for $I_{BAT,SR}$ (full-synchronous mode enabled)	I_{BAT} 0 mA → 200 mA	bq51050B, bq51051B		25		
			bq51052B		28		
$V_{HS-DIODE}$	High-side diode drop when the rectifier is in half synchronous mode	$I_{AC-VRECT}$ = 250 mA, and T_J = 25°C			0.7		V
EN2							
V_{IL}	Input low threshold for EN2					0.4	V
V_{IH}	Input high threshold for EN2			1.3			V
$R_{PD, EN}$	EN2 pulldown resistance				200		kΩ
ADC							
$P_{owerREC}$	Received power measurement	0 W – 5 W received power after calibration of Rx magnetics losses			0.25		W

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7.6 Typical Characteristics

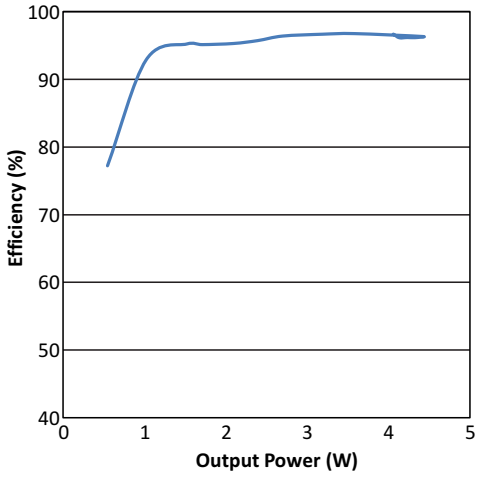

Figure 1. Rectifier Efficiency

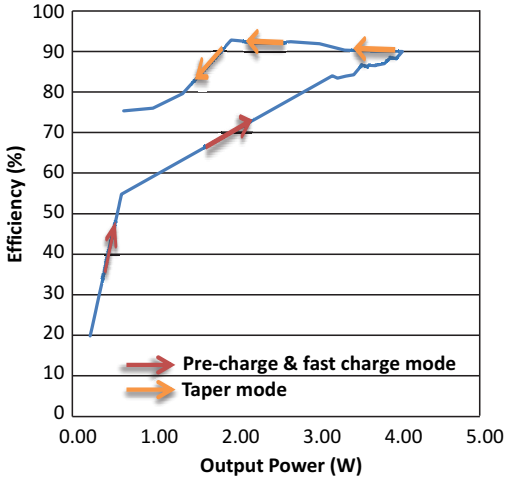

Figure 2. IC Efficiency (AC Input to DC Output)

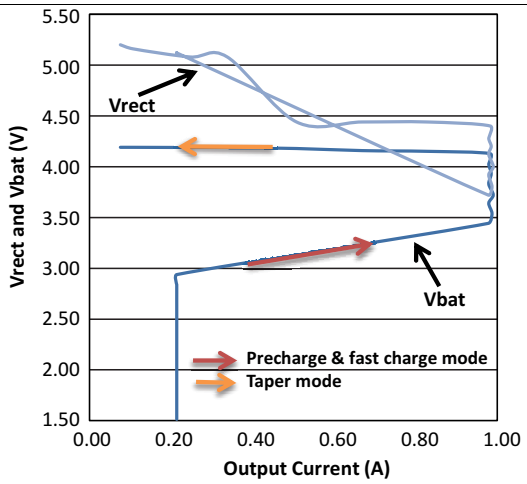

Figure 3. V_{RECT}, V_{BAT} versus Output Current

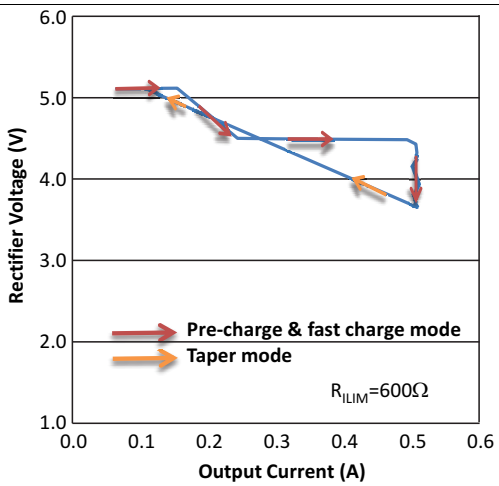

Figure 4. V_{RECT} versus Output Current at R_{ILIM}=600 Ω (I_{LIM} = 523 mA)

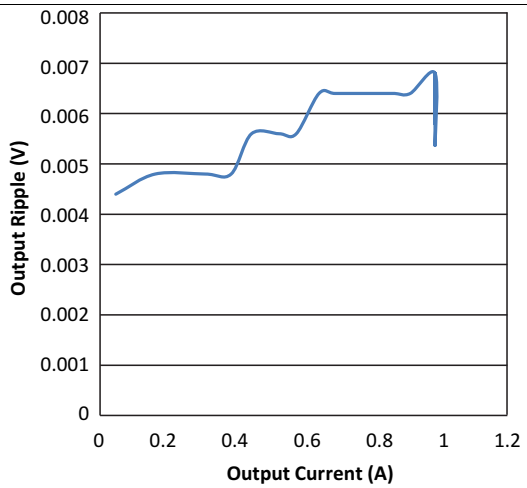

Figure 5. Output Ripple versus Output Current

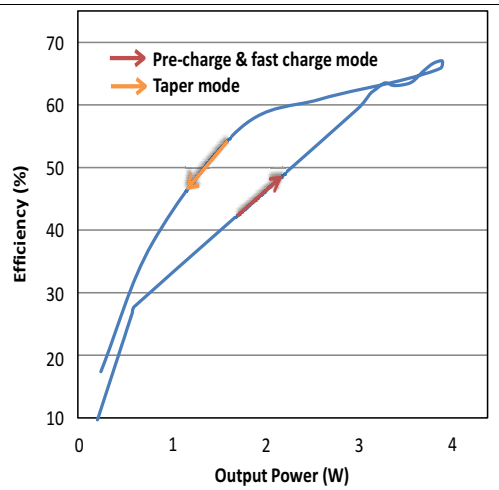

Figure 6. System Efficiency (DC Input to DC Output)

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Typical Characteristics (continued)

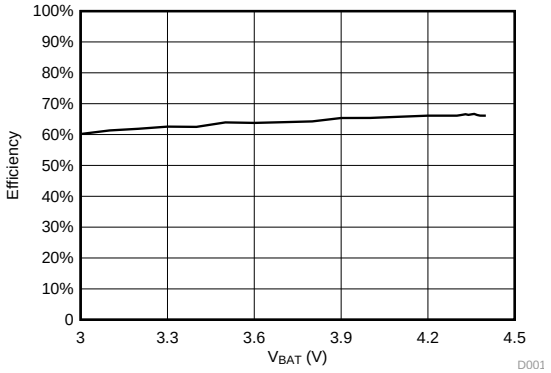

Figure 7. bq51052B 300-mA Fast Charge Efficiency (DC Input to DC Output)

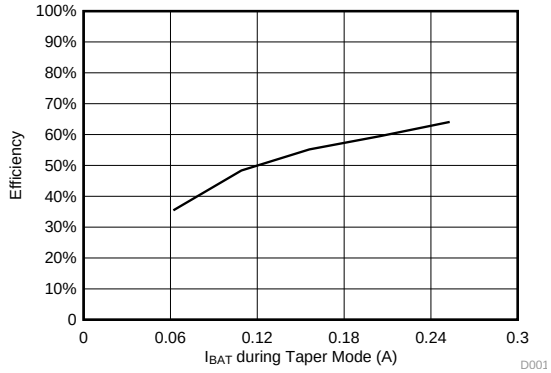

Figure 8. bq51052B 300-mA Taper Charge Efficiency (DC Input to DC Output)

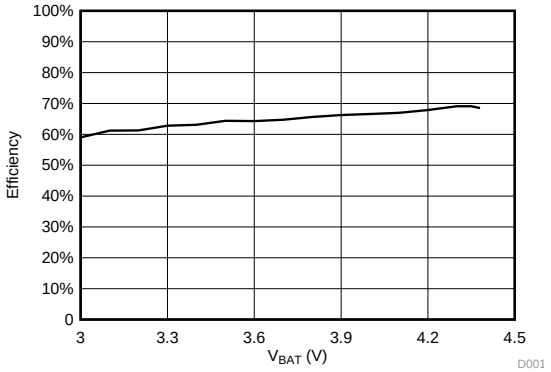

Figure 9. bq51052B 800-mA Fast Charge Efficiency (DC Input to DC Output)

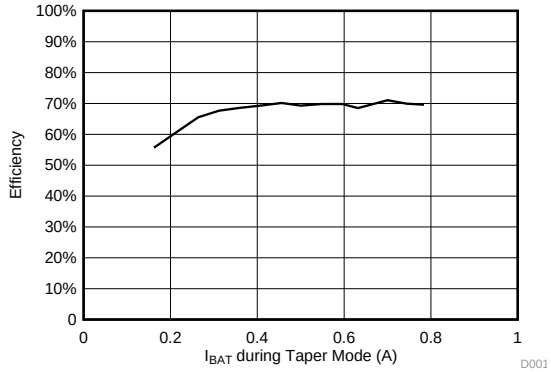

Figure 10. bq51052B 800-mA Taper Charge Efficiency (DC Input to DC Output)

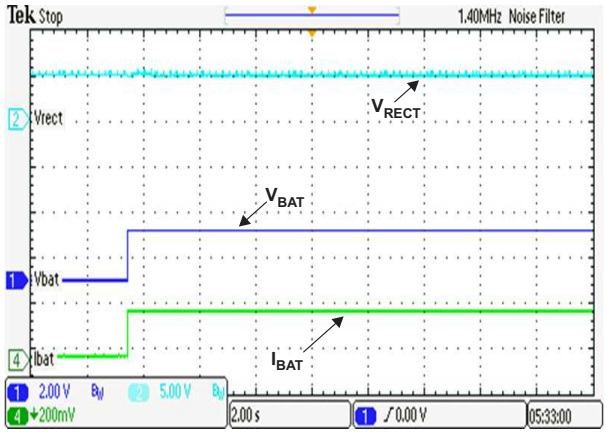

Figure 11. Battery Insertion in Precharge Mode

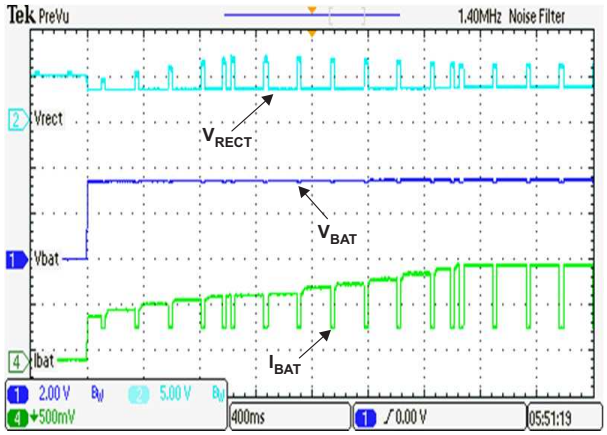

Figure 12. Battery Insertion in Fast-Charge Mode

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Typical Characteristics (continued)

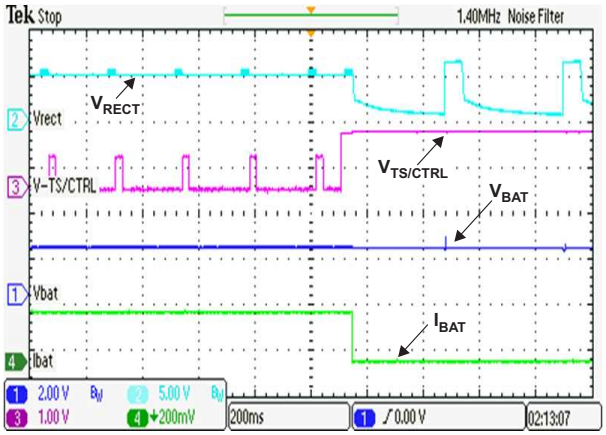

Figure 13. TS Fault

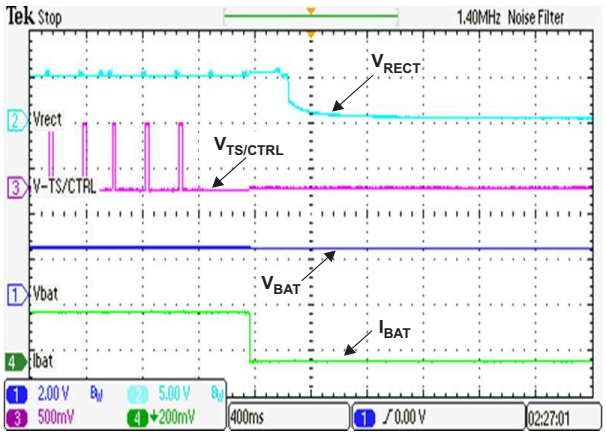

Figure 14. TS Ground Fault

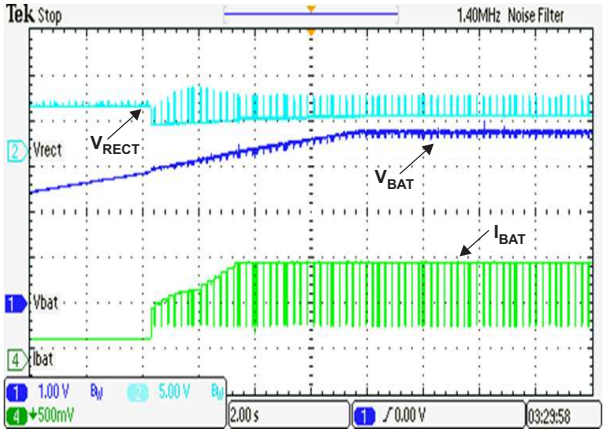

Figure 15. Precharge to Fast-Charge Transition

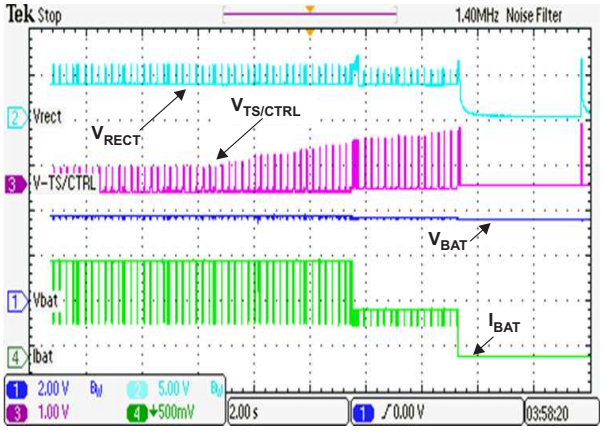

Figure 16. JEITA Functionality (Rising Temp) - bq51050B/bq51051B

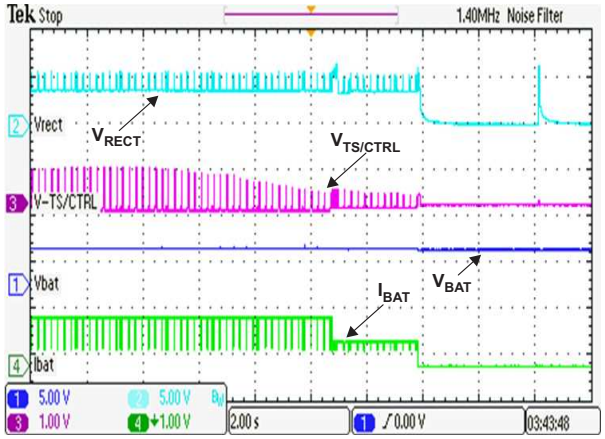

Figure 17. JEITA Functionality (Falling Temp) - bq51050B/bq51051B

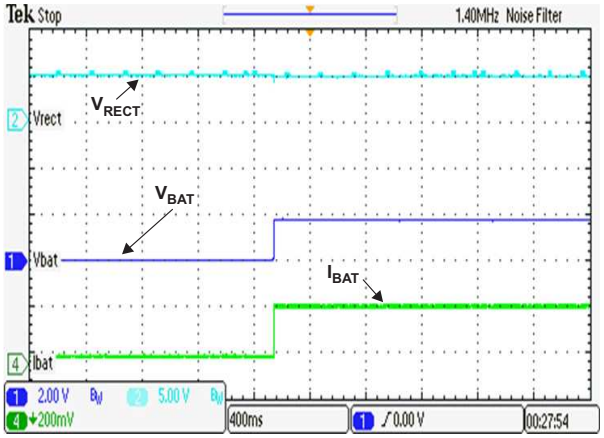

Figure 18. Battery Short to Precharge Mode Transition

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8 Detailed Description

8.1 Overview

8.1.1 A Brief Description of the Wireless System

A wireless system consists of a charging pad (primary, transmitter) and the secondary-side equipment. There are coils in the charging pad and in the secondary equipment which magnetically couple to each other when the equipment is placed on the charging pad. Power is transferred from the primary to the secondary by transformer action between the coils. Control over the amount of power transferred is achieved by changing the frequency of the primary drive.

The secondary can communicate with the primary by changing the load seen by the primary. This load variation results in a change in the primary coil current, which is measured and interpreted by a processor in the charging pad. The communication is digital - packets are transferred from the secondary to the primary. Differential bi-phase encoding is used for the packets. The rate is 2-kbps.

Various types of communication packets have been defined. These include identification and authentication packets, error packets, control packets, power usage packets, end of power packet and efficiency packets.

The primary coil is powered off most of the time. It wakes up occasionally to see if a secondary is present. If a secondary authenticates itself to the primary, the primary remains powered up. The secondary maintains full control over the power transfer using communication packets.

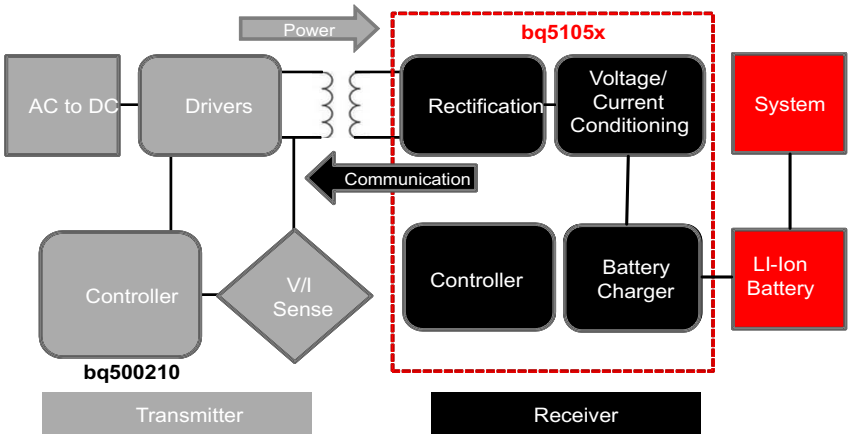
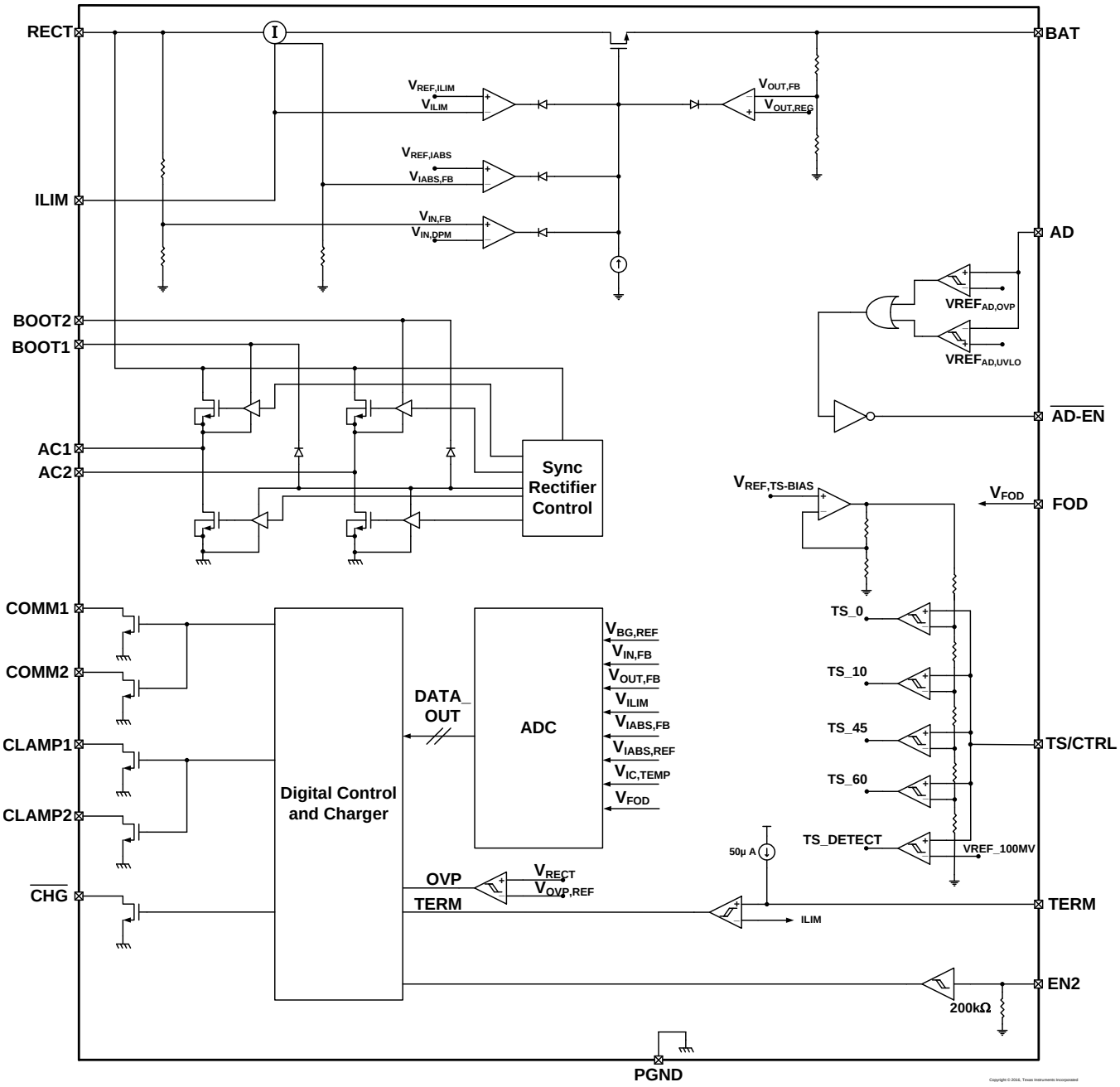


Figure 19. WPC Wireless Power Charging System Indicating the Functional Integration of the bq5105x

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Using the bq5105x as a Wireless Li-Ion/Li-Pol Battery Charger (With Reference to *Functional Block Diagram*)

Functional Block Diagram is the schematic of a system which uses the bq5105x as a direct battery charger. When the system shown in *Functional Block Diagram* is placed on the charging pad (transmitter), the receiver coil couples to the magnetic flux generated by the coil in the charging pad which consequently induces a voltage in the receiver coil. The internal synchronous rectifier feeds this voltage to the RECT pin which has the filter capacitor C_3.

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Feature Description (continued)

The bq5105x identifies and authenticates itself to the primary using the COMM pins by switching on and off the COMM FETs and hence switching in and out C_{COMM}. If the authentication is successful, the transmitter will remain powered on. The bq5105x measures the voltage at the RECT pin, calculates the difference between the actual voltage and the desired voltage $V_{RECT-REG}$ and sends back error packets to the primary. This process goes on until the RECT voltage settles at $V_{RECT-REG}$.

During power-up, the LDO is held off until the $V_{RECT-REG}$ threshold converges. The voltage control loop ensures that the output (BAT) voltage is maintained at $V_{BAT-REG}$. The values of V_{BAT} and V_{RECT} are dependant on the battery charge mode. The bq5105x continues to monitor the V_{RECT} and V_{BAT} and sends error packets to the primary every 250 ms. The bq5105x regulates the V_{RECT} voltage very close to battery voltage, this voltage tracking process minimizes the voltage difference across the internal LDO and maximizes the charging efficiency. If a large transient occurs, the feedback to the primary speeds up to every 32 ms in order to converge on an operating point in less time.

8.3.2 Details of a Qi Wireless Power System and bq5105xB Power Transfer Flow Diagrams

The bq5105xB integrates a fully compliant WPC v1.2 communication algorithm in order to streamline receiver designs (no extra software development required). Other unique algorithms such as Dynamic Rectifier Control are also integrated to provide best-in-class system performance. This section provides a high level overview of these features by illustrating the wireless power transfer flow diagram from start-up to active operation.

During start-up operation, the wireless power receiver must comply with proper handshaking to be granted a power contract from the TX. The TX will initiate the handshake by providing an extended digital ping. If an RX is present on the TX surface, the RX will then provide the signal strength, configuration and identification packets to the TX (see volume 1 of the WPC specification for details on each packet). These are the first three packets sent to the TX. The only exception is if there is a shutdown condition on the EN1/EN2, AD, or TS/CTRL pins where the Rx will shut down the TX immediately. Once the TX has successfully received the signal strength, configuration and identification packets, the RX will be granted a power contract and is then allowed to control the operating point of the power transfer. With the use of the bq5105xB Dynamic Rectifier Control algorithm, the RX will inform the TX to adjust the rectifier voltage above 5 V before enabling the output supply. This method enhances the transient performance during system start-up. See Figure 20 for the start-up flow diagram details.

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Feature Description (continued)

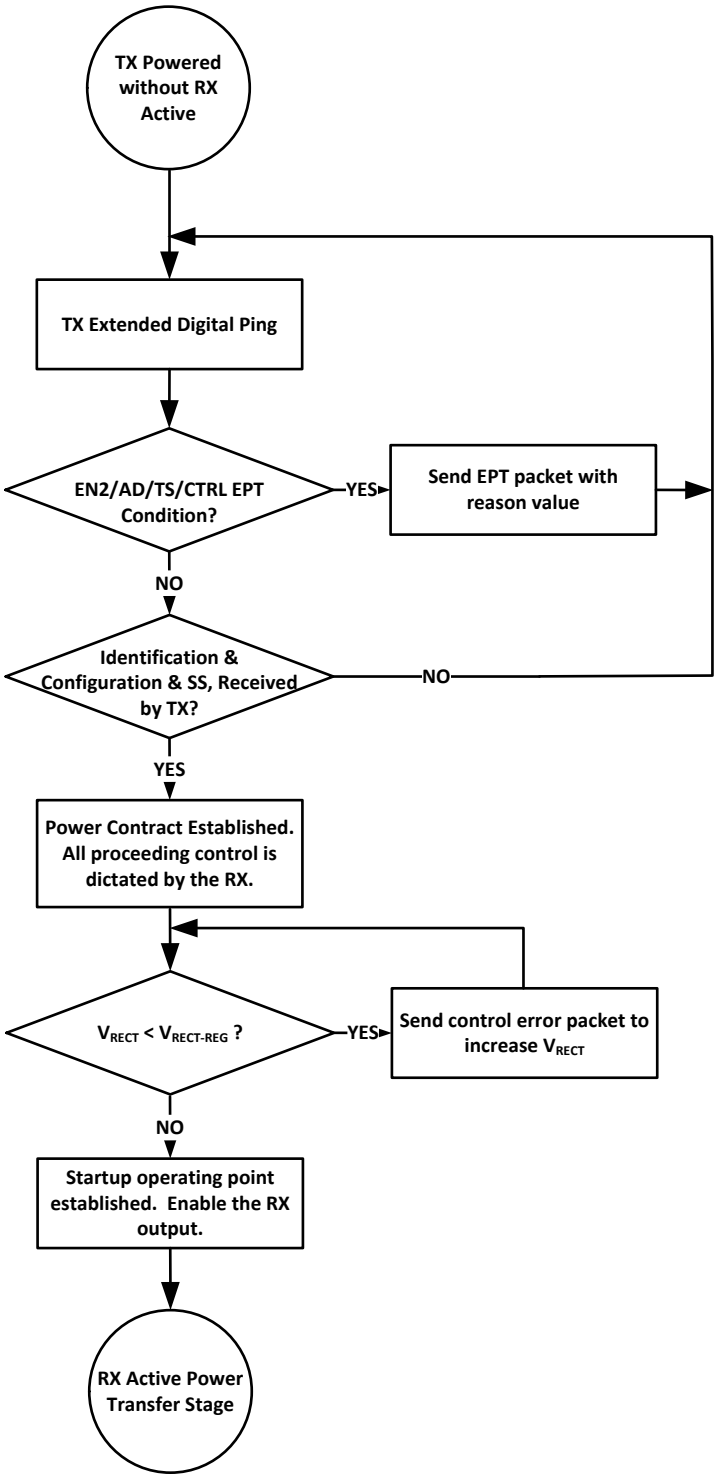

Figure 20. Wireless Power Start-up Flow Diagram

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Feature Description (continued)

Once the start-up procedure has been established, the RX will enter the active power transfer stage. This is considered the "main loop" of operation. The Dynamic Rectifier Control algorithm will determine the rectifier voltage target based on a percentage of the maximum output current level setting (set by K_{ILIM} and the I_{ILIM} resistance to PGND). The RX will send control error packets in order to converge on these targets. As the output current changes, the rectifier voltage target will dynamically change. As a note, the feedback loop of the WPC system is relatively slow where it can take up to 90 ms to converge on a new rectifier voltage target. It should be understood that the instantaneous transient response of the system is open loop and dependent on the RX coil output impedance at that operating point. More details on this will be covered in the section Receiver Coil Load-Line Analysis. The "main loop" will also determine if any conditions are true and will then discontinue the power transfer. Figure 21 shows the active power transfer loop.

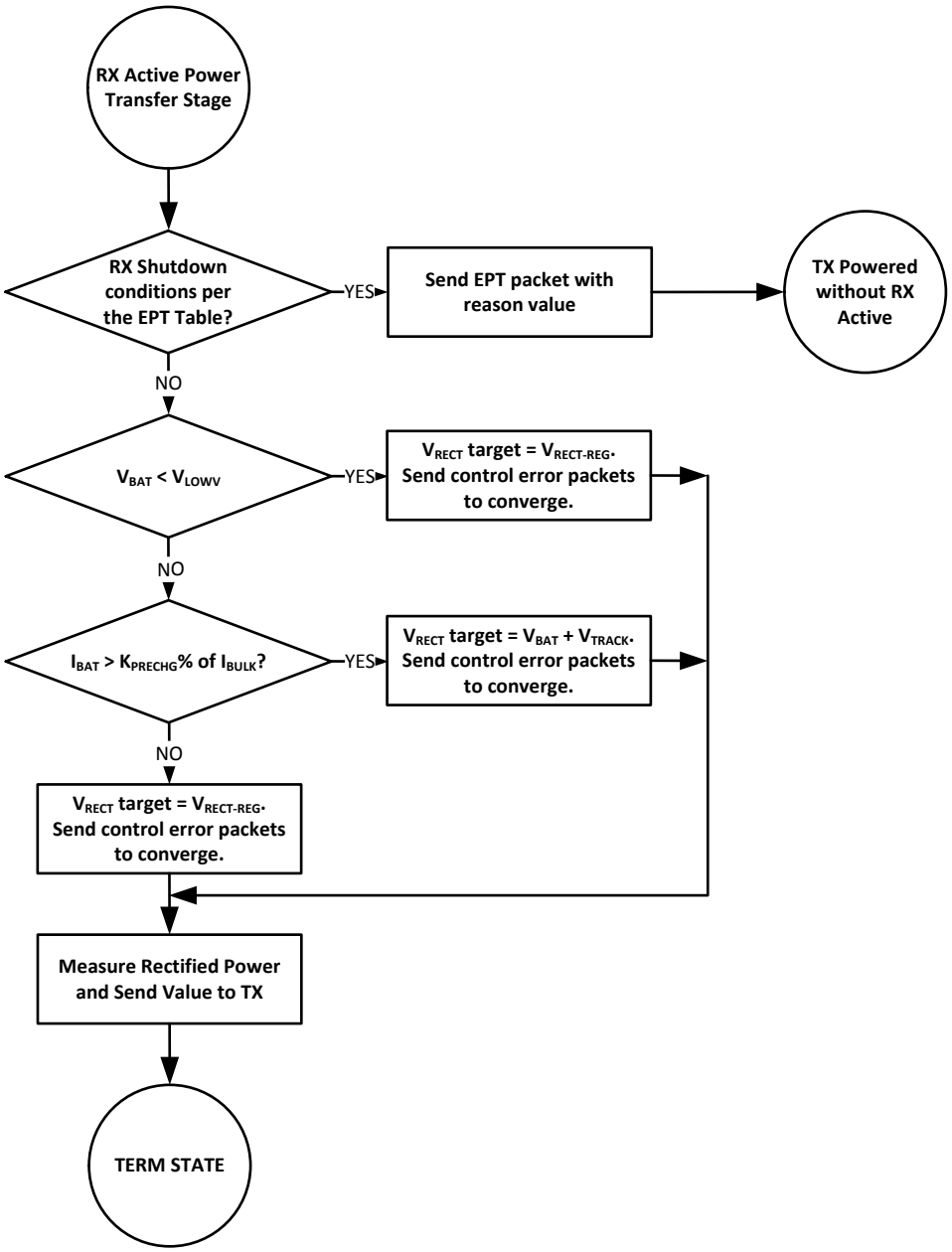

Figure 21. Active Power Transfer Flow Diagram

Feature Description (continued)

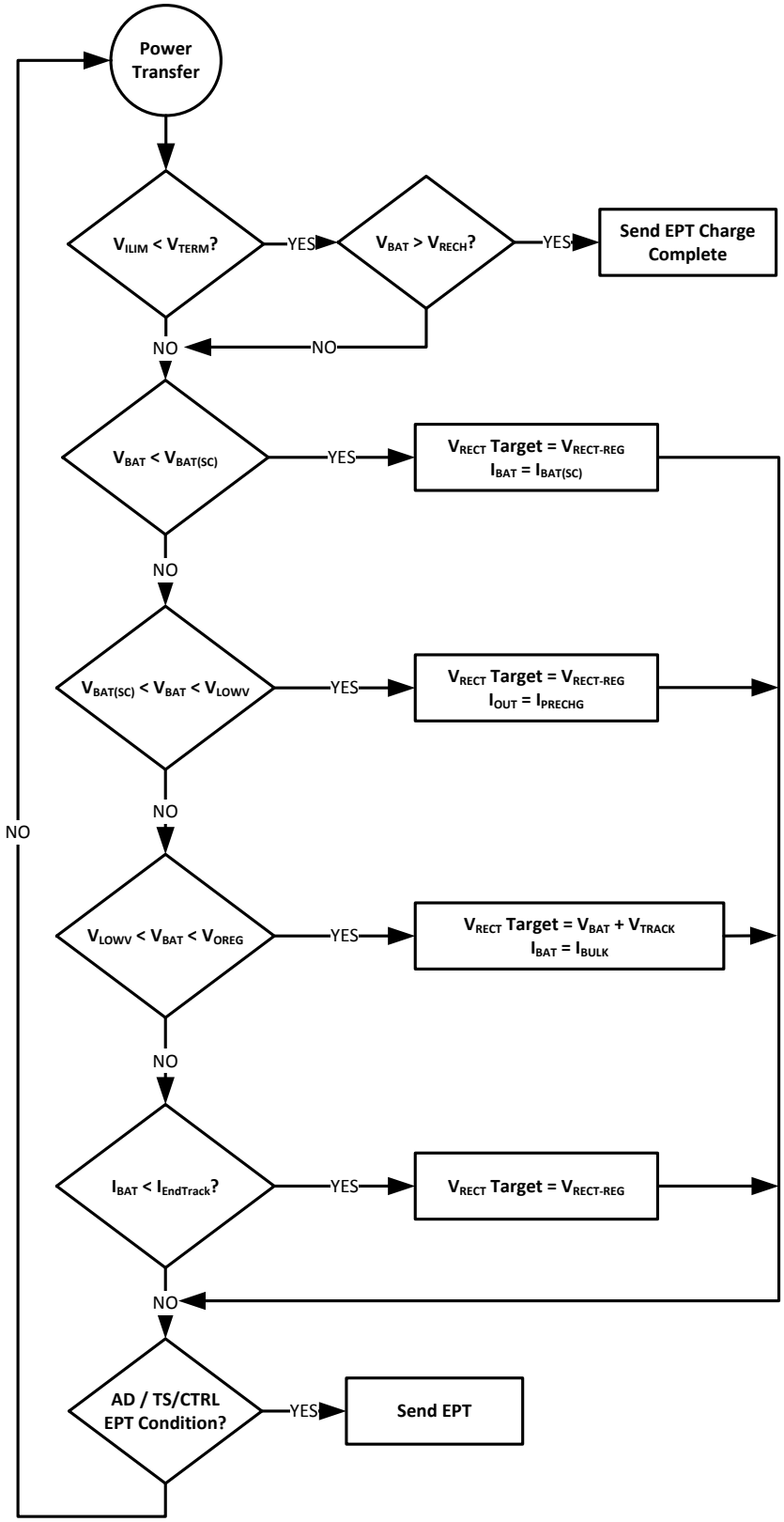

Figure 22. TERM STATE Flow Diagram of bq5105XB

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Feature Description (continued)

8.3.3 Battery Charge Profile

The battery is charged in three phases: precharge, fast-charge constant current and constant voltage. A voltage-based battery pack thermistor monitoring input (TS function of the TS/CTRL pin) is included that monitors battery temperature for safe charging. The TS function for bq51050B and bq51051B is JEITA compatible. The TS function for the bq51052B modifies the current regulation differently than standard JEITA. See *Battery-Charger Safety and JEITA Guidelines* for more details.

The rectifier voltage follows BAT voltage plus V_{TRACK} for any battery voltage above V_{LOWV} to full regulation voltage and most of the taper charging phase. If the battery voltage is below V_{LOWV} the rectifier voltage increases to $V_{RECT-REG}$.

If I_{BAT} is less than $I_{EndTrack}$ (a percentage of I_{BULK}) during taper mode, the rectifier voltage increases to $V_{RECT-REG}$.

The charge profile for the bq51050B and bq51051B is shown in Figure 23 while the bq52052B is shown in Figure 24.

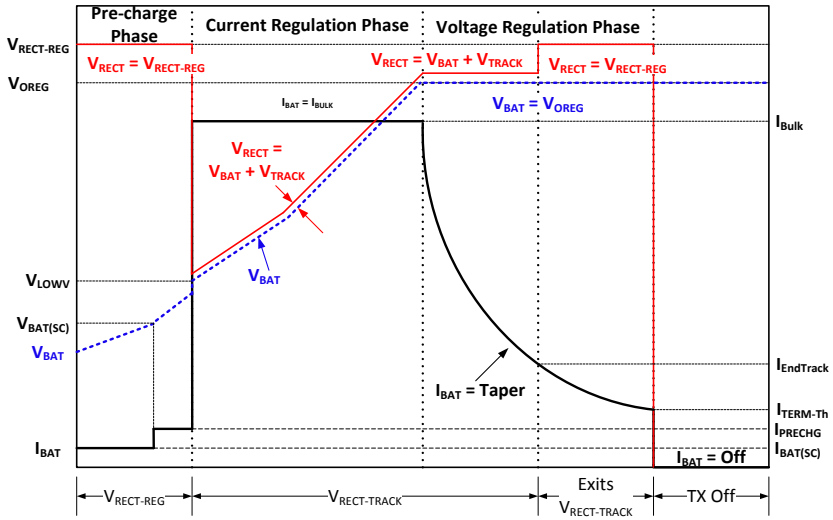

Figure 23. bq51050B and bq51051B Li-Ion Battery Charge Profile

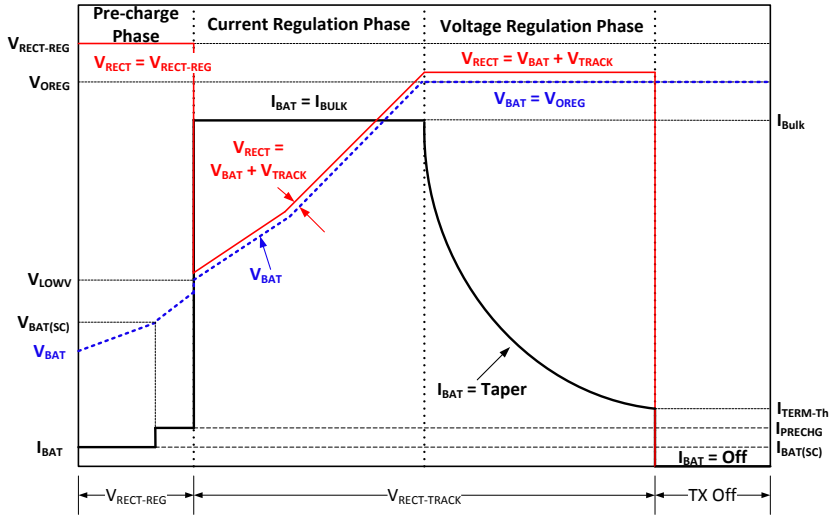

Figure 24. bq51052B Li-Ion Battery Charge Profile

Feature Description (continued)

8.3.4 Battery Charging Process

8.3.4.1 Precharge Mode ($V_{BAT} \le V_{LOWV}$)

The bq5105X enters precharge mode when $V_{BAT} \le V_{LOWV}$. Upon entering precharge mode, battery charge current limit is set to I_{PRECHG}. During precharge mode, the charge current is regulated to K_{PRECHG} percent of the fast charge current (I_{BULK}) setting. For example, if IBULK is set to 800 mA, then the precharge current would have a typical value of 160 mA.

If the battery is deeply discharged or shorted ($V_{BAT} < V_{BAT(SC)}$), the bq5105X applies $I_{BAT(SC)}$ current to bring the battery voltage up to acceptable charging levels. Once the battery rises above $V_{BAT(SC)}$, the charge current is regulated to I_{PRECHG}.

Under normal conditions, the time spent in this precharge region is a very short percentage of the total charging time and this does not affect the overall charging efficiency for very long.

8.3.4.2 Fast Charge Mode / Constant Voltage Mode

Once $V_{BAT} > V_{LOWV}$, the bq5105x enters fast charge mode (Current Regulation Phase) where charge current is regulated using the internal MOSFETs between RECT and BAT. Once the battery voltage charges up to $V_{BAT-REG}$, the bq5105x enters constant voltage (CV) phase and regulates battery voltage to V_{OREG} and the charging current is reduced.

Once I_{BAT} falls below the termination threshold ($I_{TERM-Th}$), the charger sends an EPT (Charge Complete) notification to the TX and enters high impedance mode.

8.3.4.3 Battery Charge Current Setting Calculations

8.3.4.3.1 R_{ILIM} Calculations

The bq5105x includes a means of providing hardware overcurrent protection by means of an analog current regulation loop. The hardware current limit provides an extra level of safety by clamping the maximum allowable output current (for example, a current compliance). The calculation for the total R_{ILIM} resistance is as follows:

$$R_1 = \frac{K_{ILIM}}{I_{BULK}} - R_{FOD} \qquad R_{ILIM} = R_1 + R_{FOD} \qquad I_{BULK} = \frac{K_{ILIM}}{R_{ILIM}} \tag{1}$$

Where I_{BULK} is the programmed battery charge current during fast charge mode. When referring to the application diagram shown in Figure 32, R_{ILIM} is the sum of R_{FOD} and R_1 (the total resistance from the ILIM pin to PGND).

8.3.4.3.2 Termination Calculations

The bq5105X includes a programmable upper termination threshold. The upper termination threshold is calculated using Equation 2:

$$R_{TERM} = K_{TERM} * \%I_{BULK} \qquad \%I_{BULK} = \frac{R_{TERM}}{K_{TERM}} \tag{2}$$

The K_{TERM} constant is specified in *Electrical Characteristics* as 240 Ω/%. The upper termination threshold is set as a percentage of the charge current setting (I_{BULK}).

For example, if R_{ILIM} is set to 314 Ω, I_{BULK} will be 1 A (314 ÷ 314). If the upper termination threshold is desired to be 100 mA, this would be 10% of I_{BULK}. The R_{TERM} resistor would then equal 2.4 kΩ (240 × 10).

Termination can be disabled by floating the TERM pin. If the TERM pin is grounded the termination function is effectively disabled. However, due to offsets of internal comparators, termination may occur at low battery currents.

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Feature Description (continued)

8.3.4.4 Battery-Charger Safety and JEITA Guidelines

The bq5105x continuously monitors battery temperature by measuring the voltage between the TS/CTRL pin and PGND. A negative temperature coefficient thermistor (NTC) and an external voltage divider typically develop this voltage. The bq5105x compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the voltage on TS/CTRL pin (V_{TS}) must be within the V_{T1} to V_{T4} thresholds. If V_{TS} is outside of this range, the bq5105x suspends charge and waits until the battery temperature is within the V_{T1} to V_{T4} range. Additional information on the Temperature Sense function can be found in *Internal Temperature Sense (TS Function of the TS/CTRL Pin)*.

8.3.4.4.1 bq51050B and bq51051B JEITA

If V_{TS} is within the ranges of V_{T1} and V_{T2} or V_{T3} and V_{T4}, the charge current is reduced to $I_{BULK}/2$. If V_{TS} is within the range of V_{T1} and V_{T3}, the maximum charge voltage regulation is V_{OREG}. If V_{TS} is within the range of V_{T3} and V_{T4}, the maximum charge voltage regulation is reduced to "NEW SPEC". Figure 25 summarizes the operation.

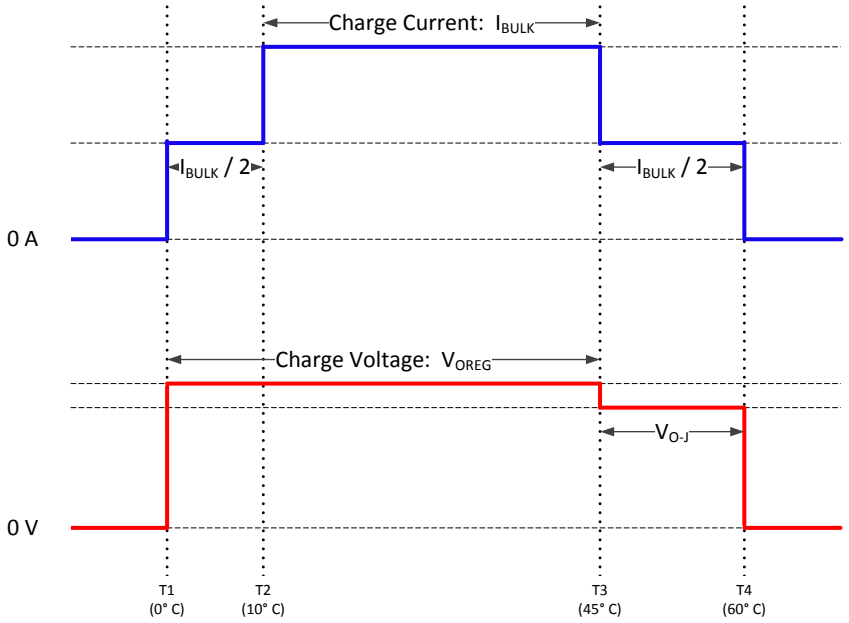

Figure 25. JEITA Compatible TS Profile for bq51050B and bq51051B

8.3.4.4.2 bq51052B Modified JEITA

The bq51052B has a modififed JEITA profile. The maximum charge current is not modified between V_{T1} and V_{T2} or between V_{T3} and V_{T4}, it remains at I_{BULK}. The maximum charge voltage is reduced to V_{O-J} when the V_{TS} is between V_{T3} and V_{T4}.

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Feature Description (continued)

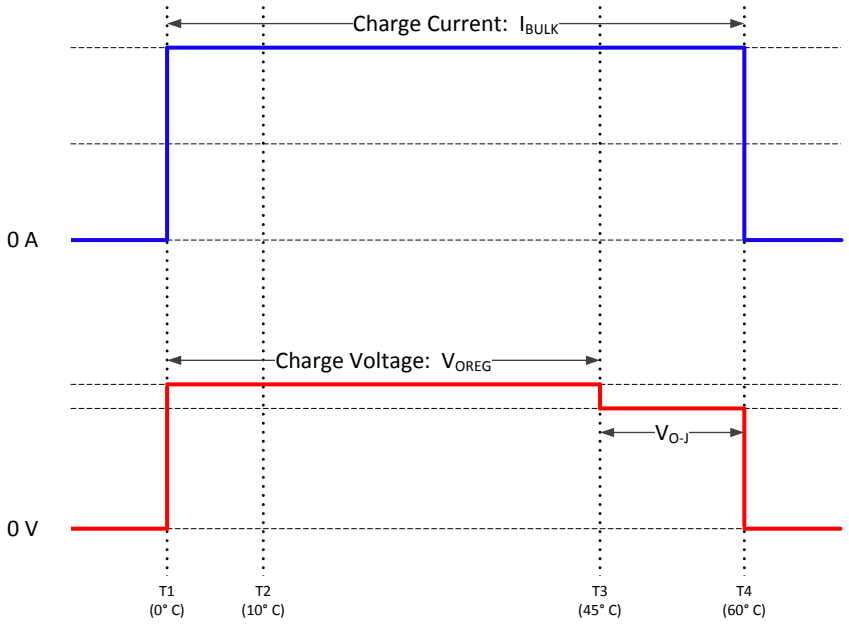

Figure 26. JEITA Compatible TS Profile for bq51052B

8.3.4.5 Input Overvoltage

If, for some condition (for example, a change in position of the equipment on the charging pad), the rectifier voltage suddenly increases in potential, the voltage-control loop inside the bq5105x becomes active, and prevents the output from going beyond $V_{BAT-REG}$. The receiver then starts sending back error packets every 32 ms until the RECT voltage comes back to an acceptable level, and then maintains the error communication every 250 ms.

If the input voltage increases in potential beyond V_{OVP}, the device switches off the internal FET and communicates to the primary to bring the voltage back to $V_{RECT-REG}$. In addition a proprietary voltage protection circuit is activated by means of C_{CLAMP1} and C_{CLAMP2} that protects the device from voltages beyond the maximum rating.

8.3.4.6 End Power Transfer Packet (WPC Header 0x02)

The WPC allows for a special command to terminate power transfer from the TX termed End Power Transfer (EPT) packet. WPC v1.2 specifies the reasons for sending a termination packet and their data field value. In Table 1, the CONDITION column corresponds to the stimulus causing the bq5105x device to send the hexidecimal code in the VALUE column.

Table 1. Termination Packets

REASON	VALUE	CONDITION
Unknown	0x00	AD > $V_{AD-Pres}$, TS/CTRL = $V_{CTRL-HI}$
Charge Complete	0x01	I_{BAT} falls below $I_{TERM-Th}$ during Taper mode
Internal Fault	0x02	T_J > 150°C or R_{ILIM} < $R_{ILIM-SHORT}$
Overtemperature	0x03	TS < V_{HOT}, TS > V_{COLD}, or TS/CTRL < $V_{CTRL-LOW}$
Overvoltage	0x04	Not Sent
Overcurrent	0x05	Not Sent
Battery failure	0x06	Battery is not coming out of precharge mode after Precharge time-out, or fast charge time-out has occured.
Reconfigure	0x07	Not Sent
No Response	0x08	V_{RECT} target does not converge

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8.3.4.7 Status Output

The bq5105x provides one status output, $\overline{CHG}$. This output is an open-drain NMOS device that is rated to 20 V. The open-drain FET connected to the $\overline{CHG}$ pin will be turned on whenever the output (BAT) of the charger is enabled. As a note, the output of the charger supply will not be enabled if the $V_{RECT-REG}$ does not converge to the no-load target voltage.

8.3.4.8 Communication Modulator

The bq5105x provides two identical, integrated communication FETs which are connected to the pins COMM1 and COMM2. These FETs are used for modulating the secondary load current which allows bq5105x to communicate error control and configuration information to the transmitter.There are two methods to implement load modulation, capacitive and resistive.

Capacitive load modulation is more commonly used. Capacitive load modulation is shown in Figure 27. In this case, a capacitor is connected from COMM1 to AC1 and from COMM2 to AC2. When the COMM switches are closed there is effectively a 22 nF capacitor connected between AC1 and AC2. Connecting a capacitor in between AC1 and AC2 modulates the impedance seen by the coil, which will be reflected to the primary and interpreted by the controller as a change in current.

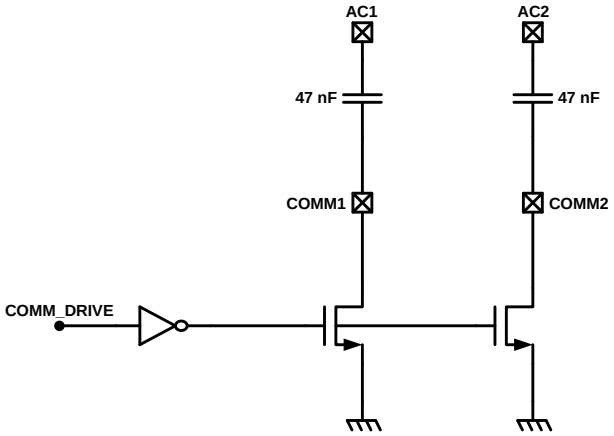

Figure 27. Capacitive Load Modulation

Figure 28 shows how the COMM pins can be used for resistive load modulation. Each COMM pin can handle at most a 24 Ω communication resistor. Therefore, if a COMM resistor between 12 Ω and 24 Ω is required, COMM1 and COMM2 pins must be connected in parallel. bq5105x does not support a COMM resistor less than 12 Ω.

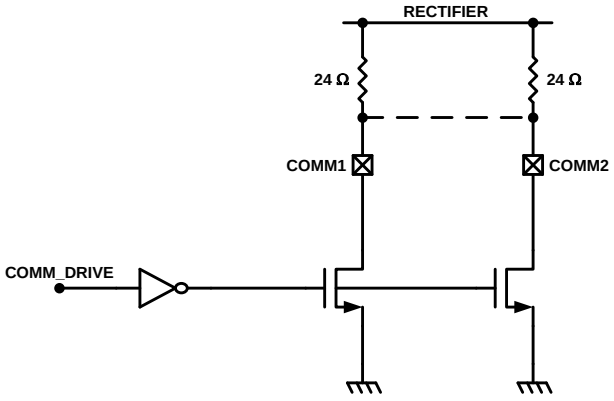

Figure 28. Resistive Load Modulation

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8.3.4.9 Adaptive Communication Limit

The Qi communication channel is established through backscatter modulation as described in the previous sections. This type of modulation takes advantage of the loosely coupled inductor relationship between the RX and TX coils. Essentially, the switching in-and-out of the communication capacitor or resistor adds a transient load to the RX coil in order to modulate the TX coil voltage and current waveform (amplitude modulation). The consequence of this technique is that a load transient (load current noise) from the mobile device has the same signature. To provide noise immunity to the communication channel, the output load transients must be isolated from the RX coil. The proprietary feature *Adaptive Communication Limit* achieves this by dynamically adjusting the current limit of the regulator.

This can be seen in Figure 12. In this plot, an output load is limited to 400 mA during communications time. The pulses on V_{RECT} indicate that a communication packet event is occurring. The regulator limits the load to a constant 400 mA and, therefore, preserves communication.

8.3.4.10 Synchronous Rectification

The bq5105x provides an integrated, self-driven synchronous rectifier that enables high-efficiency AC to DC power conversion. The rectifier consists of an all NMOS H-Bridge driver where the back gates of the diodes are configured to be the rectifier when the synchronous rectifier is disabled. During the initial start-up of the WPC system the synchronous rectifier is not enabled. At this operating point, the DC rectifier voltage is provided by the diode rectifier. Once V_{RECT} is greater than V_{UVLO}, half synchronous mode will be enabled until the load current surpasses I_{BAT-SR}. Above I_{BAT-SR} the full synchronous rectifier stays enabled until the load current drops back below the hysteresis level ($I_{BAT-SRH}$) where half synchronous mode is re-enabled.

8.3.4.11 Internal Temperature Sense (TS Function of the TS/CTRL Pin)

The bq5105x includes a ratiometric battery temperature sense circuit. The temperature sense circuit has two ratiometric thresholds which represent hot and cold conditions. An external temperature sensor is recommended to provide safe operating conditions to the receiver product. This pin is best used when monitoring the battery temperature.

The circuits in Figure 29 allow for any NTC resistor to be used with the given V_{HOT} and V_{COLD} thresholds. The thermister characteristics and threshold temperatures selected will determine which circuit is best for an application.

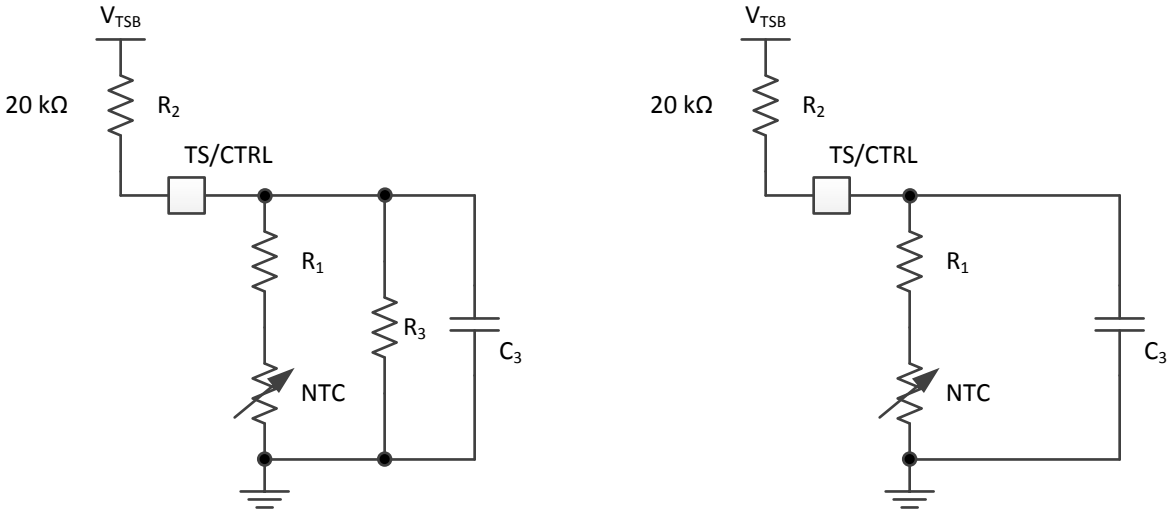

Figure 29. NTC Circuit Options for Safe Operation of the Wireless Receiver Power Supply

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The resistors R1 and R3 can be solved by resolving the system of equations at the desired temperature thresholds. The two equations are:

$$\%V_{COLD} = \frac{\left(\frac{R_3\left(R_{NTC}|_{TCOLD} + R_1\right)}{R_3 + \left(R_{NTC}|_{TCOLD} + R_1\right)}\right)}{\left(\frac{R_3\left(R_{NTC}|_{TCOLD} + R_1\right)}{R_3 + \left(R_{NTC}|_{TCOLD} + R_1\right)}\right) + R2} \times 100 \quad (3)$$

$$\%V_{HOT} = \frac{\left(\frac{R_3\left(R_{NTC}|_{THOT} + R_1\right)}{R_3 + \left(R_{NTC}|_{THOT} + R_1\right)}\right)}{\left(\frac{R_3\left(R_{NTC}|_{THOT} + R_1\right)}{R_3 + \left(R_{NTC}|_{THOT} + R_1\right)}\right) + R2} \times 100 \quad (4)$$

Where:

$$R_{NTC}|_{TCOLD} = R_o e^{\beta\left(1/T_{COLD} - 1/T_o\right)}$$

$$R_{NTC}|_{THOT} = R_o e^{\beta\left(1/T_{HOT} - 1/T_o\right)}$$

T_{COLD} and T_{HOT} are the desired temperature thresholds in degrees Kelvin. R_o is the nominal resistance at T_0 (25°C) and β is the temperature coefficient of the NTC resistor. For an example solution for part number ERT-JZEG103JA see the *BQ5105XB NTC Calculator Tool*, (SLUS629).

Where,

T_{COLD} = 0°C (273.15°K)
T_{HOT} = 60°C (333.15°K)
β = 3380
R_o = 10 kΩ

The plot of the percent V_{TSB} versus temperature is shown in Figure 30:

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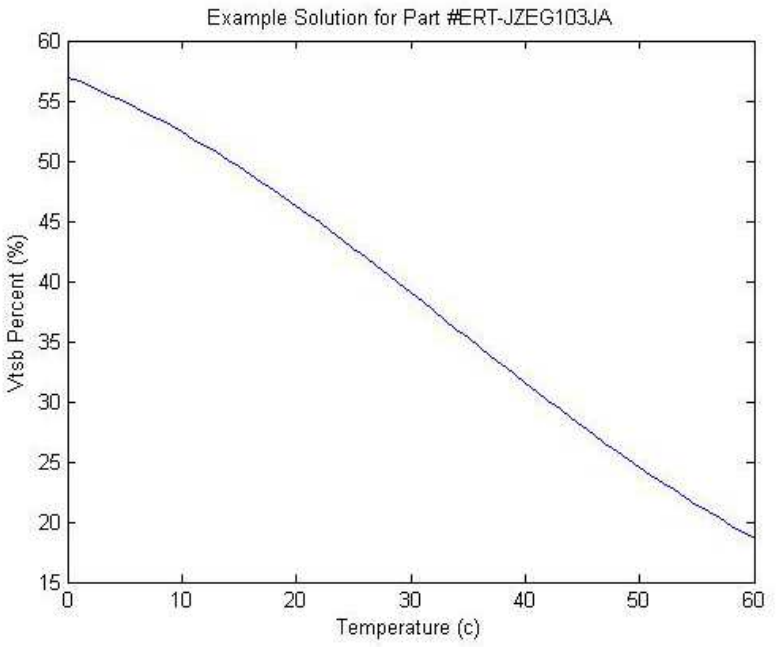

Figure 30. Example Solution for Panasonic Part # ERT-JZEG103JA

Figure 31 shows the periodic biasing scheme used for measuring the TS state. An internal TS_READ signal enables the TS bias voltage for 25 ms. During this period the TS comparators are read (each comparator has a 10-ms deglitch) and appropriate action is taken based on the temperature measurement. After this 25-ms period has elapsed the TS_READ signal goes low, which causes the TS/CTRL pin to become high impedance. During the next 100-ms period, the TS voltage is monitored and compared to $V_{CTRL-HI}$. If the TS voltage is greater than $V_{CTRL-HI}$ then a secondary device is driving the TS/CTRL pin and a CTRL = 1 is detected.

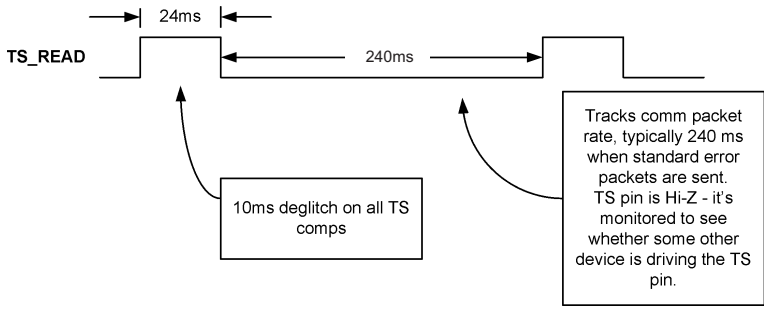

Figure 31. Timing Diagram for TS Detection Circuit

8.3.4.11.1 TS/CTRL Function

The TS/CTRL pin offers three functions:

- NTC temperature monitoring
- Charge done indication
- Fault indication

When an NTC resistor is connected between the TS/CTRL pin and PGND, the NTC function is allowed to operate. This functionality can effectively be disabled by connecting a 10 kΩ resistor from TS/CRTL to PGND. If the TS/CTRL pin is pulled above $V_{CTRL-HI}$, the RX is shut down with the indication of a charge complete condition. If the TS/CTRL pin is pulled below $V_{CTRL-LOW}$, the RX is shut down with the indication of a fault.

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8.3.4.11.2 Thermal Protection

The bq5105x includes thermal shutdown protection. If the die temperature reaches $T_{J\text{-}SD}$, the LDO is shut off to prevent any further power dissipation. Once the temperature falls $T_{J\text{-}Hys}$ below $T_{J\text{-}SD}$, operation can continue.

8.3.4.12 WPC v1.2 Compatibility

The bq5105x is a WPC v1.2 compatible device. In order to enable a Power Transmitter to monitor the power loss across the interface as one of the possible methods to limit the temperature rise of Foreign Objects, the bq5105x reports its Received Power to the Power Transmitter. The Received Power equals the power that is available from the output of the Power Receiver plus any power that is lost in producing that output power. For example, the power loss includes (but is not limited to) the power loss in the Secondary Coil and series resonant capacitor, the power loss in the Shielding of the Power Receiver, the power loss in the rectifier, the power loss in any post-regulation stage, and the eddy current loss in metal components or contacts within the Power Receiver. In the WPC v1.2 specification, foreign object detection (FOD) is enforced, that means the bq5105x will send received power information with known accuracy to the transmitter.

WPC v1.2 defines Received Power as “the average amount of power that the Power Receiver receives through its Interface Surface, in the time window indicated in the Configuration Packet”.

A Receiver will be certified as WPC v1.2 only after meeting the following requirement. The device under test (DUT) is tested on a Reference Transmitter whose transmitted power is calibrated, the receiver must send a received power such that:

$$0 < (\text{TX PWR})\ \text{REF} - (\text{RX PWR out})\ \text{DUT} < 375\ \text{mW} \quad (5)$$

This 250 mW bias ensures that system will remain interoperable.

WPC v1.2 Transmitters will be tested to see if they can detect reference Foreign Objects with a Reference receiver. The WPC v1.2 specification allows much more accurate sensing of Foreign Objects than WPC v1.0.

A Transmitter can be certified as a WPC v1.2 only after meeting the following requirement. A Transmitter is tested to see if it can prevent some reference Foreign Objects (disc, coin, foil) from exceeding their threshold temperature (60°C, 80°C).

8.4 Device Functional Modes

The general modes of battery charging are described above in the *Feature Description*. The bq5105x devices have several functional modes. Start-up refers to the initial power transfer and communication between the receiver (bq5105x circuit) and the transmitter. Power transfer refers to any time that the TX and RX are communicating and power is being delivered from the TX to the RX. Charge termination covers intentional termination (charge complete) and unintentional termination (removal of the RX from the TX, over temperature or other fault conditions).

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The bq51050B is an integrated wireless power receiver and charger in a single device. The device complies with the WPC v1.2 specifications for a wireless power receiver. When paired with a WPC v1.2 compliant transmitter, it can provide up to 5-W of power for battery charging. There are several tools available for the design of the system. These tools may be obtained by checking the product page at www.ti.com/product/bq51050b.

9.2 Typical Application

9.2.1 bq51050B Used as a Wireless Power Receiver and Li-Ion/Li-Pol Battery Charger

The following application discussion covers the requirements for setting up the bq51050B in a Qi-compliant system for charging a battery.

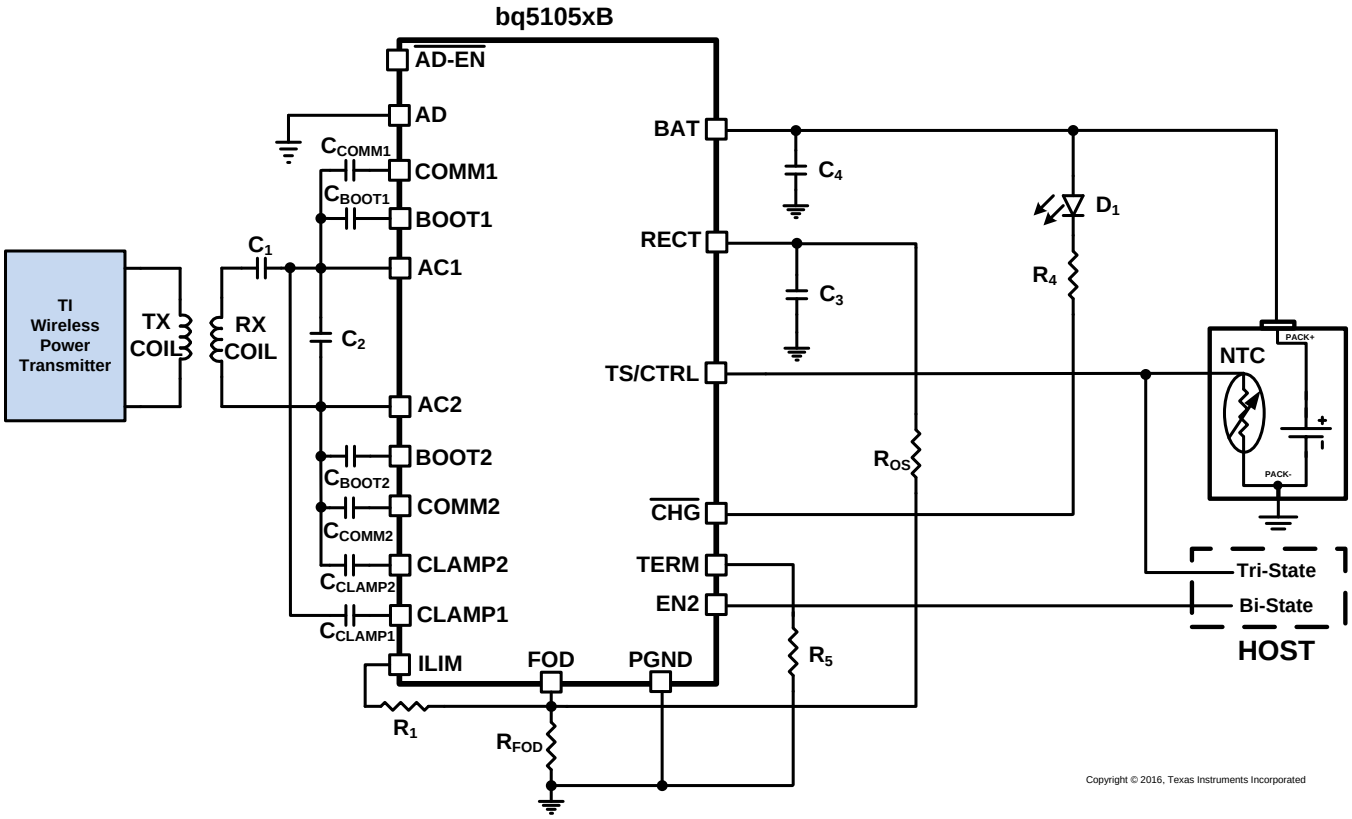

Figure 32. Typical Application Schematic

9.2.1.1 Design Requirements

This application is for a 4.2-V Lithium-Ion battery to be charged at 800 mA. Because this is planned for a WPC v1.2 solution, any of the Qi-certified transmitters can be used interchangeably so no discussion of the TX is required. To charge a 4.20-V Li-Ion battery, the bq51050B will be chosen. Each of the components from the application drawing will be examined. Temperature sensing of the battery must be done with JEITA specifications. An LED indicator is required to notify the user if charging is active.

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Typical Application (continued)

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Series and Parallel Resonant Capacitor Selection

Shown in Figure 33, the capacitors C1 (series) and C2 (parallel) make up the dual resonant circuit with the receiver coil. These two capacitors must be sized correctly per the WPC v1.2 specification. Figure 33 shows the equivalent circuit of the dual resonant circuit:

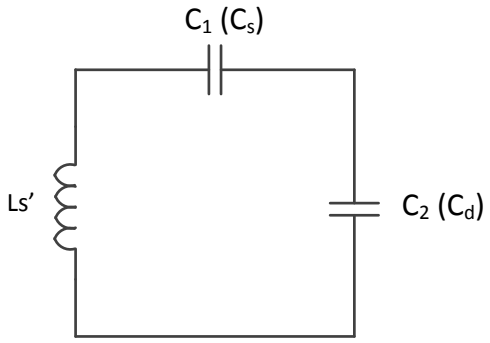

Figure 33. Dual Resonant Circuit with the Receiver Coil

The power receiver design requirements in volume 1 of the WPC v1.2 specification highlights in detail the sizing requirements. To summarize, the receiver designer will be required take inductance measurements with a fixed test fixture. The test fixture is shown in Figure 34:

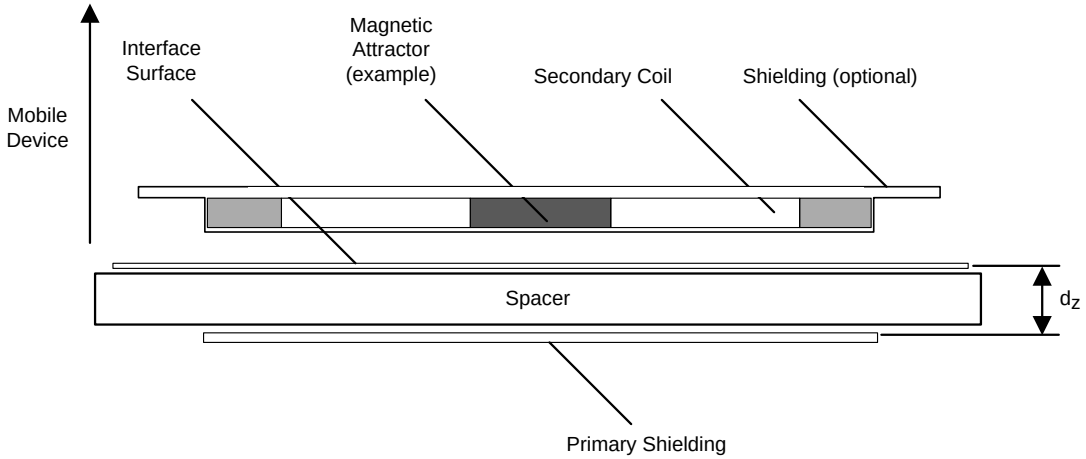

Figure 34. WPC v1.2 Receiver Coil Test Fixture for the Inductance Measurement Ls'

The primary shield is to be 50 mm × 50 mm × 1 mm of Ferrite material PC44 from TDK Corp. The gap (dZ) is to be 3.4 mm. The receiver coil, as it will be placed in the final system (for example, the back cover and battery must be included if the system calls for this), is to be placed on top of this surface and the inductance is to be measured at 1-V RMS and a frequency of 100 kHz. This measurement is termed Ls'. The measurement termed Ls is the free-space inductance. Each capacitor can then be calculated using Equation 6:

$$C_1 = \frac{1}{(2\pi \times fs)^2 \times L's}$$

$$C_2 = \left((f_D \times 2\pi)^2 \times L_s - \frac{1}{C_1} \right)^{-1} \quad (6)$$

Where f_S is 100 kHz +5/–10% and f_D is 1 MHz ±10%. C_1 must be chosen first prior to calculating C_2. The quality factor must be greater than 77 and can be determined by Equation 7:

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Typical Application (continued)

$$Q = \frac{2\pi \times f_D \times Ls}{R} \quad (7)$$

Where R is the DC resistance of the receiver coil. All other constants are defined above.

For this application, we will design with an inductance measurement (L) of 11 µH and an Ls' of 16 µH with a DC resistance of 191 mΩ. Plugging Ls' into Equation 6 above, we get a value for C_1 to be 158.3 nF. The range on the capacitance is about 144 nF to 175 nF. To build the resulting value, the optimum solution is usually found with 3 capacitors in parallel. This allows for more precise selection of values, lower effective resistance and better thermal results. To get 158 nF, choose from standard values. In this case, the values are 68 nF, 47 nF and 39 nF for a total of 154 nF. Well in the required range. Now that C_1 is chosen, the value of C_2 can be calculated. The result of this calculation is 2.3 nF. The practical solution for this is 2 capacitors, a 2.2 nF capacitor and a 100 pF capacitor. In all cases, these capacitors must have at least a 25-V rating. Solving for the quality factor (Q) this solution shows a rating over 500.

9.2.1.2.2 COMM, CLAMP and BOOT Capacitors

For most applications, the COMM, CLAMP and BOOT capacitors will be chosen to match the Evaluation Module.

The BOOT capacitors are used to allow the internal rectifier FETs to turn on and off properly. These capacitors are on the AC1 or AC2 lines to the Boot nodes and should have a minimum of 10-V rating. A 10-nF capacitor with a 10-V rating is chosen.

The CLAMP capacitors are used to aid the clamping process to protect against overvoltage. Choosing a 0.47-µF capacitor with a 25-V rating is appropriate for most applications.

The COMM capacitors are used to facilitate the communication from the RX to the TX. This selection can vary a bit more than the BOOT and CLAMP capacitors. In general, a 22-nF capacitor is recommended. Based on the results of testing of the communication robustness, a change to a 47-nF capacitor may be in order. The larger the capacitor the larger the deviation will be on the coil which sends a stronger signal to the TX. This also decreases the efficiency somewhat. In this case, choose the 22-nF capacitor with the 25-V rating.

9.2.1.2.3 Charging and Termination Current

The *Design Requirements* show an 800-mA charging current and an 80-mA termination current.

Setting the charge current (I_{BULK}) is done by selecting the R_1 and R_{FOD}. Solving Equation 1 results in R_{ILIM} of 393 Ω. Setting R_{FOD} to 200 Ω as a starting point before the FOD calibration is recommended. This leaves 205 Ω for R_1. Using standard resistor values (or resistors in series / parallel) can improve accuracy.

Setting the termination current is done with Equation 2. Because 80 mA is 10% of the I_{BULK} (800mA), the R_{TERM} is calculated as (240 * 10) or 2.4 kΩ.

9.2.1.2.4 Adapter Enable

The AD pin will be tied to the external USB power source to allow for an external source to power the system. AD_EN is tied to the gate of Q1 (CSD75205W1015). This allows the bq51050B to sense when power is applied to the AD pin. The EN2 pin controls whether the wired source will be enabled or not. EN2 is tied to the system host to allow it to control the use of the USB power. If wired power is enabled and present, the AD pin will disable the BAT output and then enable Q1 through the AD_EN pin. An external charger is required to take control of the battery charging.

9.2.1.2.5 Charge Indication and Power Capacitors

The $\overline{CHG}$ pin is open-drain. D_1 and R_4 are selected as a 2.1-V forward bias capable of 2 mA and a 100-Ω current-limiting resistor.

RECT is used to smooth the internal AC to DC conversion. Two 10-µF capacitors and a 0.1-µF capacitor are chosen. The rating is 25 V.

BAT capacitors are 1.0 µF and 0.1 µF.

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Typical Application (continued)

9.2.1.3 Application Curves

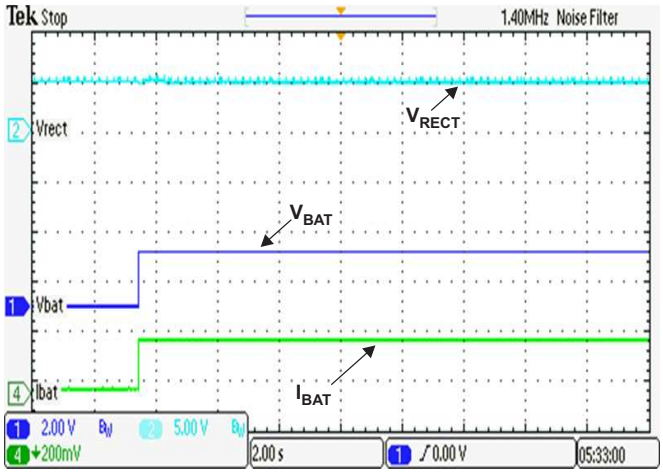

Figure 35. Battery Insertion During Precharge

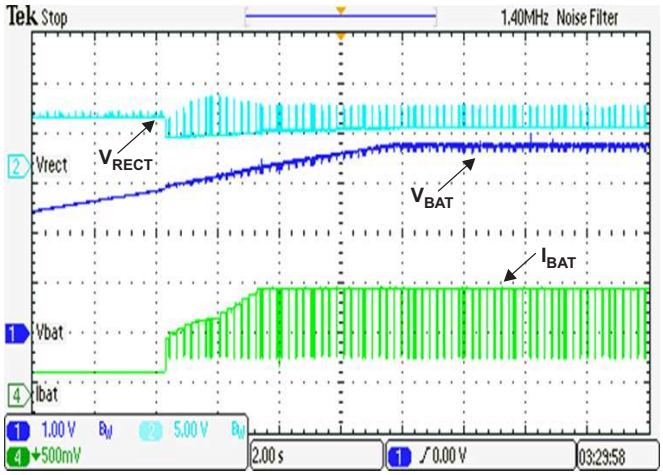

Figure 36. Precharge to Fast-Charge Transition

Typical Application (continued)

9.2.2 Application for Wired Charging

The application discussed below will cover the same requirements as the first example and will add a DC supply with a secondary charger. This solution covers using a standard DC supply or a USB port as the supply.

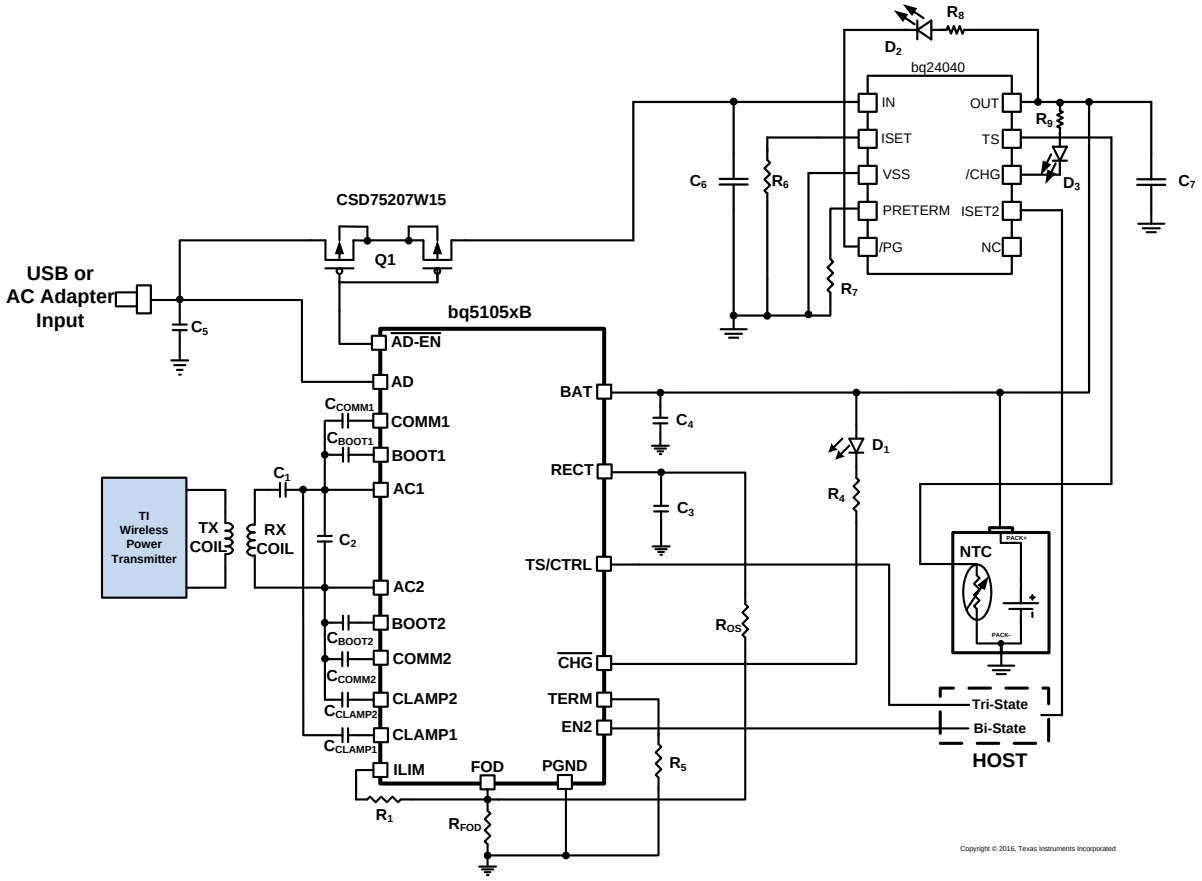

Figure 37. bq51050B Wireless Power Receiver and Wired Charger

9.2.2.1 Design Requirements

The requirements for this solution are identical to the first application so all common components are identical. This solution adds a wired charger and a blocking back-back FET (Q1).

The addition of a wired charger is simply enabled. The AD pin on the bq5105x is tied to the input of the DC supply. When the bq5105x senses a voltage greater than $V_{AD\text{-}Pres}$ on the AD pin, the BAT pin will be disabled (high impedance). Once the BAT pin is disabled, the $\overline{AD_EN}$ pin will transition and enable Q1. If wireless power is not present, the functionality of AD and $\overline{AD_EN}$ remains and wired charging can take place.

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Blocking Back-Back FET

Q1 is recommended to eliminate the potential for both wired and wireless systems to drive current to the simultaneously. The charge current and DC voltage level will set up parmerters for the blocking FET. The requirements for this system are 1 A for the wired charger and 5 V DC. The CSD75207W15 is chosen for its low RON and small size.

The wired charger in this solution is the bq24040. See the bq24040 datasheet (SLUS941) for specific component selection.

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10 Power Supply Recommendations

The bq51050B requires a Qi-compatible transmitter as its power supply.

11 Layout

11.1 Layout Guidelines

- Keep the trace resistance as low as possible on AC1, AC2, and BAT.
- Detection and resonant capacitors need to be as close to the device as possible.
- COMM, CLAMP, and BOOT capacitors need to be placed as close to the device as possible.
- Via interconnect on PGND net is critical for appropriate signal integrity and proper thermal performance.
- High frequency bypass capacitors need to be placed close to RECT and OUT pins.
- ILIM and FOD resistors are important signal paths and the loops in those paths to PGND must be minimized.
- For the RHL package, connect the thermal pad to ground to help dissipate heat.

  Signal and sensing traces are the most sensitive to noise; the sensing signal amplitudes are usually measured in mV, which is comparable to the noise amplitude. Make sure that these traces are not being interfered by the noisy and power traces. AC1, AC2, BOOT1, BOOT2, COMM1, and COMM2 are the main source of noise in the board. These traces should be shielded from other components in the board. It is usually preferred to have a ground copper area placed underneath these traces to provide additional shielding. Also, make sure they do not interfere with the signal and sensing traces. The PCB should have a ground plane (return) connected directly to the return of all components through vias (two vias per capacitor for power-stage capacitors, one via per capacitor for small-signal components).

  For a 1-A fast charge current application, the current rating for each net is as follows:
  - AC1 = AC2 = 1.2 A
  - OUT = 1 A
  - RECT = 100 mA (RMS)
  - COMMx = 300 mA
  - CLAMPx = 500 mA
  - All others can be rated for 10 mA or less

11.2 Layout Example

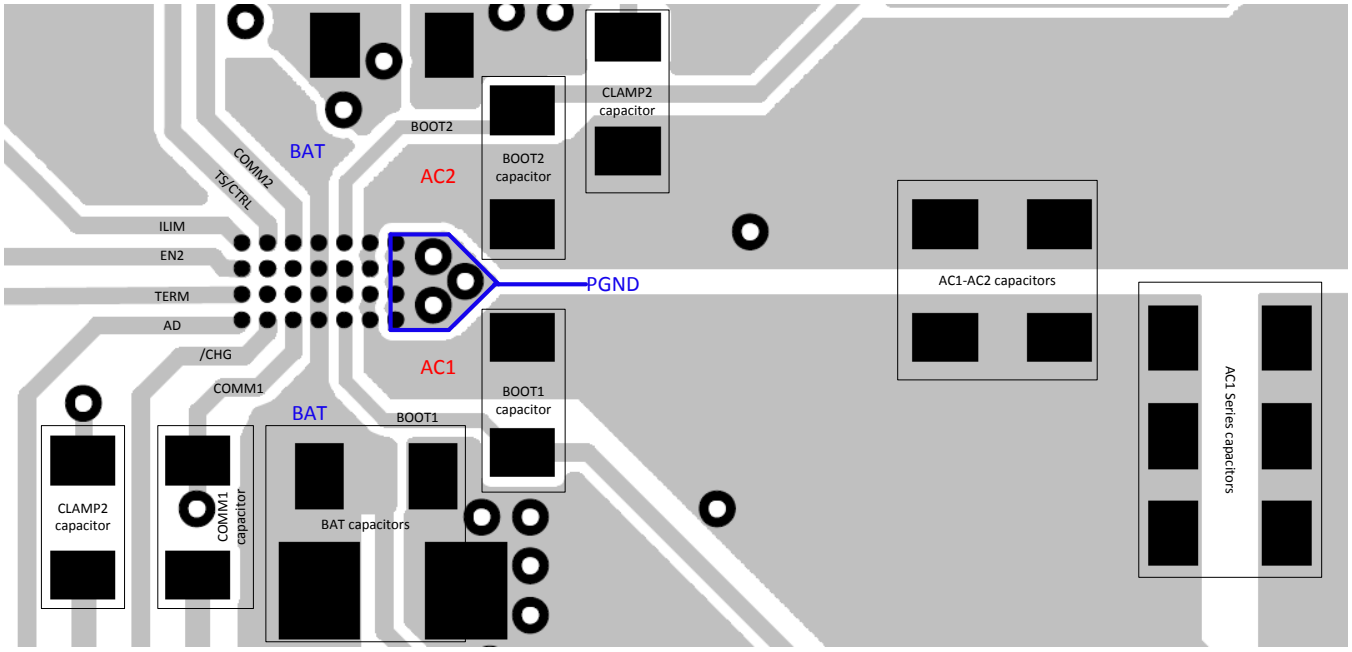

Figure 38. bq5105x Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

bq2404x 1A, Single-Input, Single Cell Li-Ion and Li-Pol Battery Charger With Auto Start, SLUS941

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
bq51050B	Click here	Click here	Click here	Click here	Click here
bq51051B	Click here	Click here	Click here	Click here	Click here
bq51052B	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates — go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button to register and receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ51050BRHLR	Active	Production	VQFN (RHL) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	BQ51050B
BQ51050BRHLR.A	Active	Production	VQFN (RHL) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	BQ51050B
BQ51050BRHLT	Active	Production	VQFN (RHL) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	BQ51050B
BQ51050BRHLT.A	Active	Production	VQFN (RHL) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	BQ51050B
BQ51050BRHLTG4	Active	Production	VQFN (RHL) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	BQ51050B
BQ51050BRHLTG4.A	Active	Production	VQFN (RHL) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	BQ51050B
BQ51050BYFPR	Active	Production	DSBGA (YFP) | 28	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51050B
BQ51050BYFPR.A	Active	Production	DSBGA (YFP) | 28	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51050B
BQ51050BYFPR.B	Active	Production	DSBGA (YFP) | 28	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51050B
BQ51050BYFPT	Active	Production	DSBGA (YFP) | 28	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51050B
BQ51050BYFPT.A	Active	Production	DSBGA (YFP) | 28	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51050B
BQ51050BYFPT.B	Active	Production	DSBGA (YFP) | 28	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51050B
BQ51051BRHLR	Active	Production	VQFN (RHL) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	BQ51051B
BQ51051BRHLR.A	Active	Production	VQFN (RHL) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	BQ51051B
BQ51051BRHLT	Active	Production	VQFN (RHL) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	BQ51051B
BQ51051BRHLT.A	Active	Production	VQFN (RHL) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 125	BQ51051B
BQ51051BYFPR	Active	Production	DSBGA (YFP) | 28	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51051B
BQ51051BYFPR.A	Active	Production	DSBGA (YFP) | 28	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51051B
BQ51051BYFPR.B	Active	Production	DSBGA (YFP) | 28	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51051B
BQ51051BYFPT	Active	Production	DSBGA (YFP) | 28	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51051B
BQ51051BYFPT.A	Active	Production	DSBGA (YFP) | 28	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51051B
BQ51051BYFPT.B	Active	Production	DSBGA (YFP) | 28	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51051B
BQ51052BYFPR	Active	Production	DSBGA (YFP) | 28	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51052B
BQ51052BYFPR.A	Active	Production	DSBGA (YFP) | 28	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51052B
BQ51052BYFPT	Active	Production	DSBGA (YFP) | 28	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51052B
BQ51052BYFPT.A	Active	Production	DSBGA (YFP) | 28	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	0 to 125	BQ51052B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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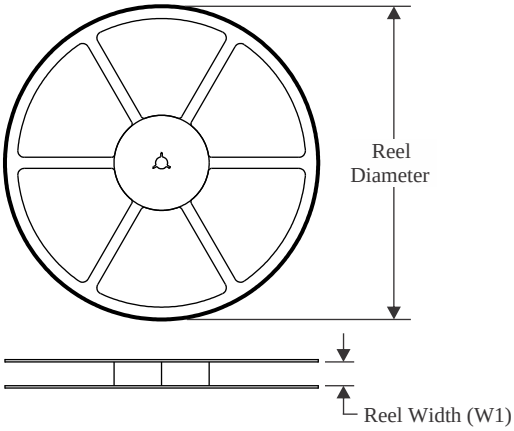
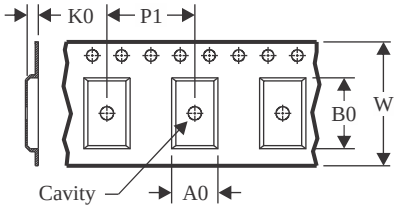
TAPE AND REEL INFORMATION

REEL DIMENSIONS

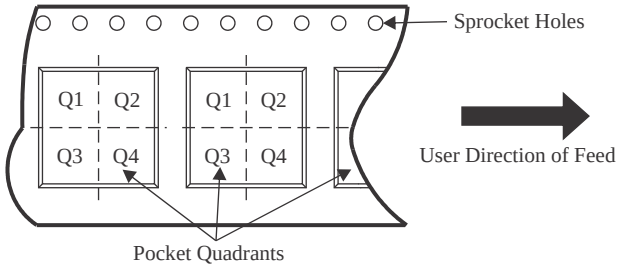


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

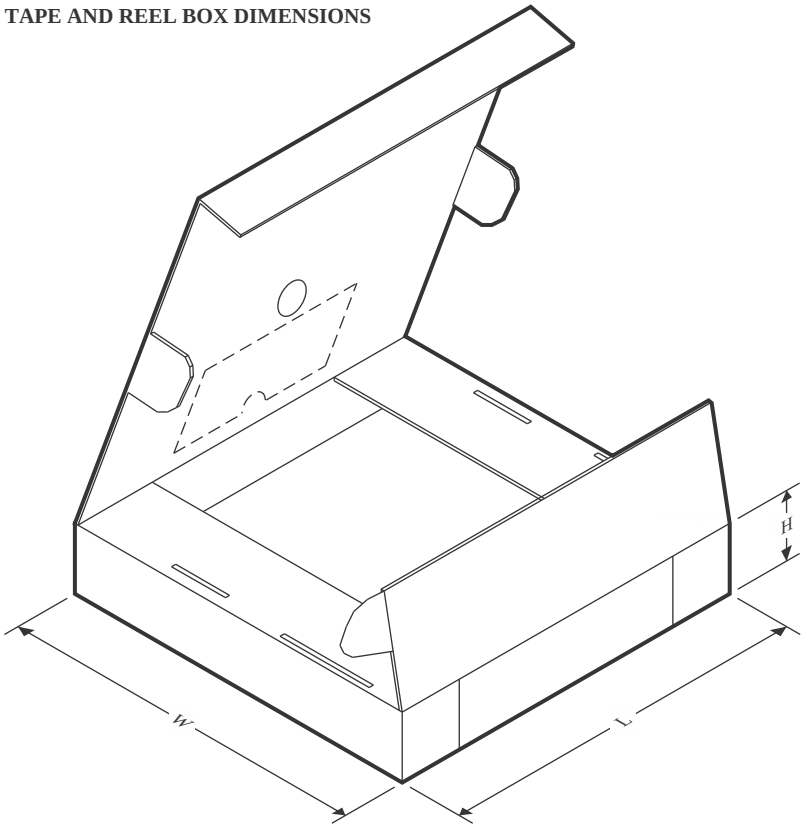
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ51050BRHLR	VQFN	RHL	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
BQ51050BRHLT	VQFN	RHL	20	250	180.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
BQ51050BRHLTG4	VQFN	RHL	20	250	180.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
BQ51050BYFPR	DSBGA	YFP	28	3000	180.0	8.4	2.0	3.13	0.6	4.0	8.0	Q1
BQ51050BYFPT	DSBGA	YFP	28	250	180.0	8.4	2.0	3.13	0.6	4.0	8.0	Q1
BQ51051BRHLR	VQFN	RHL	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
BQ51051BRHLT	VQFN	RHL	20	250	180.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
BQ51051BYFPR	DSBGA	YFP	28	3000	180.0	8.4	2.0	3.13	0.6	4.0	8.0	Q1
BQ51051BYFPT	DSBGA	YFP	28	250	180.0	8.4	2.0	3.13	0.6	4.0	8.0	Q1
BQ51052BYFPR	DSBGA	YFP	28	3000	180.0	8.4	2.0	3.13	0.6	4.0	8.0	Q1
BQ51052BYFPT	DSBGA	YFP	28	250	180.0	8.4	2.0	3.13	0.6	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

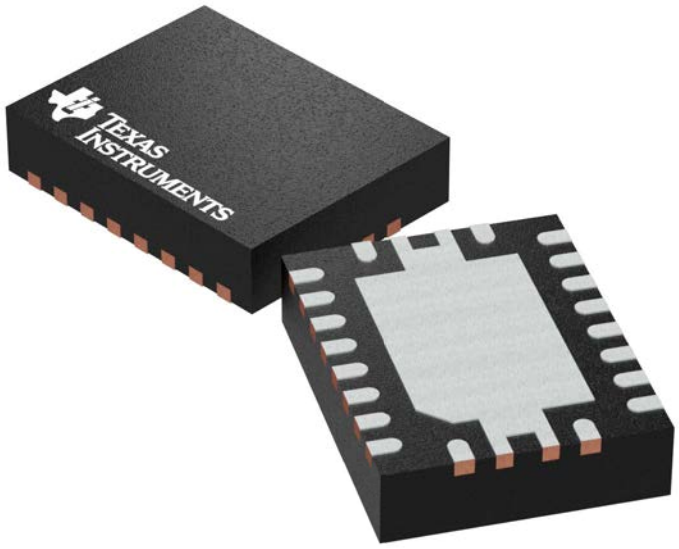
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ51050BRHLR	VQFN	RHL	20	3000	346.0	346.0	33.0
BQ51050BRHLT	VQFN	RHL	20	250	210.0	185.0	35.0
BQ51050BRHLTG4	VQFN	RHL	20	250	210.0	185.0	35.0
BQ51050BYFPR	DSBGA	YFP	28	3000	182.0	182.0	20.0
BQ51050BYFPT	DSBGA	YFP	28	250	182.0	182.0	20.0
BQ51051BRHLR	VQFN	RHL	20	3000	346.0	346.0	33.0
BQ51051BRHLT	VQFN	RHL	20	250	210.0	185.0	35.0
BQ51051BYFPR	DSBGA	YFP	28	3000	182.0	182.0	20.0
BQ51051BYFPT	DSBGA	YFP	28	250	182.0	182.0	20.0
BQ51052BYFPR	DSBGA	YFP	28	3000	182.0	182.0	20.0
BQ51052BYFPT	DSBGA	YFP	28	250	182.0	182.0	20.0

RHL 20

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

3.5 x 4.5 mm, 0.5 mm pitch



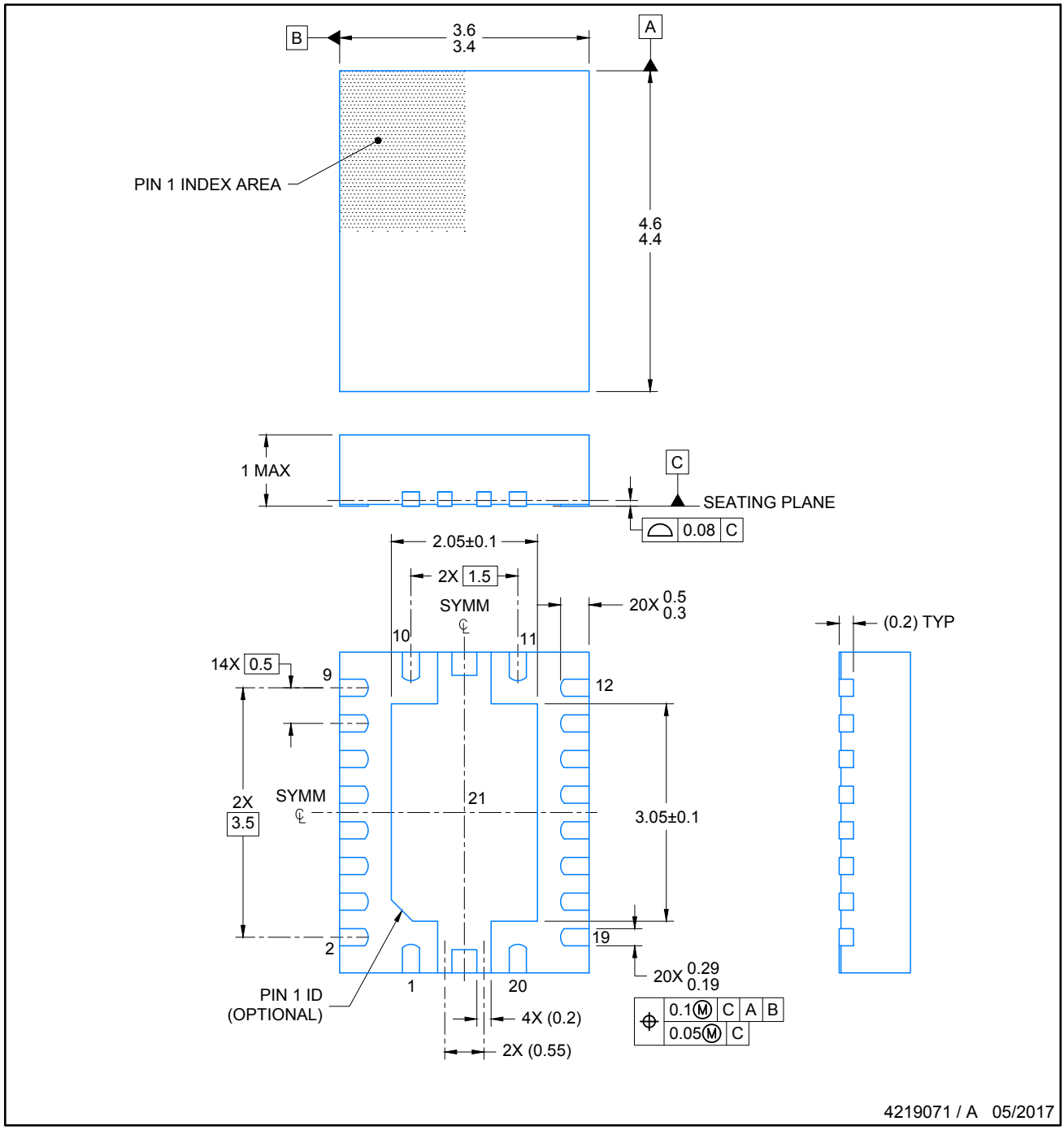
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RHL0020A

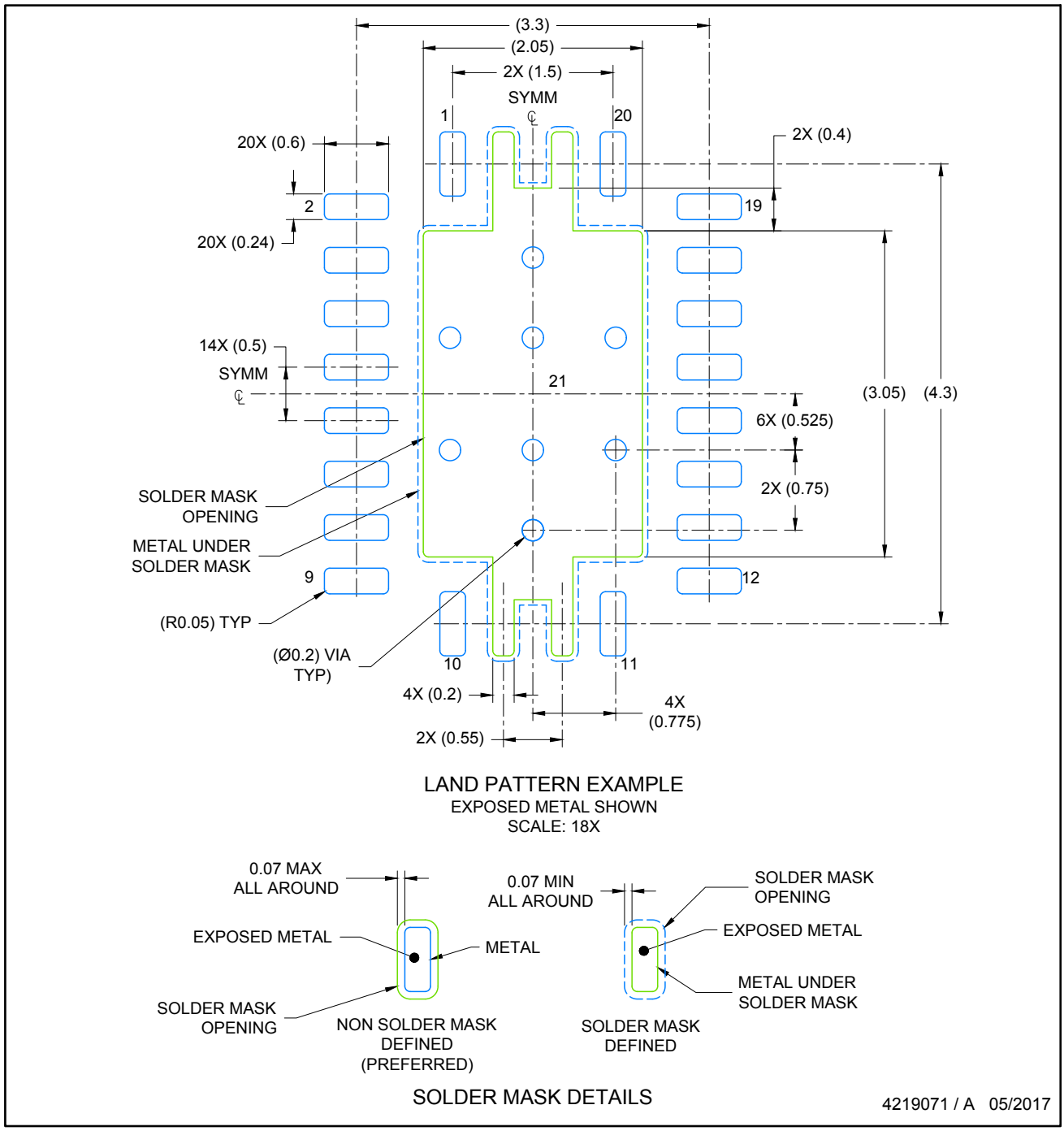
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

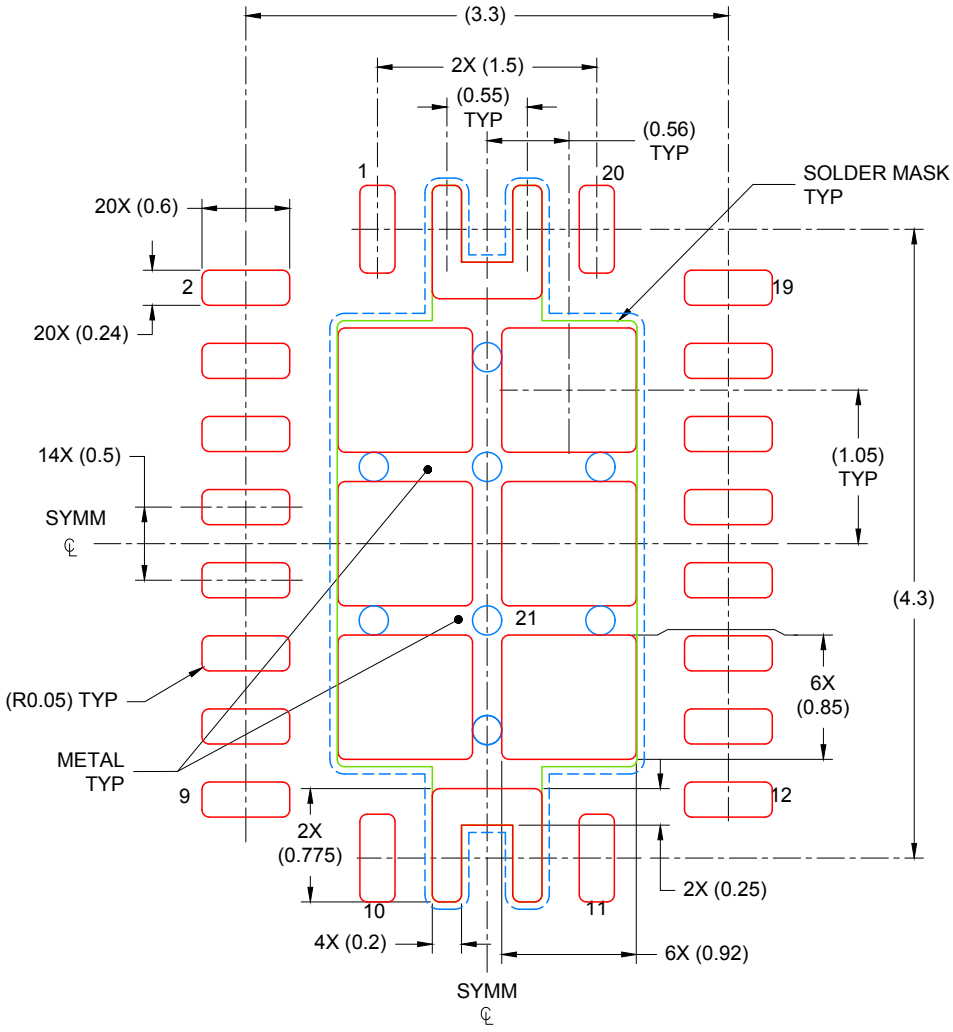


NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to theri locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL

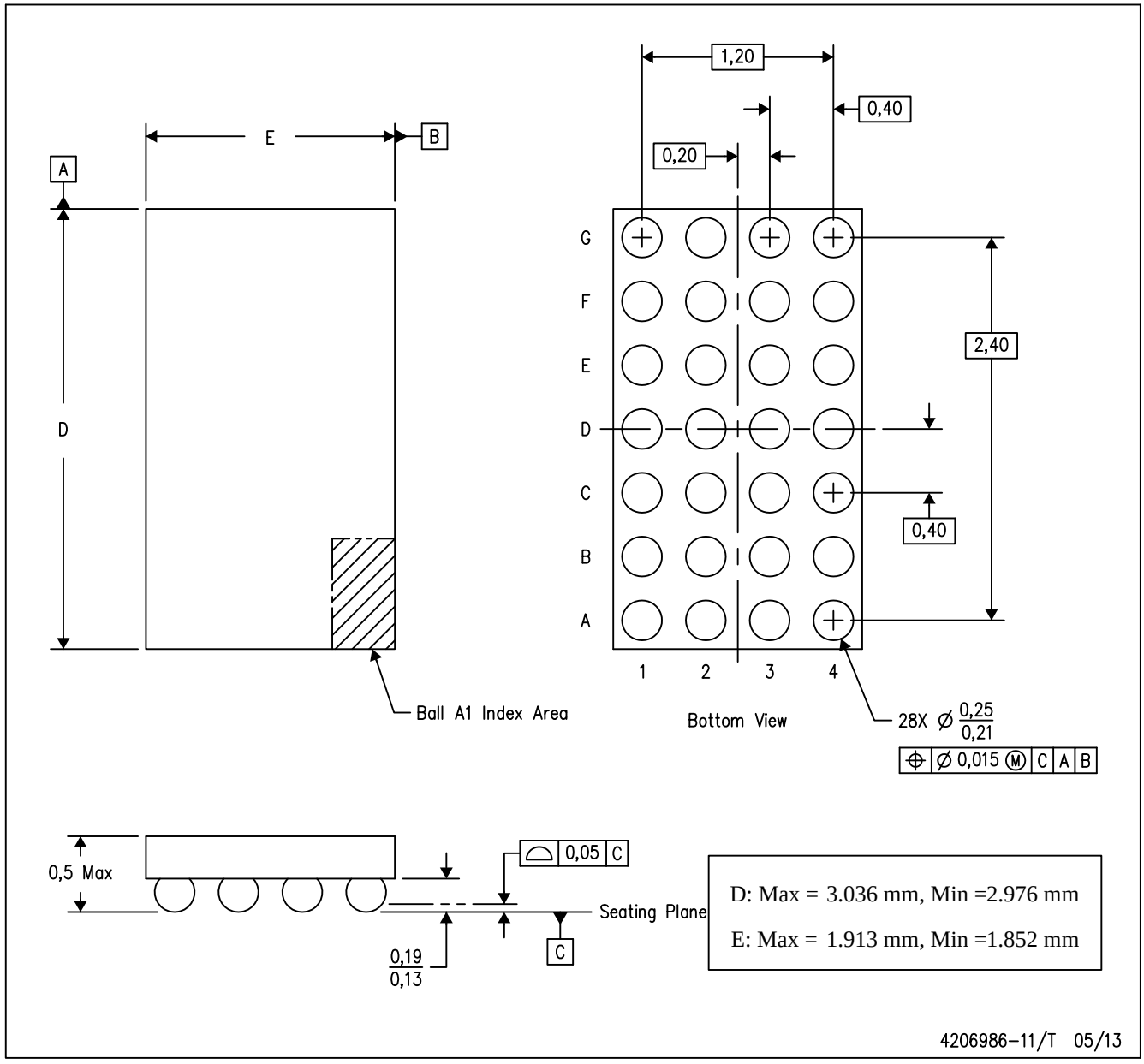
EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 20X

4219071 / A 05/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

YFP (R–XBGA–N28) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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