THE DATASHEET OF

CD74HCT164MT

Data sheet acquired from Harris Semiconductor
SCHS155C

CD54HC164, CD74HC164, CD54HCT164, CD74HCT164

High-Speed CMOS Logic 8-Bit Serial-In/Parallel-Out Shift Register

October 1997 - Revised August 2003

Features

- **Buffered Inputs**
- **Asynchronous Master Reset**
- **Typical f_{MAX} = 60MHz at V_{CC} = 5V, C_L = 15pF, $T_A = 25^oC$**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55^oC to 125^oC**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Description

The ’HC164 and ’HCT164 are 8-bit serial-in parallel-out shift registers with asynchronous reset. Data is shifted on the positive edge of Clock (CP). A LOW on the Master Reset ($\overline{MR}$) pin resets the shift register and all outputs go to the LOW state regardless of the input conditions. Two Serial Data inputs (DS1 and DS2) are provided, either one can be used as a Data Enable control.

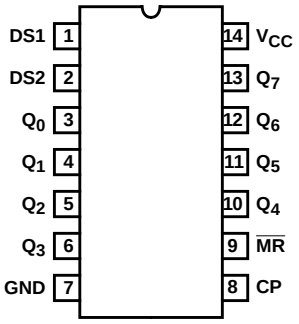
Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE
CD54HC164F3A	-55 to 125	14 Ld CERDIP
CD54HCT164F3A	-55 to 125	14 Ld CERDIP
CD74HC164E	-55 to 125	14 Ld PDIP
CD74HC164M	-55 to 125	14 Ld SOIC
CD74HC164MT	-55 to 125	14 Ld SOIC
CD74HC164M96	-55 to 125	14 Ld SOIC
CD74HCT164E	-55 to 125	14 Ld PDIP
CD74HCT164M	-55 to 125	14 Ld SOIC
CD74HCT164MT	-55 to 125	14 Ld SOIC
CD74HCT164M96	-55 to 125	14 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

Pinout

CD54HC164, CD54HCT164
(CERDIP)
CD74HC164, CD74HCT164
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.
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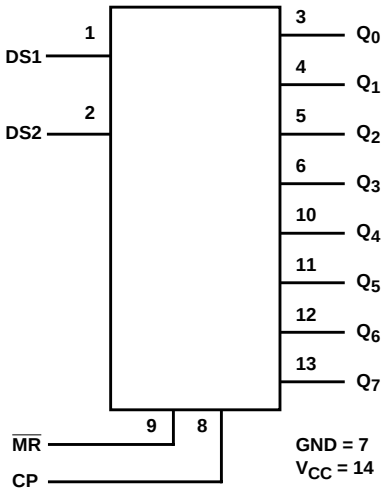
Functional Diagram



TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{MR}$	CP	DS1	DS2	Q_0	Q_1 - Q_7
RESET (CLEAR)	**L**	**X**	**X**	**X**	**L**	**L - L**
Shift	H	↑	l	l	L	q_0 - q_6
	H	↑	l	h	L	q_0 - q_6
	H	↑	h	l	L	q_0 - q_6
	H	↑	h	h	H	q_0 - q_6

H= High Voltage Level.
h= High Voltage Level One Set-up Time Prior To The Low-to-high Clock Transition.
l= Low Voltage Level One Set-up Time Prior To The Low-to-high Clock Transition.
L= Low Voltage Level.
X= Don't Care.
↑= Transition from Low to High Level.
q_n= Lower Case Letters Indicate The State Of the Reference Input Clock Transition.

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} or I_{GND} . . . . . ±50mA

Operating Conditions

Temperature Range (T_A) . . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
E (PDIP) Package	80
M (SOIC) Package	86

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} to GND	0	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 2)	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE:

2. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
Date Shift-In (1, 2)	0.3
$\overline{MR}$	0.9
Clock	0.7

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g. 360µA max at 25°C.

Prerequisite For Switching Function

PARAMETER	SYMBOL	V_{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
HC TYPES									
Maximum Clock Frequency	f_{MAX}	2	6	-	5	-	4	-	MHz
		4.5	30	-	24	-	20	-	MHz
		6	35	-	28	-	24	-	MHz
$\overline{MR}$ Pulse Width	t_w	2	60	-	75	-	90	-	ns
		4.5	12	-	15	-	18	-	ns
		6	10	-	13	-	15	-	ns

Prerequisite For Switching Function (Continued)

PARAMETER	SYMBOL	V_{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
CP Pulse Width	t_W	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns
Set-up Time	t_{SU}	2	60	-	75	-	90	-	ns
		4.5	12	-	15	-	18	-	ns
		6	10	-	13	-	15	-	ns
Hold Time	t_H	2	4	-	4	-	4	-	ns
		4.5	4	-	4	-	4	-	ns
		6	4	-	4	-	4	-	ns
$\overline{MR}$ to Clock, Removal Time	t_{REM}	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns
HCT TYPES									
Maximum Clock Frequency	f_{MAX}	4.5	27	-	22	-	18	-	MHz
$\overline{MR}$ Pulse Width	t_w	6	18	-	23	-	27	-	ns
CP Pulse Width	t_w	4.5	18	-	23	-	27	-	ns
Set-up Time	t_{SU}	6	12	-	15	-	18	-	ns
Hold Time	t_H	4.5	4	-	4	-	4	-	ns
$\overline{MR}$ to Clock, Removal Time	t_{REM}	6	16	-	20	-	24	-	ns

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
HC TYPES								
Propagation Delay, CP to Q_n	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	170	212	255	ns
			4.5	-	34	43	51	ns
		C_L = 15pF	5	14	-	-	-	ns
		C_L = 50pF	6	-	29	36	43	ns
$\overline{MR}$ to Q_n	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	140	175	210	ns
			4.5	-	28	35	42	ns
		C_L = 15pF	5	11	-	-	-	ns
		C_L = 50pF	6	-	24	30	36	ns
Output Transition Times	t_{TLH}, t_{THL}	C_L = 50pF	2	-	75	-	110	ns
			4.5	-	15	-	22	ns
			6	-	13	-	19	ns
Maximum Clock Frequency	f_{MAX}	C_L = 15pF	5	60	-	-	-	MHz
Input Capacitance	C_{IN}	-	-	-	10	10	10	pF

Switching Specifications Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	-	5	47	-	-	-	pF
HCT TYPES								
Propagation Delay, CP to Q_n	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	36	45	54	ns
		C_L = 15pF	5	15	-	-	-	ns
$\overline{MR}$ to Q_n	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	38	46	57	ns
		C_L = 15pF	5	16	-	-	-	ns
Output Transition Times	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	15	19	22	ns
Input Capacitance	C_{IN}	-	-	-	-	-	-	pF
Maximum Clock Frequency	f_{MAX}	C_L = 15pF	-	54	-	-	-	MHz
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	-	5	49	10	10	10	pF

NOTES:

3. C_{PD} is used to determine the dynamic power consumption, per device.
4. $P_D = V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 + f_O)$ where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms

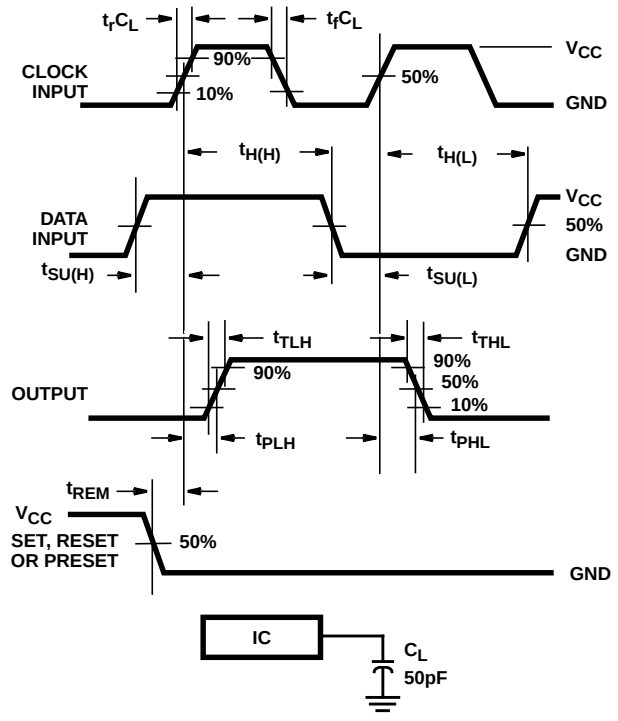


FIGURE 1. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

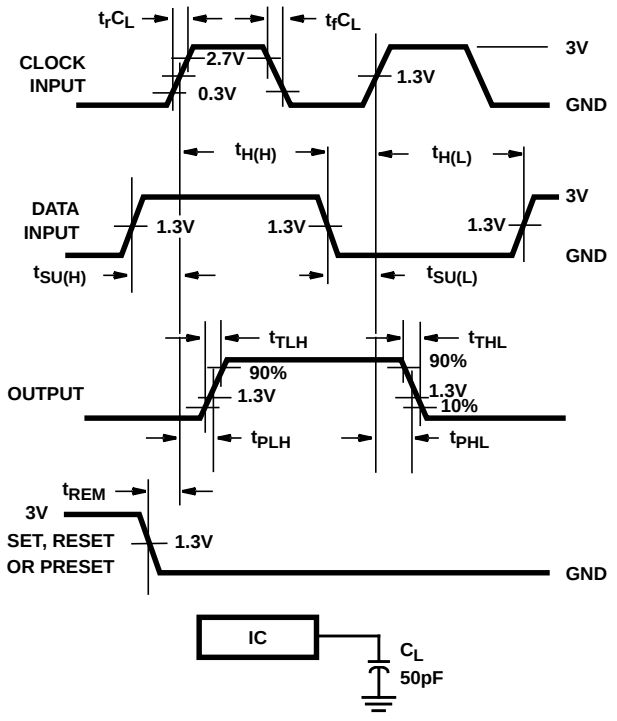


FIGURE 2. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8970401CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8970401CA CD54HCT164F3A	Samples
CD54HC164F	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54HC164F	Samples
CD54HC164F3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8416201CA CD54HC164F3A	Samples
CD54HCT164F3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8970401CA CD54HCT164F3A	Samples
CD74HC164E	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC164E	Samples
CD74HC164M	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC164M	Samples
CD74HC164M96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC164M	Samples
CD74HC164M96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC164M	Samples
CD74HC164ME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC164M	Samples
CD74HC164MG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC164M	Samples
CD74HC164MT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC164M	Samples
CD74HCT164E	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT164E	Samples
CD74HCT164M	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT164M	Samples
CD74HCT164M96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT164M	Samples
CD74HCT164M96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT164M	Samples
CD74HCT164MT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT164M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD54HC164, CD54HCT164, CD74HC164, CD74HCT164 :

- Catalog: CD74HC164, CD74HCT164
- Military: CD54HC164, CD54HCT164

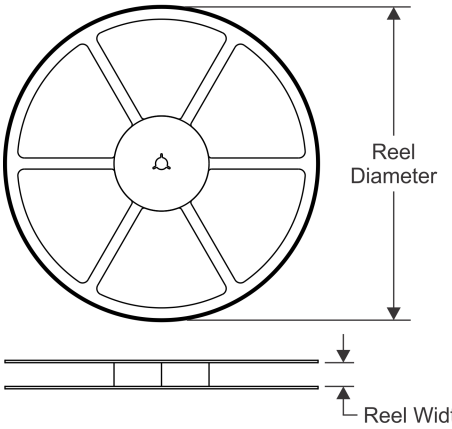
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

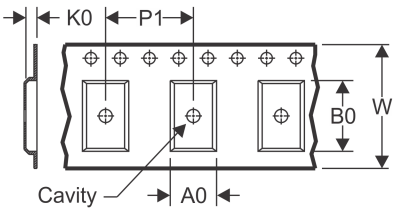
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

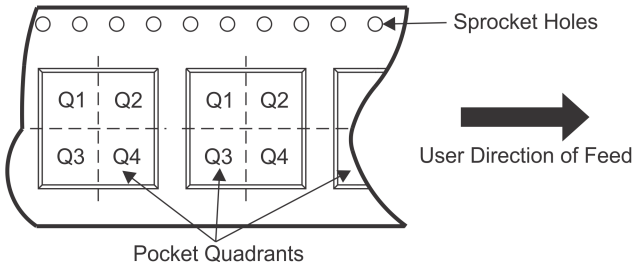


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

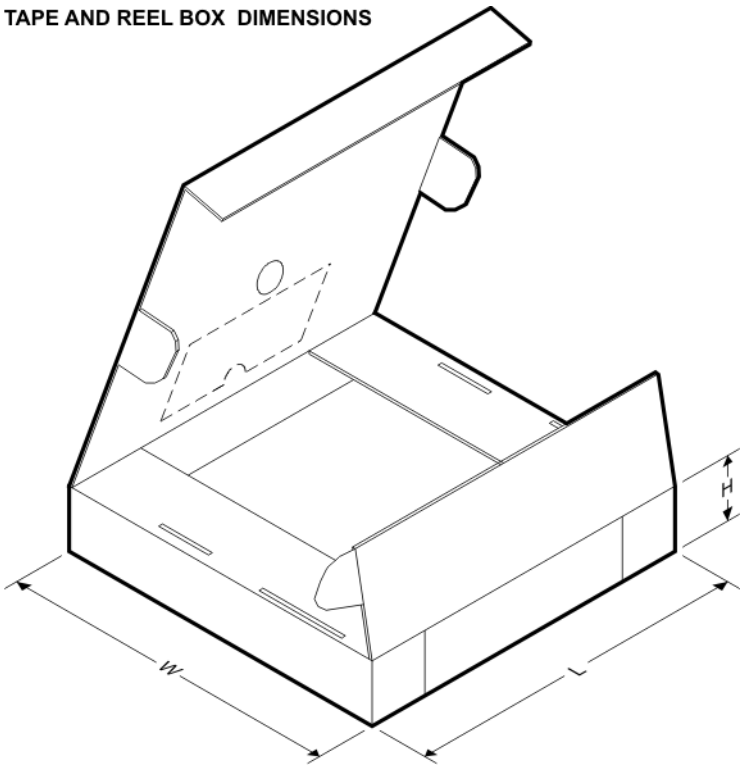
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC164M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC164MT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HCT164M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HCT164MT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



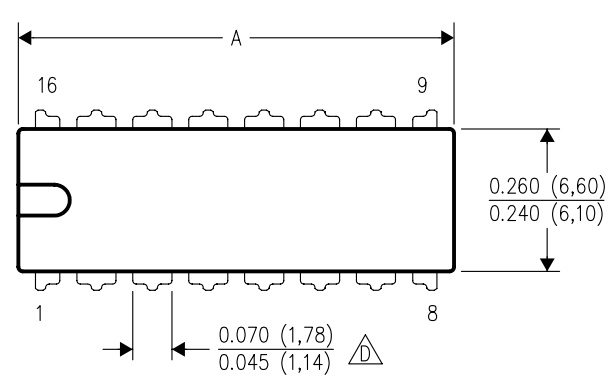
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC164M96	SOIC	D	14	2500	367.0	367.0	38.0
CD74HC164MT	SOIC	D	14	250	210.0	185.0	35.0
CD74HCT164M96	SOIC	D	14	2500	367.0	367.0	38.0
CD74HCT164MT	SOIC	D	14	250	210.0	185.0	35.0

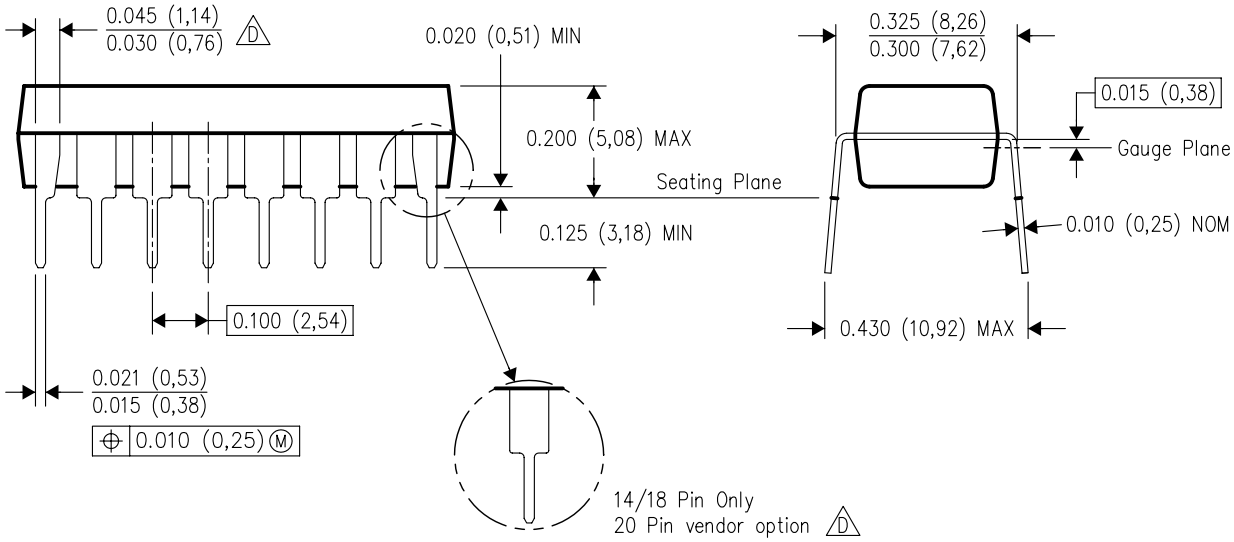
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



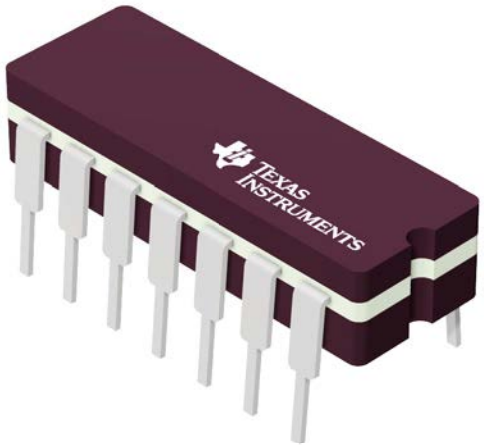
4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

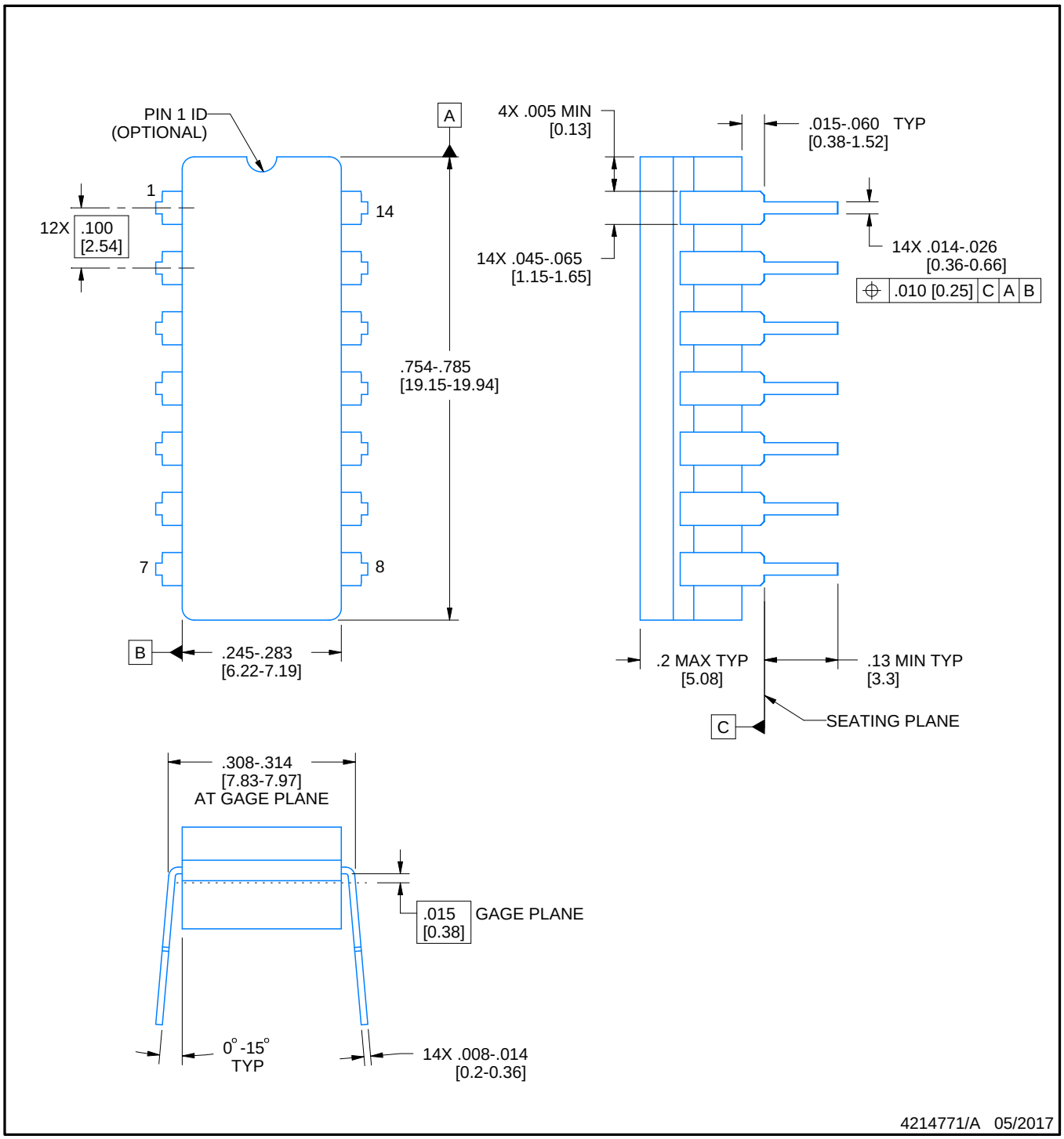
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

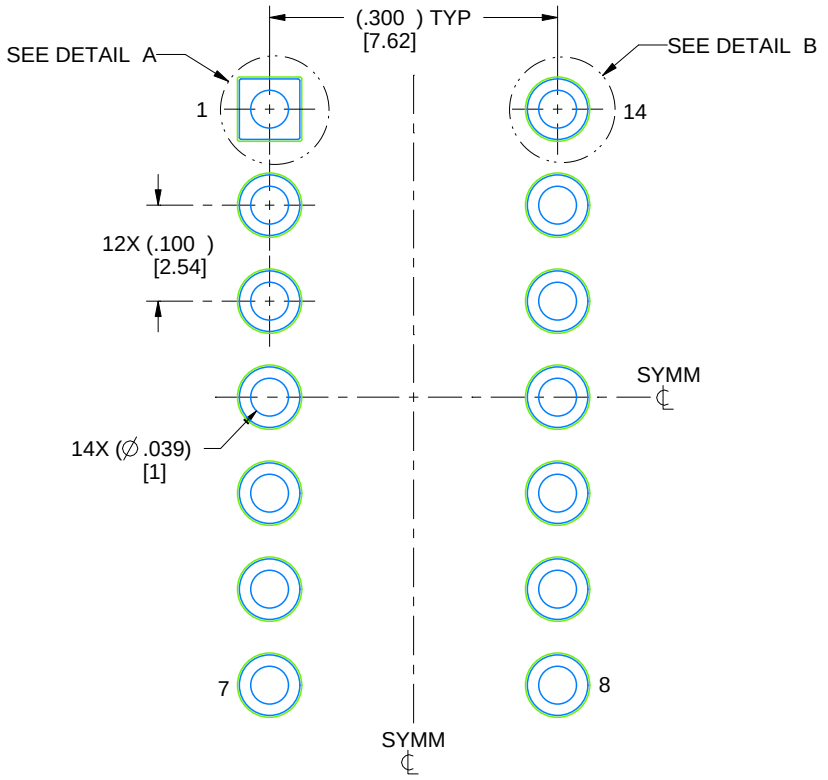
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

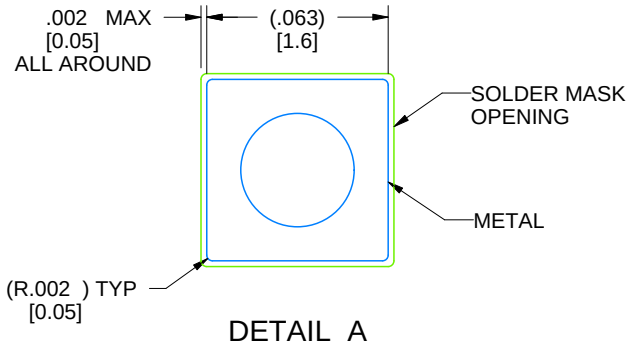
J0014A

CDIP - 5.08 mm max height

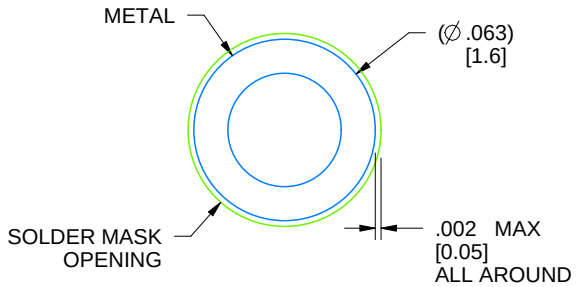
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



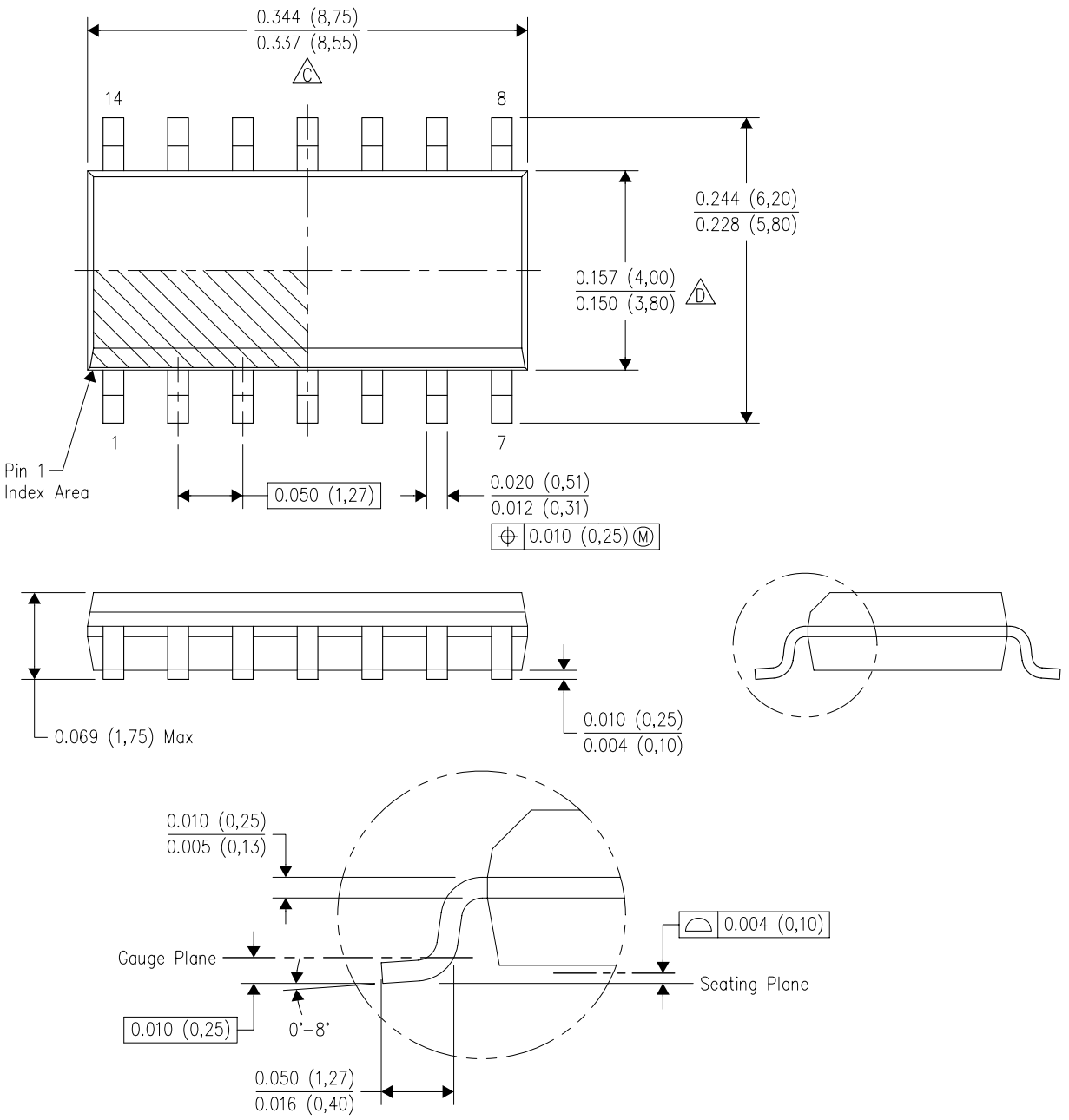
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

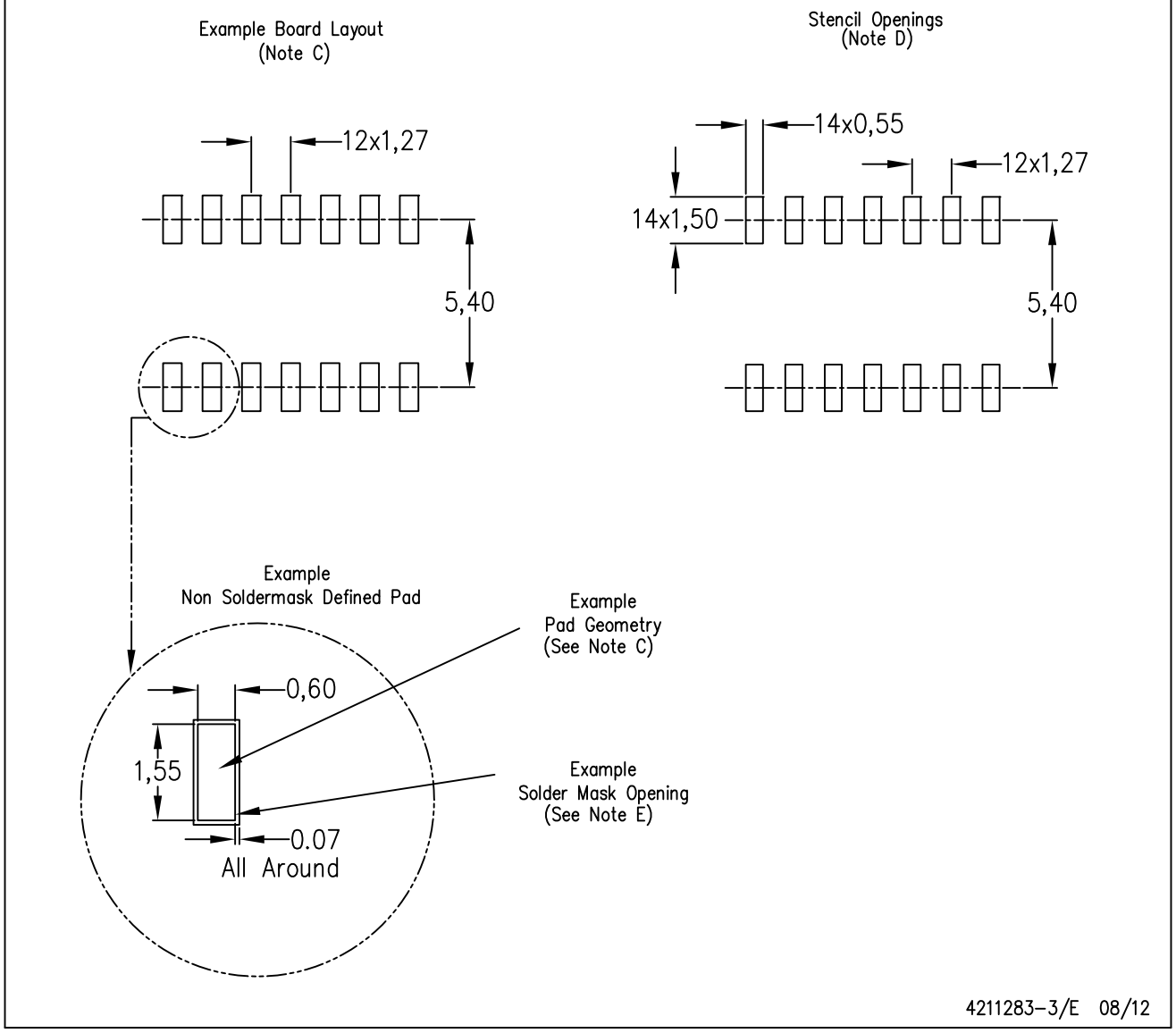
4214771/A 05/2017

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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