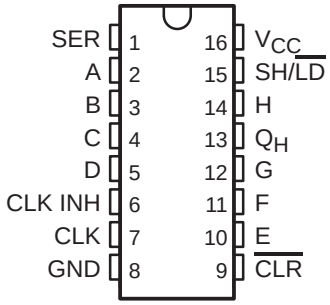
THE DATASHEET OF

SN74ALS166DR

www.win-source.net 0086-755-83957316

- **Synchronous Load**
- **Direct Overriding Clear**
- **Parallel-to-Serial Conversion**
- **Package Options Include Plastic Small-Outline (D) and Shrink Small-Outline (DB) Packages and Standard Plastic (N) DIP**

D, DB, OR N PACKAGE
(TOP VIEW)



description

The SN74ALS166 parallel-load 8-bit shift register is compatible with most other TTL logic families. All inputs are buffered to lower the drive requirements. Input clamping diodes minimize switching transients and simplify system design.

These parallel-in or serial-in, serial-out registers have a complexity of 77 equivalent gates on the chip. They feature gated clocks (CLK and CLK INH) inputs and an overriding clear ($\overline{CLR}$) input. The parallel-in or serial-in modes are established by the shift/load (SH/$\overline{LD}$) input. When high, SH/$\overline{LD}$ enables the serial data (SER) input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data (A–H) inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive-NOR gate, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free running and the register can be stopped on command with the clock input. CLK INH should be changed to the high level only when CLK is high. The buffered $\overline{CLR}$ overrides all other inputs, including CLK, and sets all flip-flops to zero.

The SN74ALS166 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS						INTERNAL OUTPUTS		OUTPUT
$\overline{CLR}$	SH/$\overline{LD}$	CLK INH	CLK	SER	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

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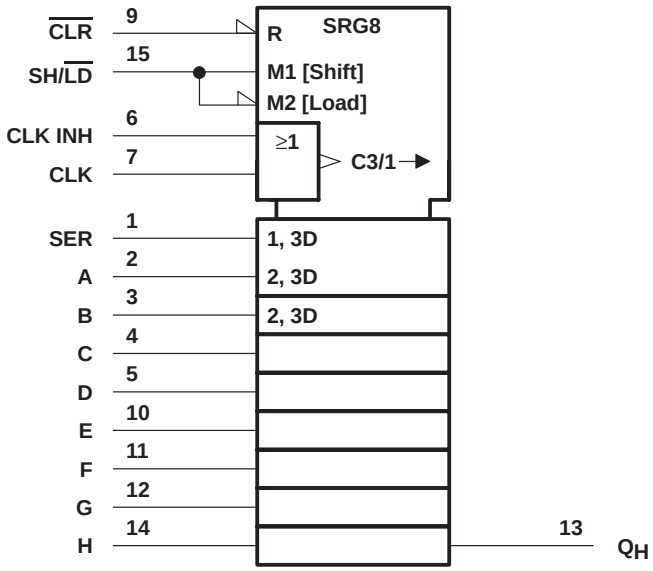
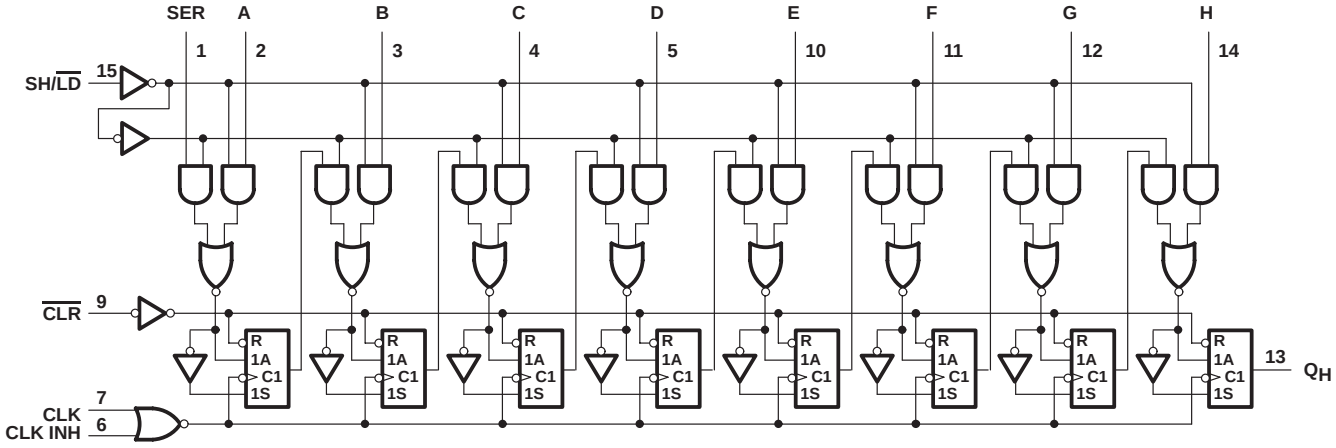
logic symbol†

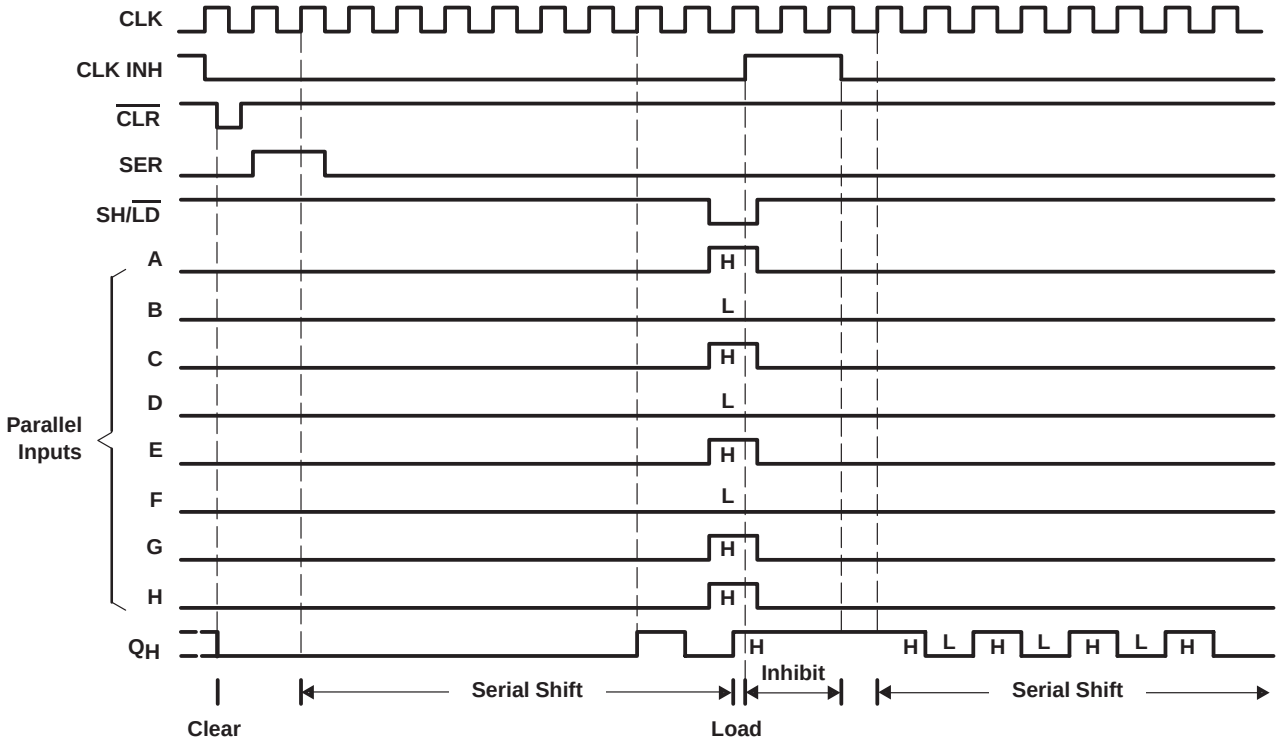


† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



typical clear, shift, load, inhibit, and shift sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I . . . . . –0.5 V to 7 V
Package thermal impedance, θ_{JA} (see Note 1): D package . . . . . 73°C/W
DB package . . . . . 82°C/W
N package . . . . . 67°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –0.4 mA	V_{CC}–2			V
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4	V
		I_{OL} = 8 mA		0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 2		14	24	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 2: With 4.5 V applied to SER and all other inputs, except the clock, grounded, I_{CC} is measured after a clock transition from 0 V to 4.5 V.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

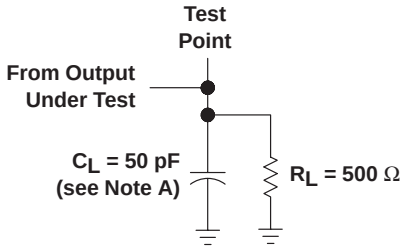
			MIN	MAX	UNIT
f_{clock}	Clock frequency			45	MHz
t_w	Pulse duration	$\overline{CLR}$ low	9		ns
		CLK high	10		
		CLK low	10		
t_{su}	Setup time before CLK↑	SH/$\overline{LD}$	16		ns
		Data	7		
		$\overline{CLR}$ inactive	11		
t_h	Hold time, data after CLK↑		3		ns

switching characteristics over recommended operating conditions (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
f_{max}			45			MHz
t_{PHL}	$\overline{CLR}$	Q_H	4	9	14	ns
t_{PLH}	CLK	Q_H	2	7	12	ns
t_{PHL}			2	9	13	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

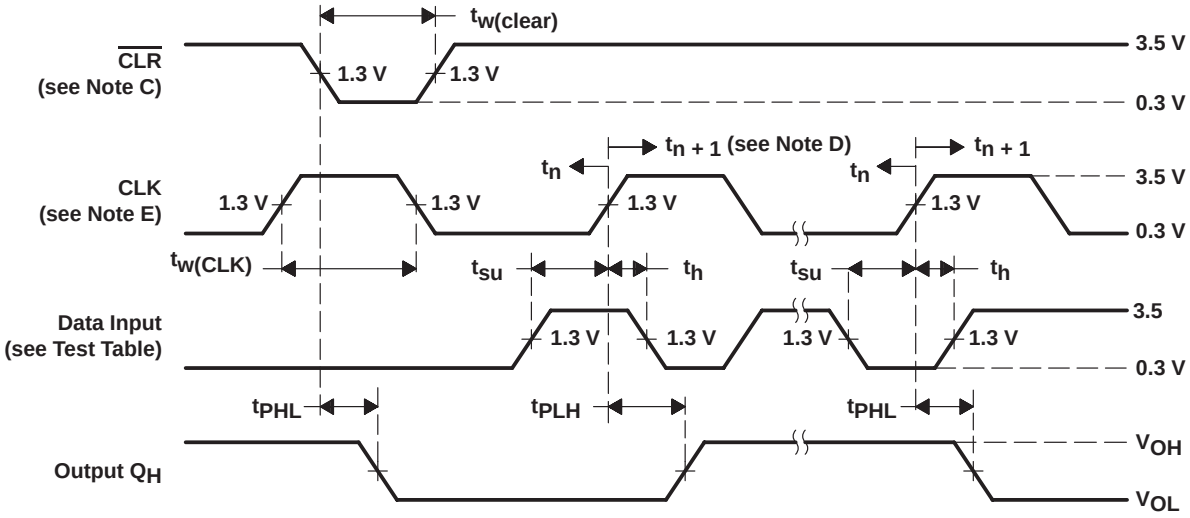
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUT UNDER TEST

TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	SH/$\overline{LD}$	OUTPUT TESTED (see Note B)
H	0 V	Q_H at t_{n+1}
Serial input	4.5 V	Q_H at t_{n+1}



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+8} with a functional test.
C. A clear pulse is applied prior to each test.
D. t_n = bit time before clocking transition, t_{n+1} = bit time after one clocking transition, and t_{n+8} = bit time after eight clocking transitions.
E. The clock pulse has the following characteristics: $t_{w(clock)} \leq 20$ ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{w(clear)} \leq 20$ ns.
F. All pulse generators have the following characteristics: $Z_O \approx 50\ \Omega$; $t_r = t_f = 2$ ns. Duty cycle = 50% when testing f_{max}.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALS166DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	G166	Samples
SN74ALS166DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS166	Samples
SN74ALS166N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS166N	Samples
SN74ALS166NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS166	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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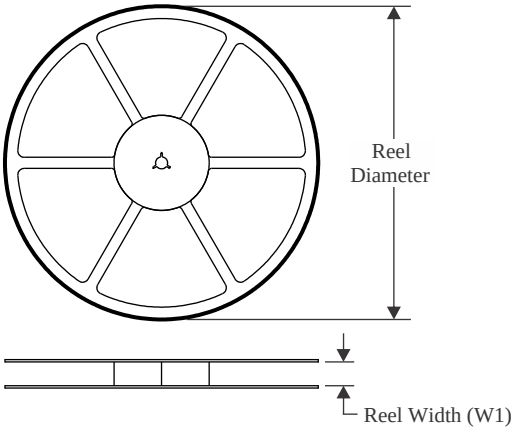
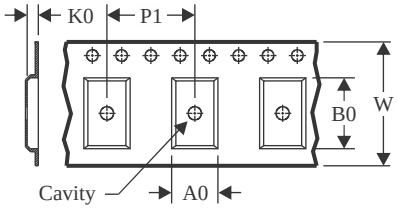
TAPE AND REEL INFORMATION

REEL DIMENSIONS

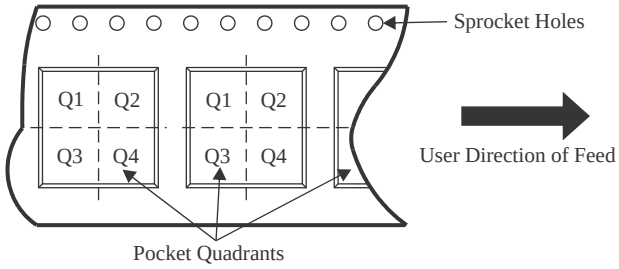


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

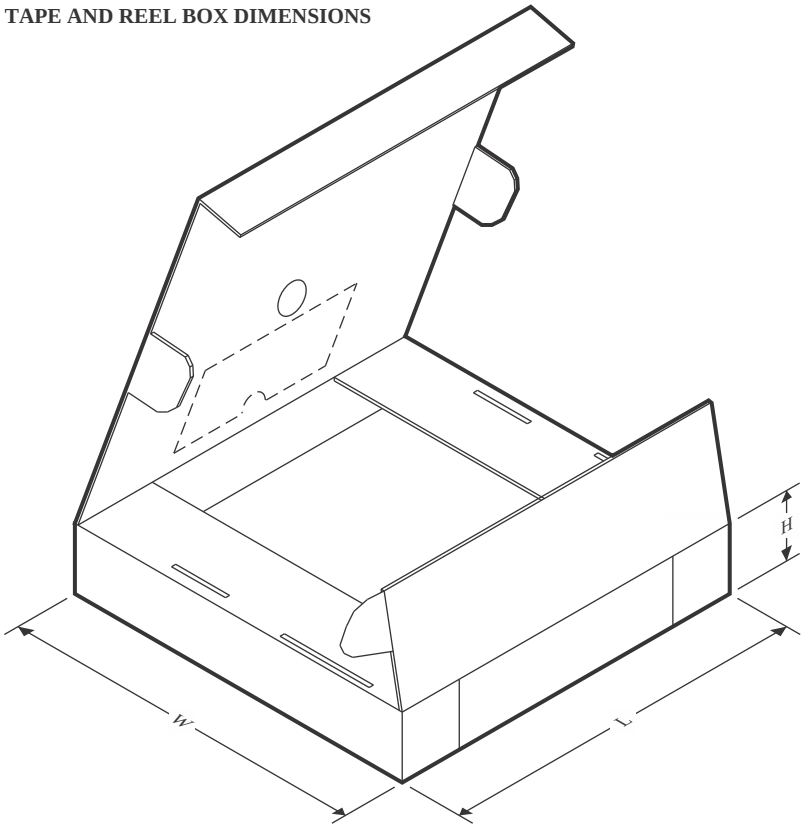
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS166DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74ALS166DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74ALS166NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

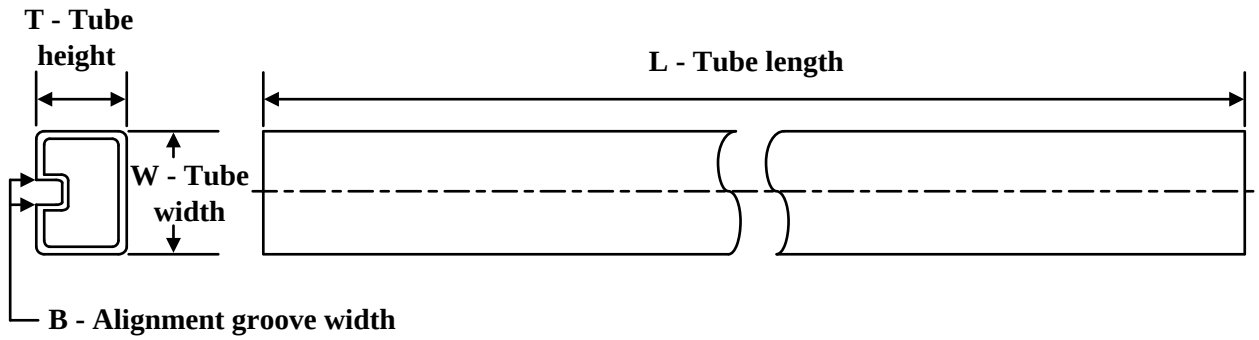
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

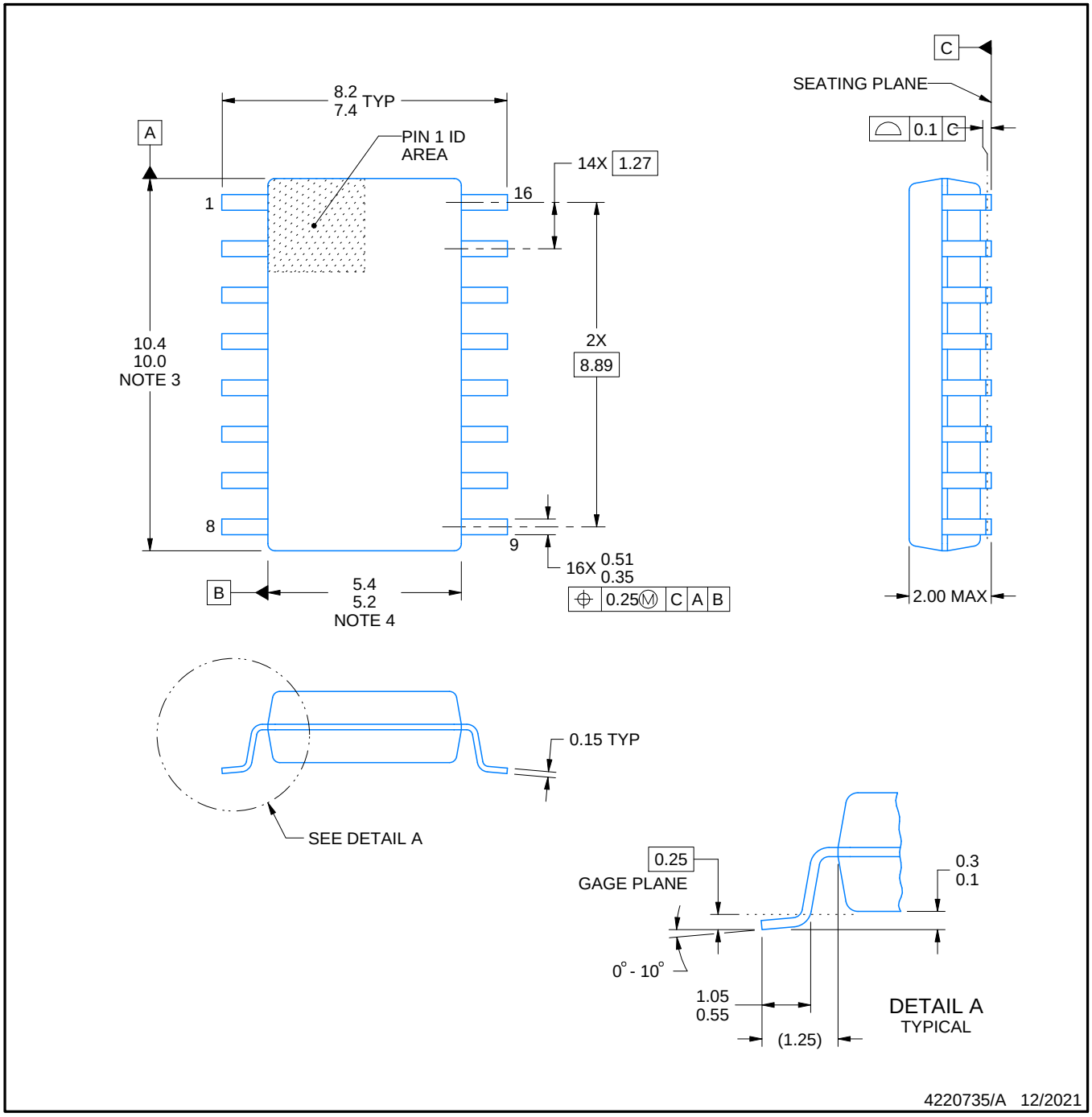
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS166DBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74ALS166DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74ALS166NSR	SO	NS	16	2000	356.0	356.0	35.0

TUBE



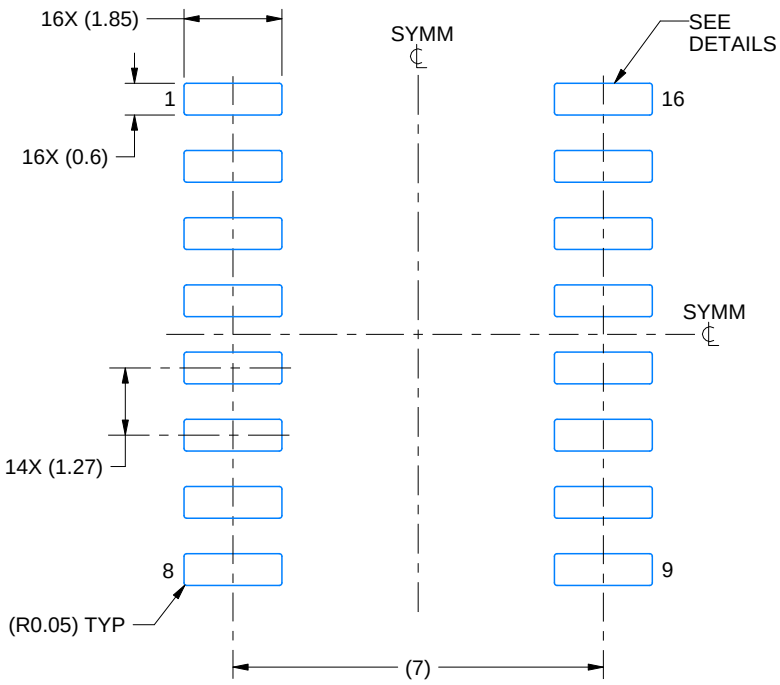
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74ALS166N	N	PDIP	16	25	506	13.97	11230	4.32
SN74ALS166N	N	PDIP	16	25	506	13.97	11230	4.32

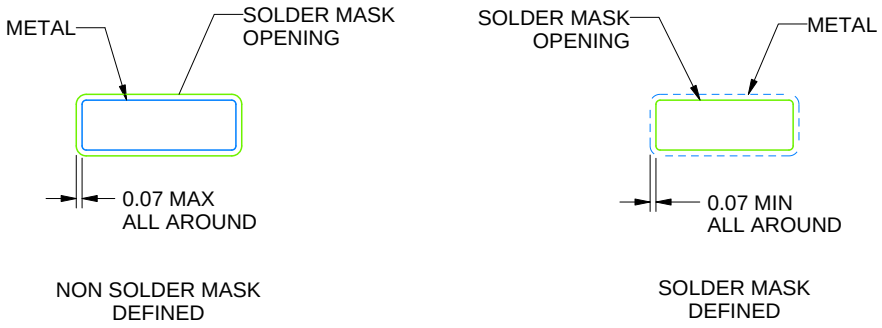


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X

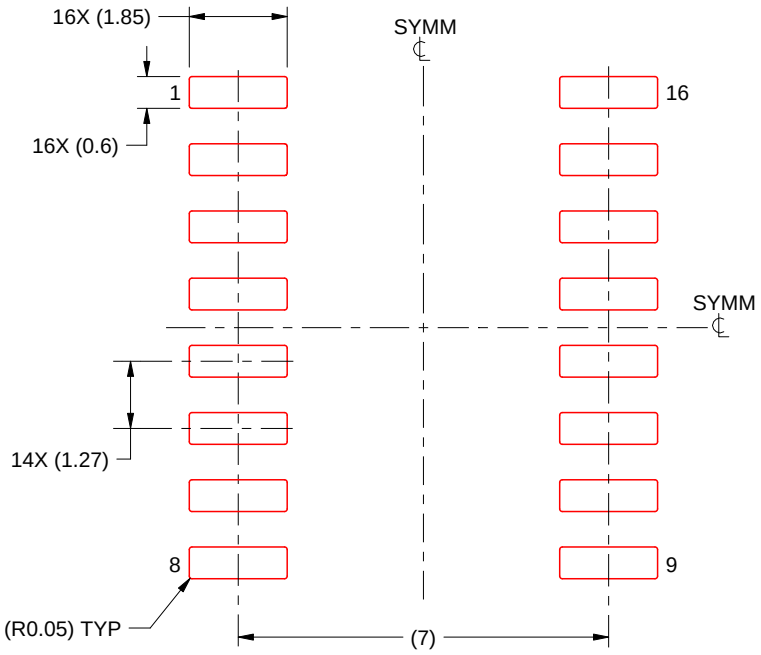


SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



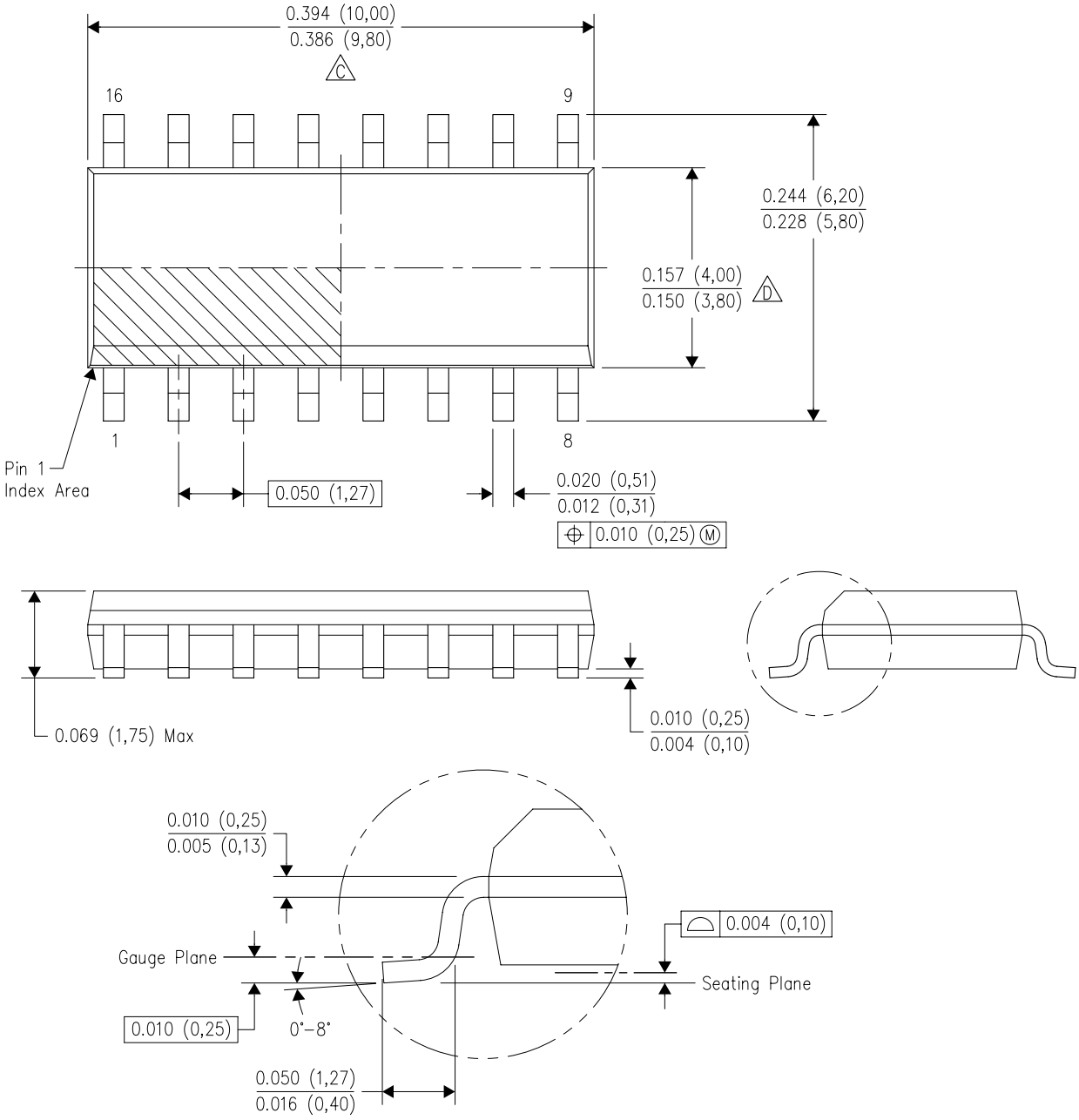
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

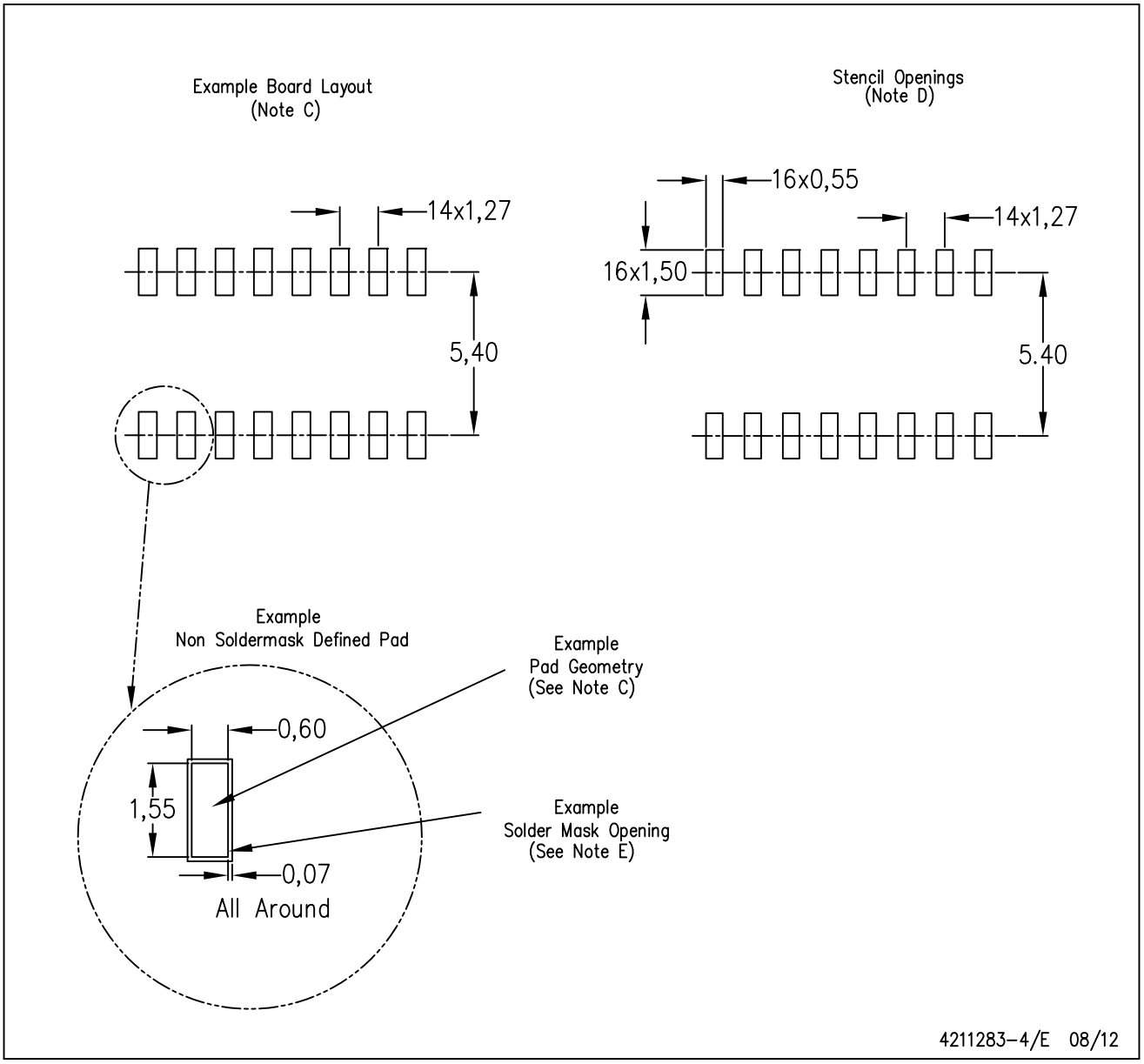
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



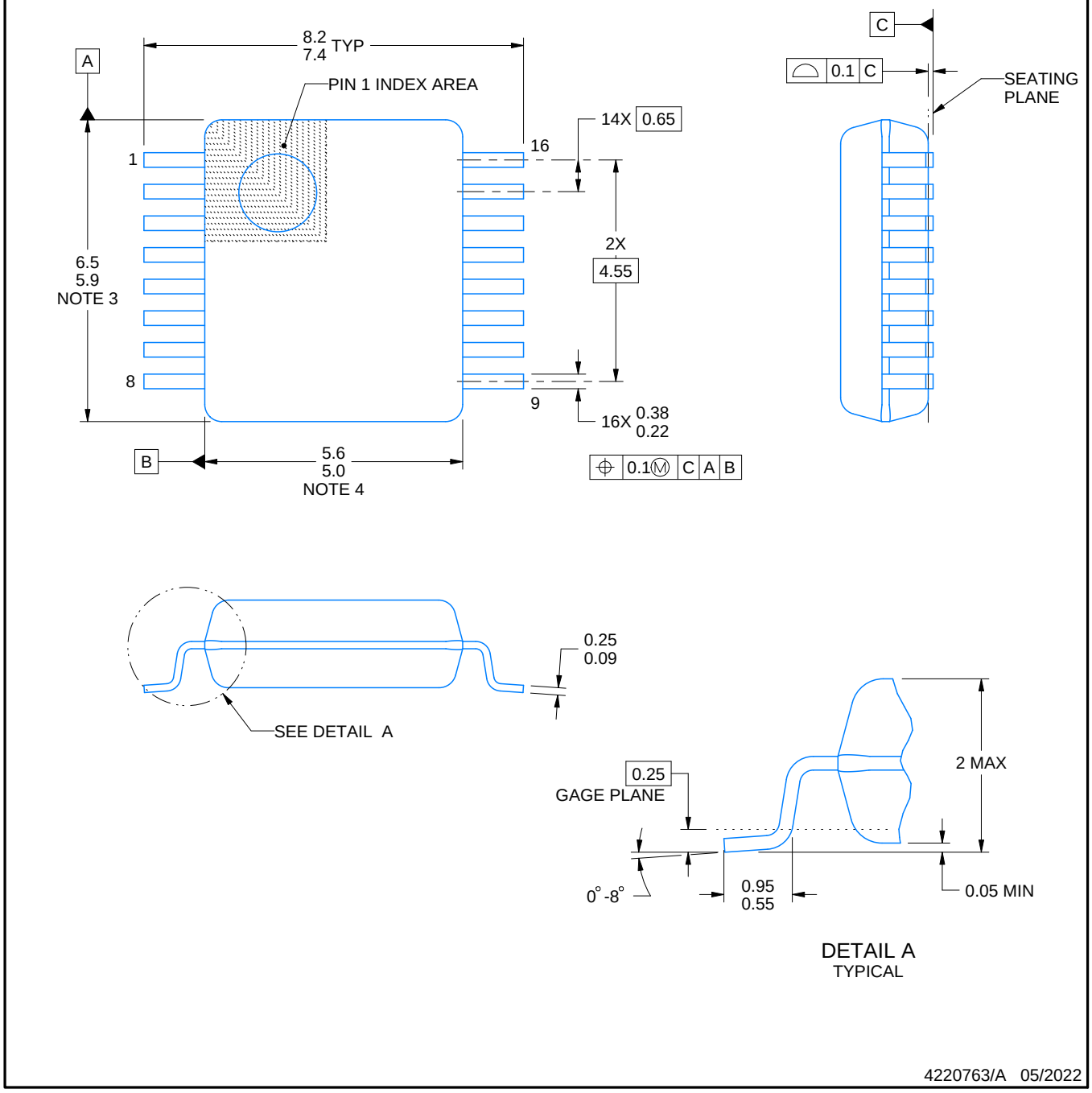
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

DB0016A

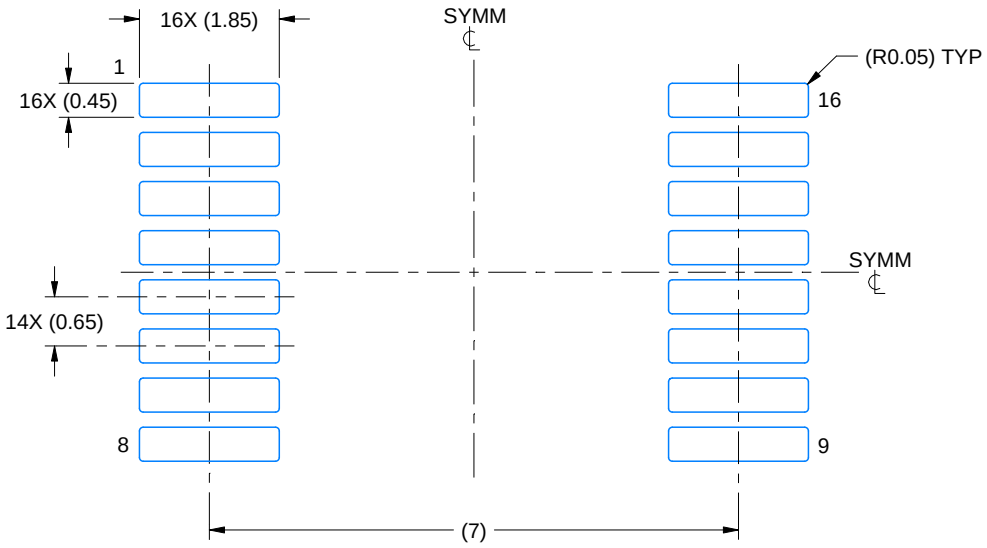
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

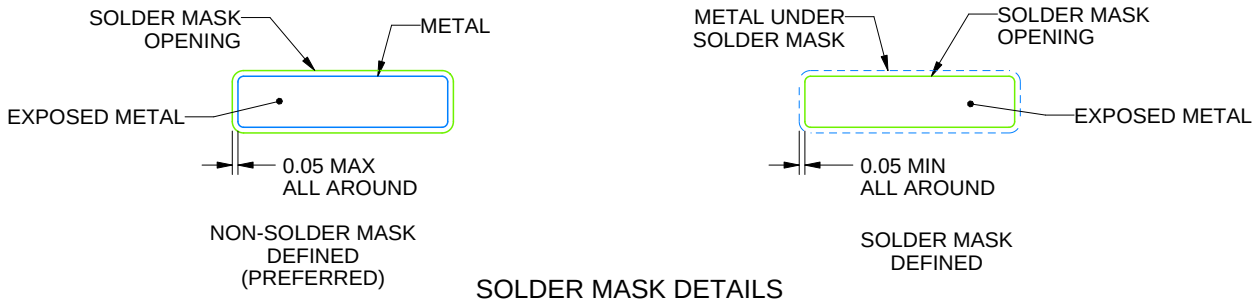


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

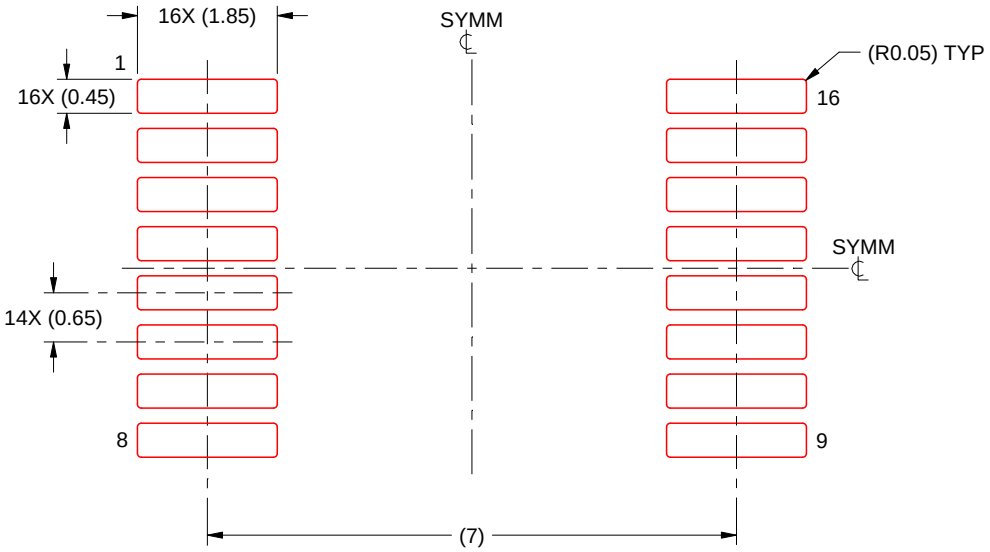
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

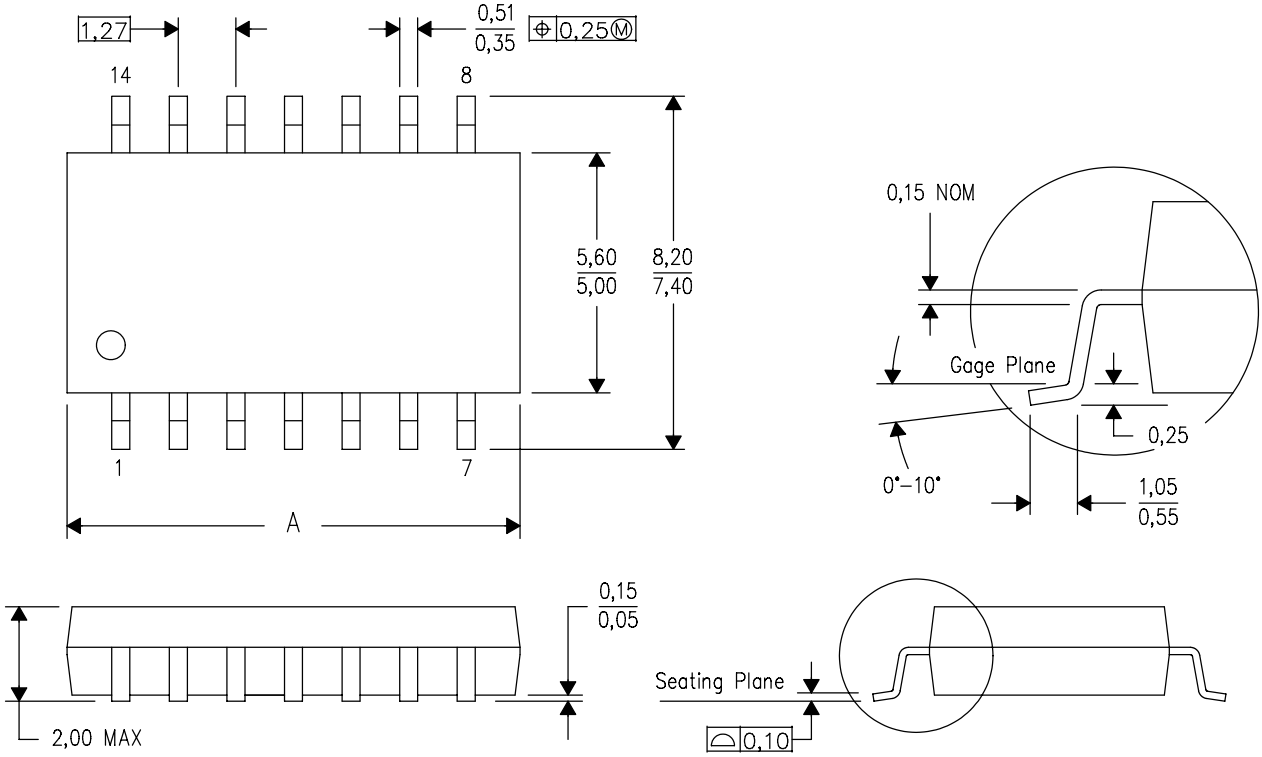
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

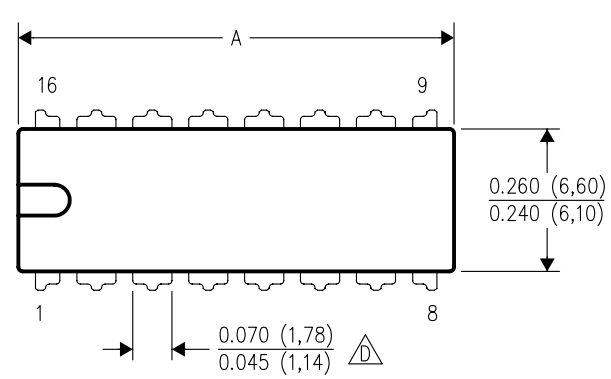
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

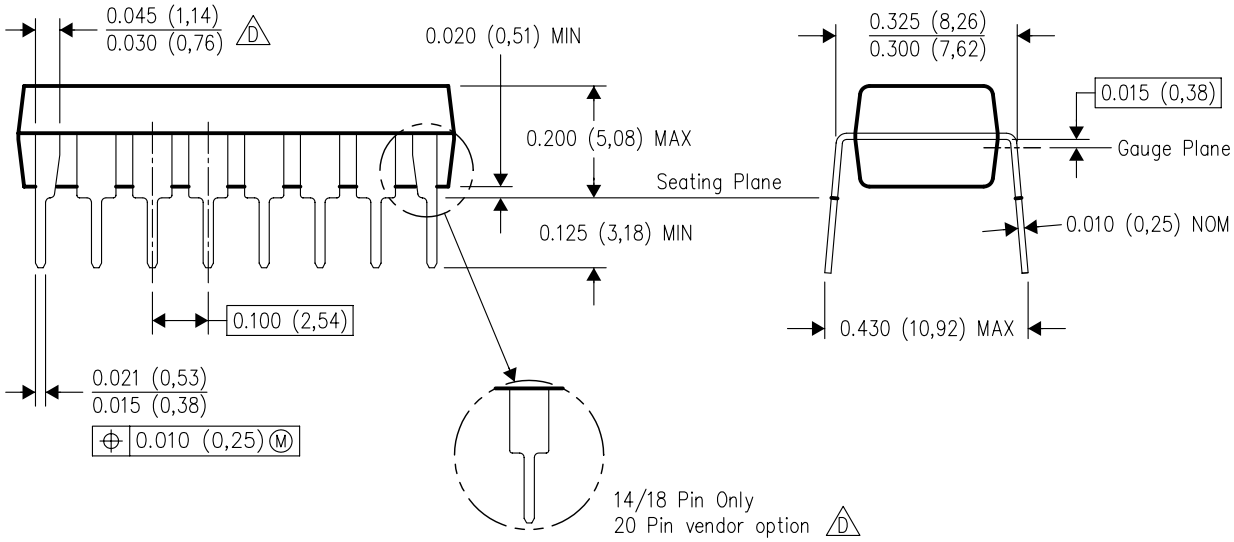
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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