WINSOURCE ELECTRONICS

THE DATASHEET OF

SN74LV165APW

SNx4LV165A Parallel-Load 8-Bit Shift Registers

1 Features

- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 10.5 ns at 5 V
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- IP Routers
- Enterprise Switches
- Access Control and Security: Access Keypads and Biometrics
- Smart Meters: Power Line Communication

3 Description

The ’LV165A devices are parallel-load, 8-bit shift registers designed for 2-V to 5.5-V V_{CC} operation.

When the devices are clocked, data is shifted toward the serial output Q_H. Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the shift/load (SH/$\overline{LD}$) input. The ’LV165A devices feature a clock-inhibit function and a complemented serial output, $\overline{Q}_H$.

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while SH/$\overline{LD}$ is held high and clock inhibit (CLK INH) is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH accomplishes clocking, CLK INH must be changed to the high level only while CLK is high. Parallel loading is inhibited when SH/$\overline{LD}$ is held high. The parallel inputs to the register are enabled while SH/$\overline{LD}$ is held low, independently of the levels of CLK, CLK INH, or SER.

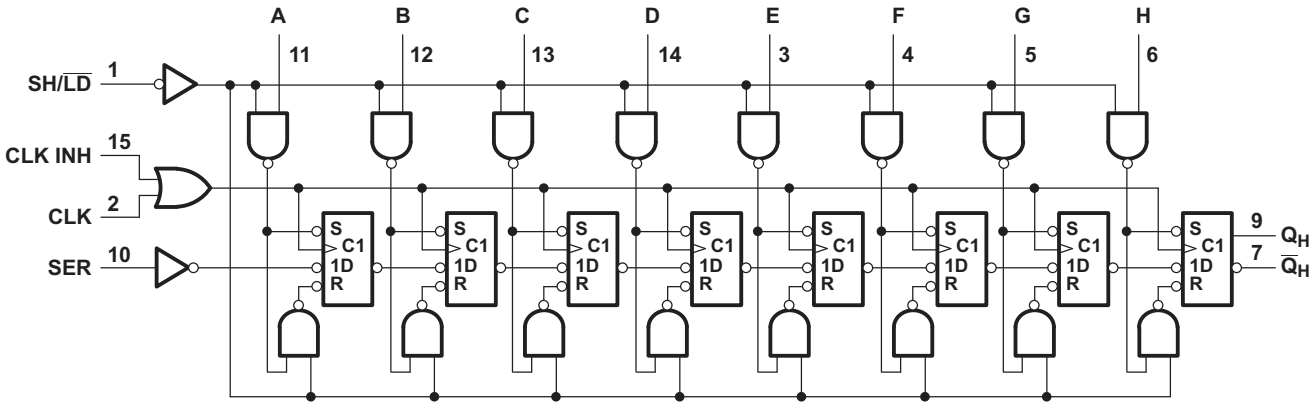
These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SNx4LV165AD	SOIC (16)	9.90 mm × 3.91 mm
SNx4LV165ADB	SSOP (16)	6.20 mm × 5.30 mm
SNx4LV165ANS	SO (16)	10.30 mm × 5.30 mm
SNx4LV165APW	TSSOP (16)	5.00 mm × 4.40 mm
SNx4LV165ADGV	TVSOP (16)	3.60 mm × 4.40 mm
SNx4LV165ARGY	VQFN (16)	4.00 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision N (July 2013) to Revision O **Page**

- Added *Applications* section, *Device Information* table, *Table of Contents*, *Pin Configuration and Functions* section, *Specifications* section, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics* section, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision M (December 2010) to Revision N **Page**

- Extended maximum temperature operating range from 85°C to 125°C ... 5

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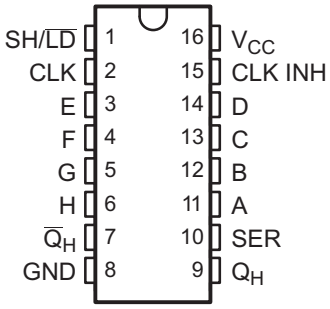
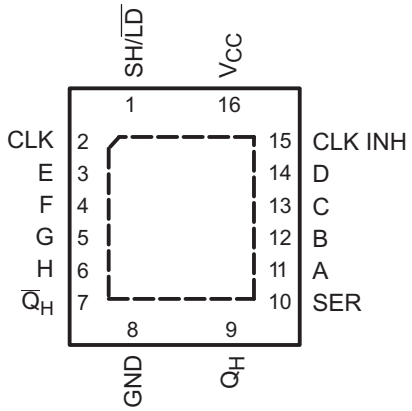
5 Pin Configuration and Functions

SN74LV165A: D, DB, DGV, NS or PW Package
SN54LV165A: J or W Package
16-Pin SOIC, SSOP, TVSOP, SOP, TSSOP
Top View



SN74LV165A: RGY Package
16-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	11	I	Serial input A
B	12	I	Serial input B
C	13	I	Serial input C
CLK	2	I	Storage clock
CLK INH	15	I	Storage clock
D	14	I	Serial input D
E	3	I	Serial input E
F	4	I	Serial input F
G	5	I	Serial input G
GND	8	—	Ground pin
H	6	I	Serial input H
Q_H	7	O	Output H
	9		
SH/$\overline{LD}$	1	I	Load Input
SER	10	I	Serial input
V_{CC}	16	—	Power pin

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6 Specifications

6.1 Absolute Maximum Ratings

see (1)

			MIN	MAX	UNIT
	Supply voltage		–0.5	7	V
	Input voltage(2)		–0.5	7	V
	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	7	V
	Output voltage (2)(3)		–0.5	V_{CC} + 0.5	V
	Input clamp current	V_I < 0		–20	mA
	Output clamp current	V_O < 0		–50	mA
	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{jmax}	Maximum virtual junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5 V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50	μA
		V_{CC} = 2.3 V to 2.7 V		–2	mA
		V_{CC} = 3 V to 3.6 V		–6	
		V_{CC} = 4.5 V to 5.5 V		–12	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 2.3 V to 2.7 V		2	mA
		V_{CC} = 3 V to 3.6 V		6	
		V_{CC} = 4.5 V to 5.5 V		12	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200	ns/V
		V_{CC} = 3 V to 3.6 V		100	
		V_{CC} = 4.5 V to 5.5 V		20	
T_A	Operating free-air temperature	SN54LV165A	–55	125	°C
		SN74LV165A	–40	125	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the *Implications of Slow or Floating CMOS Inputs* application report.

6.4 Thermal Information

THERMAL METRIC(1)		SN74LV165A						UNIT
		D (SOIC)	DB (SSOP)	NS (SO)	PW (TSSOP)	DGV (TVSOP)	RGY (VQFN)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.2	102.8	89.4	113.3	125.9	48.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.1	53.3	47.9	48.3	51	46.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.8	53.5	49.8	58.4	57.7	24.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.2	16.6	16.6	6.4	5.7	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.5	52.9	49.5	57.8	57.2	24.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	11.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). Recommended T_A = –40°C to +125°C

PARAMETER		V_{CC}	T_A	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = –50 mA	2 V to 5.5 V	–55°C to +125°C	V_{CC} – 0.1			V
			–40°C to +85°C	$_{CC}$ – 0.1			
			–40°C to +125°C	V_{CC} – 0.1			
	I_{OH} = –2 mA	2.3 V	–55°C to +125°C	2			
			–40°C to +85°C	2			
			–40°C to +125°C	2			
	I_{OH} = –6 mA	3 V	–55°C to +125°C	2.48			
			–40°C to +85°C	2.48			
			–40°C to +125°C	2.48			
	I_{OH} = –12 mA	4.5 V	–55°C to +125°C	3.8			
			–40°C to +85°C	3.8			
			–40°C to +125°C	3.8			
V_{OL}	I_{OL} = 50 mA	2 V to 5.5 V	–55°C to +125°C			0.1	V
			–40°C to +85°C			0.1	
			–40°C to +125°C			0.1	
	I_{OL} = 2 mA	2.3 V	–55°C to +125°C			0.4	
			–40°C to +85°C			0.4	
			–40°C to +125°C			0.4	
	I_{OL} = 6 mA	3 V	–55°C to +125°C			0.44	
			–40°C to +85°C			0.44	
			–40°C to +125°C			0.44	
	I_{OL} = 12 mA	4.5 V	–55°C to +125°C			0.55	
			–40°C to +85°C			0.55	
			–40°C to +125°C			0.55	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V	–55°C to +125°C			±1	µA
			–40°C to +85°C			±1	
			–40°C to +125°C			±1	
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V	–55°C to +125°C			20	µA
			–40°C to +85°C			20	
			–40°C to +125°C			20	
I_{off}	V_I or V_O = 0 to 5.5 V	0	–55°C to +125°C			5	µA
			–40°C to +85°C			5	
			–40°C to +125°C			5	
C_i	V_I = V_{CC} or GND	3.3 V	–55°C to +125°C		1.7		pF
			–40°C to +85°C		1.7		
			–40°C to +125°C		1.7		

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6.6 Timing Requirements—V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 2)

PARAMETER		TEST CONDITION	T_A	MIN	MAX	UNIT
t_w	Pulse duration	CLK high or low	25°C	8.5		ns
			–55°C to +125°C	9		
			–40°C to +85°C	9		
			–40°C to +125°C	9		
		SH/$\overline{LD}$ low	25°C	11		
			–55°C to +125°C	13		
			–40°C to +85°C	13		
			–40°C to +125°C	13		
t_{su}	Setup time	SH/$\overline{LD}$ high before CLK↑	25°C	7		ns
			–55°C to +125°C	8.5		
			–40°C to +85°C	8.5		
			–40°C to +125°C	8.5		
		SER before CLK↑	25°C	8.5		
			–55°C to +125°C	9.5		
			–40°C to +85°C	9.5		
			–40°C to +125°C	9.5		
		CLK INH before CLK↑	25°C	7		
			–55°C to +125°C	7		
			–40°C to +85°C	7		
			–40°C to +125°C	7		
		Data before SH/$\overline{LD}$↑	25°C	11.5		
			–55°C to +125°C	12		
			–40°C to +85°C	12		
			–40°C to +125°C	12		
t_h	Hold time	SER data after CLK↑	25°C	−1		ns
			–55°C to +125°C	0		
			–40°C to +85°C	0		
			–40°C to +125°C	0		
		Parallel data after SH/$\overline{LD}$↑	25°C	0		
			–55°C to +125°C	0.5		
			–40°C to +85°C	0.5		
			–40°C to +125°C	0.5		
		SH/$\overline{LD}$ high after CLK↑	25°C	0		
			–55°C to +125°C	0		
			–40°C to +85°C	0		
			–40°C to +125°C	0		

6.7 Timing Requirements—V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

PARAMETER		TEST CONDITION	T_A	MIN	MAX	UNIT
t_w	Pulse duration	CLK high or low	25°C	6		ns
			–55°C to +125°C	7		
			–40°C to +85°C	7		
			–40°C to +125°C	7		
		SH/$\overline{LD}$ low	25°C	7.5		
			–55°C to +125°C	9		
			–40°C to +85°C	9		
			–40°C to +125°C	9		

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Timing Requirements—V_{CC} = 3.3 V ± 0.3 V (continued)

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

PARAMETER		TEST CONDITION	T_A	MIN	MAX	UNIT
t_{su}	Setup time	SH/$\overline{LD}$ high before CLK↑	25°C	5		ns
			–55°C to +125°C	6		
			–40°C to +85°C	6		
			–40°C to +125°C	6		
		SER before CLK↑	25°C	5		
			–55°C to +125°C	6		
			–40°C to +85°C	6		
			–40°C to +125°C	6		
		CLK INH before CLK↑	25°C	5		
			–55°C to +125°C	5		
			–40°C to +85°C	5		
			–40°C to +125°C	5		
		Data before SH/$\overline{LD}$↑	25°C	7.5		
			–55°C to +125°C	8.5		
			–40°C to +85°C	8.5		
			–40°C to +125°C	8.5		
t_h	Hold time	SER data after CLK↑	25°C	0		ns
			–55°C to +125°C	0		
			–40°C to +85°C	0		
			–40°C to +125°C	0		
		Parallel data after SH/$\overline{LD}$↑	25°C	0.5		
			–55°C to +125°C	0.5		
			–40°C to +85°C	0.5		
			–40°C to +125°C	0.5		
		SH/$\overline{LD}$ high after CLK↑	25°C	0		
			–55°C to +125°C	0		
			–40°C to +85°C	0		
			–40°C to +125°C	0		

6.8 Timing Requirements—V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

PARAMETER		TEST CONDITION	T_A	MIN	MAX	UNIT
t_w	Pulse duration	CLK high or low	25°C	4		ns
			–55°C to +125°C	4		
			–40°C to +85°C	4		
			–40°C to +125°C	4		
		SH/$\overline{LD}$ low	25°C	5		
			–55°C to +125°C	5		
			–40°C to +85°C	6		
			–40°C to +125°C	6		

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Timing Requirements—V_{CC} = 5 V ± 0.5 V (continued)

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

PARAMETER		TEST CONDITION	T_A	MIN	MAX	UNIT
t_{su}	Setup time	SH/$\overline{LD}$ high before CLK↑	25°C	4		ns
			–55°C to +125°C	4		
			–40°C to +85°C	4		
			–40°C to +125°C	4		
		SER before CLK↑	25°C	4		
			–55°C to +125°C	4		
			–40°C to +85°C	4		
			–40°C to +125°C	4		
		CLK INH before CLK↑	25°C	3.5		
			–55°C to +125°C	3.5		
			–40°C to +85°C	3.5		
			–40°C to +125°C	3.5		
		Data before SH/$\overline{LD}$↑	25°C	5		
			–55°C to +125°C	5		
			–40°C to +85°C	5		
			–40°C to +125°C	5		
t_h	Hold time	SER data after CLK↑	25°C	0.5		ns
			–55°C to +125°C	0.5		
			–40°C to +85°C	0.5		
			–40°C to +125°C	0.5		
		Parallel data after SH/$\overline{LD}$↑	25°C	1		
			–55°C to +125°C	1		
			–40°C to +85°C	1		
			–40°C to +125°C	1		
		SH/$\overline{LD}$ high after CLK↑	25°C	0.5		
			–55°C to +125°C	0.5		
			–40°C to +85°C	0.5		
			–40°C to +125°C	0.5		

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6.9 Switching Characteristics—V_{CC} = 2.5 V ± 0.2 V

over operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted), (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAP	T_A	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF	25°C	50(1)	80(1)		MHz
				–55°C to +125°C	45(1)			
				–40°C to +85°C	45			
				–40°C to +125°C	45			
			C_L = 50 pF	25°C	40	65		
				–55°C to +125°C	35			
				–40°C to +85°C	35			
				–40°C to +125°C	35			
t_{pd}	CLK	Q_H or $\overline{Q}$	C_L = 15 pF	25°C		12.2(1)	19.8(1)	ns
				–55°C to +125°C	1(1)		22(1)	
				–40°C to +85°C	1		22	
				–40°C to +125°C	1		22	
	SH/$\overline{LD}$			25°C		13.1(1)	21.5(1)	
				–55°C to +125°C	1(1)		23.5(1)	
				–40°C to +85°C	1		23.5	
				–40°C to +125°C	1		23.5	
	H			25°C		12.9(1)	21.7(1)	
				–55°C to +125°C	1(1)		24(1)	
				–40°C to +85°C	1		24	
				–40°C to +125°C	1		24	
t_{pd}	CLK	Q_H or $\overline{Q}$	C_L = 50 pF	25°C		15.3	23.3	ns
				–55°C to +125°C	1		26	
				–40°C to +85°C	1		26	
				–40°C to +125°C	1		26	
	SH/$\overline{LD}$			25°C		16.1	25.1	
				–55°C to +125°C	1		28	
				–40°C to +85°C	1		28	
				–40°C to +125°C	1		28	
	H			25°C		15.9	25.3	
				–55°C to +125°C	1		28	
				–40°C to +85°C	1		28	
				–40°C to +125°C	1		28	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

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6.10 Switching Characteristics—V_{CC} = 3.3 V ± 0.3 V

over operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted), (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAP	T_A	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF	25°C	65(1)	115(1)		MHz
				–55°C to +125°C	55(1)			
				–40°C to +85°C	55			
				–40°C to +125°C	55			
			C_L = 50 pF	25°C	60	90		
				–55°C to +125°C	50			
				–40°C to +85°C	50			
				–40°C to +125°C	50			
t_{pd}	CLK	Q_H or $\overline{Q}$	C_L = 15 pF	25°C		8.6(1)	15.4(1)	ns
				–55°C to +125°C	1(1)		18(1)	
				–40°C to +85°C	1		18	
				–40°C to +125°C	1		18	
	SH/$\overline{LD}$			25°C		9.1(1)	15.8(1)	
				–55°C to +125°C	1(1)		18.5(1)	
				–40°C to +85°C	1		18.5	
				–40°C to +125°C	1		18.5	
	H			25°C		8.9(1)	14.1(1)	
				–55°C to +125°C	1(1)		16.5(1)	
				–40°C to +85°C	1		16.5	
				–40°C to +125°C	1		16.5	
t_{pd}	CLK	Q_H or $\overline{Q}$	C_L = 50 pF	25°C		10.9	14.9	ns
				–55°C to +125°C	1		16.9	
				–40°C to +85°C	1		16.9	
				–40°C to +125°C	1		16.9	
	SH/$\overline{LD}$			25°C		11.3	19.3	
				–55°C to +125°C	1		22	
				–40°C to +85°C	1		22	
				–40°C to +125°C	1		22	
	H			25°C		11.1	17.6	
				–55°C to +125°C	1		20	
				–40°C to +85°C	1		20	
				–40°C to +125°C	1		20	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

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6.11 Switching Characteristics—V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAP	T_A	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF	25°C	110(1)	165(1)		MHz
				–55°C to +125°C	90(1)			
				–40°C to +85°C	90			
				–40°C to +125°C	90			
			C_L = 50 pF	25°C	95	125		
				–55°C to +125°C	85			
				–40°C to +85°C	85			
				–40°C to +125°C	85			
t_{pd}	CLK	Q_H or $\overline{Q}$	C_L = 15 pF	25°C		6(1)	9.9(1)	ns
				–55°C to +125°C	1(1)		11.5(1)	
				–40°C to +85°C	1		11.5	
				–40°C to +125°C	1		11.5	
	SH/$\overline{LD}$			25°C		6(1)	9.9(1)	
				–55°C to +125°C	1(1)		11.5(1)	
				–40°C to +85°C	1		11.5	
				–40°C to +125°C	1		11.5	
	H			25°C		6(1)	9.9(1)	
				–55°C to +125°C	1(1)		10.5(1)	
				–40°C to +85°C	1		10.5	
				–40°C to +125°C	1		10.5	
t_{pd}	CLK	Q_H or $\overline{Q}$	C_L = 50 pF	25°C		7.7	11.9	ns
				–55°C to +125°C	1		13.5	
				–40°C to +85°C	1		13.5	
				–40°C to +125°C	1		13.5	
	SH/$\overline{LD}$			25°C		7.7	11.9	
				–55°C to +125°C	1		13.5	
				–40°C to +85°C	1		13.5	
				–40°C to +125°C	1		13.5	
	H			25°C		7.6	11	
				–55°C to +125°C	1		12.5	
				–40°C to +85°C	1		12.5	
				–40°C to +125°C	1		12.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.12 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF	f = 10 MHz	3.3 V	36.1	pF
				5 V	37.5	

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6.13 Typical Characteristics

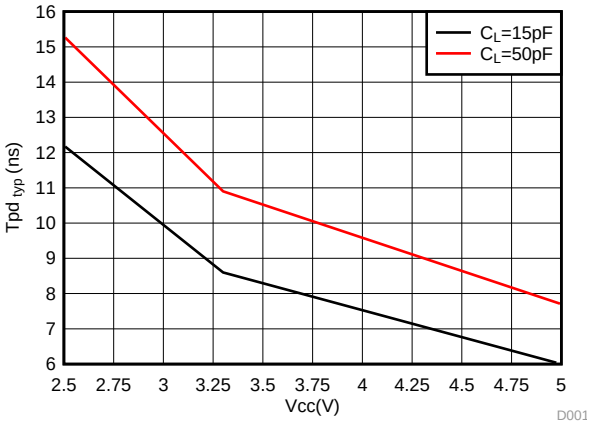
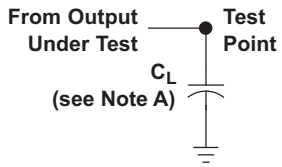
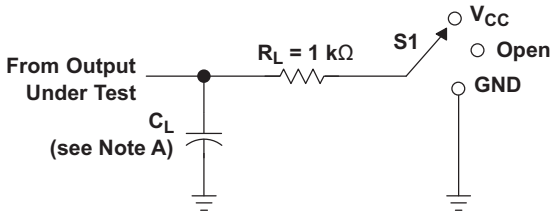


Figure 1. T_{PD} Typical (25°C) vs V_{cc}

7 Parameter Measurement Information

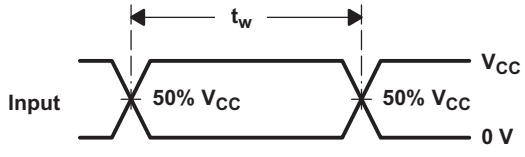


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

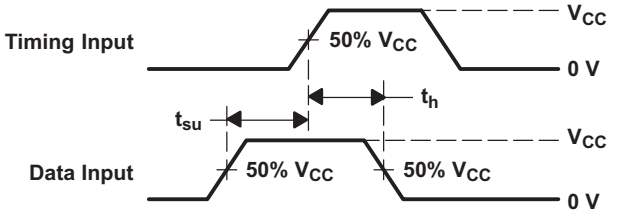


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

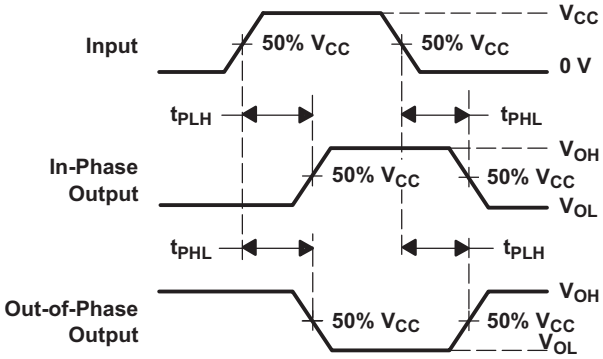
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



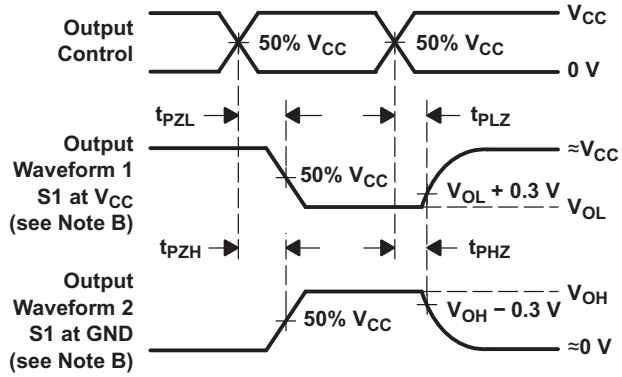
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.

D. The outputs are measured one at a time, with one input transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.

G. t_{PHL} and t_{PLH} are the same as t_{pd}.

H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

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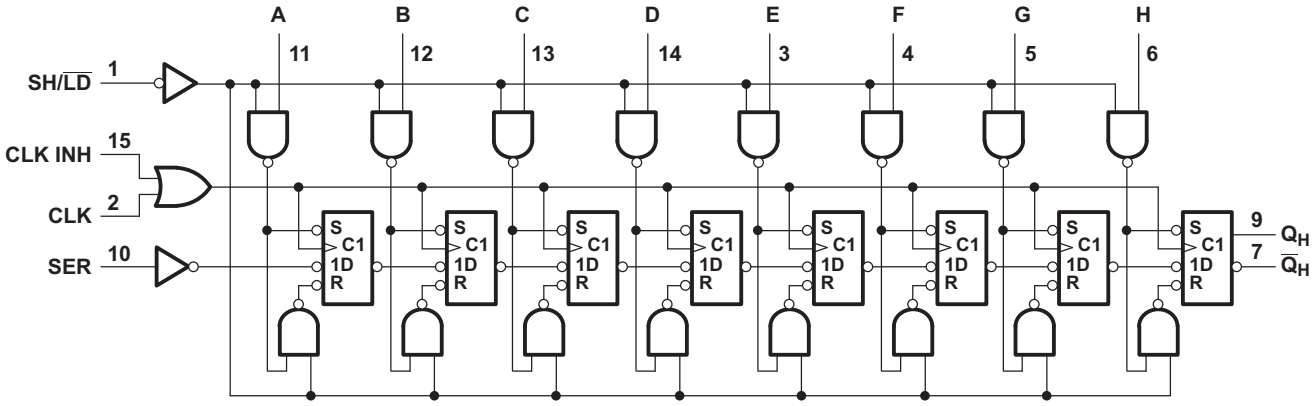
8 Detailed Description

8.1 Overview

The ’LV165A devices are parallel-load, 8-bit shift registers designed for 2-V to 5.5-V V_{CC} operation.

When the devices are clocked, data is shifted toward the serial output Q_H. Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the shift/load ($\overline{SH/LD}$) input. The ’LV165A devices feature a clock-inhibit function and a complemented serial output, $\overline{Q}_H$.

8.2 Functional Block Diagram



Pin numbers shown are for the D, DB, DGV, J, NS, PW, RGY, and W packages.

Figure 3. Logic Diagram (Positive Logic)

Functional Block Diagram (continued)

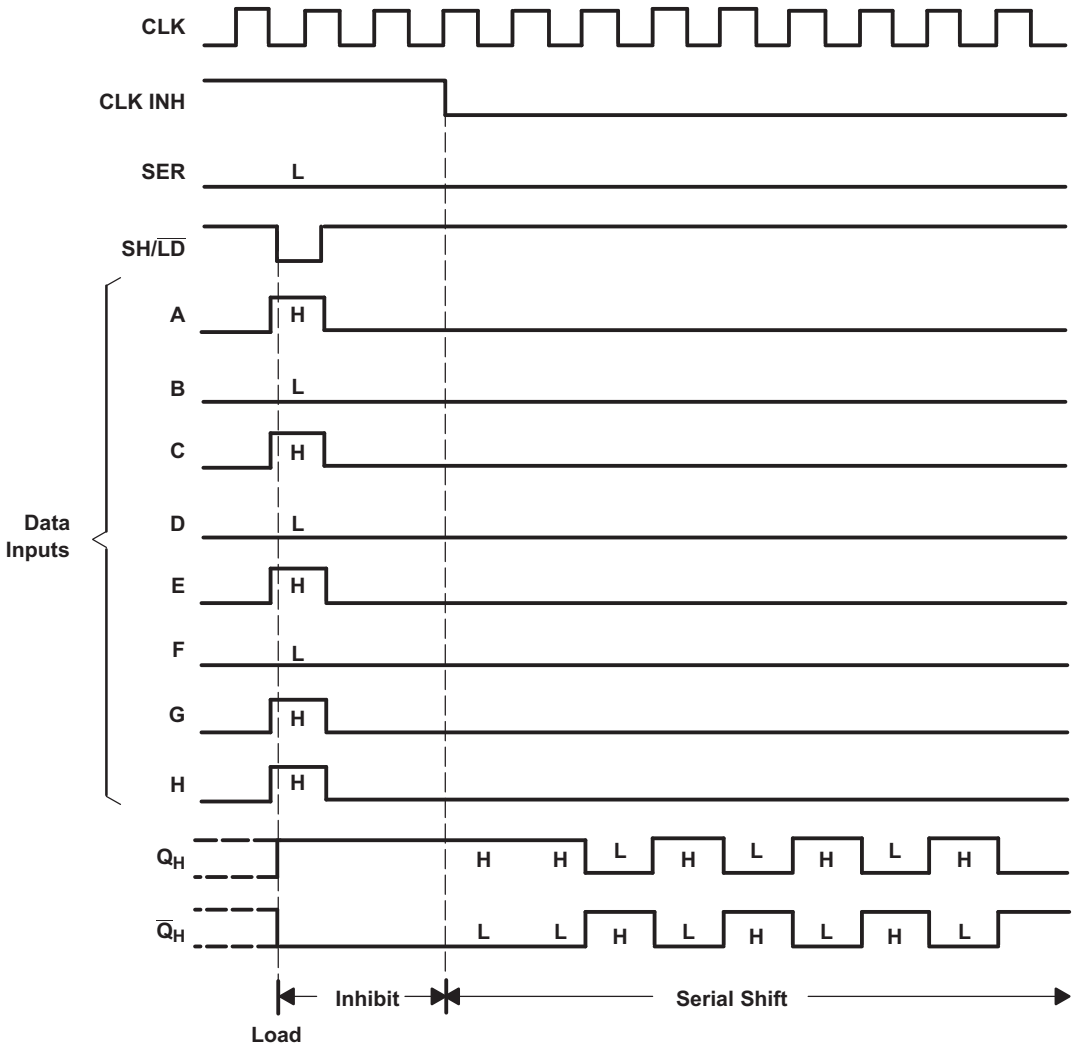


Figure 4. Typical Shift, Load, and Inhibit Sequences

8.3 Feature Description

The wide operating range allows the device to be used in a variety of systems that use different logic levels. The low propagation delay allows fast switching and higher speeds of operation. In addition, the low ground bounce stabilizes the performance of non-switching outputs while another output is switching.

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8.4 Device Functional Modes

Table 1 lists the functional modes of SNx4LV165A.

Table 1. Device Functional Modes

INPUTS			OPERATION
SH/$\overline{LD}$	CLK	CLK INH	
L	X	X	Parallel load
H	H	X	Q_0
H	X	H	Q_0
H	L	↑	Shift
H	↑	L	Shift

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LV165A is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low-drive and slow-edge rates minimize overshoot and undershoot on the outputs.

9.2 Typical Application

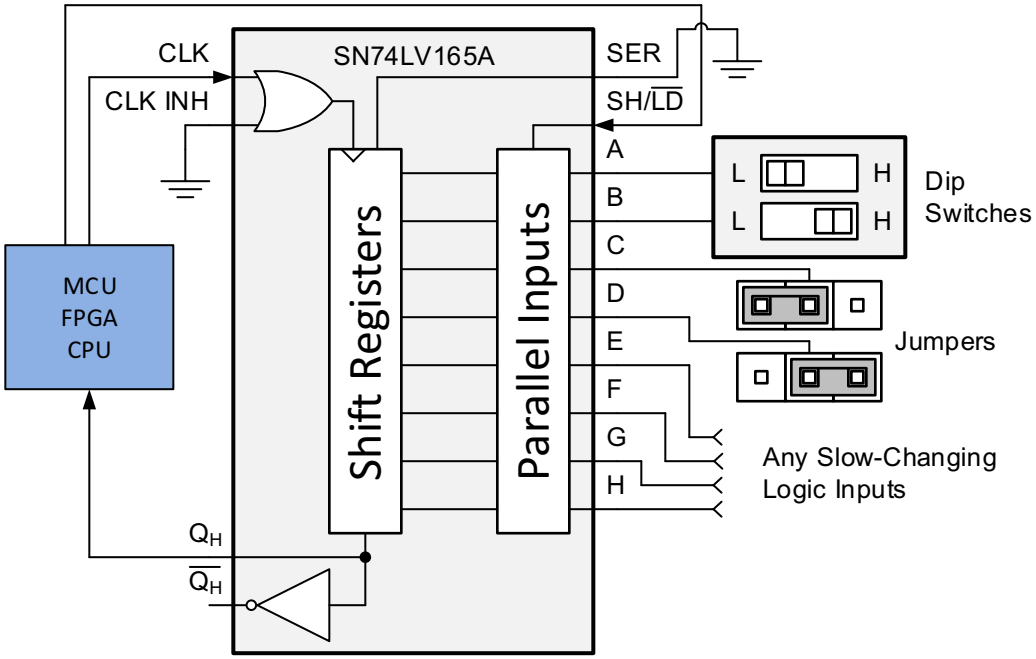

Figure 5. Input Expansion with Shift Registers

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that can exceed maximum limits. The high drive also creates fast edges into light loads so consider routing and load conditions to prevent ringing.

9.2.2 Detailed Design Procedure

Recommended input conditions:

- Rise time and fall time specs. See the *Recommended Operating Conditions* section, ($\Delta t/\Delta V$)
- Specified high and low level. See the *Recommended Operating Conditions* section, (V_{IH} and V_{IL})
- Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}

Recommended output conditions:

- Load currents must not exceed 25 mA per output and 50 mA total for the part.
- Outputs must not be pulled above V_{CC}.

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Typical Application (continued)

9.2.3 Application Curves

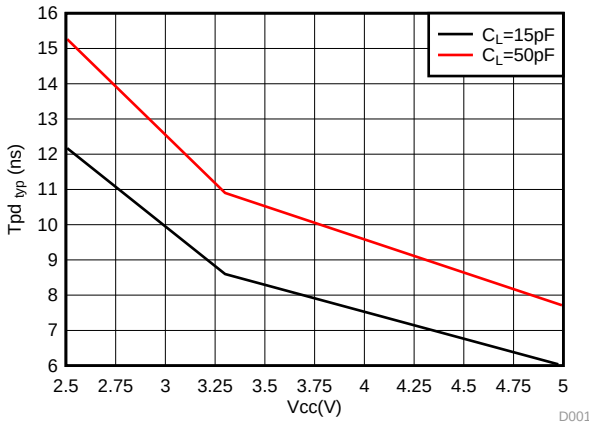

Figure 6. Switching Characteristics Comparison

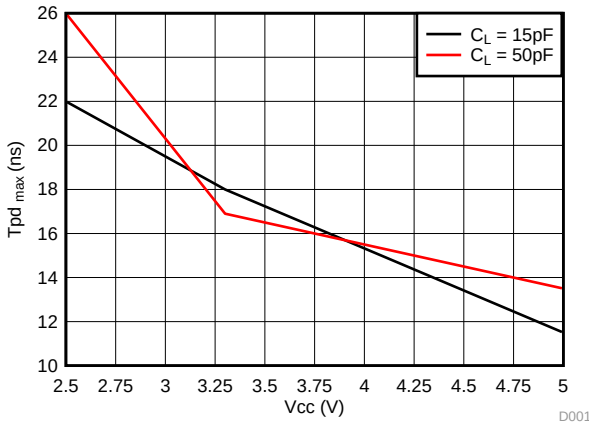

Figure 7. $T_{pd(max)}$ vs V_{CC}

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings* section. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-μF capacitor and if there are multiple V_{CC} terminals then TI recommends a 0.01-μF or 0.022-μF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs must never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC} whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it disables the outputs section of the part when asserted. This does not disable the input section of the IOs so they also cannot float when disabled.

11.2 Layout Example

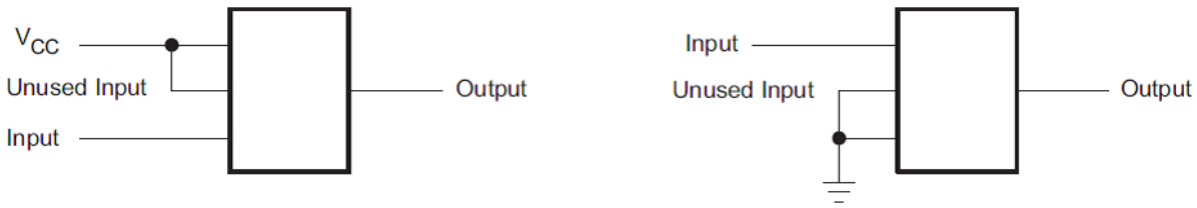

Figure 8. Layout Example

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12 Device and Documentation Support

12.1 Related Documentation

For related documentation see the following:

- *Power-Up Behavior of Clocked Devices*
- *Introduction to Logic*

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54LV165A	Click here	Click here	Click here	Click here	Click here
SN74LV165A	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV165AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ADRG3	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV165A	Samples
SN74LV165APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165APWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165APWRG3	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165APWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ARGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV165A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV165ARGYRG4	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV165A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV165A :

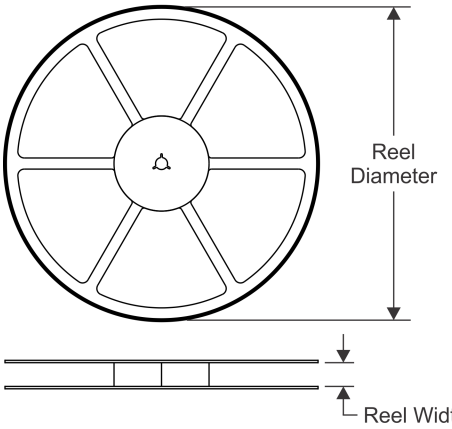
- Enhanced Product: SN74LV165A-EP

NOTE: Qualified Version Definitions:

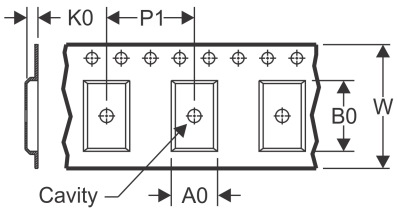
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

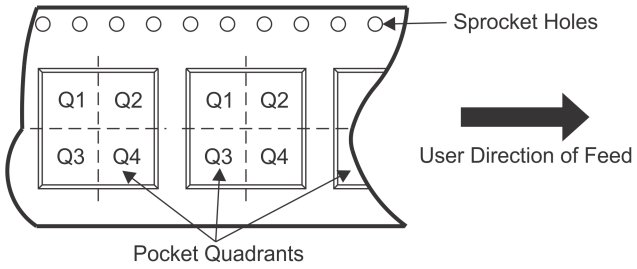


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

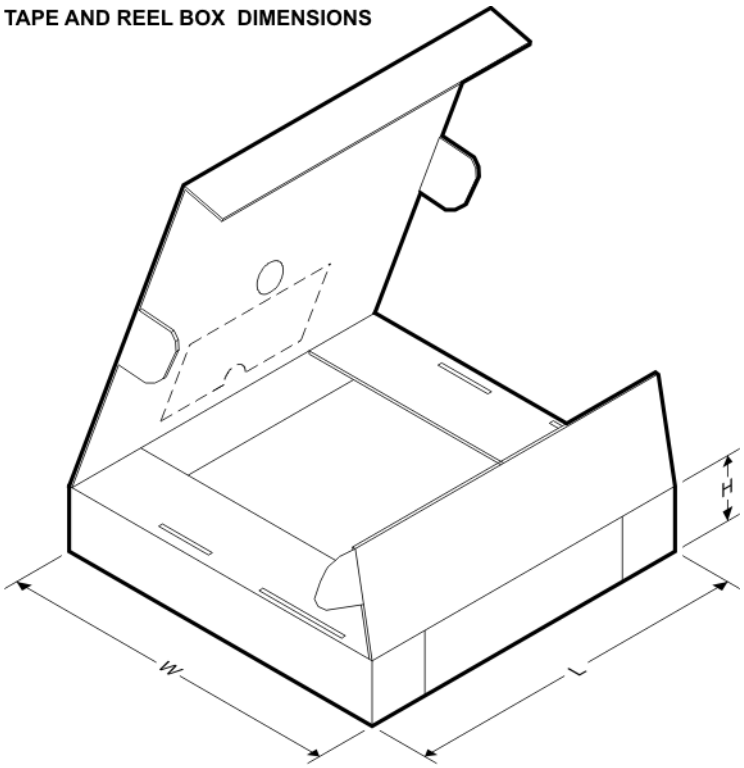
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV165ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV165ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV165ADR	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV165ADRG3	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV165ADRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV165ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV165APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV165APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV165APWRG3	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV165APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV165APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV165ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

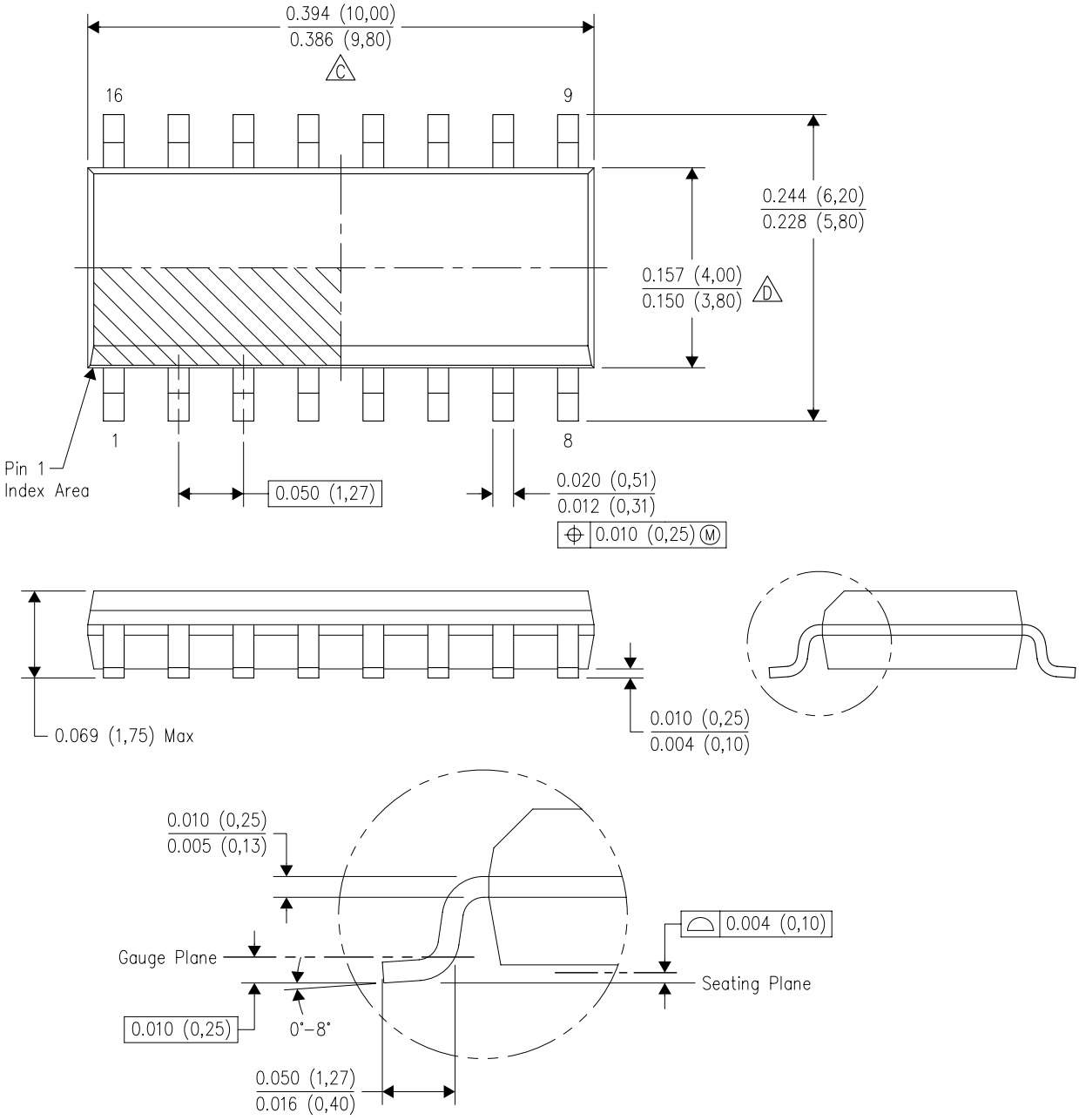
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

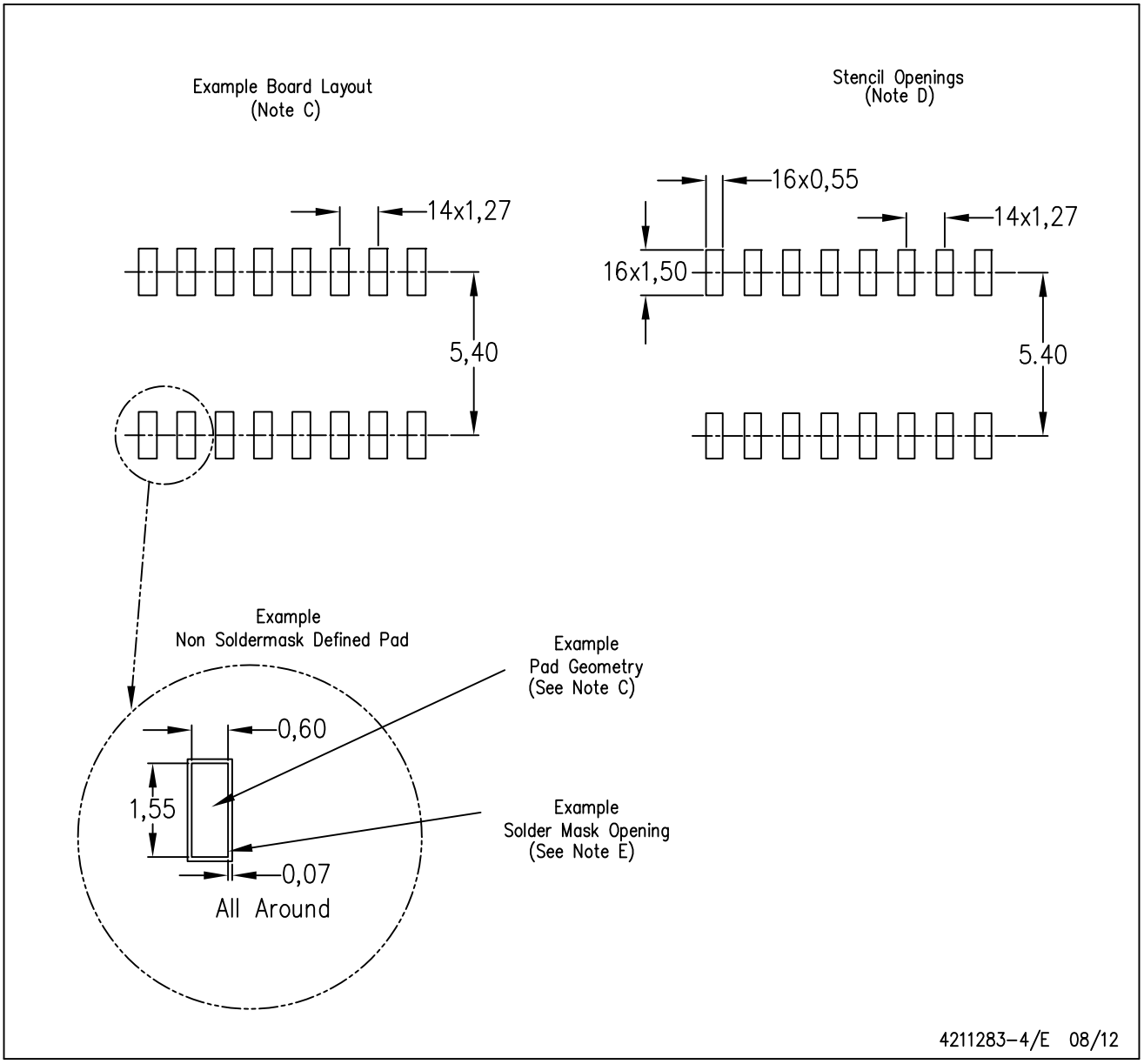
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV165ADGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74LV165ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LV165ADR	SOIC	D	16	2500	364.0	364.0	27.0
SN74LV165ADRG3	SOIC	D	16	2500	364.0	364.0	27.0
SN74LV165ADRG4	SOIC	D	16	2500	333.2	345.9	28.6
SN74LV165ANSR	SO	NS	16	2000	367.0	367.0	38.0
SN74LV165APWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV165APWR	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74LV165APWRG3	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74LV165APWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV165APWT	TSSOP	PW	16	250	367.0	367.0	35.0
SN74LV165ARGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



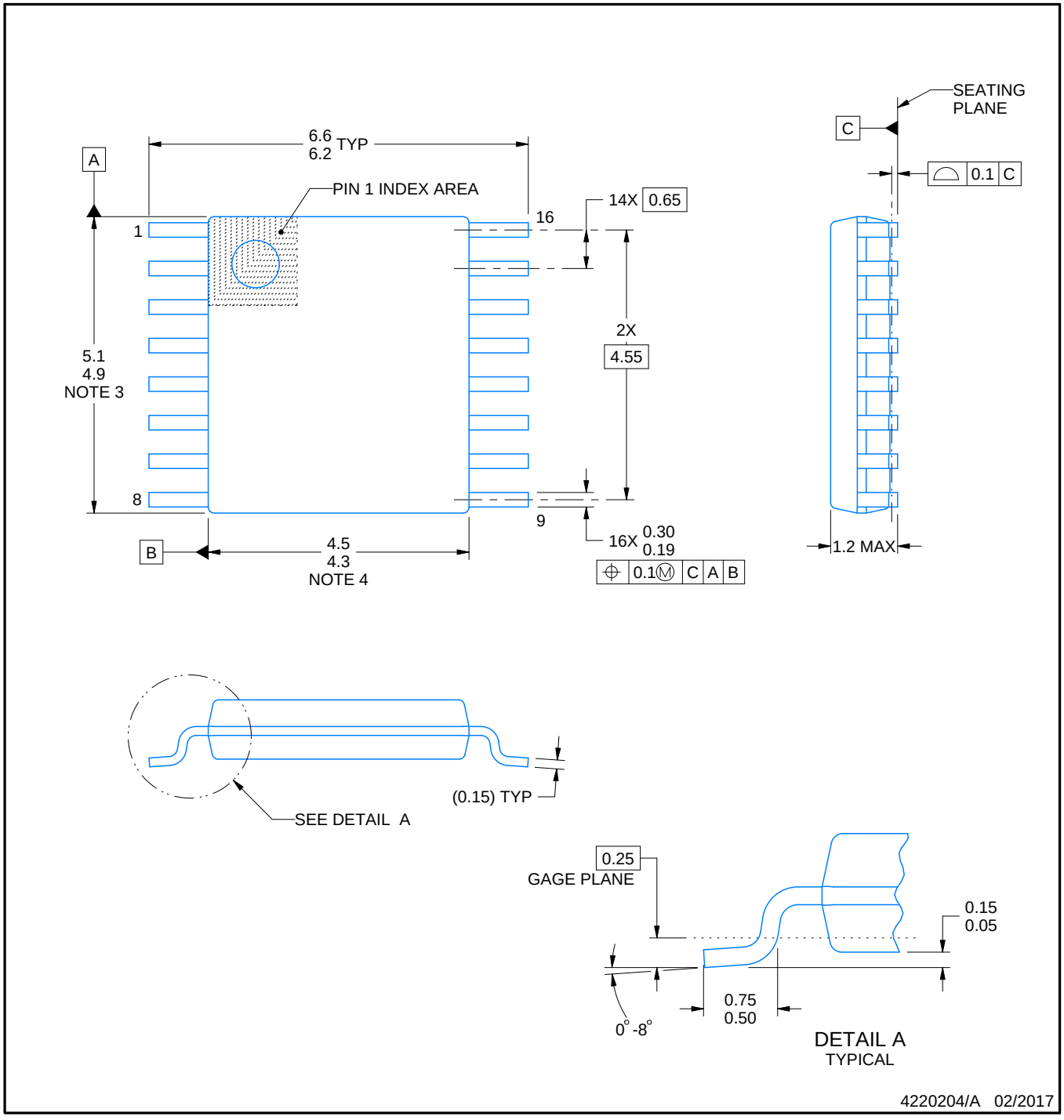
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

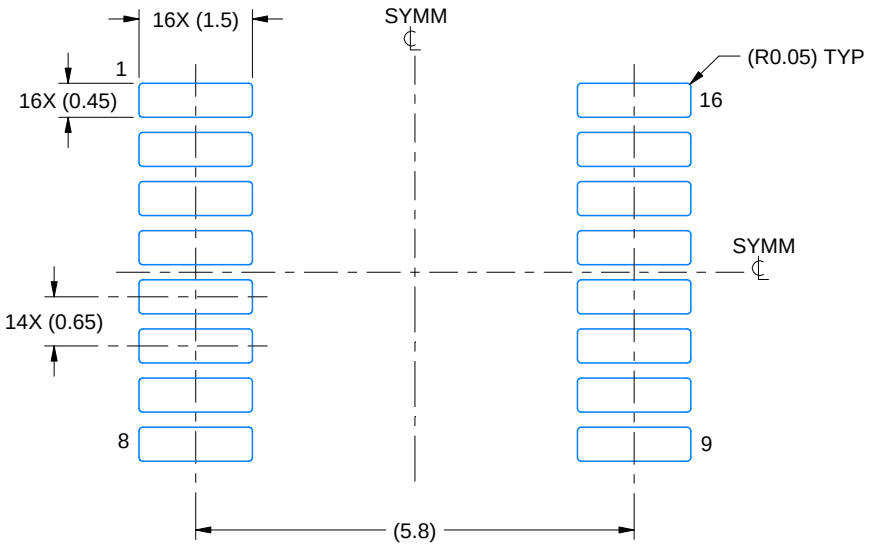
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



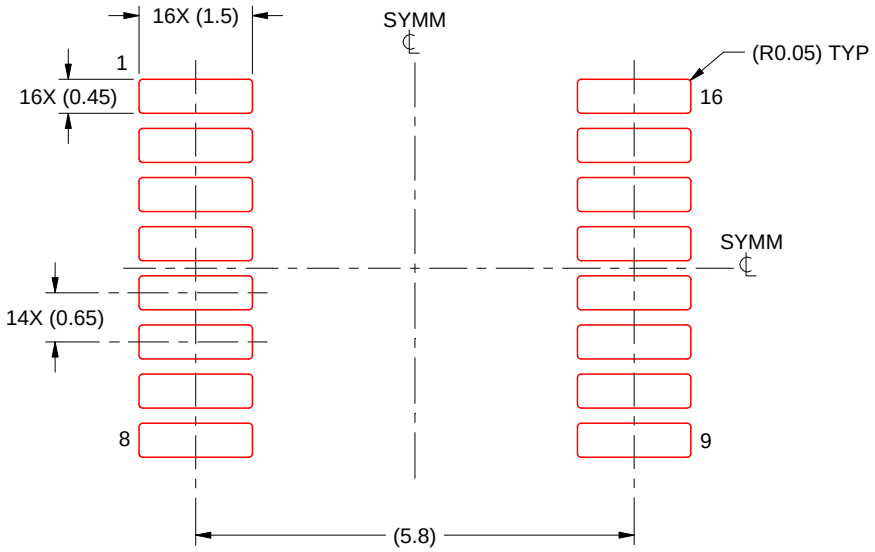
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

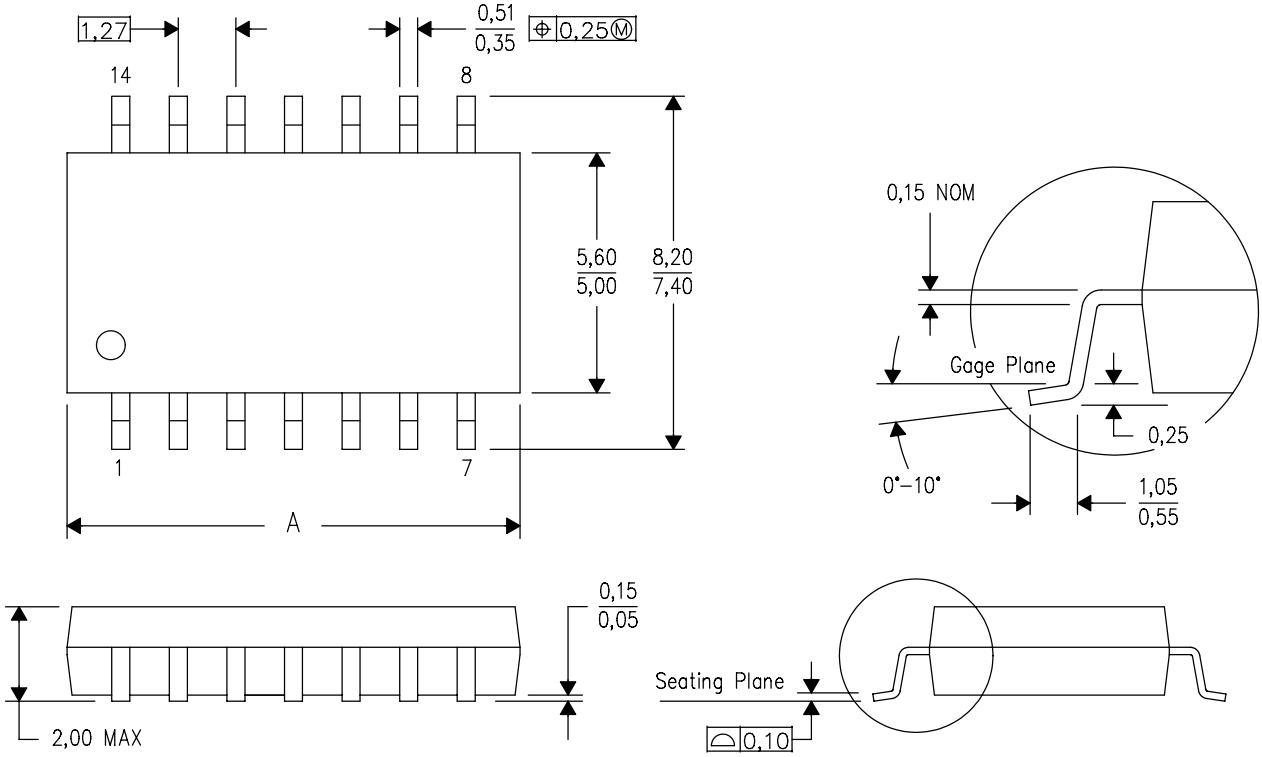
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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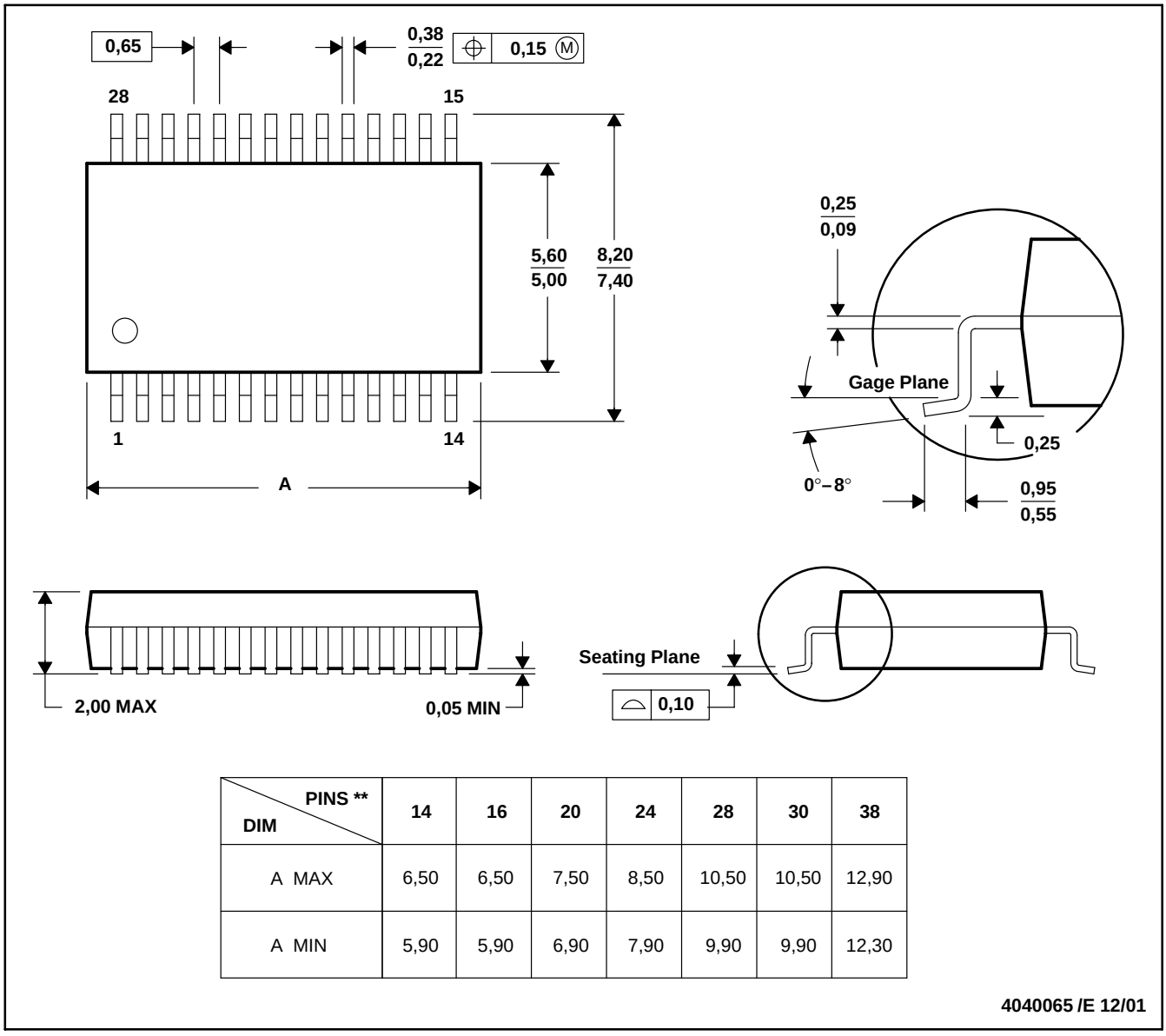
DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

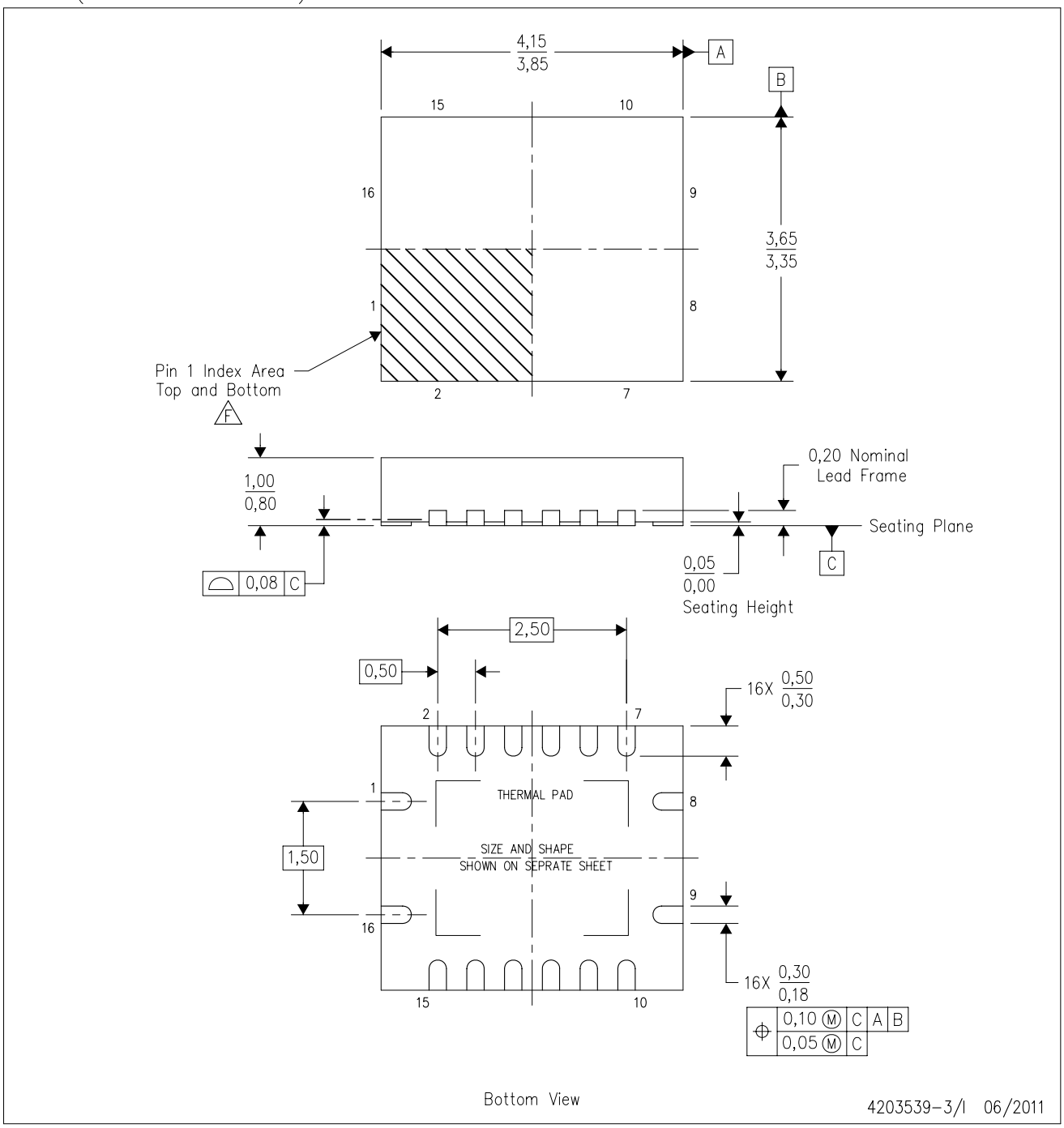


DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

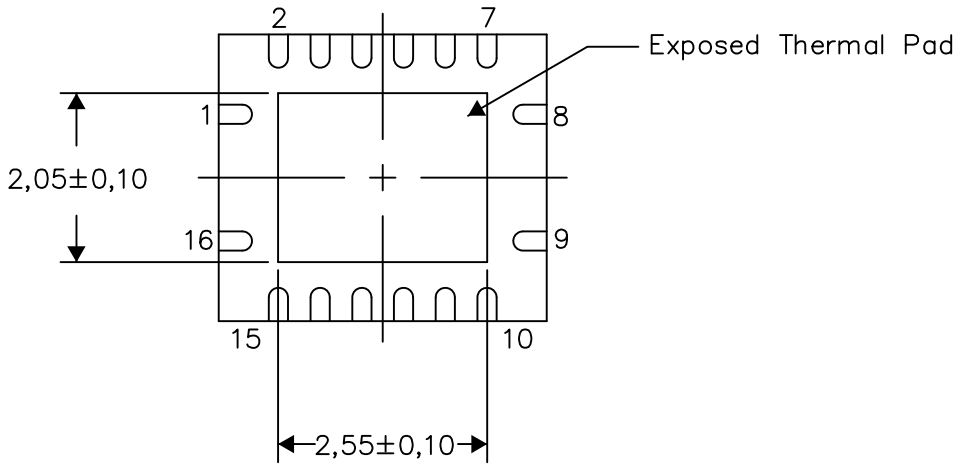
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



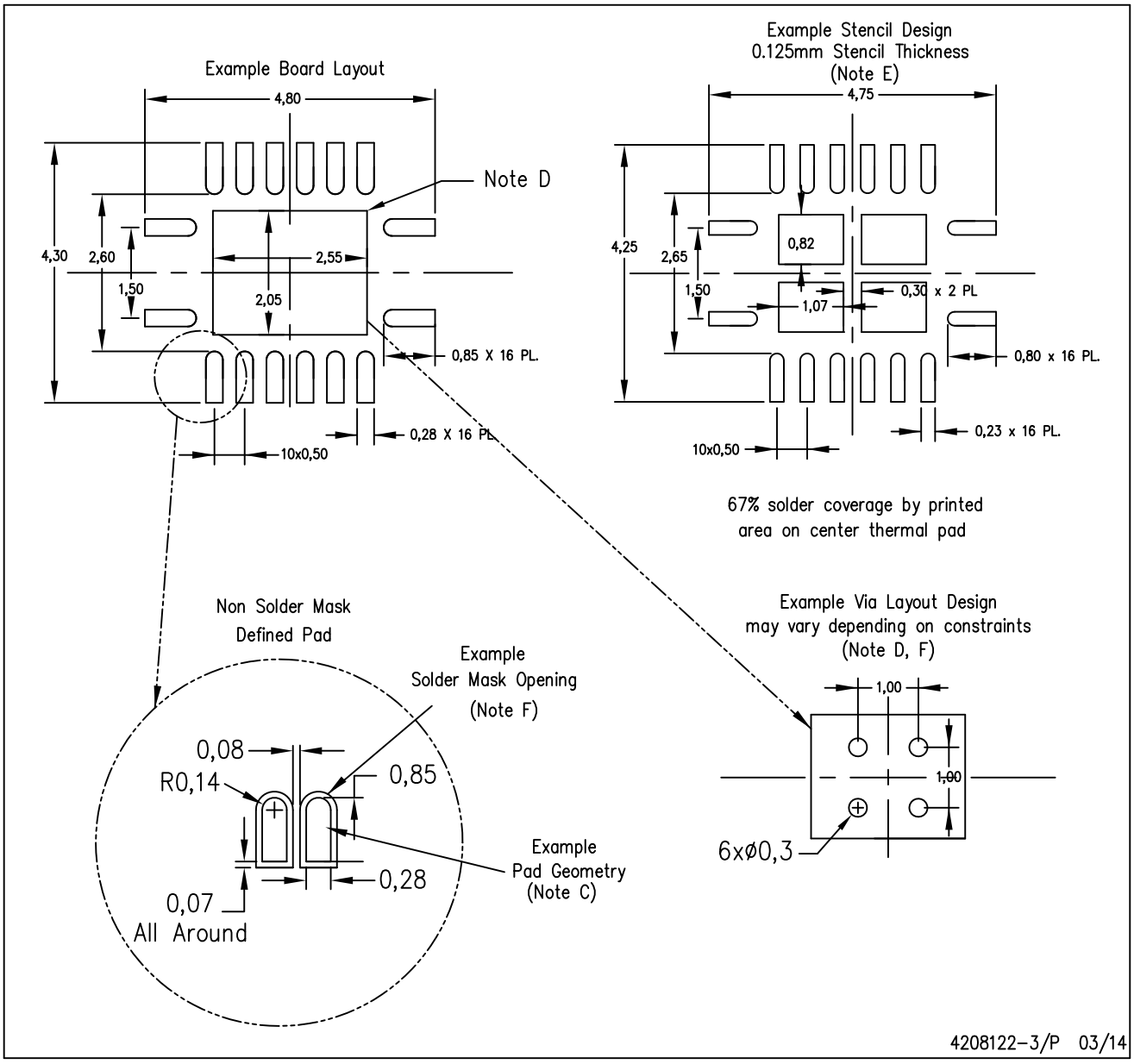
Bottom View

Exposed Thermal Pad Dimensions

4206353–3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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