THE DATASHEET OF

TS3USB30EDGSR

www.win-source.net 0086-755-83957316

TS3USB30E ESD-Protected, High-Speed USB 2.0 (480-Mbps) 1:2 Multiplexer/Demultiplexer Switch With Single Enable

1 Features

- V_{CC} Operation at 3 V to 4.3 V
- D+/D– Pins Tolerate up to 5.25 V
- 1.8-V Compatible Control-Pin Inputs
- I_{OFF} Supports Partial Power-Down-Mode Operation
- R_{ON} = 10 Ω Maximum
- ΔR_{ON} = 0.35 Ω Typical
- $C_{io(ON)}$ = 7.5 pF Typical
- Low Power Consumption (1 µA Maximum)
- –3-dB Bandwidth = 900 MHz Typical
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II (1)
- ESD Performance Tested Per JESD 22
  - 8000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- ESD Performance I/O Port to GND (2)
  - 15000-V Human-Body Model
- Packaged in 10-pin UQFN (1.4 mm × 1.8 mm)

2 Applications

- Routes Signals for USB 1.0, 1.1, and 2.0
- Multi-Purpose Signal Switching
- Portable Electronics
- Industrial
- Consumer Products

(1) Except $\overline{OE}$ and S inputs
(2) High-voltage HBM is performed in addition to the standard HBM testing (A114-B, Class II) and applies to I/O ports tested with respect to GND only.

3 Description

The TS3USB30E is a high-bandwidth 1:2 switch specially designed for the switching of high-speed USB 2.0 signals in handset and consumer applications, such as cell phones, digital cameras, and notebooks with hubs or controllers with limited USB I/Os. The wide bandwidth (900 MHz) of this switch allows signals to pass with minimum edge and phase distortion. The device multiplexes differential outputs from a USB host device to one of two corresponding outputs, or from two different hosts to one corresponding output. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. It is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480 Mbps).

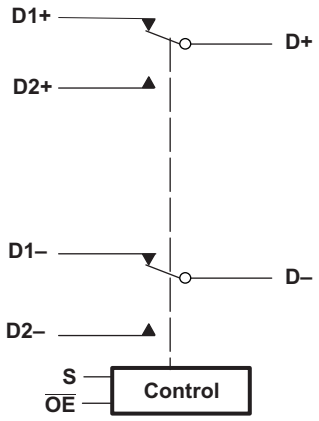
The TS3USB30E integrates ESD protection cells on all pins, is available in a tiny UQFN package (1.8 mm × 1.4 mm) or a VSSOP package, and is characterized over the free-air temperature range of –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS3USB30E	VSSOP (10)	3.00 mm × 3.00 mm
	UQFN (10)	1.80 mm × 1.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Functional Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

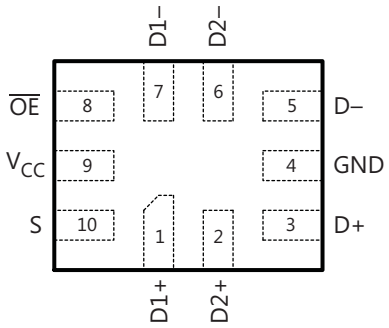
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (August 2012) to Revision F	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Changed package type in Description from DGS to VSSOP	1

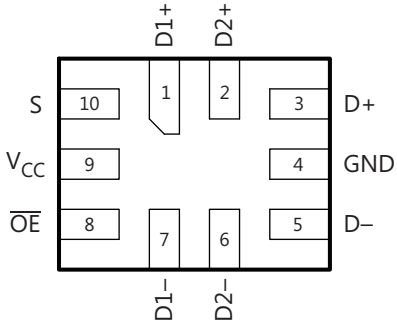
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5 Pin Configuration and Functions

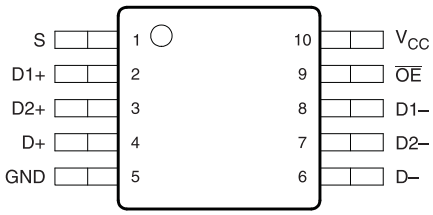
RSW PACKAGE
10-PIN UQFN
TOP VIEW



RSW PACKAGE
10-PIN UQFN
BOTTOM VIEW



DGS PACKAGE
10-PIN VSSOP
TOP VIEW



Pin Functions

PIN			I/O	DESCRIPTION
NAME	UQFN	VSSOP		
D1+	1	2	I/O	USB signal path port 1
D1–	7	8	I/O	
D+	3	4	I/O	Common USB signal path
D-	5	6	I/O	
D2+	2	3	I/O	USB signal path port 2
D2–	6	7	I/O	
$\overline{OE}$	8	9	I	Bus-switch enable
S	10	1	I	Select input
GND	4	5	—	Ground
VCC	9	10	—	Voltage supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (see (1) (2))

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_{IN}	Control input voltage(3)		–0.5	7	V
$V_{I/O}$	Signal path I/O voltage(3) (4)	D+, D– when V_{CC} > 0	–0.5	V_{CC} + 0.3	V
		D+, D– when V_{CC} = 0	–0.5	5.25	
I_{IK}	Control input clamp current	V_{IN} < 0		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O}$ < 0		–50	mA
$I_{I/O}$	ON-state switch current(5)			±64	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	8000	V
			I/O port to GND	15000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See (1).

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	4.3	V
V_{IH}	High-level control input voltage	V_{CC} = 3 V to 3.6 V	1.3	V_{CC}	V
		V_{CC} = 4.3 V	1.7	V_{CC}	
V_{IL}	Low-level control input voltage	V_{CC} = 3 V to 3.6 V	0	0.5	V
		V_{CC} = 4.3 V	0	0.7	
$V_{I/O}$	Data input/output voltage		0	V_{CC}	V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to *Implications of Slow or Floating CMOS Inputs* (SCBA004).

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6.4 Thermal Information

THERMAL METRIC[1]		TS3USB30E		UNIT
		DGS (VSSOP)	RSW (UQFN)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	203.1	114.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	88.7	64.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	123.0	21.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	21.2	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	121.6	21.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
V_{IK}	Control input clamp voltage	V_{CC} = 3 V, I_I = –18 mA			–1.2	V
I_{IN}	Control inputs	V_{CC} = 4.3 V, 0 V, V_{IN} = 0 to 4.3 V			±1	µA
I_{OZ}	D+ and D– OFF-state leakage current[3]	V_{CC} = 4.3 V, V_O = 0 to 3.6 V, V_I = 0, Switch OFF			±1	µA
I_{OFF}	Powered off leakage current	V_{CC} = 0 V, V_O = 0 to 4.3 V, V_I = 0, V_{IN} = V_{CC} or GND			±2	µA
I_{CC}	Supply current	V_{CC} = 4.3 V, $I_{I/O}$ = 0, Switch ON or OFF			1	µA
ΔI_{CC} [4]	Control inputs	V_{CC} = 4.3 V, V_{IN} = 2.6 V			10	µA
C_{in}	Control inputs digital input capacitance	V_{CC} = 0 V, V_{IN} = V_{CC} or GND		1		pF
$C_{io(OFF)}$	OFF-state input capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 3.3 V or 0, Switch OFF		2		pF
$C_{io(ON)}$	ON-state input capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 3.3 V or 0, Switch ON		7.5		pF
R_{ON}	ON-state resistance[5]	V_{CC} = 3 V, V_I = 0.4, I_O = –8 mA		6	10	Ω
ΔR_{ON}	ON-state resistance match between channels	V_{CC} = 3 V, V_I = 0.4, I_O = –8 mA		0.35		Ω
$r_{on(flat)}$	ON-state resistance flatness	V_{CC} = 3 V, V_I = 0 V or 1 V, I_O = –8 mA		2		Ω

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

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6.6 Dynamic Electrical Characteristics

over operating range, T_A = –40°C to 85°C, V_{CC} = 3.3 V ± 10%, GND = 0 V

PARAMETER		TEST CONDITIONS	TYP(1)	UNIT
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 240 MHz, See Figure 6	–54	dB
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 240 MHz, See Figure 5	–40	dB
BW	Bandwidth (–3 dB)	R_L = 50 Ω, C_L = 5 pF, See Figure 7	900	MHz

(1) For Max or Min conditions, use the appropriate value specified under *Electrical Characteristics* for the applicable device type.

6.7 Switching Characteristics

over operating range, T_A = –40°C to 85°C, V_{CC} = 3.3 V ± 10%, GND = 0 V

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{pd}	Propagation delay(2) (3)	R_L = 50 Ω, C_L = 5 pF, See Figure 8		0.25		ns
t_{ON}	Line enable time, SEL to D, nD	R_L = 50 Ω, C_L = 5 pF, See Figure 4			30	ns
t_{OFF}	Line disable time, SEL to D, nD	R_L = 50 Ω, C_L = 5 pF, See Figure 4			25	ns
t_{ON}	Line enable time, $\overline{OE}$ to D, nD	R_L = 50 Ω, C_L = 5 pF, See Figure 4			30	ns
t_{OFF}	Line disable time, $\overline{OE}$ to D, nD	R_L = 50 Ω, C_L = 5 pF, See Figure 4			25	ns
$t_{SK(O)}$	Output skew between center port to any other port(2)	R_L = 50 Ω, C_L = 5 pF, See Figure 9			50	ps
$t_{SK(P)}$	Skew between opposite transitions of the same output (t_{PHL} – t_{PLH})(2)	R_L = 50 Ω, C_L = 5 pF, See Figure 9			20	ps
t_J	Total jitter(2)	R_L = 50 Ω, C_L = 5 pF, t_R = t_F = 500 ps at 480 Mbps (PRBS = 2^{15} – 1)			20	ps

(1) For Max or Min conditions, use the appropriate value specified under *Electrical Characteristics* for the applicable device type.
(2) Specified by design
(3) The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10-pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

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6.8 Typical Characteristics

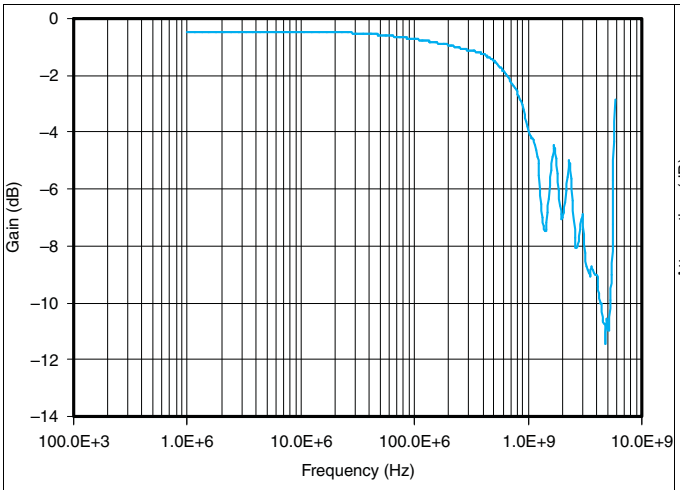


Figure 1. Gain vs Frequency

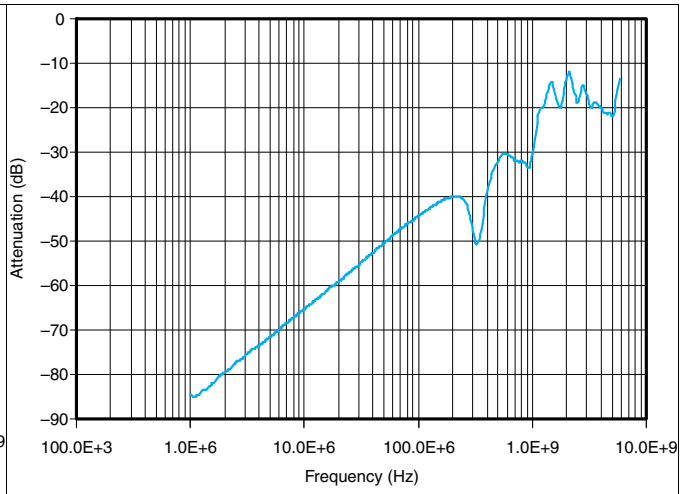


Figure 2. OFF Isolation

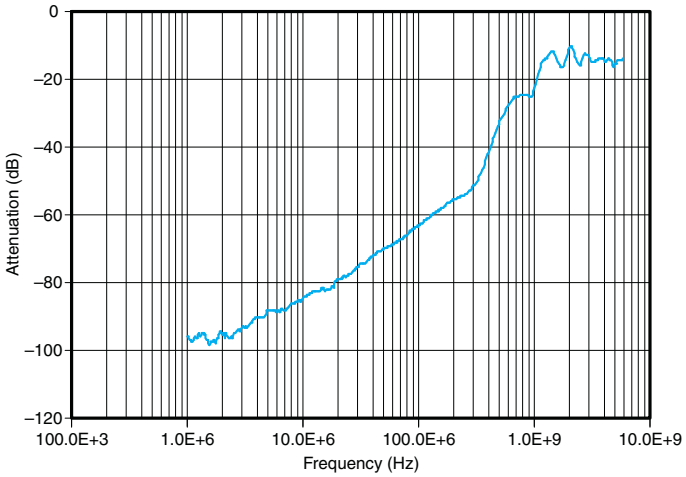
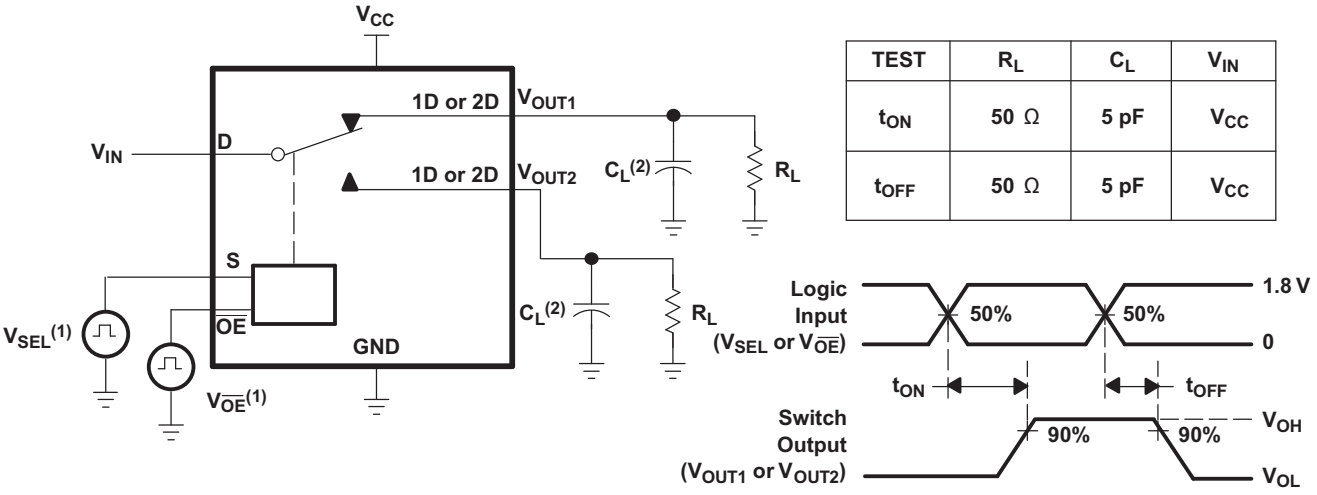


Figure 3. Crosstalk

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7 Parameter Measurement Information

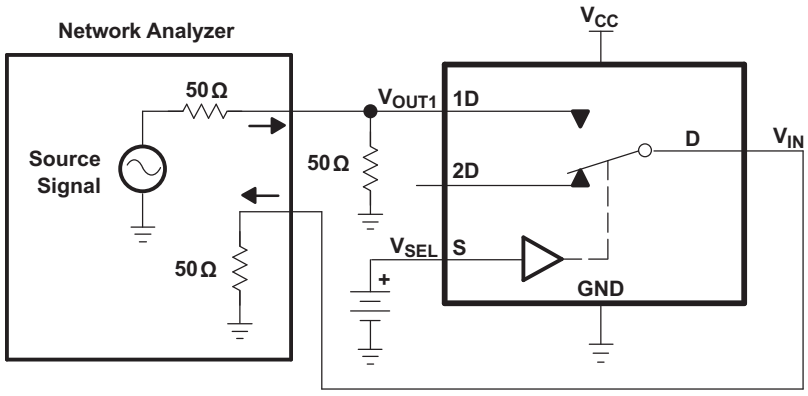


TEST	R_L	C_L	V_{IN}
t_{ON}	50 Ω	5 pF	V_{CC}
t_{OFF}	50 Ω	5 pF	V_{CC}

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 4. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})



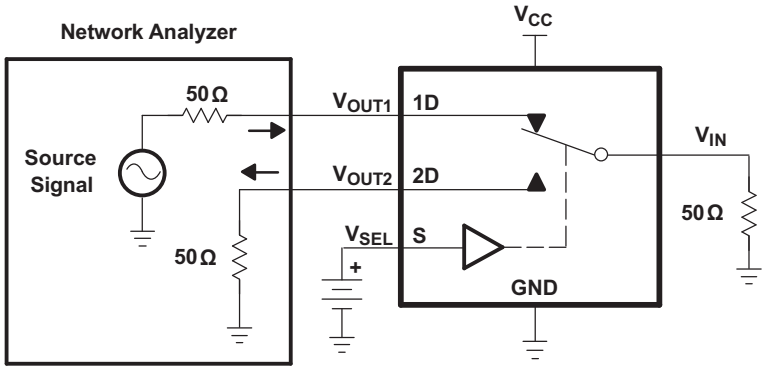
Channel OFF: 1D to D
V_{SEL} = V_{CC}

Network Analyzer Setup

Source Power = 0 dBm (632-mV P-P at 50-Ω load)

DC Bias = 350 mV

Figure 5. OFF Isolation (O_{ISO})



Channel ON: 1D to D
Channel OFF: 2D to D
V_{SEL} = V_{CC}

Network Analyzer Setup

Source Power = 0 dBm (632-mV P-P at 50-Ω load)

DC Bias = 350 mV

Figure 6. Crosstalk (X_{TALK})

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Parameter Measurement Information (continued)

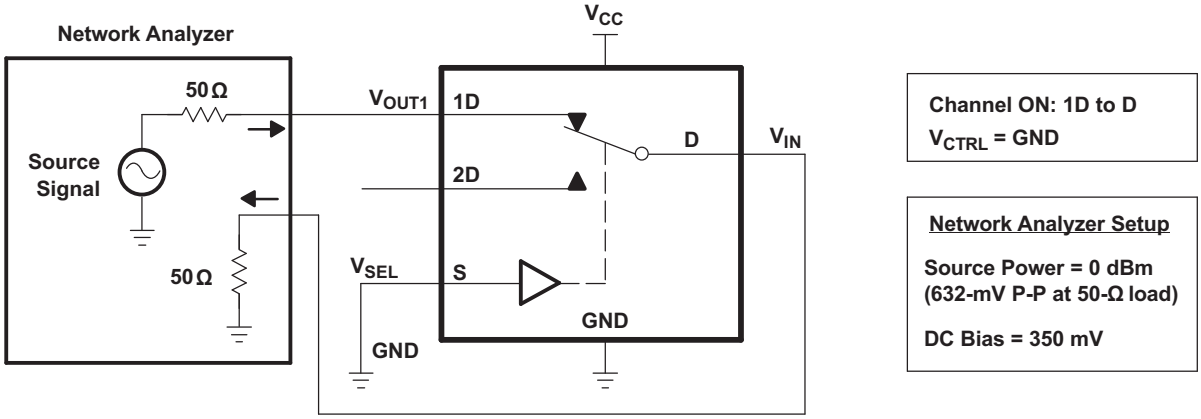


Figure 7. Bandwidth (BW)

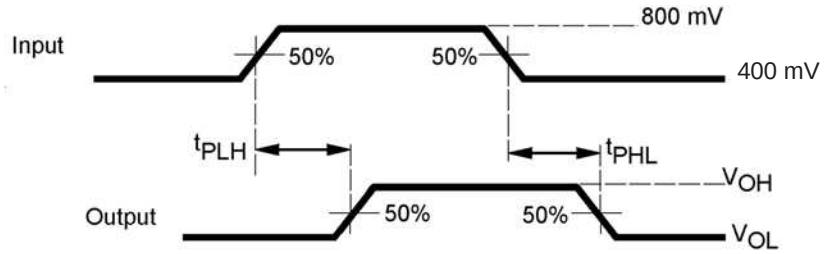
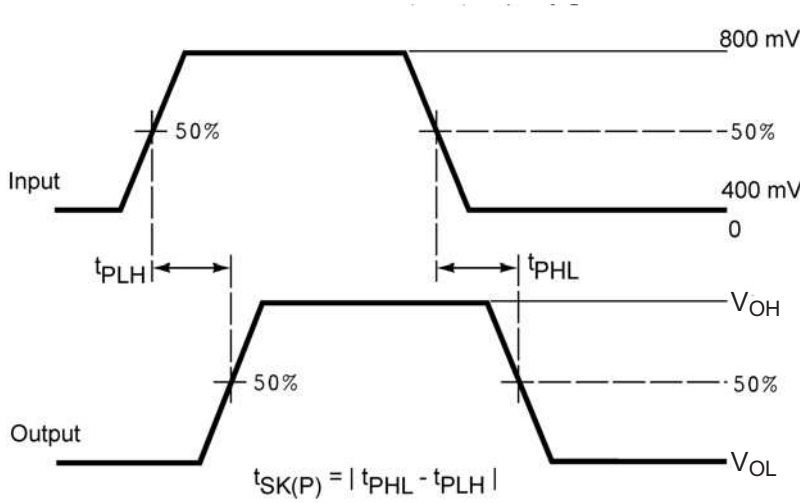
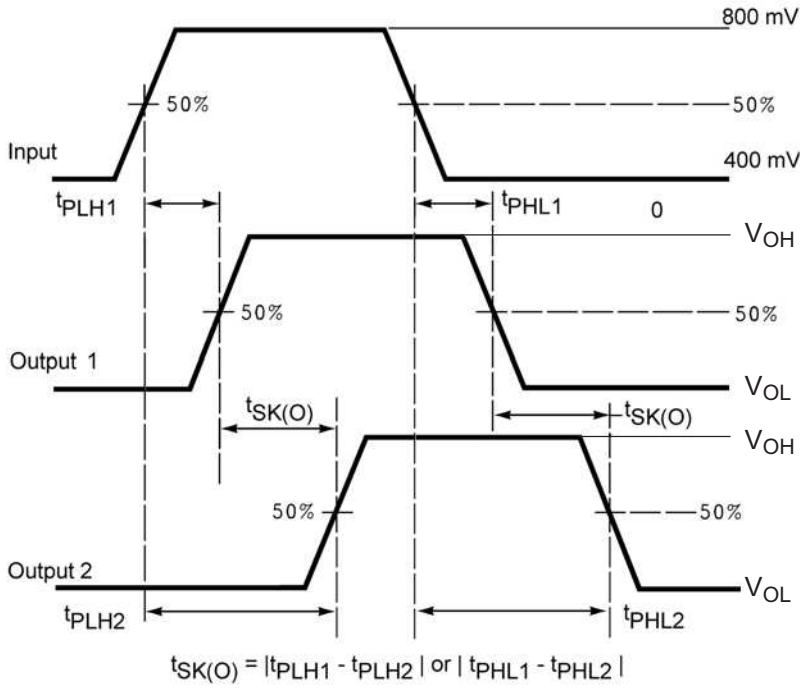


Figure 8. Propagation Delay

Parameter Measurement Information (continued)



Pulse Skew $t_{SK(P)}$



Output Skew $t_{SK(P)}$

Figure 9. Skew Test

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Parameter Measurement Information (continued)

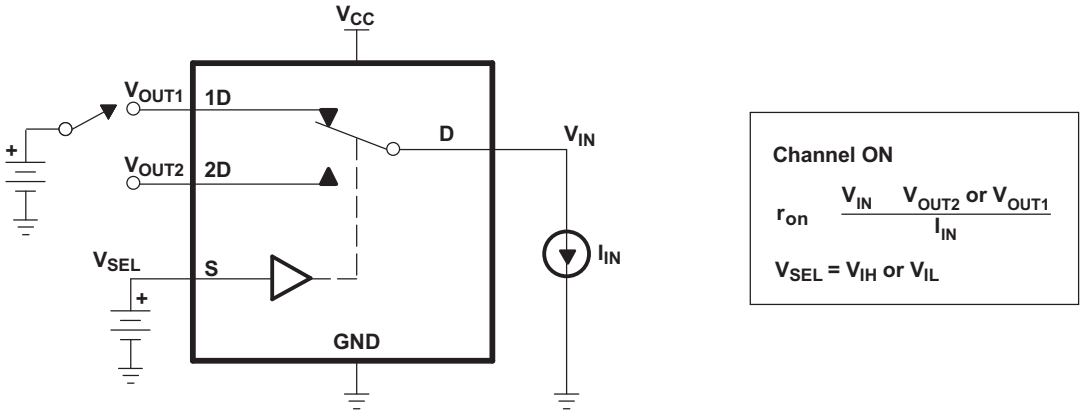


Figure 10. ON-State Resistance (R_{ON})

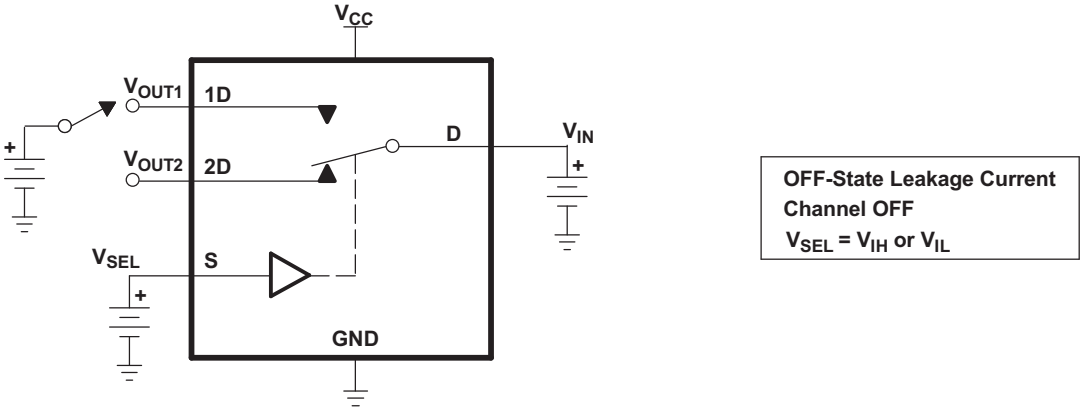


Figure 11. OFF-State Leakage Current

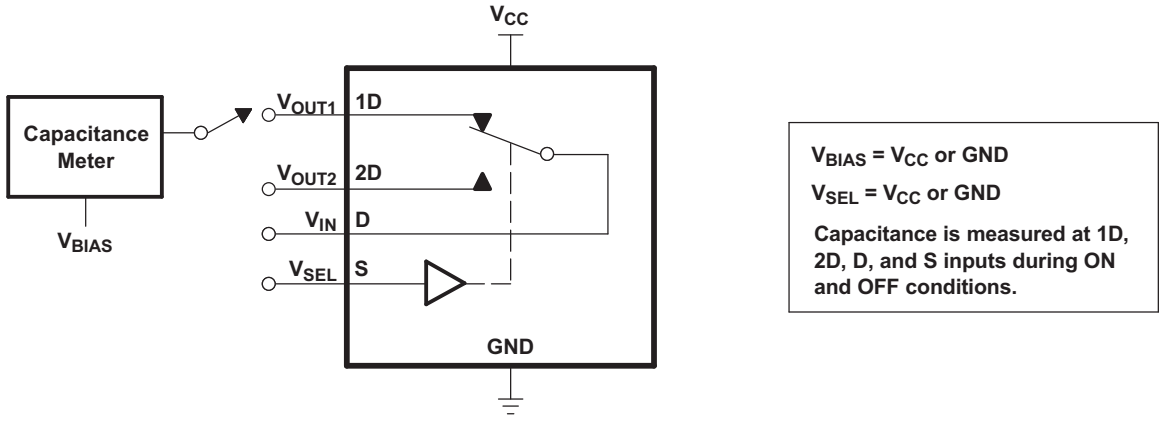


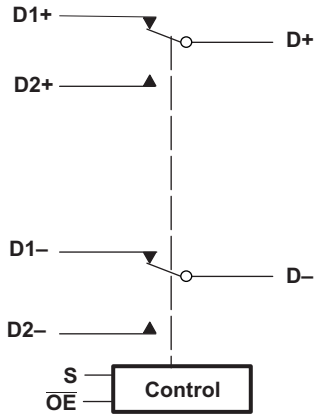
Figure 12. Capacitance

8 Detailed Description

8.1 Overview

The TS3USB30E is a high-bandwidth switch specially designed for the switching and isolating of high-speed USB 2.0 signals in systems with limited USB I/Os. The wide bandwidth (900 MHz) of this switch allows signals to pass with minimum edge and phase distortion. The device multiplexes differential outputs from a USB host device to one of two corresponding outputs or from two different hosts to one corresponding output. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. It is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480 Mbps).

8.2 Functional Block Diagram



8.3 Feature Description

The TS3USB30E has a bus-switch enable pin $\overline{OE}$ that can place the signal paths in high impedance. This allows the user to isolate the bus when it is not in use and consume less current.

8.4 Device Functional Modes

The device functional modes are shown in Table 1.

Table 1. Truth Table

S	$\overline{OE}$	FUNCTION
X	H	Disconnect
L	L	D = D1
H	L	D = D2

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

There are many USB applications in which the USB hubs or controllers have a limited number of USB I/Os. The TS3USB30E solution can effectively expand the limited USB I/Os by switching between multiple USB buses in order to interface them to a single USB hub or controller. TS3USB221E can also be used to connect a single controller to two USB connectors or controllers.

9.2 Typical Application

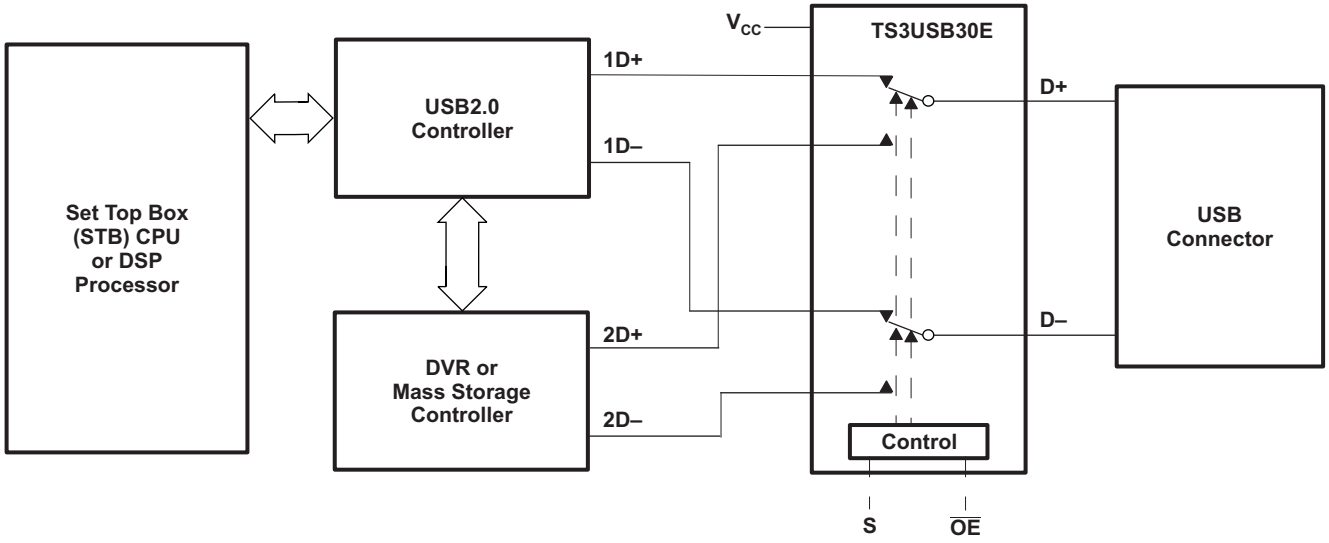


Figure 13. Application Diagram

9.2.1 Design Requirements

Design requirements of the USB 1.0, 1.1, and 2.0 standards should be followed. TI recommends that the digital control pins S and $\overline{OE}$ be pulled up to V_{CC} or down to GND to avoid undesired switch positions that could result from the floating pin.

9.2.2 Detailed Design Procedure

The TS3USB30E can be properly operated without any external components. However, it is recommended that unused pins be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device.

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Typical Application (continued)

9.2.3 Application Curves

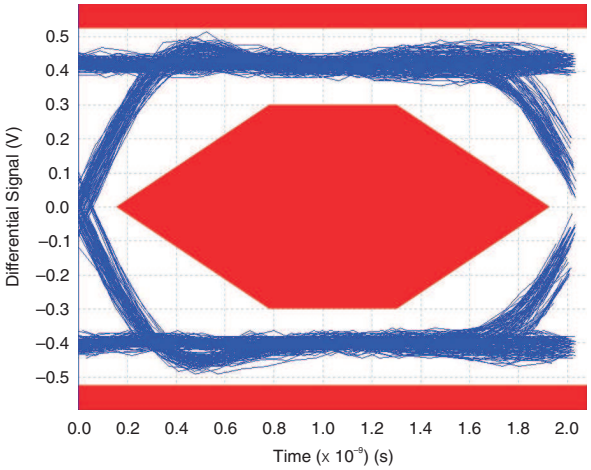


Figure 14. Eye Pattern: 480-Mbps USB Signal With No Switch (Through Path)

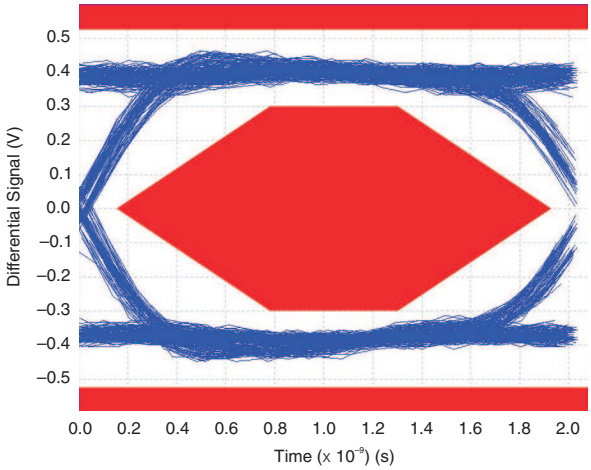


Figure 15. Eye Pattern: 480-Mbps USB Signal With Switch NC Path

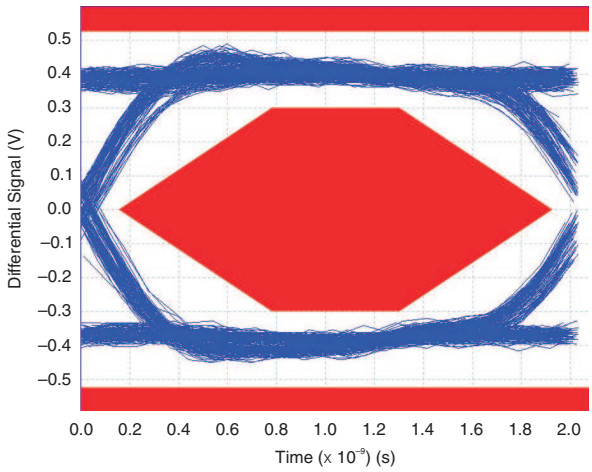


Figure 16. Eye Pattern: 480-Mbps USB Signal With Switch NO Path

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10 Power Supply Recommendations

Power to the device is supplied through the V_{CC} pin and should follow the USB 1.0, 1.1, and 2.0 standards. TI recommends placing a bypass capacitor as close as possible to the supply pin V_{CC} to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

11 Layout

11.1 Layout Guidelines

Place supply bypass capacitors as close to V_{CC} pin as possible and avoid placing the bypass caps near the D+ and D– traces.

The high-speed D+ and D– traces should always be of equal length and must be no more than 4 inches; otherwise, the eye diagram performance may be degraded. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In layout, the impedance of D+ and D– traces should match the cable characteristic differential impedance for optimal performance.

Route the high-speed USB signals using a minimum of vias and corners which will reduce signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the transmission line of the signal and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices, or IC's that use or duplicate clock signals.

Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub should be less than 200 mm.

Route all high-speed USB signal traces over continuous planes (VCC or GND), with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended: two signal layers separated by a ground layer and a power layer. The majority of signal traces should run on a single layer, preferably Signal 1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies. For more information on layout guidelines, see *High Speed Layout Guidelines* (SCAA082) and *USB 2.0 Board Design and Layout Guidelines* (SPRAAR7).

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11.2 Layout Example

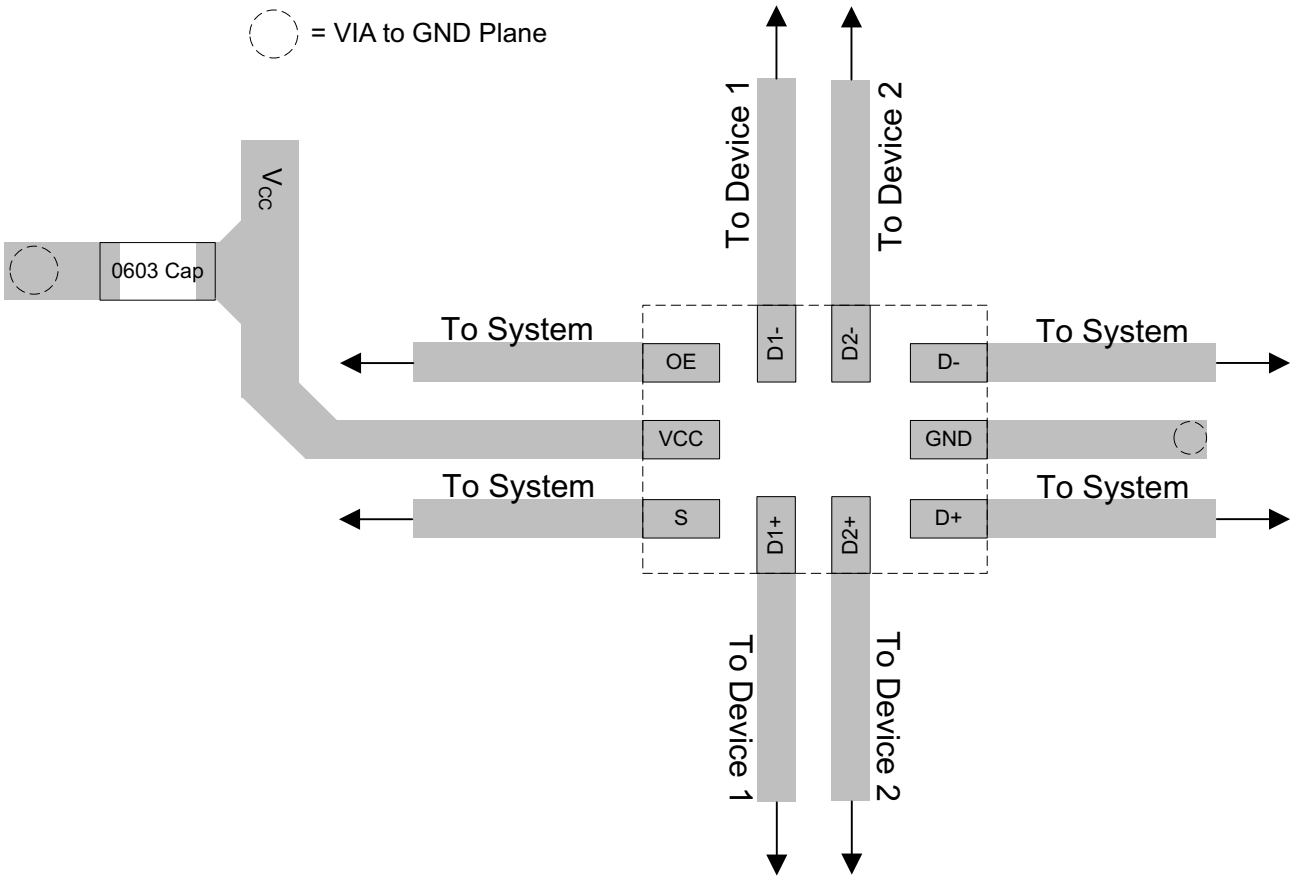


Figure 17. Layout Recommendation

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *Implications of Slow or Floating CMOS Inputs*, SCBA004
- *High Speed Layout Guidelines*, SCAA082
- *USB 2.0 Board Design and Layout Guidelines*, SPRAAR7

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3USB30EDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(L6Q, L6R)	Samples
TS3USB30ERSWR	ACTIVE	UQFN	RSW	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(LY7, LYO, LYV)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

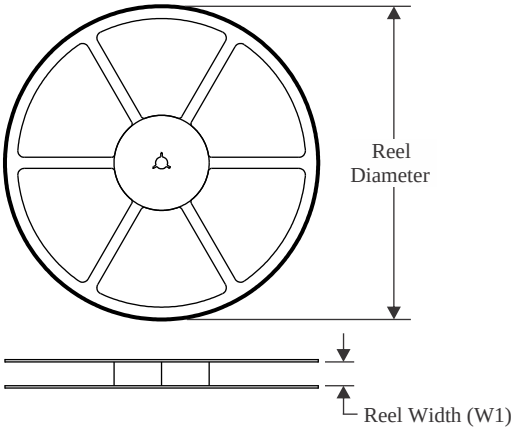
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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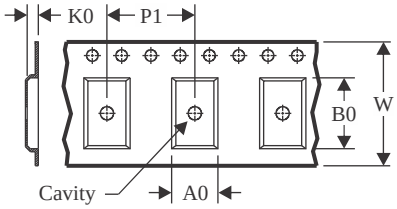
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

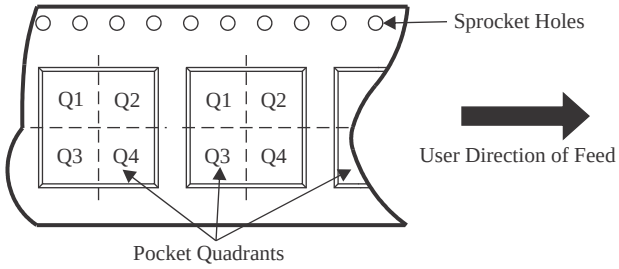


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

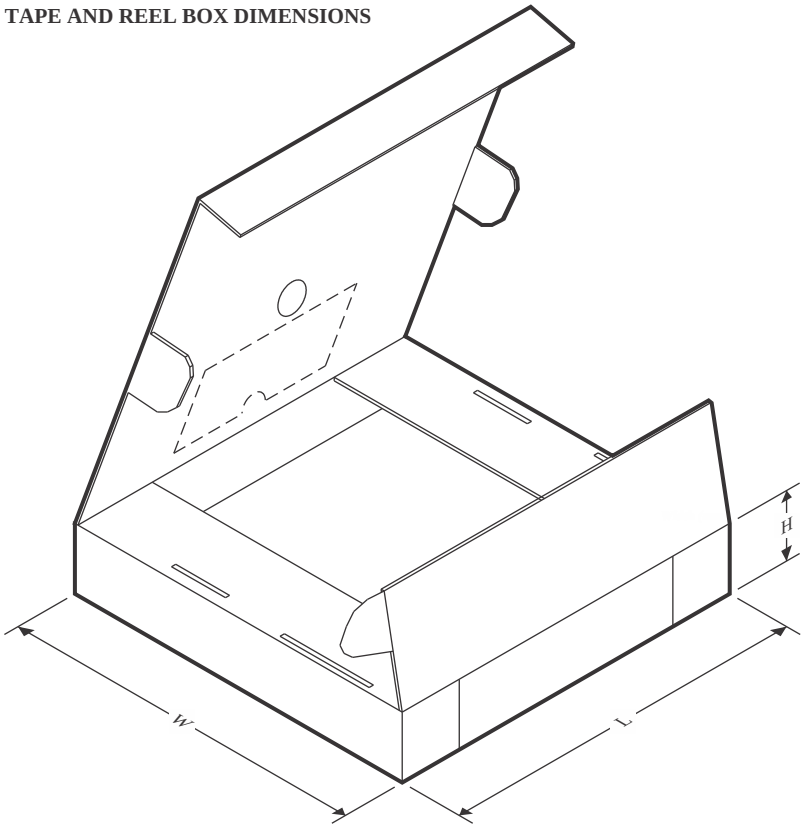
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3USB30EDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TS3USB30ERSWR	UQFN	RSW	10	3000	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

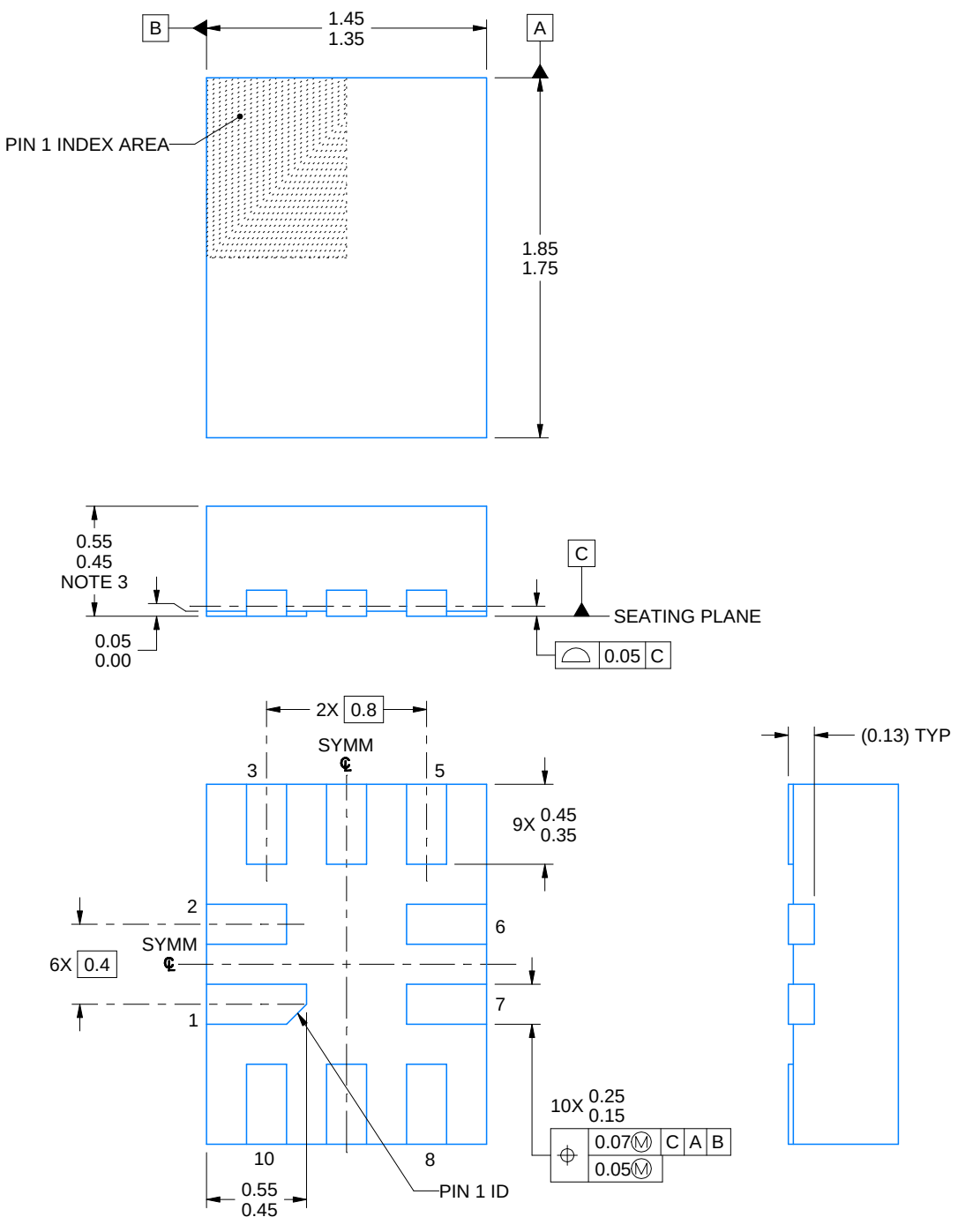
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3USB30EDGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TS3USB30ERSWR	UQFN	RSW	10	3000	189.0	185.0	36.0

PACKAGE OUTLINE

RSW0010A

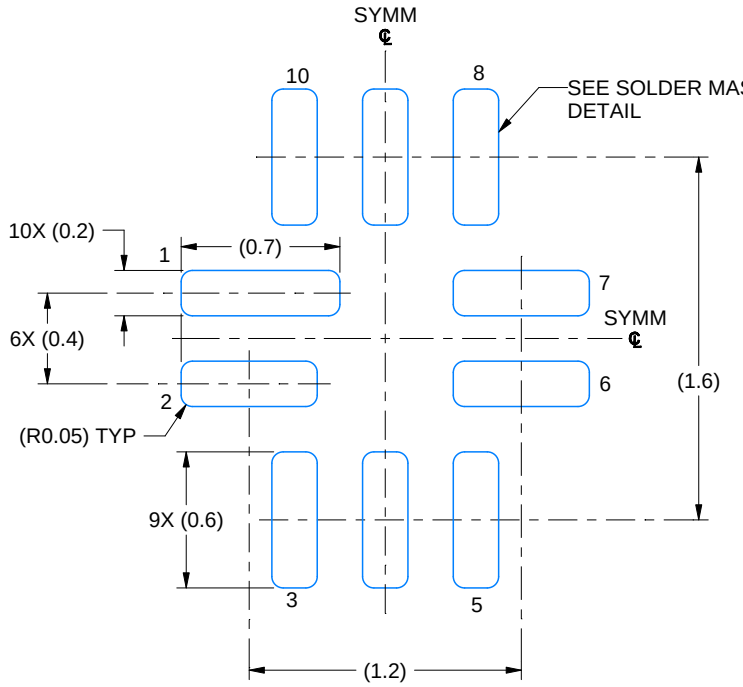
UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

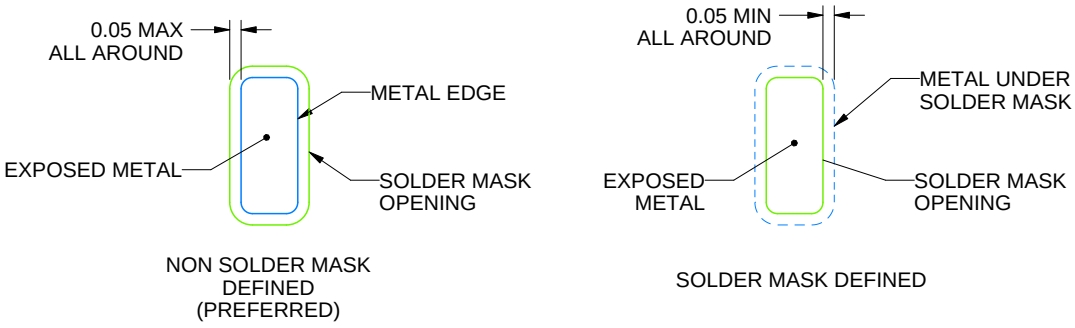


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-288 variation UDEE, except minimum package height.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

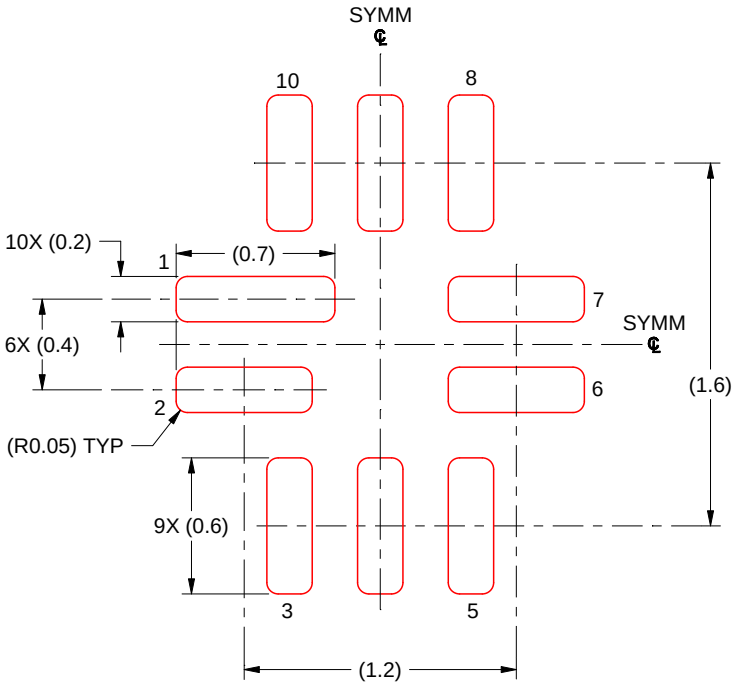


SOLDER MASK DETAILS

4224897/A 03/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

4224897/A 03/2019

NOTES: (continued)

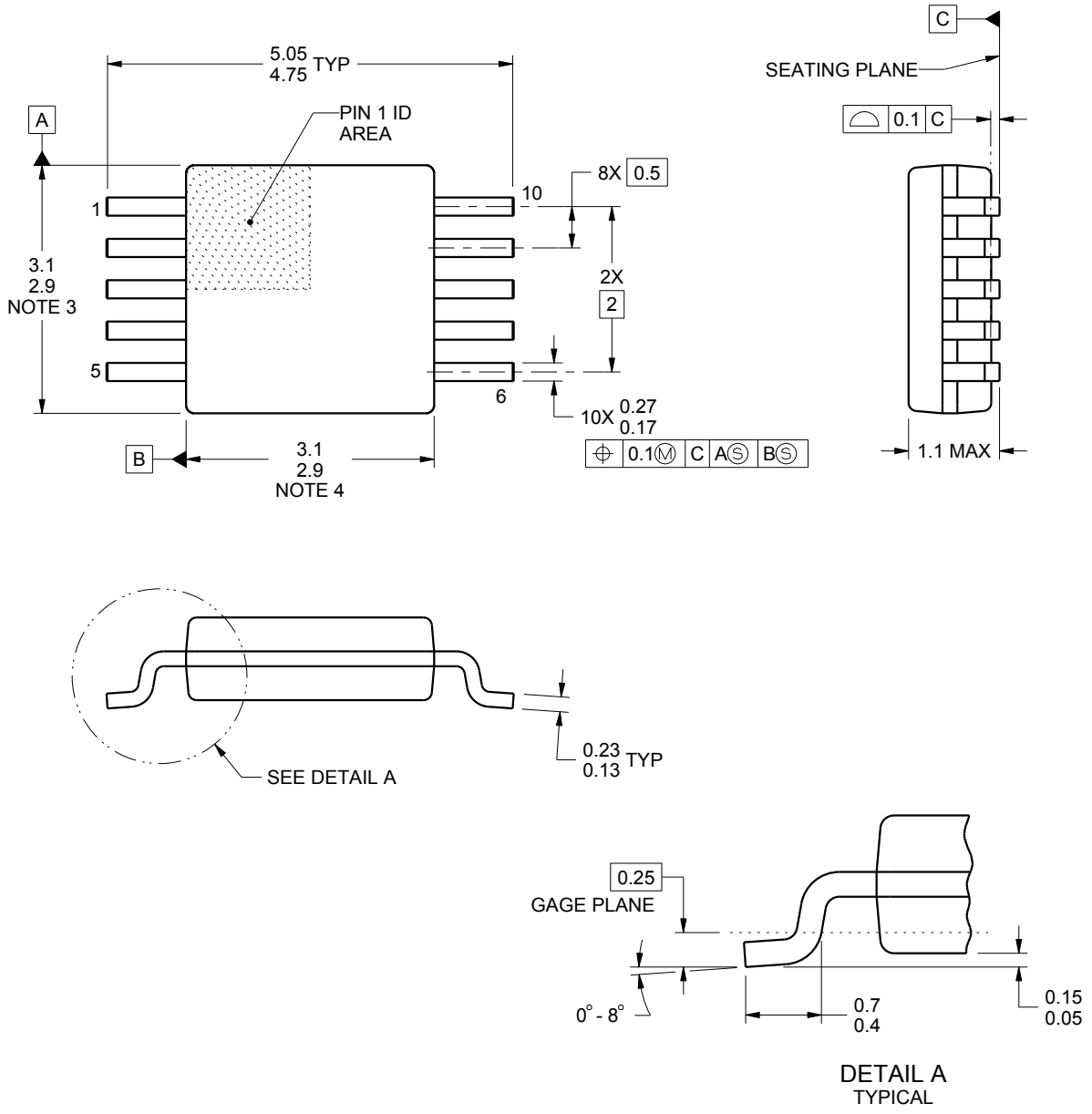
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DGS0010A

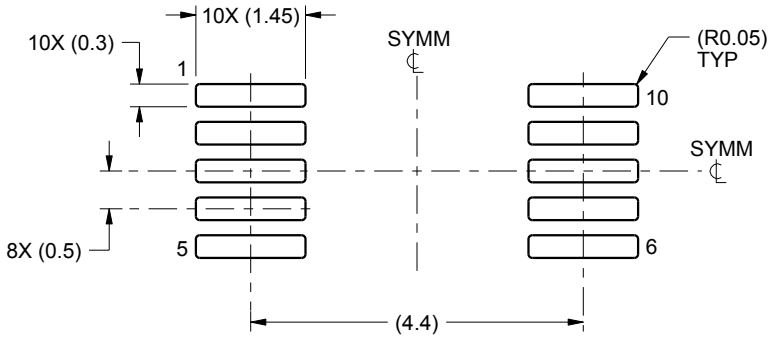
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

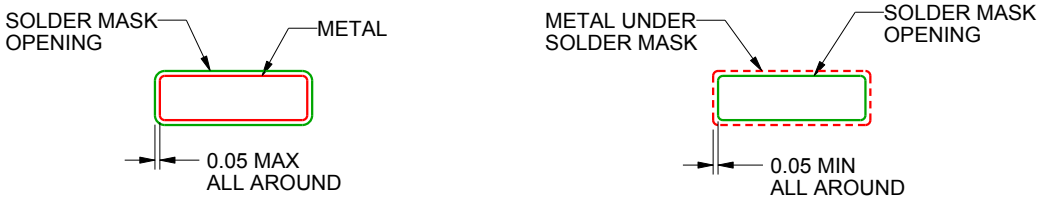


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

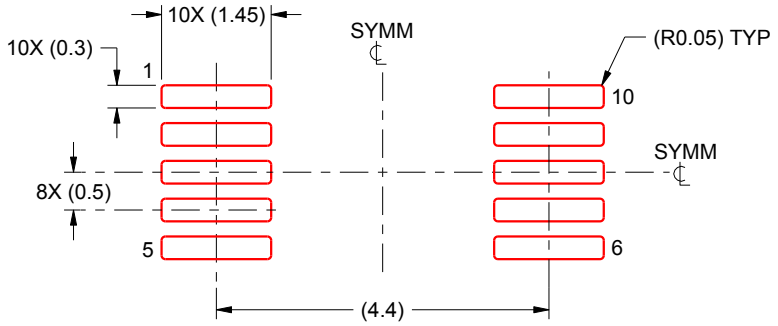


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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- Shortage Management
- Alternative Solution
- Excess Inventory Management