THE DATASHEET OF

XC3S400A-4FGG320C

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Xilinx Spartan™-3A FPGA Platform
The World's Lowest-Cost I/O Optimized FPGAs



The Programmable Logic Challenge of I/O Intensive Designs

- Traditional FPGAs are proportionate between logic and I/O not being cost-effective for I/O intensive designs
- System designers need to quickly adapt to fast-evolving I/O standards
- High volume consumer applications require low-cost and robust security solutions

The Xilinx FPGA Solution

- The Spartan™-3A FPGAs were designed for applications where I/O count and capabilities matter more than logic density
- The Spartan-3A platform delivers up to 502 I/Os with support for industry-leading 26 popular and emerging I/O standards
- The industry's first 90nm FPGA electronic ID - Device DNA serial number provides a cost-effective, robust mechanism to help protect against reverse-engineering, cloning and overbuilding

Xilinx is driving the multiple domain-optimized platforms for highly efficient and optimal design solutions, instead of forcing inefficient, one-size-fits-all solutions on significantly varying application requirements.

Spartan-3A Platform Key Features

Standard Low-Cost Features

The Spartan-3A FPGA platform is a full feature platform of five devices with system gates ranging from 50K to 1.4M gates, and I/Os ranging from 108 to 502 I/Os, with density migration. The Spartan-3A FPGAs also support up to 576 Kbits of fast-block RAM with byte-write enable, and up to 176 Kbits of distributed RAM. Additionally, there are built-in multipliers for efficient DSP implementation and Digital Clock Managers (DCMs) for system level clock management functions.

Advance Features

The advance features in the Spartan-3A platform include unique Device DNA serial number, support for 26 I/O standards, enhanced Multi-Boot capability with watchdog timer, dual power management modes, and Dynamic Input Delay for precise data-to-clock centering. These advance features significantly help shorten design cycles and lower system cost.

XILINX®

Industry's first 90nm FPGA Electronic Serial Numbering

Each FPGA includes a permanent unique Device DNA serial number that can be used to safeguard both hardware and software IP. It is ideal for tracking production serial numbers, product registrations and system ID. Customers have complete flexibility in implementing custom algorithms for the security solutions that can significantly deter reverse-engineering, cloning and overbuilding.

Widest Support for I/O Standards

The Spartan-3A FPGA is especially suitable for display devices supporting both TMDS and PPDS standards. With support for 26 popular single-ended and differential signaling standards including TMDS, PPDS, SSTL3 Class I & II, full hot-swap compliance, and pre-engineered interface IP solutions such as PCI, PCI Express, USB, Firewire, CAN, SPI, I2C, etc, the Spartan-3A platform provides an industry-leading connectivity solution.

Comprehensive Configuration Capabilities

The Spartan-3A platform features enhanced Multi-Boot capability with watchdog timer for guaranteed "golden" configuration. This enables intelligent recovery from configuration errors and improves field upgradeability.

Flexible Power-Management Modes

A new Suspend mode provides a very flexible and effective way to preserve power. In this mode, the power is comparable to quiescent current, and the configuration data as well as flip-flop and RAM values are maintained. It also includes a fast wake-up mechanism and system level synchronization across time domains.

Dynamic Input Delay

Selecting delay-length for both registered and combinatorial inputs allows for precise timing relationship adjustment between clock and data. Combinatorial input delay can now also be dynamically changed through the interconnect. Source synchronous designs will significantly benefit from this feature.

	Spartan-3A FPGA Platform				
Device	**XC3S50A**	**XC3S200A**	**XC3S400A**	**XC3S700A**	**XC3S1400A**
System Gates	50K	200K	400K	700K	1400K
Logic Cells	1,584	4,032	8,064	13,248	25,344
Dedicated Multipliers	3	16	20	20	32
Block RAM Blocks	3	16	20	20	32
Block RAM Bits	54K	288K	360K	360K	576K
Distributed RAM Bits	11K	28K	56K	92K	176K
DCMs	2	4	4	8	8
I/O Standards	26	26	26	26	26
Max Differential I/O	64	112	142	165	227
Max Single Ended I/O	144	248	311	372	502
	Package and I/O Offerings				
Device	**XC3S50A**	**XC3S200A**	**XC3S400A**	**XC3S700A**	**XC3S1400A**
TQ144 20 x 20 mm	108				
FT256 17 x 17 mm	144	195	195		
FG320 19 x 19 mm		248	251		
FG400 21 x 21 mm			311	311	
FG484 23 x 23 mm				372	375
FG676 27 x 27 mm					502

Take the Next Step

Visit our website ***www.xilinx.com/spartan3a*** or call your local sale office or distributor for more information about Spartan-3A FPGAs. To start your design immediately, download your free ISE WebPACK™ design tools at ***www.xilinx.com/ise***. To begin evaluating Spartan-3A FPGAs, order your hardware development board at ***www.xilinx.com/s3astarter***

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